### **Ve 370 Introduction to Computer Organization**

## **Project 2**

#### **Project Description**

Model both single cycle (individual work) and pipelined implementation (team work) of RISC-V (64bit) computer in Verilog that support a subset of RISC-V (64bit) instruction set including:

- The memory-reference instructions load word (ld) and store word (sd)
- The arithmetic-logical instructions add, addi, sub, and, andi, xor, slt, slti, sll, slli
- The jumping instructions beq, bne, bge, blt, j, jal, jr

Use Figure 1 as a top-level block diagram of your single cycle implementation and Figure 2 for the pipelined structure.

Note: there may be some components and control signals omitted from the figures that you will have to add to support all instructions listed above. Forwarding and Hazard Detection should be implemented in the pipelined structure to handle hazards.

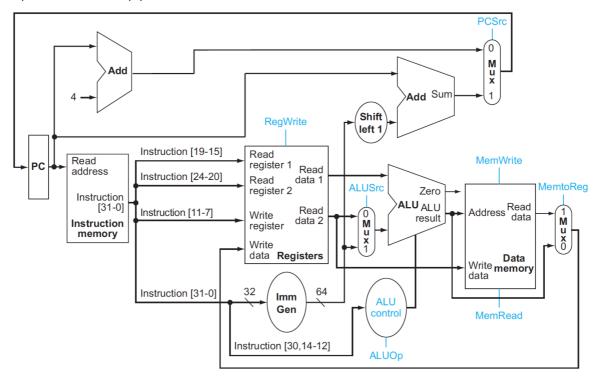


Figure 1. Single cycle implementation of RISC-V architecture

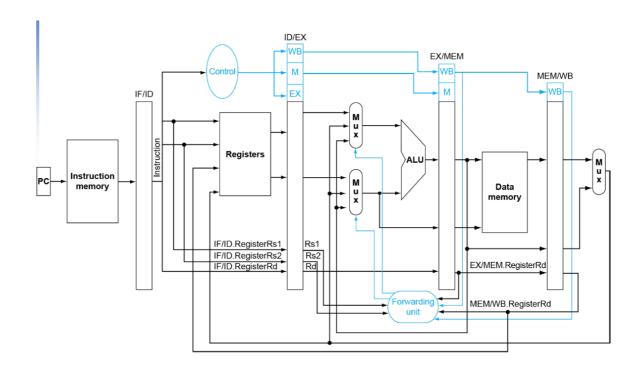


Figure 2. Pipelined implement of RISC-V architecture

#### **Project Requirements**

This project must be modeled and simulated in Verilog HDL and synthesized by using Xilinx synthesis tool.

Every student is required to model a single cycle processor individually. An individual written report should be submitted to show simulation results and source codes.

Each team is required to submit a group report on the pipelined processor.

FPGA implementation of the single cycle and pipeline processor are NOT required.

### **Team Organization**

The part of pipelined processor shall be team work. Each team is composed of 4 students. The work should be appropriately divided and distributed among all team members.

Students are not allowed to switch teams unless approved by the instructor.

#### **Deliverables**

All deliverables should be submitted electronically on Canvas. The project must be demonstrated to the teaching group.

• Team report:

The team report should be a written report. One submission is required for each team and should be submitted electronically by one of the team members. Make sure names of all team members are clearly shown on the cover page of the report. The report must include:

- 1) Elaborated description of all aspects of the modeling and implementation of the pipelined processor;
- 2) Screen shots and explanations of simulation results. This will help you to earn partial credits if a project is not completed;
- 3) RTL schematic of your Verilog design generated with Xilinx Vivado software;

- 4) All your Verilog source files and any other files, as appendix.
- Individual report The individual report should include:
- 1) Screen shots of simulation results for each instruction;
- 2) Verilog source files
- 3) Peer evaluation describing your own contribution to the lab as well as contributions of every other team member, as explained below.

#### PEER EVALUATION

Each team member is required to provide a peer evaluation for the team effort of Project 2. The marks of the peer evaluation should be integers ranging between 0 to 5, inclusively, with 5 indicating the biggest contribution. A mark should be given to each team member including yourself according the team member's contribution based on your observation. A brief description of contribution of each team member should also be provided, as shown in the following table.

Name	Level of contribution (0 ~ 5)	Description of contribution
(yourself)		
(your lab partner)		
(your lab partner)		
(your lab partner)		

Additionally, the teaching team (instructor and/or TAs) will give an oral examination to each team member during the demonstration. We will ask some basic but important questions related to the project. Basing on your answers, we will give an evaluation mark, ranging in between 0 to 5 as well.

An average mark for individual contribution of each student is calculated as:

Individual\_Average = (sum of all team member's marks + teaching team's mark \* 2) / (size of the student team + 2)

A group average is calculated as:

Group\_Average = sum of Individual\_Average of all team members / size of student team

Then we calculate a difference ratio with the following equation:

Individual\_Difference = Individual\_Average / Group\_Average - 1.0

Using the calculated Individual\_Difference, we find a factor from the following lookup table.

Individual\_Difference Factor Individual\_Difference Factor

Individual_Difference	Factor	Individual_Difference	Factor
>=0 and < +10%	1.0	> -10% and < 0	1.0
>= +10% and < +20%	1.1	> -20% and <= -10%	0.9
>= +20% and < +30%	1.2	> -30% and <= -20%	0.8
>= +30%	1.3	<= -30%	0.7

Your final Project 2 grade is calculated as:

Final grade of Project 2 = points for Individual report + points for team effort \* factor

The final grade of Project 2 will not exceed the maximum points assigned to the project.

# **Grading Policy**

Factor	Percentage
Individual Report	30%
Team Report	10%
Team Demonstration	60%

### **Due Date**

The due date for individual report is 11:59 p.m , 28th Jun.

The due date for team report is 11:59 p.m, 11 Jul.

Time and location for demonstration will be post 11 Jul, and will be announced on Canvas later.