VE370 Project Report

Project 2 - Summer 2021

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VE370 Project 2 Individual Report

Overview

VE370 Project 2 is designed for students to get a better understanding of **Single-cycle and Pipelined Processor Design**.

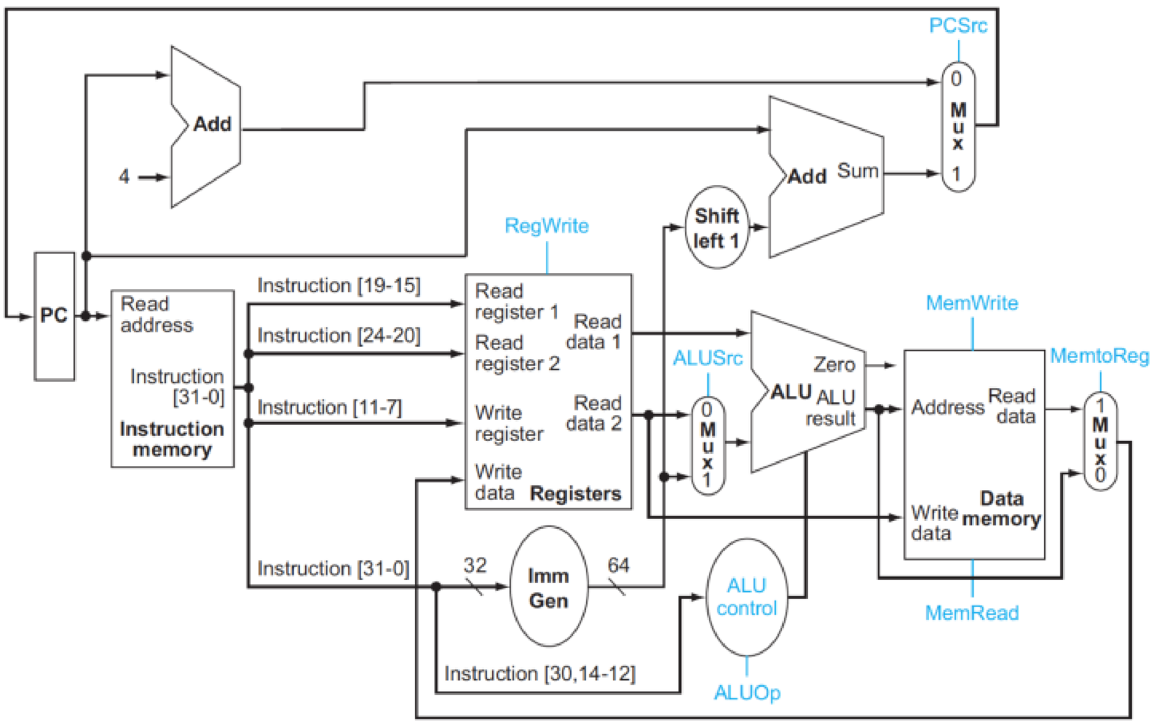

Figure 1. Single cycle implementation of RISC-V architecture

Figure 1. Single Cycle Diagram (RISC-V 64 bit)

Verilog Simulation

A set of instructions are used to test the single-cycle implementation.

Testcase:

```
    6300193 //  addi    x3  x0  99
    09c00213    //  addi    x4  x0  156
    13  //  nop
    13  //  nop
    004182b3    //  add x5  x3  x4
    40418333    //  sub x6  x3  x4
    403200b3    //  sub x1  x4  x3
    600113  //  addi    x2  x0  6
    100393  //  addi    x7  x0  1
    13  //  nop
    117413  //  andi    x8  x2  1
    007174b3    //  and x9  x2  x7
    714533  //  xor x10 x2  x7
    002395b3    //  sll x11 x7  x2
    639613  //  slli    x12 x7  6
    339693  //  slli    x13 x7  3
    712733  //  slt x14 x2  x7
    712793  //  slti    x15 x2  7
    13  //  nop
    13  //  nop
//  <branch1>:  //
    13  //  nop
    13  //  nop
    04210e63    //  beq x2  x2  92  <first>
    13  //  nop
    13  //  nop
```

```
//  <branch2>:  //
    13  //  nop
    13  //  nop
    6211463 //  bne x2  x2  104 <second>
    13  //  nop
    13  //  nop
//  <branch3>:  //
    13  //  nop
    13  //  nop
    0623c663    //  blt x7  x2  108 <third>
    13  //  nop
    13  //  nop
//  <branch4>:  //
    13  //  nop
    13  //  nop
    06715c63    //  bge x2  x7  120 <fourth>
    13  //  nop
    13  //  nop
//  <branch5>:  //
    13  //  nop
    13  //  nop
    0840006f    //  jal x0  0x12c   <exit>
    13  //  nop
    13  //  nop
//  <first>:    //
    13  //  nop
    13  //  nop
    100813  //  addi    x16 x0  1
    13  //  nop
    13  //  nop
    f9dff0ef    //  jal x1  0x64    <branch2>
    13  //  nop
    13  //  nop
//  <second>:   //
    13  //  nop
    13  //  nop
    200893  //  addi    x17 x0  2
    13  //  nop
    13  //  nop
    f91ff06f    //  jal x0  0x78    <branch3>
//  <third>:    //
    13  //  nop
    13  //  nop
    300913  //  addi    x18 x0  3
    13  //  nop
    13  //  nop
    f8dff06f    //  jal x0  0x8c    <branch4>
    13  //  nop
    13  //  nop
//  <fourth>:   //
    13  //  nop
    13  //  nop
    400993  //  addi    x19 x0  4
    13  //  nop
    13  //  nop
    f81ff06f    //  jal x0  0xa0    <branch5>
    13  //  nop
    13  //  nop
```

```
//  <exit>: //
    13  //  nop
```

Simulation result:

```
# run 10000
Time:    0   , PC=xxxx
Reg[          0]: xxxxxxxxxxxxxxxx ,Reg[          1]: xxxxxxxxxxxxxxxx ,Reg[
     2]: xxxxxxxxxxxxxxxx ,Reg[          3]: xxxxxxxxxxxxxxxx
Reg[          4]: xxxxxxxxxxxxxxxx ,Reg[          5]: xxxxxxxxxxxxxxxx ,Reg[
     6]: xxxxxxxxxxxxxxxx ,Reg[          7]: xxxxxxxxxxxxxxxx
Reg[          8]: xxxxxxxxxxxxxxxx ,Reg[          9]: xxxxxxxxxxxxxxxx ,Reg[
    10]: xxxxxxxxxxxxxxxx ,Reg[         11]: xxxxxxxxxxxxxxxx
Reg[         12]: xxxxxxxxxxxxxxxx ,Reg[         13]: xxxxxxxxxxxxxxxx ,Reg[
    14]: xxxxxxxxxxxxxxxx ,Reg[         15]: xxxxxxxxxxxxxxxx
Reg[         16]: xxxxxxxxxxxxxxxx ,Reg[         17]: xxxxxxxxxxxxxxxx ,Reg[
    18]: xxxxxxxxxxxxxxxx ,Reg[         19]: xxxxxxxxxxxxxxxx
Reg[         20]: xxxxxxxxxxxxxxxx ,Reg[         21]: xxxxxxxxxxxxxxxx ,Reg[
    22]: xxxxxxxxxxxxxxxx ,Reg[         23]: xxxxxxxxxxxxxxxx
Reg[         24]: xxxxxxxxxxxxxxxx ,Reg[         25]: xxxxxxxxxxxxxxxx ,Reg[
    26]: xxxxxxxxxxxxxxxx ,Reg[         27]: xxxxxxxxxxxxxxxx
Reg[         28]: xxxxxxxxxxxxxxxx ,Reg[         29]: xxxxxxxxxxxxxxxx ,Reg[
    30]: xxxxxxxxxxxxxxxx ,Reg[         31]: xxxxxxxxxxxxxxxx
--------------------------------------------------------------------------------



Time:    21   , PC=0000
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000000 ,Reg[
     2]: 0000000000000000 ,Reg[          3]: 0000000000000000
Reg[          4]: 0000000000000000 ,Reg[          5]: 0000000000000000 ,Reg[
     6]: 0000000000000000 ,Reg[          7]: 0000000000000000
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000000 ,Reg[         11]: 0000000000000000
Reg[         12]: 0000000000000000 ,Reg[         13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000000
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:    31   , PC=0004
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000000 ,Reg[
     2]: 0000000000000000 ,Reg[          3]: 0000000000000063
Reg[          4]: 0000000000000000 ,Reg[          5]: 0000000000000000 ,Reg[
     6]: 0000000000000000 ,Reg[          7]: 0000000000000000
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000000 ,Reg[         11]: 0000000000000000
```

```
Reg[          12]: 0000000000000000 ,Reg[          13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000000
Reg[          16]: 0000000000000000 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
----------------------------------------------------------------------------



Time:    41   , PC=0008
Reg[           0]: 0000000000000000 ,Reg[           1]: 0000000000000000 ,Reg[
     2]: 0000000000000000 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 0000000000000000 ,Reg[
     6]: 0000000000000000 ,Reg[           7]: 0000000000000000
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000000 ,Reg[          11]: 0000000000000000
Reg[          12]: 0000000000000000 ,Reg[          13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000000
Reg[          16]: 0000000000000000 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
----------------------------------------------------------------------------



Time:    51   , PC=000c
Reg[           0]: 0000000000000000 ,Reg[           1]: 0000000000000000 ,Reg[
     2]: 0000000000000000 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 0000000000000000 ,Reg[
     6]: 0000000000000000 ,Reg[           7]: 0000000000000000
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000000 ,Reg[          11]: 0000000000000000
Reg[          12]: 0000000000000000 ,Reg[          13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000000
Reg[          16]: 0000000000000000 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
----------------------------------------------------------------------------



Time:    61   , PC=0010
```

```
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000000 ,Reg[
     2]: 0000000000000000 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 0000000000000000 ,Reg[
     6]: 0000000000000000 ,Reg[          7]: 0000000000000000
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000000 ,Reg[         11]: 0000000000000000
Reg[         12]: 0000000000000000 ,Reg[         13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000000
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------



Time:   71   , PC=0014
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000000 ,Reg[
     2]: 0000000000000000 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: 0000000000000000 ,Reg[          7]: 0000000000000000
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000000 ,Reg[         11]: 0000000000000000
Reg[         12]: 0000000000000000 ,Reg[         13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000000
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------



Time:   81   , PC=0018
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000000 ,Reg[
     2]: 0000000000000000 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000000
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000000 ,Reg[         11]: 0000000000000000
Reg[         12]: 0000000000000000 ,Reg[         13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000000
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
```

```
----------------------------------------------------------------------------



Time:   91  , PC=001c
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000039 ,Reg[
     2]: 0000000000000000 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000000
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000000 ,Reg[         11]: 0000000000000000
Reg[         12]: 0000000000000000 ,Reg[         13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000000
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------



Time:   101  , PC=0020
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000000
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000000 ,Reg[         11]: 0000000000000000
Reg[         12]: 0000000000000000 ,Reg[         13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000000
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------



Time:   111  , PC=0024
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000000 ,Reg[         11]: 0000000000000000
Reg[         12]: 0000000000000000 ,Reg[         13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000000
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
```

```
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
----------------------------------------------------------------------------



Time:   121   , PC=0028
Reg[           0]: 0000000000000000 ,Reg[           1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000000 ,Reg[          11]: 0000000000000000
Reg[          12]: 0000000000000000 ,Reg[          13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000000
Reg[          16]: 0000000000000000 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
----------------------------------------------------------------------------



Time:   131   , PC=002c
Reg[           0]: 0000000000000000 ,Reg[           1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000000 ,Reg[          11]: 0000000000000000
Reg[          12]: 0000000000000000 ,Reg[          13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000000
Reg[          16]: 0000000000000000 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
----------------------------------------------------------------------------



Time:   141   , PC=0030
Reg[           0]: 0000000000000000 ,Reg[           1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
```

```
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000000 ,Reg[         11]: 0000000000000000
Reg[         12]: 0000000000000000 ,Reg[         13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000000
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   151   , PC=0034
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000000
Reg[         12]: 0000000000000000 ,Reg[         13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000000
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   161   , PC=0038
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000000 ,Reg[         13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000000
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------
```

```
Time:   171  , PC=003c
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000000 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000000
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   181  , PC=0040
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000000
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   191  , PC=0044
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000000
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
```

```
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   201   , PC=0048
Reg[           0]: 0000000000000000 ,Reg[           1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000000 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   211   , PC=004c
Reg[           0]: 0000000000000000 ,Reg[           1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000000 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   221   , PC=0050
Reg[           0]: 0000000000000000 ,Reg[           1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
```

```
Reg[          16]: 0000000000000000 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   231   , PC=0054
Reg[           0]: 0000000000000000 ,Reg[           1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000000 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   241   , PC=0058
Reg[           0]: 0000000000000000 ,Reg[           1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000000 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   251   , PC=00b4
Reg[           0]: 0000000000000000 ,Reg[           1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
```

```
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
      6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
     10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
     14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
     18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
     22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
     26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
     30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------



Time:   261  , PC=00b8
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000039 ,Reg[
      2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
      6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
     10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
     14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
     18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
     22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
     26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
     30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------



Time:   271  , PC=00bc
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000039 ,Reg[
      2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
      6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
     10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
     14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000000 ,Reg[         17]: 0000000000000000 ,Reg[
     18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
     22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
     26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
     30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------
```

```
Time:   281  , PC=00c0
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
-------------------------------------------------------------------------------



Time:   291  , PC=00c4
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
-------------------------------------------------------------------------------



Time:   301  , PC=00c8
Reg[          0]: 0000000000000000 ,Reg[          1]: 0000000000000039 ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
```

```
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   311  , PC=0068
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   321  , PC=006c
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   331  , PC=0070
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
```

```
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:    341   , PC=0074
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:    351   , PC=0078
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:    361   , PC=007c
```

```
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
-------------------------------------------------------------------------------



Time:   371  , PC=0080
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
-------------------------------------------------------------------------------



Time:   381  , PC=00ec
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
```

```
--------------------------------------------------------------------------------



Time:   391  , PC=00f0
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   401  , PC=00f4
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000000 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   411  , PC=00f8
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000000
```

```
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   421   , PC=00fc
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   431   , PC=0100
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000000
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   441   , PC=0090
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
```

```
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------



Time:   451   , PC=0094
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------



Time:   461   , PC=010c
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------
```

```
Time:   471  , PC=0110
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
-------------------------------------------------------------------------------



Time:   481  , PC=0114
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000000
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
-------------------------------------------------------------------------------



Time:   491  , PC=0118
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
```

```
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   501  , PC=011c
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   511  , PC=0120
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   521  , PC=00a4
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
```

```
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   531  , PC=00a8
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   541  , PC=0130
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   551  , PC=0134
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
```

```
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------



Time:    561   , PC=0138
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------



Time:    571   , PC=013c
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------
```

```
Time:   581  , PC=0140
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   591  , PC=0144
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   601  , PC=0148
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
```

```
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   611  , PC=014c
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   621  , PC=0150
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   631  , PC=0154
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
```

```
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   641   , PC=0158
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   651   , PC=015c
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   661   , PC=0160
```

```
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
-------------------------------------------------------------------------------



Time:   671  , PC=0164
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
-------------------------------------------------------------------------------



Time:   681  , PC=0168
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
```

```
--------------------------------------------------------------------------------



Time:   691  , PC=016c
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   701  , PC=0170
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   711  , PC=0174
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
```

```
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   721   , PC=0178
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   731   , PC=017c
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   741   , PC=0180
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
```

```
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------



Time:    751   , PC=0184
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------



Time:    761   , PC=0188
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------
```

```
Time:   771  , PC=018c
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
------------------------------------------------------------------------------



Time:   781  , PC=0190
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
------------------------------------------------------------------------------



Time:   791  , PC=0194
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
```

```
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   801  , PC=0198
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   811  , PC=019c
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   821  , PC=01a0
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
```

```
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   831   , PC=01a4
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   841   , PC=01a8
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   851   , PC=01ac
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
```

```
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------------



Time:   861   , PC=01b0
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------------



Time:   871   , PC=01b4
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
----------------------------------------------------------------------------------
```

```
Time:   881  , PC=01b8
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   891  , PC=01bc
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   901  , PC=01c0
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
```

```
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
-------------------------------------------------------------------------------



Time:   911   , PC=01c4
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
-------------------------------------------------------------------------------



Time:   921   , PC=01c8
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
-------------------------------------------------------------------------------



Time:   931   , PC=01cc
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
```

```
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
-------------------------------------------------------------------------------



Time:    941   , PC=01d0
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
-------------------------------------------------------------------------------



Time:    951   , PC=01d4
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
-------------------------------------------------------------------------------



Time:    961   , PC=01d8
```

```
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   971  , PC=01dc
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   981  , PC=01e0
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
```

```
--------------------------------------------------------------------------------



Time:   991  , PC=01e4
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   1001  , PC=01e8
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
Reg[         20]: 0000000000000000 ,Reg[         21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[         23]: 0000000000000000
Reg[         24]: 0000000000000000 ,Reg[         25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[         27]: 0000000000000000
Reg[         28]: 0000000000000000 ,Reg[         29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[         31]: 0000000000000000
--------------------------------------------------------------------------------



Time:   1011  , PC=01ec
Reg[          0]: 0000000000000000 ,Reg[          1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[          3]: 0000000000000063
Reg[          4]: 000000000000009c ,Reg[          5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[          7]: 0000000000000001
Reg[          8]: 0000000000000000 ,Reg[          9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[         11]: 0000000000000040
Reg[         12]: 0000000000000040 ,Reg[         13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[         15]: 0000000000000001
Reg[         16]: 0000000000000001 ,Reg[         17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[         19]: 0000000000000004
```

```
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:    1021   , PC=01f0
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



Time:    1821   , PC=0330
Reg[           0]: 0000000000000000 ,Reg[           1]: 00000000000000cc ,Reg[
     2]: 0000000000000006 ,Reg[           3]: 0000000000000063
Reg[           4]: 000000000000009c ,Reg[           5]: 00000000000000ff ,Reg[
     6]: ffffffffffffffc7 ,Reg[           7]: 0000000000000001
Reg[           8]: 0000000000000000 ,Reg[           9]: 0000000000000000 ,Reg[
    10]: 0000000000000007 ,Reg[          11]: 0000000000000040
Reg[          12]: 0000000000000040 ,Reg[          13]: 0000000000000008 ,Reg[
    14]: 0000000000000000 ,Reg[          15]: 0000000000000001
Reg[          16]: 0000000000000001 ,Reg[          17]: 0000000000000000 ,Reg[
    18]: 0000000000000003 ,Reg[          19]: 0000000000000004
Reg[          20]: 0000000000000000 ,Reg[          21]: 0000000000000000 ,Reg[
    22]: 0000000000000000 ,Reg[          23]: 0000000000000000
Reg[          24]: 0000000000000000 ,Reg[          25]: 0000000000000000 ,Reg[
    26]: 0000000000000000 ,Reg[          27]: 0000000000000000
Reg[          28]: 0000000000000000 ,Reg[          29]: 0000000000000000 ,Reg[
    30]: 0000000000000000 ,Reg[          31]: 0000000000000000
--------------------------------------------------------------------------------



done!
```

Note: since `syscall` is not implemented here, a series of NOP instructions will be run by default after PC reaches EXIT. Several repeated NOP results are omitted here.

Verilog Source Code

top module

On top of the program, `top.v` interconnects different modules:

```
module top #(
  parameter ADDRESS_BITS = 16
) (
  input clock,
  input reset,

  output [63:0] wb_data
);

// Fetch Wires
    // OUTPUT OF FETCH
wire [ADDRESS_BITS-1:0] PC;

// Decode Wires -----------------------------------------------------------------
-----------------------------------------
    //OUTPUT FROM DECODE
wire next_PC_Select; //TO FETCH
wire [ADDRESS_BITS-1:0] Target_PC; //TO FETCH
wire [1:0] op_A_sel; //TO ALU MUX
wire op_B_sel;
//wire [31:0] imm32;
wire [63:0] imm64;
wire [5:0] ALU_Control;


//To Reg File
wire [4:0] read_Sel_1;
wire [4:0] read_Sel_2;
wire wEn;
wire [4:0] write_Sel;
wire mem_wEn;
wire branch_OP;
// Reg File Wires ---------------------------------------------------------------
--
wire [63:0] read_Data_1; //TO ALU A MUX
wire [63:0] read_Data_2; //TO ALU B MUX
//mem write back wires
wire wb_Sel;
// Execute Wires
wire [63:0] JALR_target_long;
wire [ADDRESS_BITS-1:0] JALR_target; // Assigned outside of ALU
wire [63:0] ALU_Res;
wire branch;
//wire for writeback to REG
wire [63:0] reg_WB_Data;

//OP A WIRE
wire [63:0] OP_A_IN;
wire [63:0] OP_B_IN;

// Memory Wires
```

```verilog
//OUTPUT FROM RAM - INSTRUCTION
wire [31:0] Instruction;
wire [63:0] d_Read_Data;

assign wb_data = reg_WB_Data;

//assign JALR_target_long = imm32 + read_Data_1;
assign JALR_target_long = imm64 + read_Data_1;
assign JALR_target = JALR_target_long[ADDRESS_BITS-1:0];

//mux for OP A and OP B - ask if in the right place
//These values are input into ALU.
assign OP_A_IN = (op_A_sel === 2'b00) ? read_Data_1:
                 (op_A_sel === 2'b01) ? PC:
                 (op_A_sel === 2'b10) ? PC+4:
                 read_Data_1;
/*
assign OP_B_IN = (op_B_sel === 1'b0) ? read_Data_2:
                 (op_B_sel === 1'b1) ? imm32:
                 imm32;
                 */

assign OP_B_IN = (op_B_sel === 1'b0) ? read_Data_2:
                 (op_B_sel === 1'b1) ? imm64:
                 imm64;
//assign mux to what is written back to REG
assign reg_WB_Data = (wb_Sel === 1'b0) ? ALU_Res:
                     (wb_Sel === 1'b1) ? d_Read_Data: //only from a load
instruction.
                      ALU_Res;

//DONE but needs to be checked
fetch #(
  .ADDRESS_BITS(ADDRESS_BITS)
) fetch_inst (
  .clock(clock),
  .reset(reset),
  .next_PC_select(next_PC_Select),
  .target_PC(Target_PC),
  .PC(PC)
);


decode #(
  .ADDRESS_BITS(ADDRESS_BITS)
) decode_unit (

  // Inputs from Fetch
  .PC(PC),
  .instruction(Instruction),

  // Inputs from Execute/ALU
  .JALR_target(JALR_target),
  .branch(branch),

  // Outputs to Fetch
  .next_PC_select(next_PC_Select),
  .target_PC(Target_PC),
  // Outputs to Reg File
  .read_sel1(read_Sel_1),
  .read_sel2(read_Sel_2),
  .write_sel(write_Sel),
  .wEn(wEn),

  // Outputs to Execute/ALU
  .branch_op(branch_OP),
  /*.imm32(imm32),*/
  .imm64(imm64),
  .op_A_sel(op_A_sel),
  .op_B_sel(op_B_sel),
  .ALU_Control(ALU_Control),

  // Outputs to Memory
  .mem_wEn(mem_wEn),

  // Outputs to Writeback
  .wb_sel(wb_Sel)

);


//DONE but needs to be checked
regFile regFile_inst (
  .clock(clock),
  .reset(reset),
  .wEn(wEn), // Write Enable
  .write_data(reg_WB_Data),
  .read_sel1(read_Sel_1),
  .read_sel2(read_Sel_2),
  .write_sel(write_Sel),
  .read_data1(read_Data_1),
  .read_data2(read_Data_2)
);



ALU alu_inst(
  .branch_op(branch_OP),
  .ALU_Control(ALU_Control),
  .operand_A(OP_A_IN),
  .operand_B(OP_B_IN),
  .ALU_result(ALU_Res),
  .ALU_branch(branch)
);


ram #(
  .ADDR_WIDTH(ADDRESS_BITS)
) data_memory (
  .clock(clock),
  // Data Port
  .wEn(mem_wEn),
  .d_address(ALU_Res[15:0]),    //ALU_Res is 64 bits, d_address is 16 bits
  .d_write_data(read_Data_2),   //write data comes from rs2 for load/store
operations
```

```
  .d_read_data(d_Read_Data)
);

inst_mem #(
  .ADDR_WIDTH(ADDRESS_BITS)
) inst_memory (
  .clock(clock),

  // Instruction Port
  .i_address(PC >> 2),
  .i_read_data(Instruction)
);

endmodule
```

fetch instruction module

`fetch.v` describes the functionality of the program counter and the fetch instruction process:

```
module fetch #(
  parameter ADDRESS_BITS = 16
) (
  input  clock,
  input  reset,
  input  next_PC_select,
  input  [ADDRESS_BITS-1:0] target_PC,
  output [ADDRESS_BITS-1:0] PC
);

reg [ADDRESS_BITS-1:0] PC_reg;

assign PC = PC_reg;


always @(posedge clock)
begin
    if(reset)
    begin
        PC_reg <= 16'b0; //not sure what should happen if reset = 0, just set PC
to 16'b0.
    end
    else if(next_PC_select)
    begin
        PC_reg <= target_PC;
    end
    else
    begin
        PC_reg <= PC + 4;
    end
end

endmodule
```

instruction memory

`inst_mem.v` describes the functionality of the instruction memory:

```
module inst_mem #(
  parameter DATA_WIDTH = 32,
  parameter ADDR_WIDTH = 16
) (
  input  clock,

  // Instruction Port
  input  [ADDR_WIDTH-1:0] i_address,
  output [DATA_WIDTH-1:0] i_read_data


);

localparam RAM_DEPTH = 1 << ADDR_WIDTH; // right shifts 1 by 64 places. Thus
there are 2^64 addresses

reg [DATA_WIDTH-1:0] inst_mem [0:RAM_DEPTH-1];


//combinational read instruction
assign i_read_data = inst_mem[i_address];

//assign d_read_data = inst_mem[d_address];

  integer n;
  initial begin

    for(n=0;n<RAM_DEPTH;n=n+1) begin
      inst_mem[n] = 32'b0;
    end

  end


endmodule
```

decode instruction module

`decode.v` describes the functionality of decoding instruction process:

```
module decode #(
  parameter ADDRESS_BITS = 16  //parameters are constants, thus you cant change
their value at runtime <- note
) (
  // Inputs from Fetch
  input [ADDRESS_BITS-1:0] PC, //curent PC value
  input [31:0] instruction,   //the the 32 bit instruction we are decoding ig

  // Inputs from Execute/ALU
  input [ADDRESS_BITS-1:0] JALR_target,  //target of JALR instruction
  input branch,      //Result of a branch instruction, 1 means branch taken
(true), 0 means not taken (false)
```

```
  // Outputs to Fetch
  output next_PC_select, //select (equivalent to PCsrc mux) 0 is PC+4, 1 is
target_PC
  output [ADDRESS_BITS-1:0] target_PC,   //selected if above is 1

  // Outputs to Reg File  - these are all inputs to Reg File
  output [4:0] read_sel1,  //read Address 1
  output [4:0] read_sel2,  //read address 2
  output [4:0] write_sel,  //write Addr
  output wEn,    //write enable

  // Outputs to Execute/ALU   -
  output branch_op, // Tells ALU if this is a branch instruction (yes)
  //output [31:0] imm32,  //the immediate
  output [63:0] imm64,  //the immediate
  output [1:0] op_A_sel,  //Select for the ALU operand_A input (00 for
read_data_1, 01 for PC, 10 for PC+4)
  output op_B_sel,  //Select for ALU operand_B input (0 for from read Data 2, 1
for Imm32)
  output [5:0] ALU_Control, //tells ALU operation

  // Outputs to Memory
  output mem_wEn, //write to memory

  // Outputs to Writeback
  output wb_sel //1 if writeback value is read from memory 0 if writeback value
comes from ALU

);

localparam [6:0]R_TYPE  = 7'b0110011, //wEn  //data2
                I_TYPE  = 7'b0010011, //wEn  //imm32
                STORE   = 7'b0100011, //NO   //imm32  //memWrite
                LOAD    = 7'b0000011, //wEn  //imm32
                BRANCH  = 7'b1100011, //NO   //data2
                JALR    = 7'b1100111, //wEn  //imm32
                JAL     = 7'b1101111,  //wEn
                AUIPC   = 7'b0010111, //wEn
                LUI     = 7'b0110111; //wEn


// Internal Wires
wire[6:0]  s_imm_msb;
wire[4:0]  s_imm_lsb;
wire[19:0] u_imm;
wire[11:0] i_imm_orig;
wire[11:0] s_imm_orig;
wire[12:0] b_imm_orig;
wire[19:0] lui_imm;

wire[31:0] b_imm_32;
wire[31:0] u_imm_32;
wire[31:0] i_imm_32;
wire[31:0] s_imm_32;
wire[31:0] uj_imm_32;
wire[31:0] lui_imm_32;
```

```
wire[63:0] b_imm_64;
wire[63:0] u_imm_64;
wire[63:0] i_imm_64;
wire[63:0] s_imm_64;
wire[63:0] uj_imm_64;
wire[63:0] lui_imm_64;

wire [6:0] opcode;
wire [6:0] funct7;
wire [2:0] funct3;
wire [1:0] extend_sel;
wire [ADDRESS_BITS-1:0] branch_target;
wire [ADDRESS_BITS-1:0] JAL_target;


// Read registers
assign read_sel2  = instruction[24:20];
assign read_sel1  = (opcode == LUI) ? 5'b0 : instruction[19:15]; //Adding x0 to
upper instruction in ALU, in order to writeback the lui_imm_32

/* Instruction decoding */
assign opcode = instruction[6:0];
assign funct7 = instruction[31:25];
assign funct3 = instruction[14:12];

/* Write register */
assign write_sel = instruction[11:7];




//I-type imm's
assign i_imm_orig = instruction[31:20];
assign i_imm_32 = {{20{i_imm_orig[11]}},i_imm_orig};
assign i_imm_64 = {{52{i_imm_orig[11]}},i_imm_orig};
//S-type imm's
assign s_imm_msb = instruction[31:25];
assign s_imm_lsb = instruction[11:7];
assign s_imm_orig = {s_imm_msb, s_imm_lsb};
assign s_imm_32 = {{20{s_imm_orig[11]}},s_imm_orig};
assign s_imm_64 = {{52{s_imm_orig[11]}},s_imm_orig};
//U-type imm's
assign u_imm = instruction[31:12];
assign u_imm_32 = { {12{u_imm[19]}},u_imm };
assign u_imm_64 = { {44{u_imm[19]}},u_imm };
//Branch imm's
//Note: we have assumed that the immediate value provided for branch instructions
only needs shifted left once.
assign b_imm_orig = { instruction[31], instruction[7], instruction[30:25],
instruction[11:8], 1'b0 }; //shift left 1
assign b_imm_32 = { {19{b_imm_orig[11]}}, b_imm_orig };
assign b_imm_64 = { {51{b_imm_orig[11]}}, b_imm_orig };
//imm for JAL
assign uj_imm_32 = { {11{u_imm[19]}},{u_imm[19]},{u_imm[7:0]},{u_imm[8]},
{u_imm[18:9]},1'b0 };
assign uj_imm_64 = { {43{u_imm[19]}},{u_imm[19]},{u_imm[7:0]},{u_imm[8]},
{u_imm[18:9]},1'b0 };
//imm for LUI
```

```
assign lui_imm = instruction[31:12];
assign lui_imm_32 = { lui_imm, 12'b0 };
assign lui_imm_64 = {32'b0, lui_imm, 12'b0 };//?is it right? add 32'b0 to the
left

assign next_PC_select = (branch===1) ? 1'b1:
                        (opcode===JAL) ? 1'b1:
                        (opcode===JALR) ? 1'b1:
                        1'b0;

assign wEn = (opcode === R_TYPE)? 1'b1:
             (opcode === I_TYPE)? 1'b1:
             (opcode === STORE) ? 1'b0:
             (opcode === LOAD) ? 1'b1:
             (opcode === BRANCH) ? 1'b0:
             (opcode === JAL) ? 1'b1:
             (opcode === JALR) ? 1'b1:
             (opcode === LUI) ? 1'b1:
             (opcode === AUIPC) ? 1'b1:
             1'b0;

assign op_B_sel= (opcode === R_TYPE)? 1'b0:
                 (opcode === I_TYPE)? 1'b1:
                 (opcode === STORE) ? 1'b1:
                 (opcode === LOAD) ? 1'b1:
                 (opcode === BRANCH) ? 1'b0:
                 (opcode === JAL) ? 1'b1:
                 (opcode === JALR) ? 1'b1:
                 (opcode === LUI) ? 1'b1:
                 (opcode === AUIPC) ? 1'b1:
                 1'b0;

assign op_A_sel = (opcode === R_TYPE)? 2'b00:
                  (opcode === I_TYPE)? 2'b00:
                  (opcode === STORE) ? 2'b00:
                  (opcode === LOAD) ? 2'b00:
                  (opcode === BRANCH) ? 2'b00:
                  (opcode === JAL) ? 2'b10:      //put PC+4 in rd
                  (opcode === JALR) ? 2'b10:     //put PC+4 in rd
                  (opcode === LUI) ? 2'b00:      //Select x0
                  (opcode === AUIPC) ? 2'b01:
                  2'b00;

assign branch_op= (opcode === BRANCH) ? 1'b1: //tell ALU this is a branch
instruction
             1'b0;

assign mem_wEn = (opcode === STORE) ? 1'b1: //only store to memory if mem_wEn is
1
             1'b0;

assign wb_sel = (opcode === LOAD) ? 1'b1: //only write back from memory if LOAD
instruction
             1'b0;
  /*
assign imm32 = (opcode == I_TYPE) ? i_imm_32:
               (opcode === STORE) ? s_imm_32:
               (opcode === LOAD) ?  i_imm_32:
```

```
               (opcode === JAL) ? uj_imm_32:
               (opcode === JALR) ? i_imm_32:
               (opcode === LUI) ? lui_imm_32:
               (opcode === AUIPC) ? lui_imm_32:
               (opcode == BRANCH) ? b_imm_32:
               32'b0;
               */


assign imm64 = (opcode == I_TYPE) ? i_imm_64:
               (opcode === STORE) ? s_imm_64:
               (opcode === LOAD) ?  i_imm_64:
               (opcode === JAL) ? uj_imm_64:
               (opcode === JALR) ? i_imm_64:
               (opcode === LUI) ? lui_imm_64:
               (opcode === AUIPC) ? lui_imm_64:
               (opcode == BRANCH) ? b_imm_64:
               64'b0;


assign ALU_Control = (opcode === R_TYPE & funct3 === 3'b000 & funct7 ===
7'b0100000) ? 6'b001000: //SUB
                     (opcode === R_TYPE & funct3 === 3'b000 & funct7 ===
7'b0000000) ? 6'b000000: //ADD
                     (opcode === R_TYPE & funct3 === 3'b111) ? 6'b000111:  //AND
                     (opcode === R_TYPE & funct3 === 3'b110) ? 6'b000110: //OR
                     (opcode === R_TYPE & funct3 === 3'b101) ? 6'b000101: //SRL
                     (opcode === R_TYPE & funct3 === 3'b100) ? 6'b000100: //XOR
                     (opcode === R_TYPE & funct3 === 3'b011) ? 6'b000010: //SLTU
                     (opcode === R_TYPE & funct3 === 3'b010) ? 6'b000010: // SLT
                     (opcode === I_TYPE & funct3 === 3'b000) ? 6'b000000: //ADDI
                     (opcode === I_TYPE & funct3 === 3'b111) ? 6'b000111: //ANDI
                     (opcode === I_TYPE & funct3 === 3'b110) ? 6'b000110: //ORI
                     (opcode === I_TYPE & funct3 === 3'b101) ? 6'b000101: //
SRLI
                     (opcode === I_TYPE & funct3 === 3'b100) ? 6'b000100: //XORI
                     (opcode === I_TYPE & funct3 === 3'b011) ? 6'b000010:
//SLTUI
                     (opcode === I_TYPE & funct3 === 3'b010) ? 6'b000010: //SLTI
                     (opcode === BRANCH & funct3 === 3'b000) ? 6'b010000: //BEQ
                     (opcode === BRANCH & funct3 === 3'b001) ? 6'b010001: //BNE
                     (opcode === BRANCH & funct3 === 3'b100) ? 6'b010100: //BLT
                     (opcode === BRANCH & funct3 === 3'b101) ? 6'b010101: //BGE
                     (opcode === BRANCH & funct3 === 3'b110) ? 6'b010110: //BLTU
                     (opcode === BRANCH & funct3 === 3'b111) ? 6'b010111: //BGEU
                     (opcode === I_TYPE & funct3 === 3'b001) ? 6'b000001:
//**SLLI
                     (opcode === R_TYPE & funct3 === 3'b001) ? 6'b000001://**SLL
                     opcode === LOAD ? 6'b000000:   //load is just an add
                     opcode === STORE ? 6'b000000: //store is just an add
                     opcode === LUI ? 6'b000000:   //Load upper imm is just an
add
                     opcode === AUIPC ? 6'b000000: //AUIPC is just an add
                     opcode === JALR ? 6'b111111:  //pass data A through
                     opcode === JAL ? 6'b011111:   //pass data A through
                     6'b000000;

//assignment statement for TARGET_PC
```

```
/*
assign target_PC = (opcode == JALR) ? {{JALR_target[15:1]}, 1'b0}: //targetPC for
JALR instructions (PC + RS1)
                    (opcode == BRANCH) ? b_imm_32 + PC:
                    imm32 + (PC+4);
    */
assign target_PC = (opcode == JALR) ? {{JALR_target[15:1]}, 1'b0}: //targetPC
for JALR instructions (PC + RS1)
                    (opcode == BRANCH) ? b_imm_64 + PC:
                    imm64 + (PC+4);

endmodule
```

register file

`regFile.v` describes the functionality of register file management:

```
module regFile (
  input clock,
  input reset,
  input wEn,      // Write Enable
  input [63:0] write_data,
  input [4:0] read_sel1,
  input [4:0] read_sel2,
  input [4:0] write_sel,
  output [63:0] read_data1,
  output [63:0] read_data2
);

reg   [63:0] register_file[0:31];


assign read_data1 = register_file[read_sel1];
assign read_data2 = register_file[read_sel2];
integer i; //for the for-loop

always @(posedge clock)
begin
    if(reset)
    begin
        for(i=0; i<32; i=i+1) begin
            register_file[i] <= 64'b0;
        end
    end
    else if( (wEn == 1) && (write_sel != 5'b0))
    begin
        register_file[write_sel] <= write_data;
    end

end

endmodule
```

ALU

`alu.v` describes the functionality of the arithmetic logic unit(ALU):

```
module ALU (
  input [5:0]  ALU_Control,
  input [63:0] operand_A,
  input [63:0] operand_B,
  input branch_op,
  output ALU_branch,
  output [63:0] ALU_result
);


assign ALU_branch = (~branch_op) ? 1'b0:
   //if not branch_op, branch = 0
            (ALU_Control == 6'b010100) ? $signed(operand_A) <
$signed(operand_B):   //BLT
            (ALU_Control == 6'b010101) ? $signed(operand_A) >=
$signed(operand_B):  //BGE
            (ALU_Control == 6'b010110) ? operand_A < operand_B:
    //BLTU
            (ALU_Control == 6'b010111) ? operand_A >= operand_B:
   //BGEU
            (ALU_Control == 6'b010000) ? operand_A == operand_B:
   //BEQ
            (ALU_Control == 6'b010001) ? operand_A != operand_B:
   //BNE
            0;
   //default to not branching

assign ALU_result = (ALU_Control == 6'b000000) ? operand_A + operand_B:
    //ADD
            (ALU_Control == 6'b001000) ? operand_A - operand_B:
    //SUB
            (ALU_Control == 6'b011111) ? operand_A:
    //JAL pass operand_A
            (ALU_Control == 6'b111111) ? operand_A + operand_B:
     //**JALR pass operand_A + operand_B
            (ALU_Control == 6'b000010) ? $signed(operand_A) <
$signed(operand_B):   //SLT, SLTI
            (ALU_Control == 6'b000011) ? operand_A < operand_B:
    //SLTIU, SLTU
            (ALU_Control == 6'b000100) ? operand_A ^ operand_B:
    //XOR, XORI
            (ALU_Control == 6'b000110) ? operand_A | operand_B:
    //ORI
            (ALU_Control == 6'b000111) ? operand_A & operand_B:
   //AND,ANDI
            (ALU_Control == 6'b000001) ? operand_A << operand_B:
   //SLLI, logical shift left Immediate
            (ALU_Control == 6'b000101) ? operand_A >> operand_B:
   //SRLI, Logical shift right immediate
            (ALU_Control == 6'b001101) ? operand_A >>> operand_B:
    //SRAI, Arithmetic shift right immediate
```

```
                64'hFFFFFFFF;
        //de facto error code

endmodule
```

data memory

`ram.v` describes the functionality of the data memory:

```
module ram #(
  parameter DATA_WIDTH = 64,
  parameter ADDR_WIDTH = 16
) (
  input  clock,
/*
  // Instruction Port
  input  [ADDR_WIDTH-1:0] i_address,
  output [DATA_WIDTH-1:0] i_read_data,
*/
  // Data Port
  input  wEn,
  input  [ADDR_WIDTH-1:0] d_address,
  input  [DATA_WIDTH-1:0] d_write_data,
  output [DATA_WIDTH-1:0] d_read_data

);

localparam RAM_DEPTH = 1 << ADDR_WIDTH; // right shifts 1 by 16 places. Thus
there are 2^16 addresses

reg [DATA_WIDTH-1:0] ram [0:RAM_DEPTH-1];


//combinational read instruction
//assign i_read_data = ram[i_address];

assign d_read_data = ram[d_address];

  integer n;
  initial begin

    for(n=0;n<RAM_DEPTH;n=n+1) begin
      ram[n] = 64'b0;
    end

  end
//sequential write data
always @(posedge clock)
begin
    if(wEn)
    begin
        ram[d_address] <= d_write_data;
    end

end
```

```
endmodule
```

test benches

Finally, several test benches is included to test and simulate the program:

`top_tb.v`

```
module top_tb();

reg clock;
reg reset;

wire [63:0] result;

integer x;
integer i;

top dut (
  .clock(clock),
  .reset(reset),
  .wb_data(result)
);

always #5 clock = ~clock;

task print_state;
  begin
    $display("Time:\t%0d  , PC=%h", $time,dut.PC);
    for( x=0; x<32; x=x+4) begin
      $display("Reg[%d]: %h ,Reg[%d]: %h ,Reg[%d]: %h ,Reg[%d]: %h "
       ,x, dut.regFile_inst.register_file[x],x+1,
dut.regFile_inst.register_file[x+1]
       ,x+2, dut.regFile_inst.register_file[x+2],x+3,
dut.regFile_inst.register_file[x+3]);
    end
    $display("------------------------------------------------------------------
---------------");
    $display("\n\n");
  end
endtask

initial begin
  clock = 1'b1;
  reset = 1'b1;

    print_state();


  $readmemh("E:/JI/3 JUNIOR/2021 summer/ve370/7-5alutest.txt",
dut.inst_memory.inst_mem);


  for( x=0; x<32; x=x+1) begin
    dut.regFile_inst.register_file[x] = 64'b0;
  end


  #1
  #20
  reset = 1'b0; //PC now at 0, should begin executing instructions
  print_state();

for( i=0; i<100; i=i+1) begin
#10
       print_state();
end
  #800
  print_state();

   #100
    $display("done!\n");
  $stop();

end

endmodule
```

`fetch_tb.v`

```
module fetch_tb();

parameter ADDRESS_BITS = 16;

reg clock;
reg reset;
reg next_PC_select;
reg [ADDRESS_BITS-1:0] target_PC;
wire [ADDRESS_BITS-1:0] PC;

fetch #(
  .ADDRESS_BITS(ADDRESS_BITS)
) uut (
  .clock(clock),
  .reset(reset),
  .next_PC_select(next_PC_select),
  .target_PC(target_PC),
  .PC(PC)
);

always #5 clock = ~clock;


initial begin
  clock = 1'b1;
  reset = 1'b1;
  next_PC_select = 1'b1;
  target_PC = 16'h0000;
  #1
  #10
  reset = 1'b0;
  next_PC_select = 1'b0;

  #10
  $display("PC: %h", PC);

  /****************************
  * Add more test cases here *
  ****************************/
  #10
  $display("PC: %h", PC);
    #10
  $display("PC: %h", PC);
    #10
  $display("PC: %h", PC);
    #10
  $display("PC: %h", PC);
    #10
  $display("PC: %h", PC);
    #10
  $display("PC: %h", PC);
    #10
  $display("PC: %h", PC);
    #10
  $display("PC: %h", PC);

  #100
  $stop();

end

endmodule
```

`decode_tb.v`

```
module decode_tb();

parameter NOP = 32'b000000000000_00000_000_00000_0010011; // addi zero, zero, 0
parameter ADDRESS_BITS = 16;

// Inputs from Fetch
reg [ADDRESS_BITS-1:0] PC;
reg [31:0] instruction;

// Inputs from Execute/ALU
reg [ADDRESS_BITS-1:0] JALR_target;
reg branch;

// Outputs to Fetch
wire next_PC_select;
```

```verilog
wire [ADDRESS_BITS-1:0] target_PC;

// Outputs to Reg File
wire [4:0] read_sel1;
wire [4:0] read_sel2;
wire [4:0] write_sel;
wire wEn;

// Outputs to Execute/ALU
wire branch_op; // Tells ALU if this is a branch instruction
//wire [31:0] imm32;
wire [63:0] imm64;
wire [1:0] op_A_sel;
wire op_B_sel;
wire [5:0] ALU_Control;

// Outputs to Memory
wire mem_wEn;

// Outputs to Writeback
wire wb_sel;

decode #(
  .ADDRESS_BITS(ADDRESS_BITS)
) uut (

  // Inputs from Fetch
  .PC(PC),
  .instruction(instruction),

  // Inputs from Execute/ALU
  .JALR_target(JALR_target),
  .branch(branch),

  // Outputs to Fetch
  .next_PC_select(next_PC_select),
  .target_PC(target_PC),

  // Outputs to Reg File
  .read_sel1(read_sel1),
  .read_sel2(read_sel2),
  .write_sel(write_sel),
  .wEn(wEn),

  // Outputs to Execute/ALU
  .branch_op(branch_op), // Tells ALU if this is a branch instruction
  //.imm32(imm32),
  .imm64(imm64),
  .op_A_sel(op_A_sel),
  .op_B_sel(op_B_sel),
  .ALU_Control(ALU_Control),

  // Outputs to Memory
  .mem_wEn(mem_wEn),

  // Outputs to Writeback
  .wb_sel(wb_sel)
);



task print_state;
  begin
    $display("Time:         %0d", $time);
    $display("instruction:  %b", instruction);
    $display("PC:           %h", PC);
    $display("JALR_target:  %h", JALR_target);
    $display("branch        %b", branch);
    $display("next_PC_sel   %b", next_PC_select);
    $display("target_PC     %h", target_PC);
    $display("read_sel1:    %d", read_sel1);
    $display("read_sel2:    %d", read_sel2);
    $display("write_sel:    %d", write_sel);
    $display("wEn:          %b", wEn);
    $display("branch_op:    %b", branch_op);
    //$display("imm32:        %b", imm32);
    $display("imm64:        %b", imm64);
    $display("op_A_sel:     %b", op_A_sel);
    $display("op_B_sel:     %b", op_B_sel);
    $display("ALU_Control:  %b", ALU_Control);
    $display("mem_wEn:      %b", mem_wEn);
    $display("wb_sel:       %b", wb_sel);
    $display("-----------------------------------------------------------------
--------------");
    $display("\n\n");
  end
endtask



initial begin
  $display("Starting Decode Test");
  $display("-------------------------------------------------------------------
------------");
  instruction = NOP;
  PC          = 0;
  JALR_target = 0;
  branch      = 0;

  #10
  // Display output of NOP instruction
  // Remember: want op_A_sel = 00 and op_B_sel = 1 for addi instructions
  $display("addi zero, zero, 0");
  print_state();
  // Test a new instruction
  instruction = 32'b111111111111_00000_000_01011_0010011; // addi a1, zero, -1

  #10
  // Here we are printing the state of the register file.
  // We should see the result of the add a6, a1, a2 instruction but not the
  // sub a7, a2, a4 instruction because there has not been a posedge clock yet
  // ^ not sure why that comment is there (from default code) because we have
not entered either of those instructions yet
  $display("addi a1, zero, -1");
  print_state();
```

```
instruction = 32'b0000000_01100_01011_000_10000_0110011; // add a6, a1, a2

#10
$display("add a6, a1, a2");
print_state();
instruction = 32'b0100000_01110_01100_000_10001_0110011; // sub a7, a2, a4

#10
$display("sub a7, a2, a4");
print_state();
instruction = 32'b0000000_01111_01011_010_01010_0110011; // slt a0, a1, a5

#10
$display("slt a0, a1, a5");
print_state();
instruction = 32'b0000000_01111_01011_100_01110_0110011; // xor a4, a1, a5

#10
$display("xor a4, a1, a5");
print_state();
instruction = 32'b0000000_01011_01101_111_01101_0110011; // and a3, a3, a1

#10
$display("and a3, a3, a1");
print_state();
instruction = 32'b011000000000_00000_000_01011_0010011; // addi a1, zero, 1536

#10
$display("addi a1, zero, 1536");
print_state();
instruction = 32'b0000000_01100_01011_010_00000_0100011; // sw a2, 0(a1);

#10
$display("sw a2, 0(a1)");
print_state();
instruction = 32'b000000000000_01011_010_10010_0000011; // lw s2, 0(a1);

#10
$display("lw s2, 0(a1)");
print_state();
instruction = NOP;

PC = 16'h0114;
instruction = 32'h0140006f; //jal zero,128 (Should jump to 0x128)

#10
$display("jal zero,128");
print_state();

JALR_target = 16'h0154; //JALR is given to use, don't worry about it right now
PC = 16'h0094;  //PC is also given to us.
instruction = 32'h0c4080e7; // jalr ra,196(ra) (should jump to ra+0x196)

#10
$display("jalr ra,196(ra)");
print_state();
```

```
  /*****************************************************************************
*
  *                     Add Test Cases Here
  *****************************************************************************
/

  //BRANCH INSTRUCTION TEST 1 - B not taken.
  PC = 16'h0004;
  branch = 0;
  instruction = 32'h00208863;

  #10
  $display("BEQ x1, x2");
  print_state();


  //BRANCH INSTRUCTION TEST 2 - B taken
  PC = 16'h0008;
  branch = 1;
  instruction = 32'h00208863;

  #10
  $display("BEQ x1, x2 - taken");
  print_state();


  //LUI instruction
  PC = 16'h0000;
  branch = 0;
  instruction = 32'hDEADB1B7; //LOAD DEADB into r1, as upper immediate

  #10
  $display("LUI rd, DEADB");
  print_state();


  //AUIPC instruction
  //add ADD DEADB (uppIMM) to PC
  PC = 16'h0004;
  instruction = 32'hDEADB197;

  #10
  $display("AUIPC rd, DEADB (Note PC = 0004 to begin");
  print_state();
  #10
  $stop();
end

endmodule
```

`ALU_tb.v`

```
module ALU_tb();

reg [5:0] ctrl;
```

```verilog
reg [63:0] opA, opB;
reg branch_op;
wire branch;
wire [63:0] result;

ALU dut (
  .ALU_Control(ctrl),
  .operand_A(opA),
  .operand_B(opB),
  .branch_op(branch_op),
  .ALU_branch(branch),
  .ALU_result(result)
);

initial begin

  branch_op = 0;
  //add 4 + 5
  ctrl = 6'b000000;
  opA = 4;
  opB = 5;
  #10
  $display("ALU Result 4 + 5: %d",result);
  #10

  //add 2 + -1
  opA = 2;//32'd2;
  opB = -1;//32'hffffffff;
  ctrl = 6'b000000;
  #10
  $display("ALU Result 2 + -1: %d", result);

  //sub 2 - (-1)
  ctrl = 6'b001000;
  opA = 2;
  opB = -1;
  #10
  $display("ALU Result 2 - (-1) %d", result);

  //slt(unsigned) 4 < 5
  ctrl = 6'b000011;
  opA = 4;
  opB = 5;
  #10
  $display("ALU Result 4 < 5: %d",result);

  //slt 4 < -1
  ctrl = 6'b000010;
  #10
  opA = 4;
  opB = -1;//32'hffffffff;
  #10
  $display("ALU Result 4 < -1: %d",result);

  //XOR
  ctrl = 6'b000100;
  opA = 32'b011;
  opB = 32'b110;
```

```
    #10
    $display("xor(0x011,0x110) = %d",result);//should be 5 (0x101)

    //AND
    ctrl = 6'b000111;
    opA = -1; //all ones
    opB = 1; //0x1
    #10
    $display("and(1,-1) = %d",result); //should be 1

    //bne
    ctrl = 6'b010001;
    branch_op = 1;
    opA = 4;
    opB = 0;
    #10
    $display("(bne 4,0) -> branch = %d",branch); //should be 1

    //bge (signed)
    ctrl = 6'b010101;
    opA = -17;
    opB = 10;
    #10
    $display("(bge -17,10) -> branch = %d", branch); //should be 0
    branch_op = 0; //done with branch tests

    //SLLI
    ctrl = 6'b000001;
    opA = 4;
    opB = 2; //shift amount
    #10
    $display("Logical shift 4 << 2 = %d",result); //result should be 16

    //JALR
    ctrl = 6'b111111;
    opA = 20;
    opB = 13;
    #10
    $display("Jump and Link. ALU_result = %d", result); //should be 33 (our JALR
  adds opA + opB, where opB is the 12-bit signed immediate)



  end

  endmodule
```

`inst_mem_tb.v`

```
 `timescale 1ns / 1ps


 module inst_mem_tb();
```

```
parameter DATA_WIDTH = 32;
parameter ADDR_WIDTH = 16;

reg  clock;

// Instruction Port
reg  [ADDR_WIDTH-1:0] i_address;
wire [DATA_WIDTH-1:0] i_read_data;

/*
// Data Port
reg  wEn;
reg  [ADDR_WIDTH-1:0] d_address;
reg  [DATA_WIDTH-1:0] d_write_data;
wire [DATA_WIDTH-1:0] d_read_data;
*/
integer x;
integer i;
inst_mem #(
  .DATA_WIDTH(DATA_WIDTH),
  .ADDR_WIDTH(ADDR_WIDTH)
) uut (
  .clock(clock),

  // Instruction Port
  .i_address(i_address),
  .i_read_data(i_read_data)/*,

  // Data Port
  .wEn(wEn),
  .d_address(d_address),
  .d_write_data(d_write_data),
  .d_read_data(d_read_data)*/
);

always #5 clock = ~clock;


initial begin
  clock = 1'b1;


  $readmemb("E:/JI/3 JUNIOR/2021 summer/ve370/7-5p2inst-test22.txt",
uut.inst_mem);


  #400
  i_address = 0;
  $display("Instruction Address %d: %b", i_address, i_read_data);

  for(i=1;i<126;i=i+1)begin
   i_address = i;
  #10
  $display("Instruction Address %d: %b", i_address, i_read_data);
  end


  #1000
  $stop();

end

endmodule
```

`ram_tb.v`

```
module ram_tb();

parameter DATA_WIDTH = 64;
parameter ADDR_WIDTH = 16;

reg  clock;
/*
// Instruction Port
reg  [ADDR_WIDTH-1:0] i_address;
wire [DATA_WIDTH-1:0] i_read_data;
*/

// Data Port
reg  wEn;
reg  [ADDR_WIDTH-1:0] d_address;
reg  [DATA_WIDTH-1:0] d_write_data;
wire [DATA_WIDTH-1:0] d_read_data;

integer x;

ram #(
  .DATA_WIDTH(DATA_WIDTH),
  .ADDR_WIDTH(ADDR_WIDTH)
) uut (
  .clock(clock),
/*
  // Instruction Port
  .i_address(i_address),
  .i_read_data(i_read_data),*/

  // Data Port
  .wEn(wEn),
  .d_address(d_address),
  .d_write_data(d_write_data),
  .d_read_data(d_read_data)

);

always #5 clock = ~clock;


initial begin
```

```
  clock = 1'b1;
  d_address = 64'b0;
  d_write_data = 64'b0;
  wEn = 1'b0;

  #10
  wEn = 1'b1;
  #10
  $display("Data Address %d: %h", d_address, d_read_data); //Data Address     0:
00000000
  d_write_data = 1;
  d_address = 4;
  #10
  $display("Data Address %d: %h", d_address, d_read_data); //Data Address     4:
00000001
  d_write_data = 2;
  d_address = 8;
  #10
  $display("Data Address %d: %h", d_address, d_read_data); //Data Address     8:
00000002
  d_write_data = 129;
  d_address = 12;
  #10
    $display("Data Address %d: %h", d_address, d_read_data);


  #1000
  $stop();

end

endmodule
```

`regFile_tb.v`

```

module regFile_tb();

reg clock, reset;

reg wEn;
reg [63:0] write_data;
reg [4:0] read_sel1;
reg [4:0] read_sel2;
reg [4:0] write_sel;
wire [63:0] read_data1;
wire [63:0] read_data2;

// Fill in port connections
regFile uut (
  .clock(clock),
  .reset(reset),
  .wEn(wEn), // Write Enable
  .write_data(write_data),
  .read_sel1(read_sel1),
  .read_sel2(read_sel2),
  .write_sel(write_sel),
  .read_data1(read_data1),
  .read_data2(read_data2)
);


always begin
    #5 clock = ~clock;
end


initial begin
  clock = 1'b1;
  reset = 1'b1;

  //write first
  #20;
  reset = 1'b0;
  wEn = 1'b1;
  write_sel = 5'b00001;
  read_sel1 = 5'b1; //read same value as write, get old value
  write_data = 32'h000F;
  #10
  write_sel = 5'b00010;
  write_data = 32'h0001;
  #10
  write_sel = 5'b00011;
  write_data = 32'h0002;
  #10
  write_sel = 5'b00100;
  write_data = 32'hFFFFFFFF;
  #10
  wEn = 1'b0;
  #10
  read_sel1 = 5'b00010; //should be 0001
  read_sel2 = 5'b00100; //should be all 1's (hex: FFFFFFFF)
  #20
  //try writing to reg 0
  write_sel = 5'b00000;
  wEn = 1'b1;
  write_data = 32'hDEADBEEF;
  read_sel1 = 5'b00000;
  #10
  wEn = 1'b0;
  #10
  read_sel1 = 5'b00000; //should be 0
  read_sel2 = 5'b00000; //should be 0

end

  // Test reads and writes to the register file here
always begin
    #15
    write_data <= write_data + 1'b1;
    //print_state();
end
```

```
endmodule
```

Peer Evaluation (to be continued)

Name	Level of contribution (0~5)	Description of contribution
Pengcheng Xu (me)	5	all the single cycle processor
Zhimin Sun	5	
Haoxiang Jin	5	
Wenhan Kou	5	