EE613:HIGH FREQUENCY ANALOG CIRCUIT DESIGN

DESIGN PROJECT-1

Task: Designing a two-stage Miller compensated opamp that takes in a differential input and provides a single-ended output.

Design Technology : 180 nm PDK(ibm018.lib), use Vdd = 1.8V , Wmin = 240 nm, and Lmin = 180 nm.

Input Stage: NMOS

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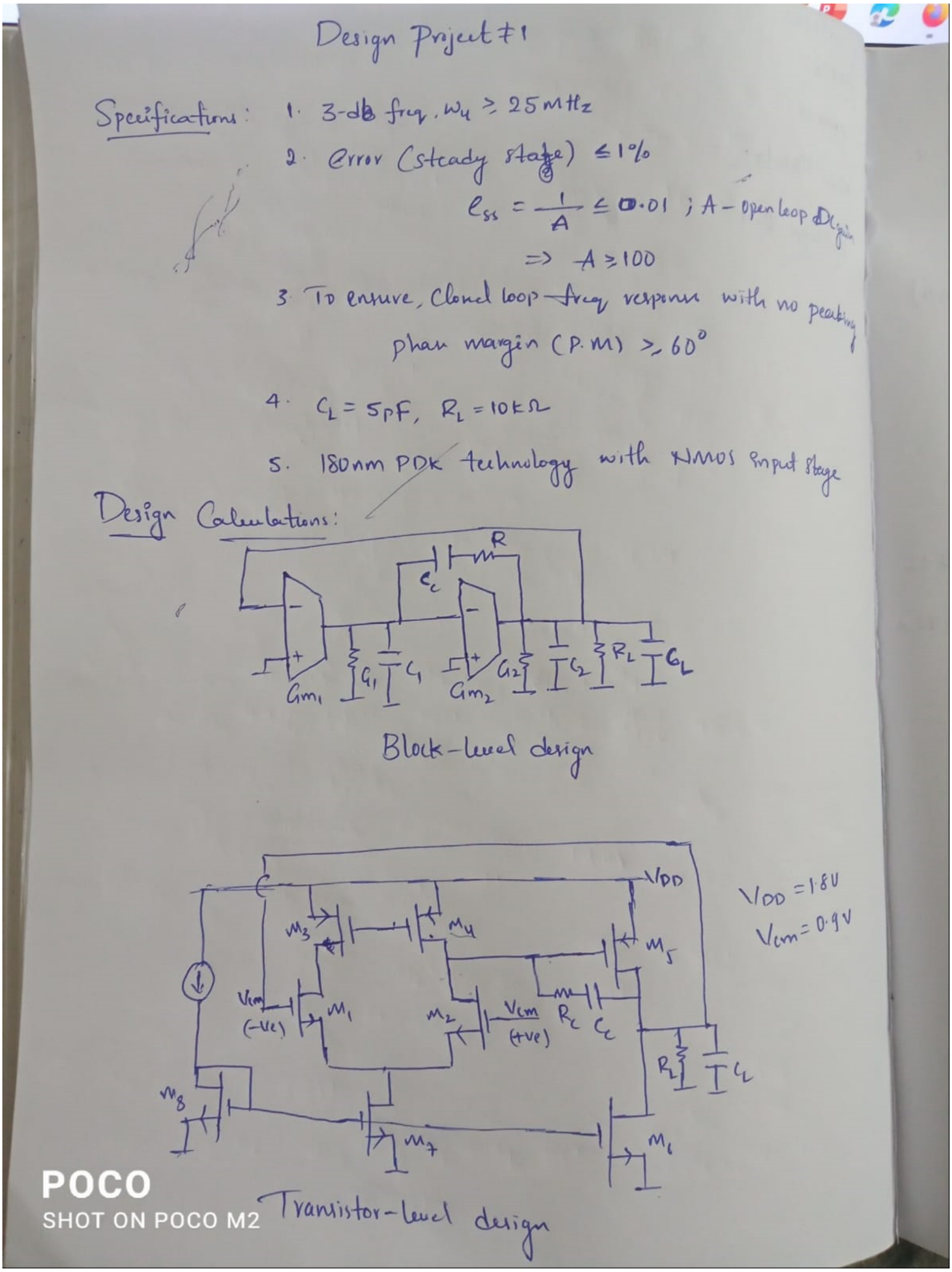
Circuit Diagram and specifications



Design Project #1

Specifications:

1. 3-dB freq, $\omega_u \geq 25\,MHz$
2. Error (steady state) $\leq 1\%$

   $e_{ss} = \frac{1}{A} \leq 0.01$; A – open loop DC gain

   $\Rightarrow A \geq 100$
3. To ensure, closed loop freq response with no peaking phase margin (P.M) $\geq 60^\circ$
4. $C_L = 5pF$, $R_L = 10k\Omega$
5. 180nm PDK technology with NMOS input stage

Design Calculations:

Block-level design

Transistor-level design

Design Calculations:

- Designing the MOSFETS using given specifications,i.e measuring the block level quantities and transistor level quantities.

- Some quantities are assumed when there are two or more unknowns present .Assumptions are done such that given specifications would be satisfied.

Design Stage 2

Step 1: take $W_u = 25MHz \times 2\pi$

$\cdot\ \phi_m = 90° - \tan^{-1}\left(\frac{W_u}{P_2}\right)$

To find P_2, Assume $\phi_m = 63°$

$\Rightarrow P_2 = 308.28M$

$P_2 = \dfrac{G_2 + G_{m_2}\left(\frac{C_c}{C_1+C_c}\right)}{C_2' + \frac{C_1 C_c}{C_1+C_c}}$ Assuming $C_1 << C_c$, $C_1 << C_2'$ $\Rightarrow P_2 = \dfrac{G_{m_2}}{C_2'}$ $C_2' = C_2 + C_L \sim C_L$

$\Rightarrow G_{m_2} = 1.54mS = g_{m_5} \Rightarrow R_c = 649.35\Omega$

→ Let us Assume $I_{D_5} = 96\mu$

$\Rightarrow \dfrac{g_{m_5}}{I_{D_5}} = 16.0V$; $\cdot$ From graph of V_{ov} vs g_m/I_D $V_{ov} = 26mV$

→ From graph of $\frac{g_m}{I_D}$ vs $\frac{I_D}{W}$

$\left(\frac{I_D}{W}\right)_5 = 1.83$

$\Rightarrow W_5 = 52.46\mu$

→ From graph of $\frac{g_m}{I_D}$ vs $\frac{g_m}{g_{ds}}$

$\left(\frac{g_m}{g_{ds}}\right)_5 = 30.32$

$\Rightarrow g_{ds,5} = 50.79\mu$

→ To avoid Symmetric offset

$\left(\frac{I_D}{W}\right)_{3,4} = \left(\frac{I_D}{W}\right)_5 = 1.83$

Step 2: Design Stage 1

$G_{m_1} = W_u \times C_c$

assume $C_c = 5pF$

$G_{m_1} = 0.785mS = g_{m_{1,2}}$

→ From $\frac{g_m}{I_D}$ vs $\frac{I_D}{W}$

$\frac{I_D}{W} = 8.8$

$\Rightarrow W_{1,2} = 5.68\mu$

To find other parameters

assume $I_{D_{1,2}} = 50\mu s = I_{D_{3,4}}$

$\Rightarrow I_{D,7} = 100\mu s$

$\left(\frac{g_m}{I_D}\right)_{1,2} = 15.7$

$V_{ov_{1,2}} = 85mV$ (From graph)

→ From $\frac{g_m}{I_D}$ vs $\frac{g_m}{g_{ds}}$

$\left(\frac{g_m}{g_{ds}}\right)_{1,2} = 26.4$

$\Rightarrow g_{ds_{1,2}} = 26.7\mu$

→ As we know from stage 2 design

$\left(\frac{I_D}{W}\right)_{3,4} = 1.83$, $\left(\frac{g_m}{I_D}\right)_{3,4} = 16.04$, $\left(\frac{g_m}{g_{ds}}\right)_{3,4} = 30.32$

$W_{3,4} = 27.32\mu$ $\Rightarrow g_{m_{3,4}} = 0.802mS$ $g_{ds_{3,4}} = 26.45\mu$

→ For $I_{D,7} = 100\mu s$, For $I_{D,6} = 96\mu$

$W_7 = 14.2\mu m$ $W_6 = 10.2$, $g_{ds_6} = 45.3\mu$

→ DC gain $A_0 = A_1 \cdot A_2$

$$A_1 = \frac{g_{m_1}}{g_{ds_2} + g_{ds_4}} = \frac{G_{m_1}}{G_1} = 14.05$$

$$A_2 = \frac{G_{m_2}}{G_2'} = \frac{g_{m_5}}{G_L + g_{ds_6} + g_{ds_5}} \simeq \frac{g_{m_5}}{G_L} = 8.1$$

$$A_0 = 113.805$$

→ $C_1 = C_{gg_5} = 85.2fF$

$C_2' = C_2 + C_L = \underbrace{C_{ds_5} + C_{d_6}}_{C_{dd} \approx 30fF} + C_L \simeq C_L = 5pF$, $C_1 << C_2'$ satisfied, $C_1 << C_c$

$C_c = 5pF$

For designing M_7, M_6.

Choose M_8 parameters such that M_7, M_6 will be in Saturation & properly biased with Currents 100μ, 96μ respectively

from Stimulations observed that, for a given Current 0.1μ for $\left(\frac{W}{L}\right)_8 > 1$, M_8 goes into Cutoff mode & also M_6, M_7

So I chose $\left(\frac{W}{L}\right)_8 < 1$

$W_8 = 240n$, $L_8 = 10\mu$

From there for $I_6 = 96\mu$, $I_7 = 100\mu$

$W_6 = 10.2\mu$ $\quad W_7 = 14.2\mu$

$L_6 = 180n$ $\quad L_7 = 180nm$

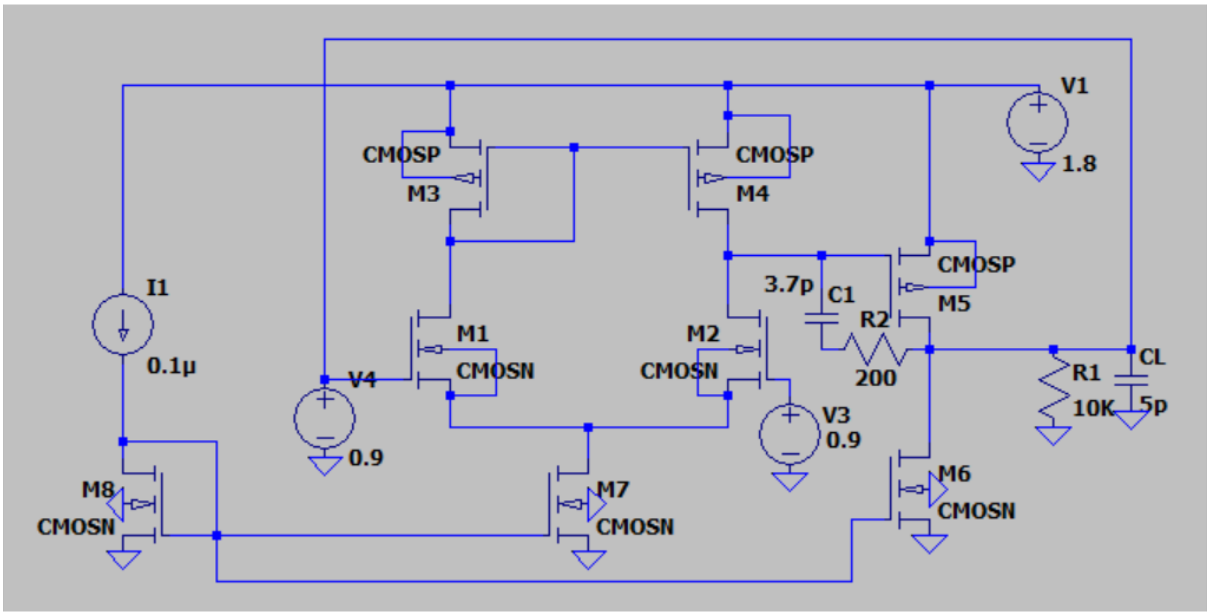
Design Calculation results

	M1/M2	M3/M4	M5	M6	M7
L(m)	180n	180n	180n	180n	180n
W(m)	5.68u	27.32u	52.46u	10.2u	14.2u
I(A)	50u	50u	96u	96u	100u

Gm1	0.785mS	A1 (1st stage gain)	14.05
G1	55.85u	A2 (2nd stage gain	8.1
Gm2	1.54m	Ao	113.805
G2	96u	P.M (phase margin)	63°
C1	85.2f	3-db frequency	25MHz
C2	30f	Rc	649.35
Cc	5p	CL	5p

STIMULATION Results:

DC analysis:



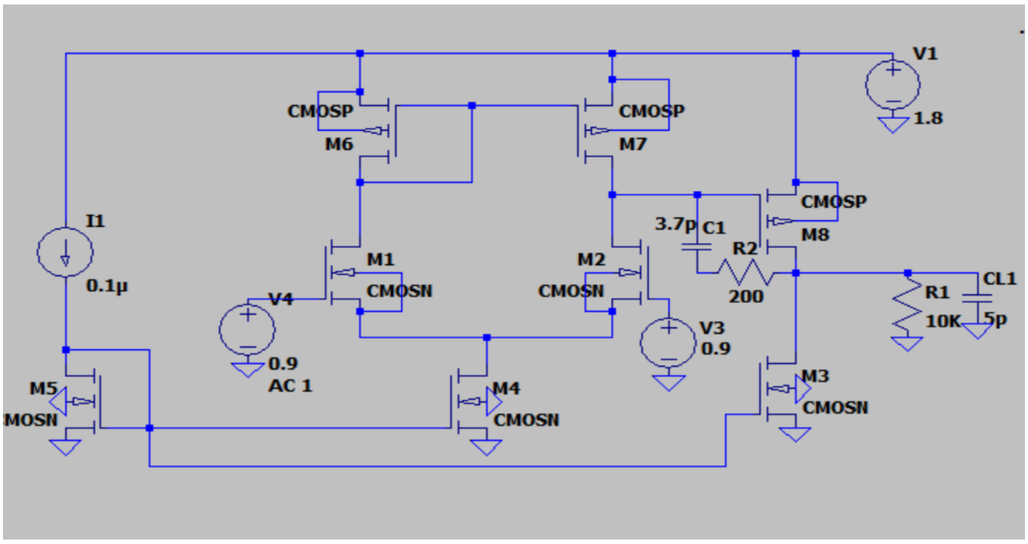
	M1/M2	**M3/M4**	**M5**	**M6**	**M7**
L(m)	180n	180n	180n	180n	180n
W(m)	5.68u	27.32u	52.46u	10.2u	14.2u
I(A)	49.9u	49.9u	118u	94.9u	99.8u

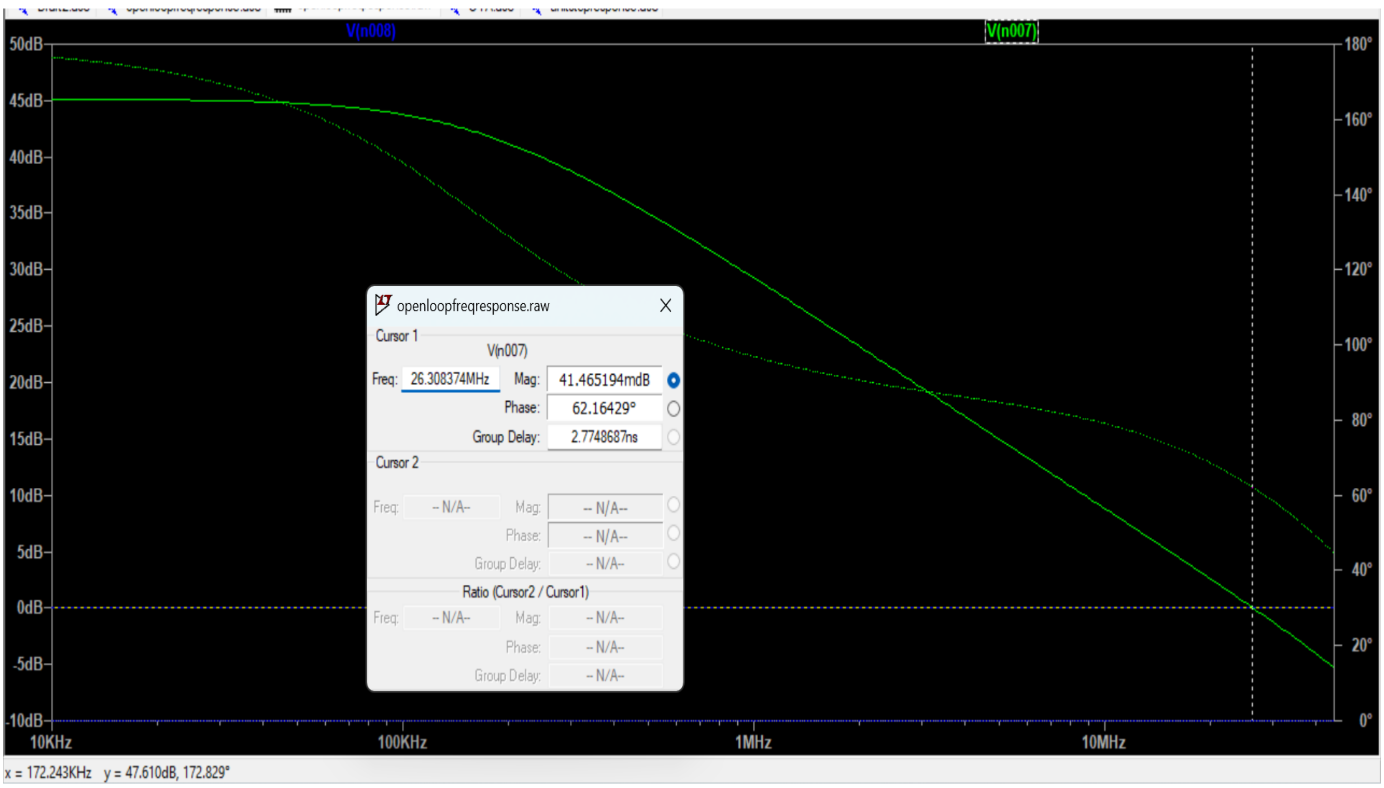
Gm1	0.8m	A1 (1st stage gain**)**	24db=15.84
G1	23.4u	A2 (2nd stage gain	21db=11.22
Gm2	1.87m	Ao	45db=177.72
G2	47.1u	P.M (phase margin)	62°
C1	85.2f	3-db frequency	26MHz
C2	27.5f	Rc	200
Cc	3.7p	CL	5p

- Reduced Rc from 649.35 to 200 to decrease phase margin from 70+ to 60+ degrees.
- Reduced Cc to increase 3-db frequency so that it is greater or equal to 25MHz

Open loop frequency response :

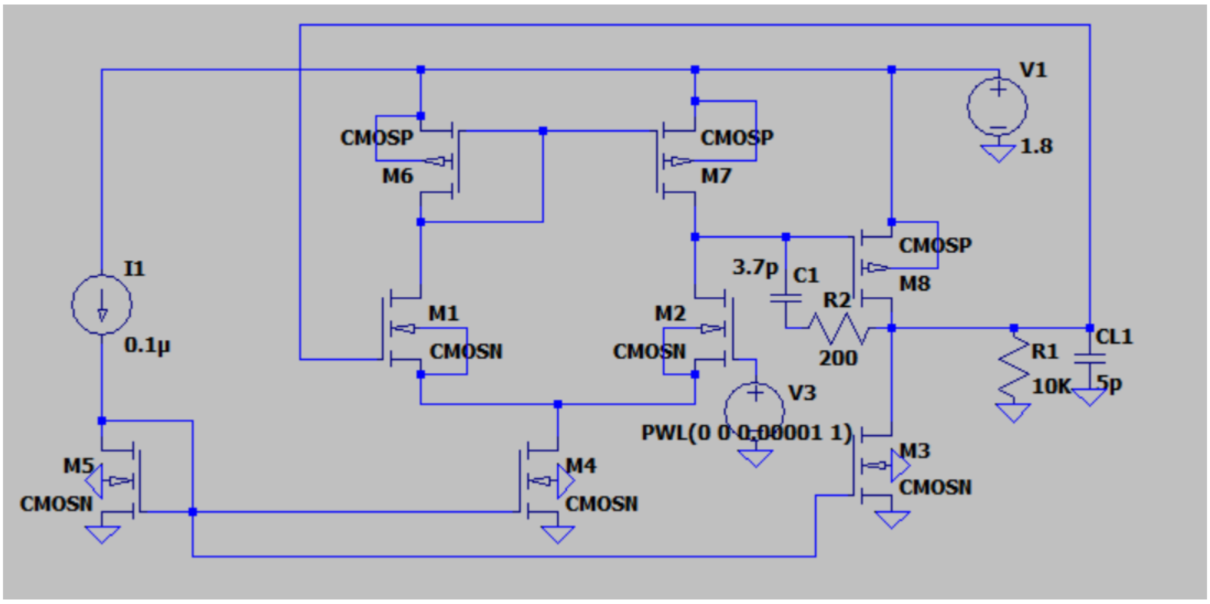
AC analysis

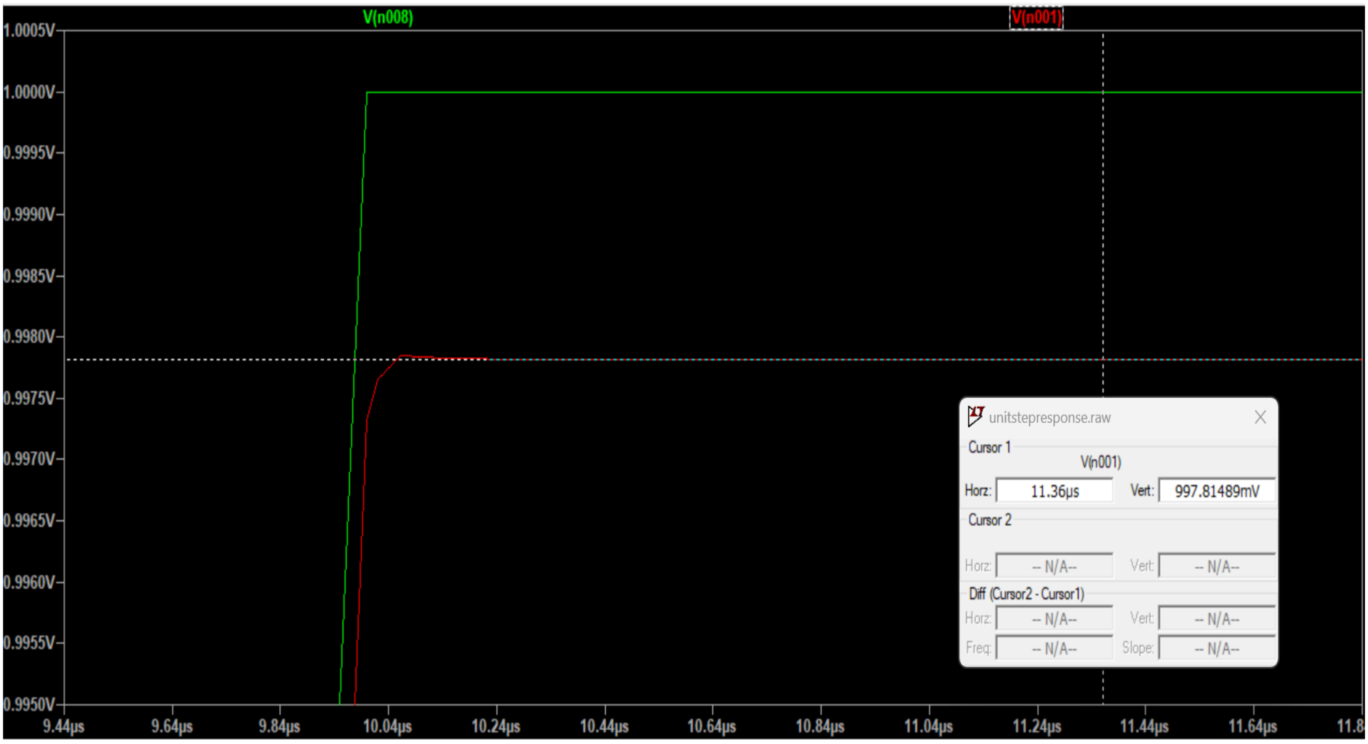




Unit step response:

Transient analysis





Weekly Report#3

Task: Designing a fully-differential two-stage opamp with CMFB.

Design Technology : 180 nm PDK(ibm018.lib), Vdd = 1.8V , Wmin = 240 nm, and Lmin = 180 nm.

Input Stage: NMOS

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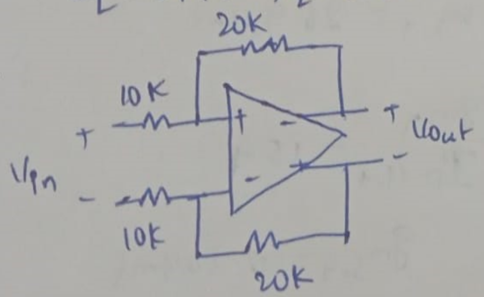
Circuit Diagram and specifications

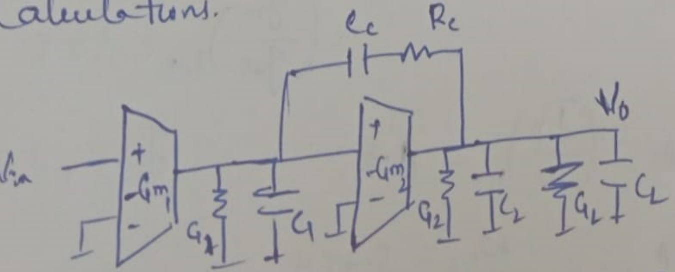
Design Project #2

Specifications:

1. 3-dB frequency, $\omega_u \geq 25MHz$
2. Error at steady state $\leq 1\%$
3. All the CMFB loops must have $PM \geq 60°$. And $\omega_u \geq \frac{25}{4} MHz$
4. $C_L = 5pF$, $R_L = 30k\Omega$
5. 

$$\frac{V_{out}}{V_{in}} = -2$$

Design Calculations:



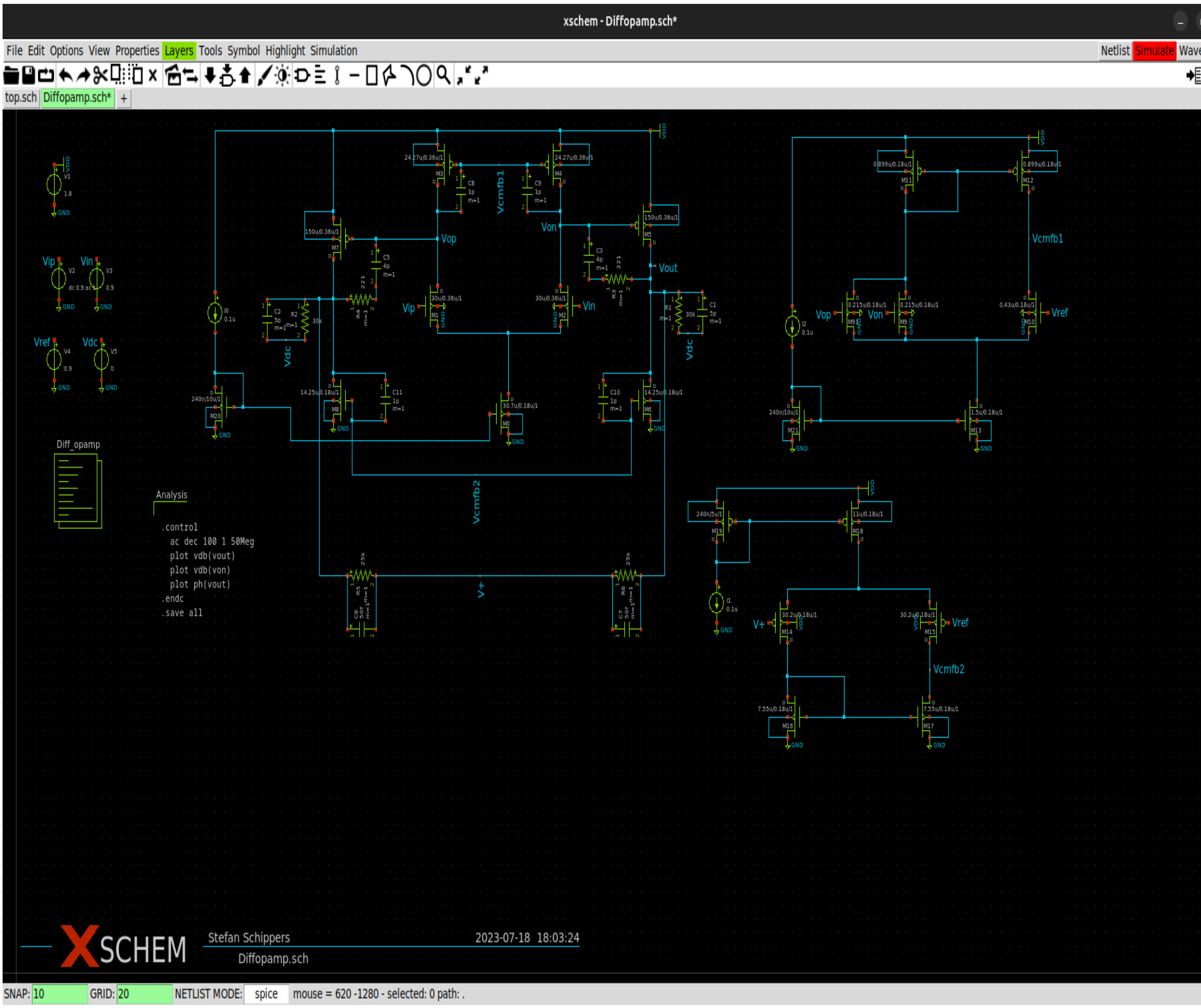
$G_L = \frac{1}{30K} = 33\mu$

$C_L = 5p$

Block-level diagram for Differential half circuit

Design results

Circuit:

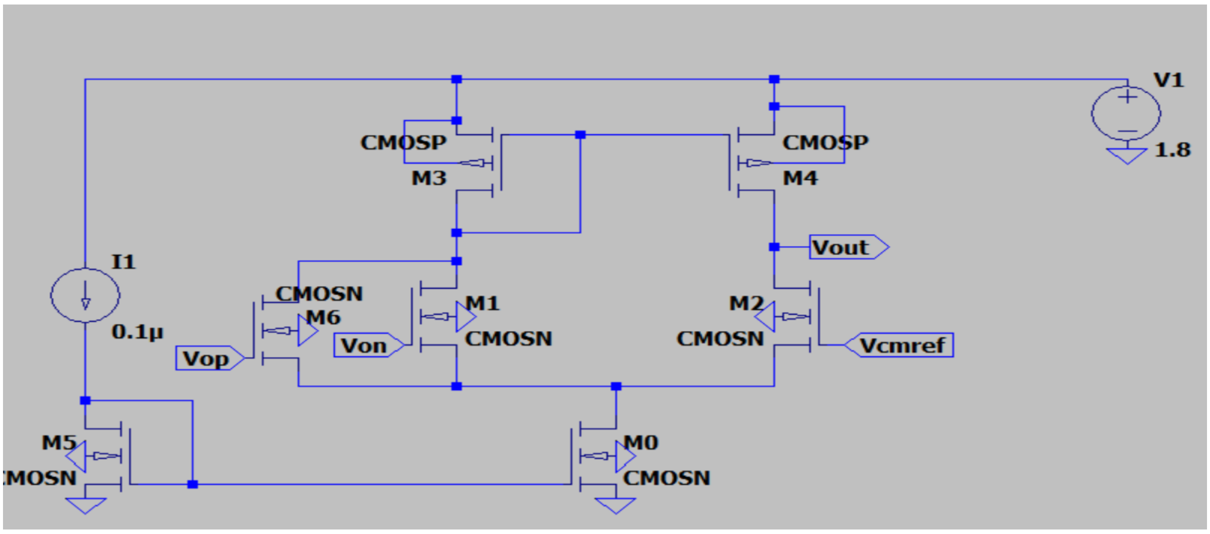


Aspect ratio:

	M1/M2	M3/M4	M5/M7	M6/M8	M0	M9
L(m)	360n	360n	360n	180n	180n	10u
W(m)	35u	24.27u	150u	14.25u	30.7u	240n

Gm1	0.785mS	A1 (1st stage gain)	26.8db
G1	56u	A2 (2nd stage gain	21.7db
Gm2	1.54m	Ao	48.5db(266)
G2	128u	P.M (phase margin)	80°
C1	1p	3-db frequency	30.4MHz
C2	1p	Rc	221
Cc	4p	CL	5p
C(cmfb#2)	50f	R(cmfb#2)	25k

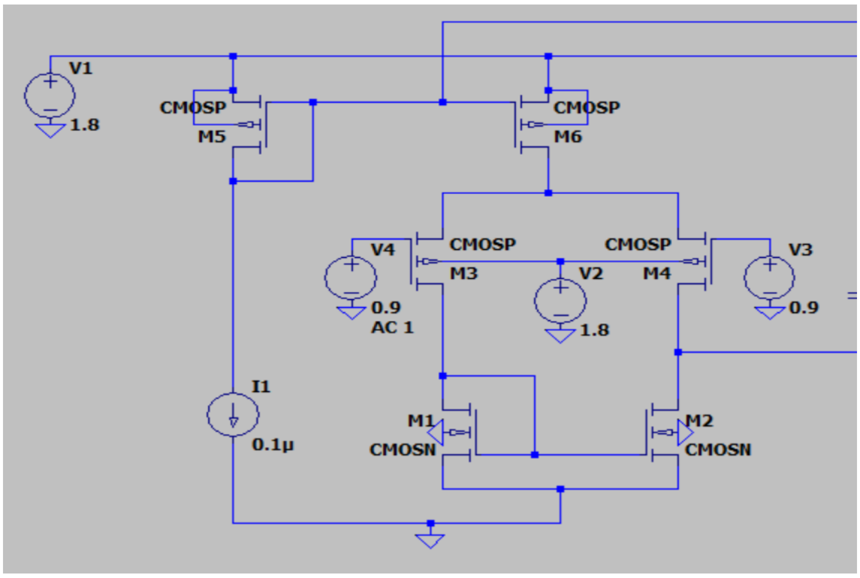
CMFB#1



Aspect ratio:

	M1/M6	M2	M4/M3	M0	M5
L(m)	180n	180n	180n	180n	10u
W(m)	0.215u	0.43u	0.899u	1.5u	240n

CMFB#2

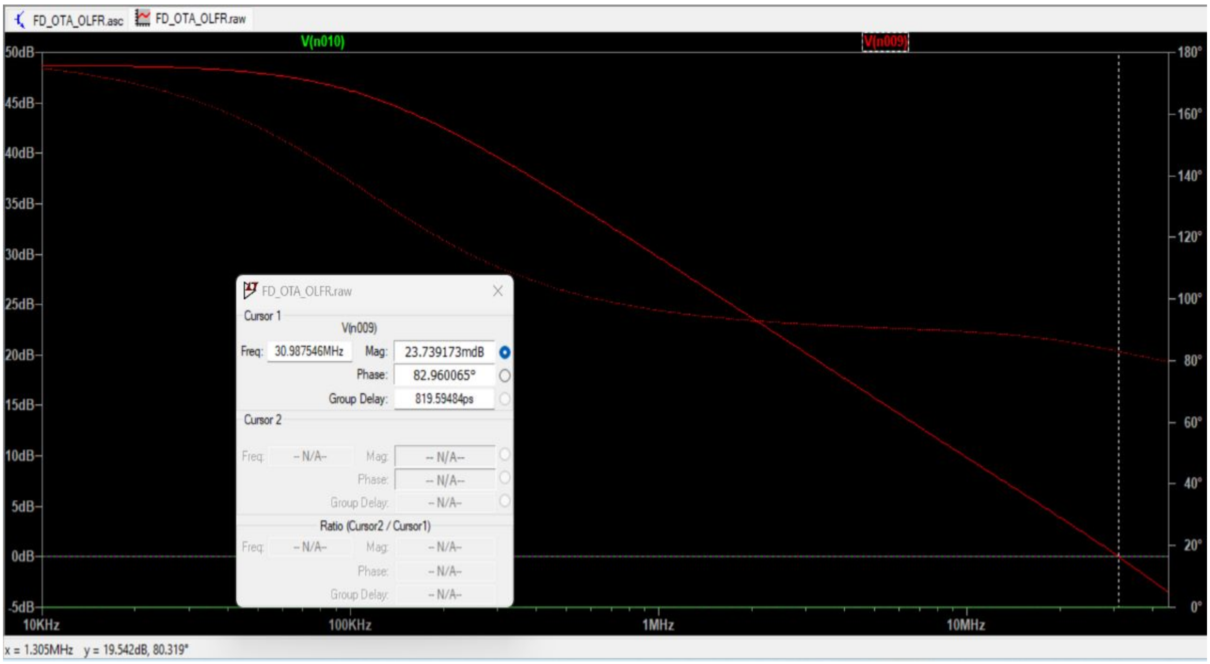


Aspect Ratio:

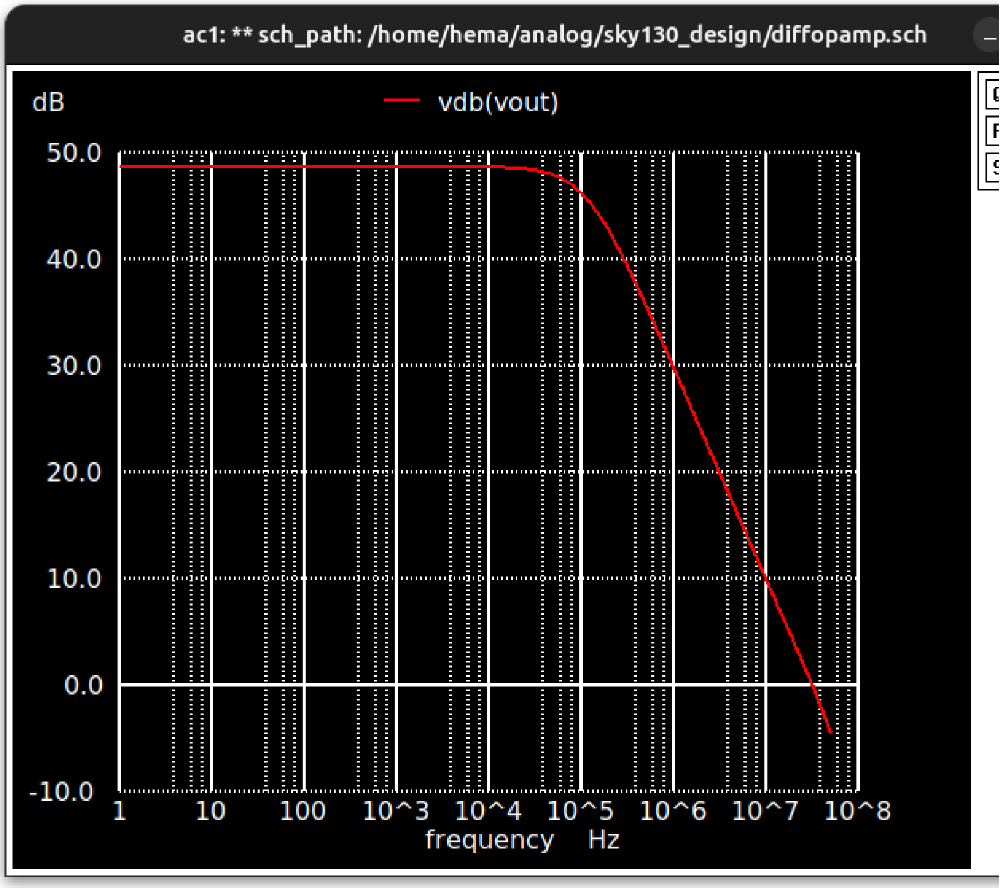
	M1/M2	M3/M4	M0	M5
L(m)	180n	180n	180n	5u
W(m)	30.2u	7.55u	11u	240n

Open loop frequency response :

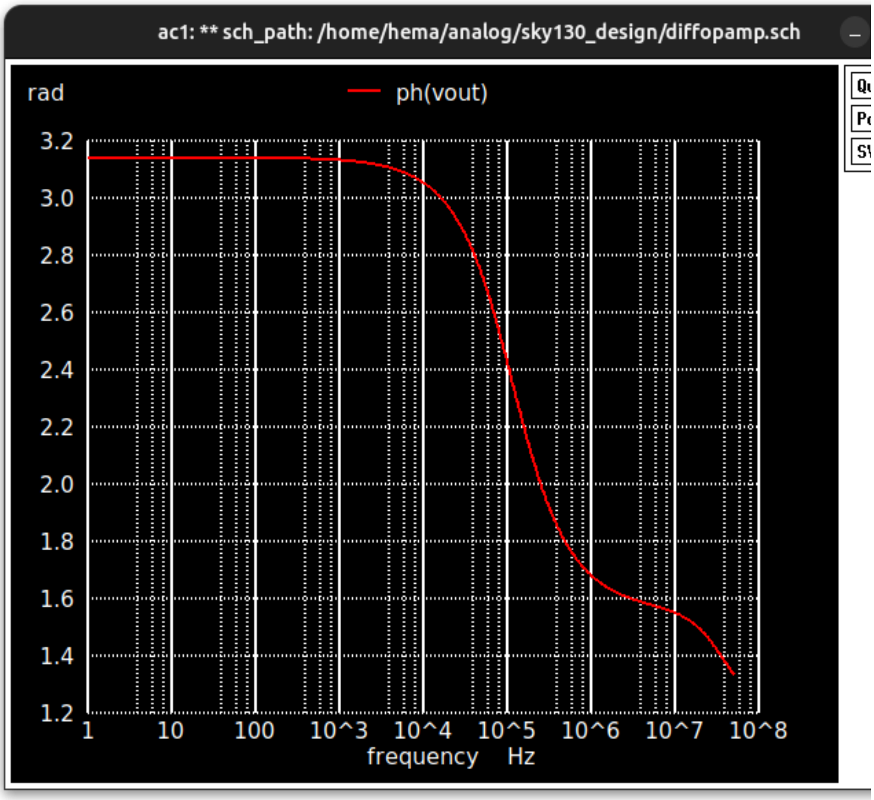
AC analysis



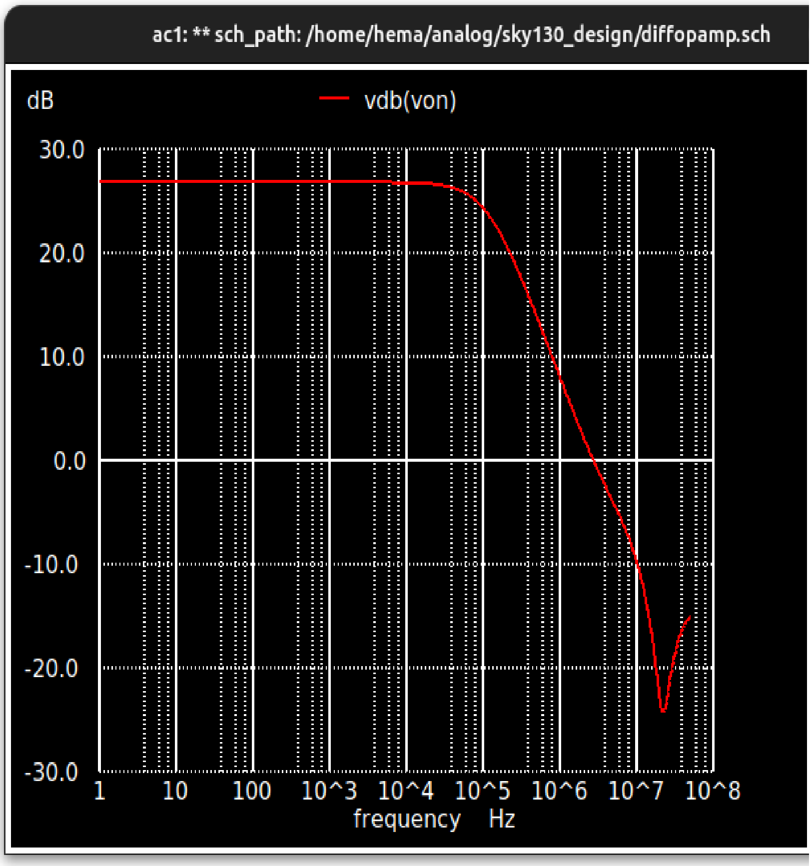
Full Stage :Gain



Full stage : phase

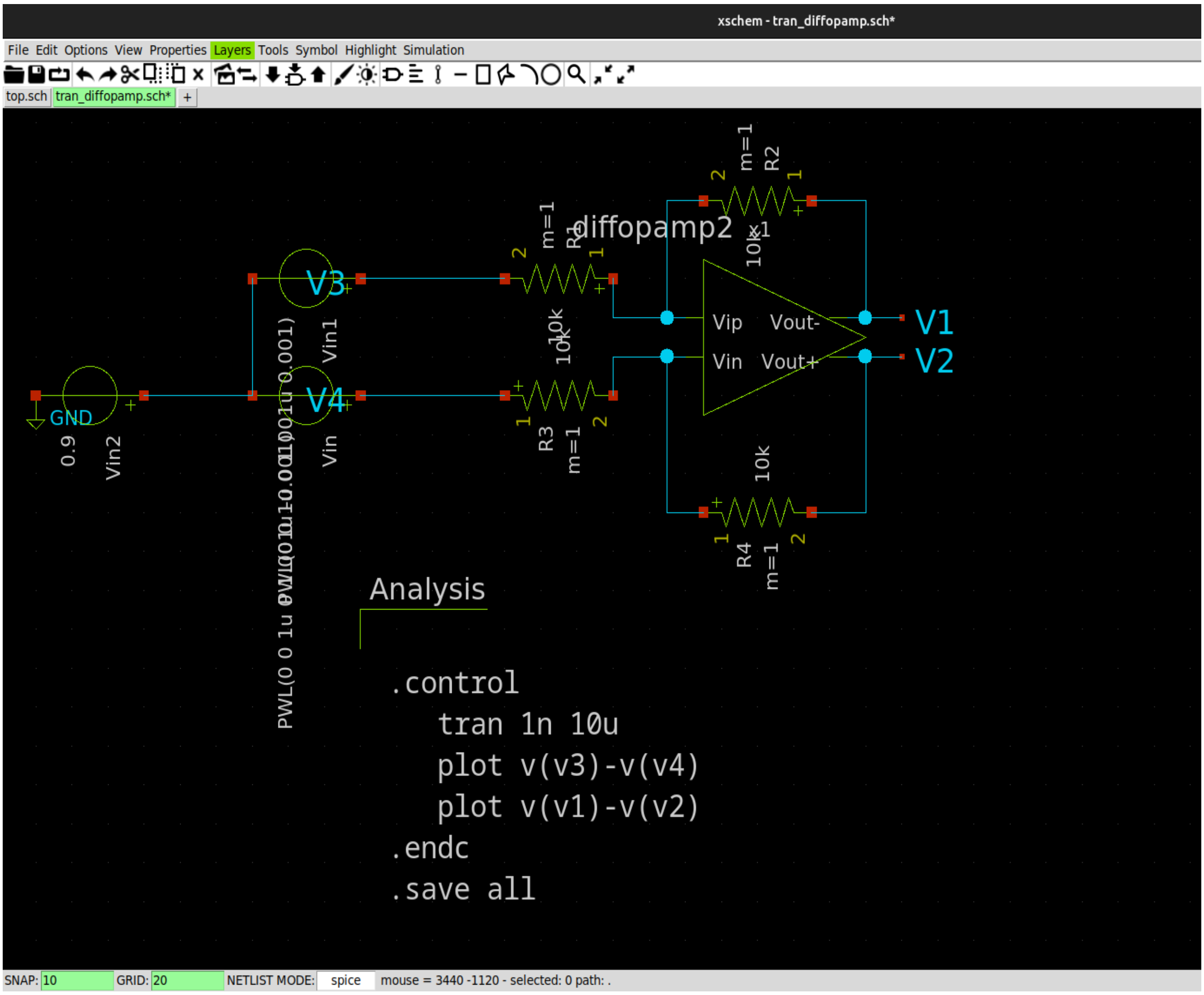


Stage-I : Gain

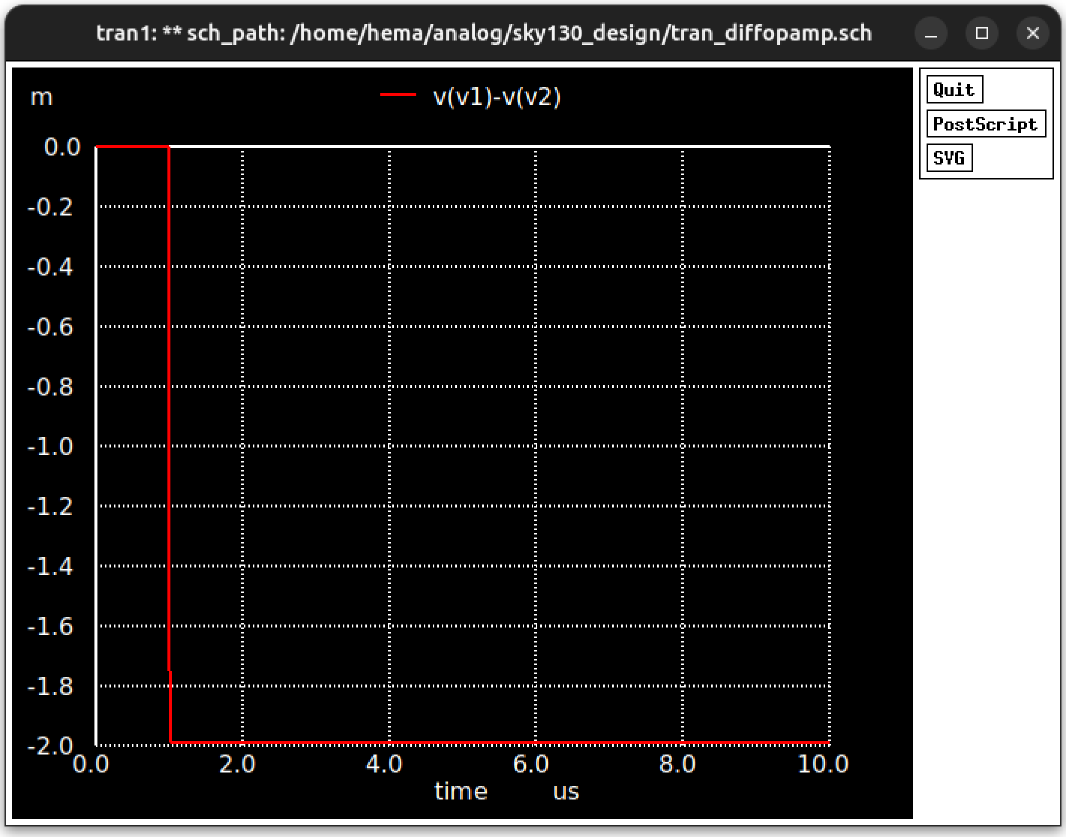


Inverting Amplifier:

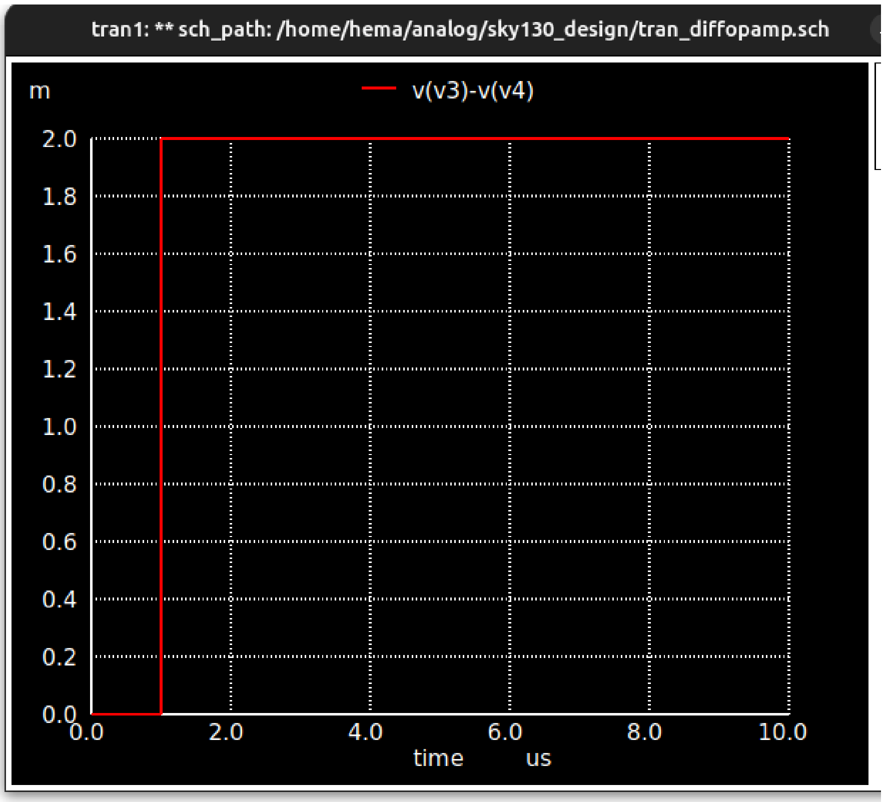
Transient analysis



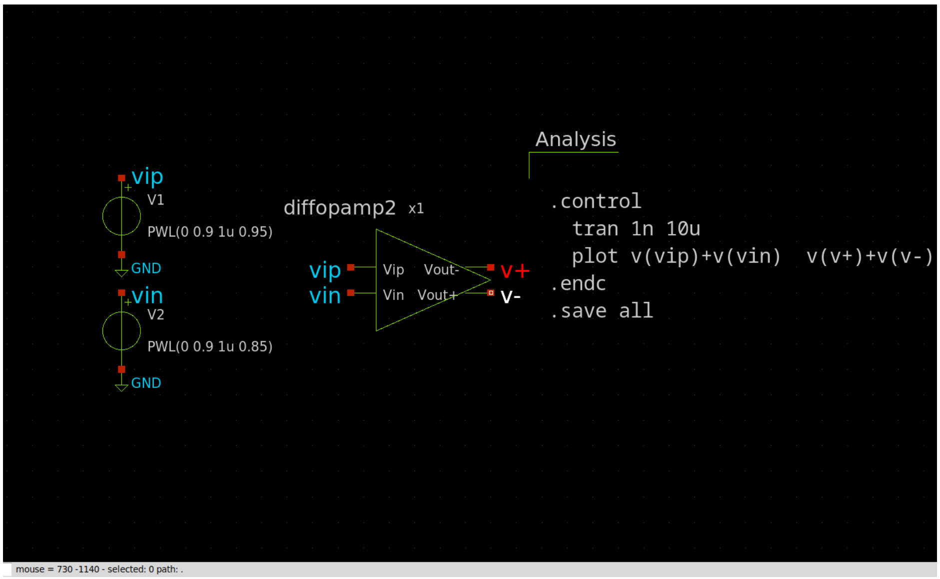
OUTPUT

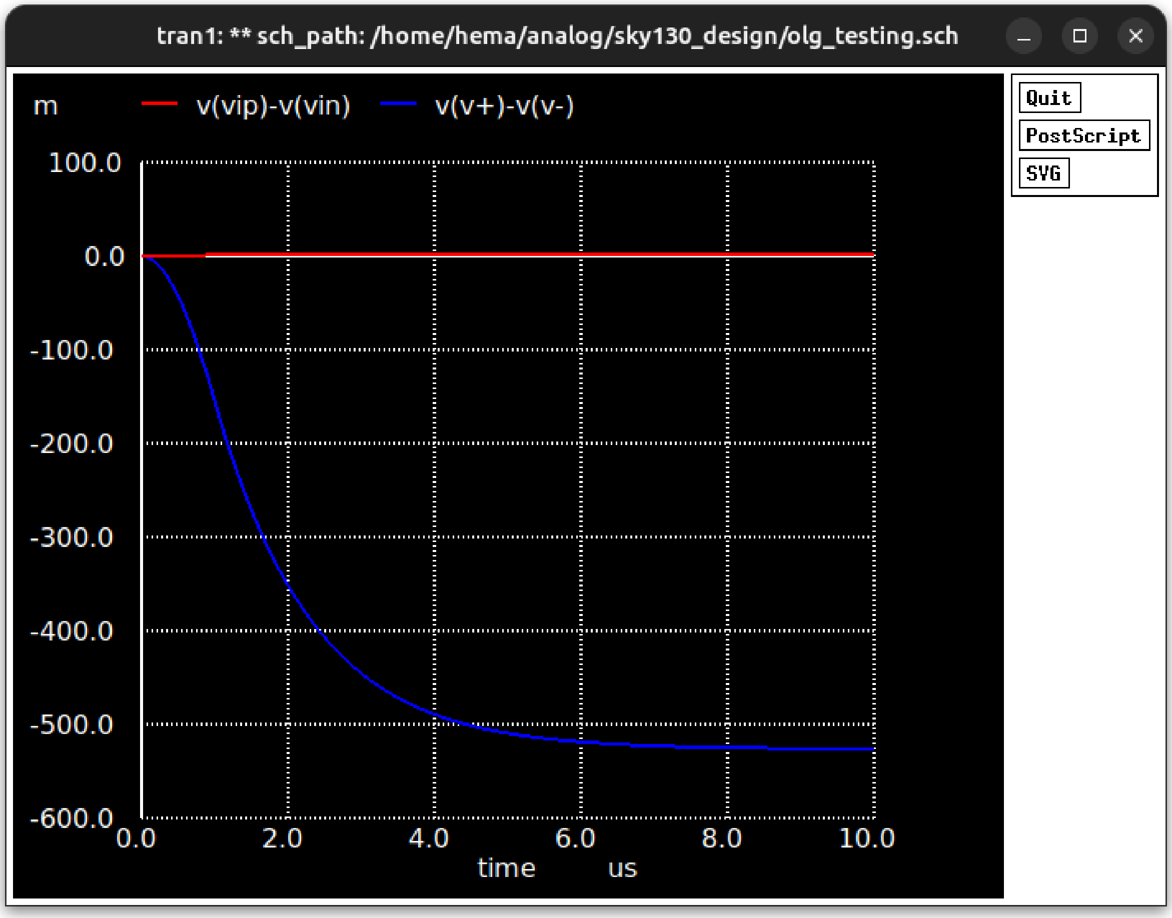


INPUT



Open loop transient analysis

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-300.0
-400.0
-500.0
-600.0
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4.0
6.0
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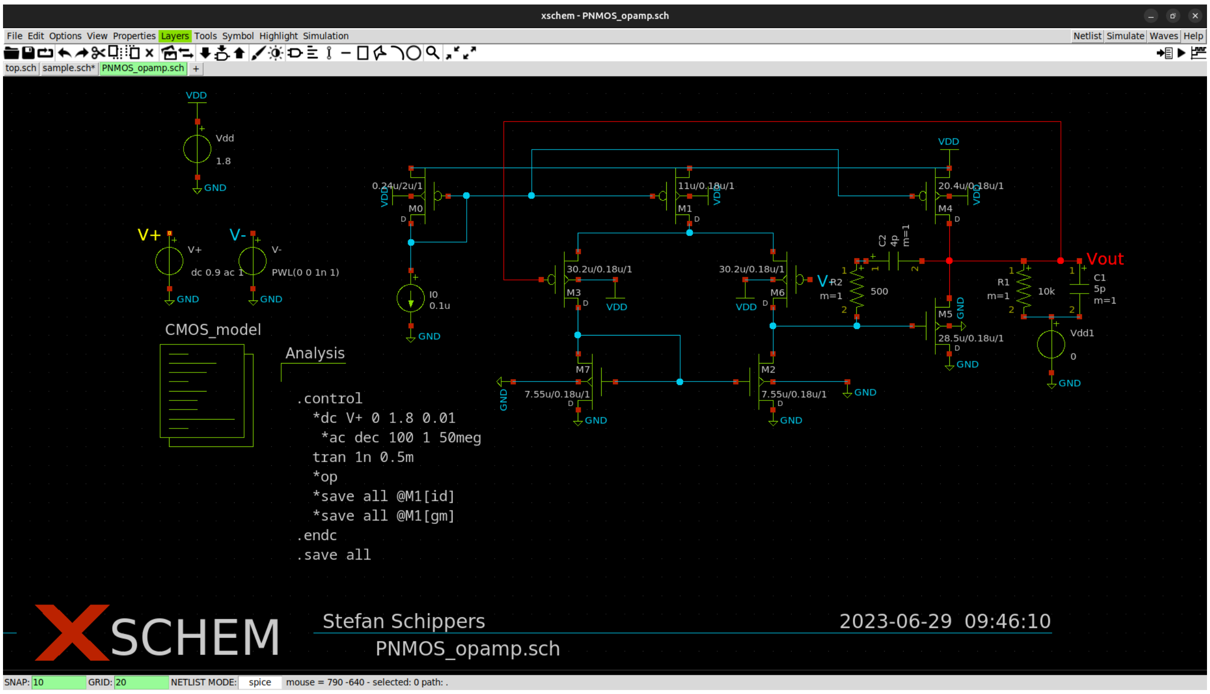
time us

Weekly Report

Subject: 2-stage Miller compensated op-amp
Input stage : PMOS
Technology: 180nmpdk
Took used: open source tool

Circuit Diagram:



Operating point:

Look up table

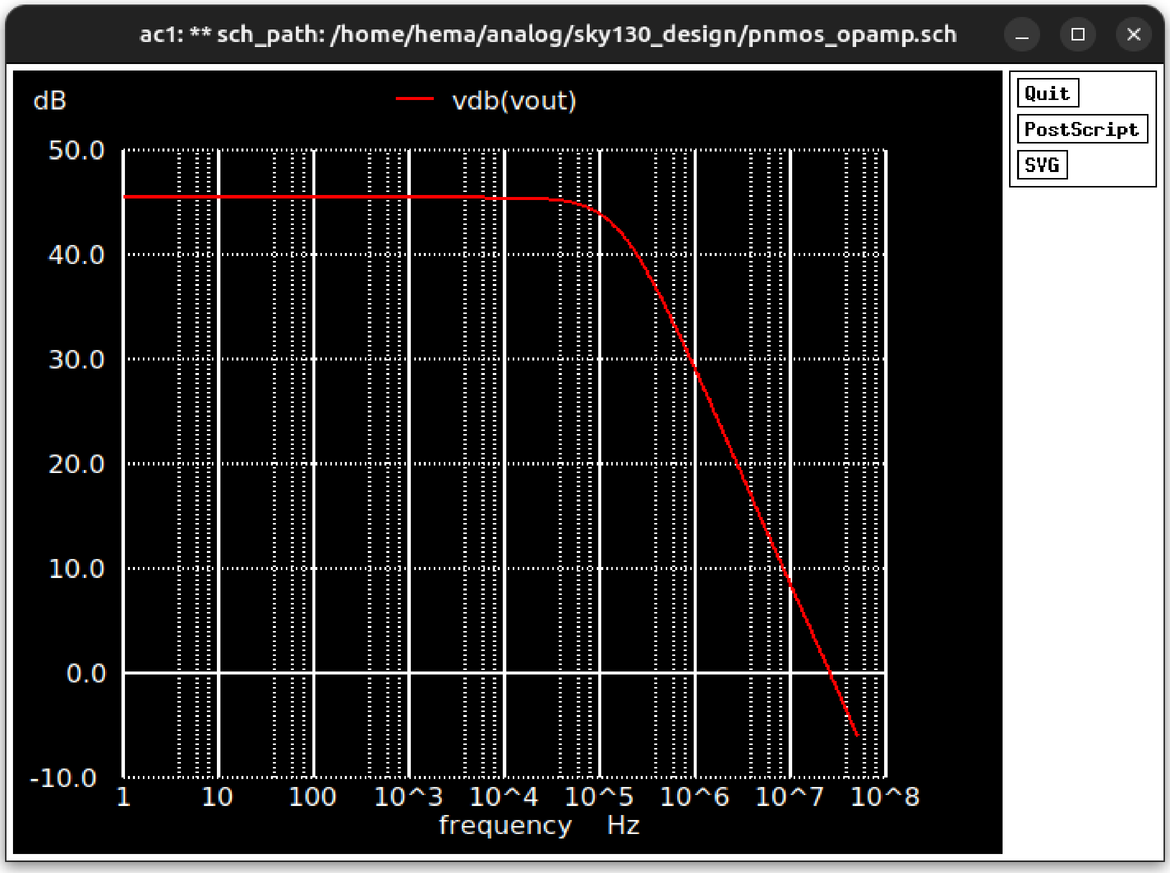
	W(um)	L(um)	I(uA)
$M_{6,3}$	30.2	0.18	50
$M_{2,7}$	7.55	0.18	50
M_1	11	0.18	100
M_4	20.4	0.18	222
M_5	28.5	0.18	220
M_0	0.24	2	0.1

Block Level Analysis:

Gm1	0.85m	**C2**	**5p**
Gm2	3.69m	**C1**	
G1	51u	**A0**	**208**
G2	280u	**UGB**	**45.7MegHz**
R0	10K	**Ph**	**84.22^0**
Rc	500	**Cc**	**4p**
A1	16	**A2**	**13**

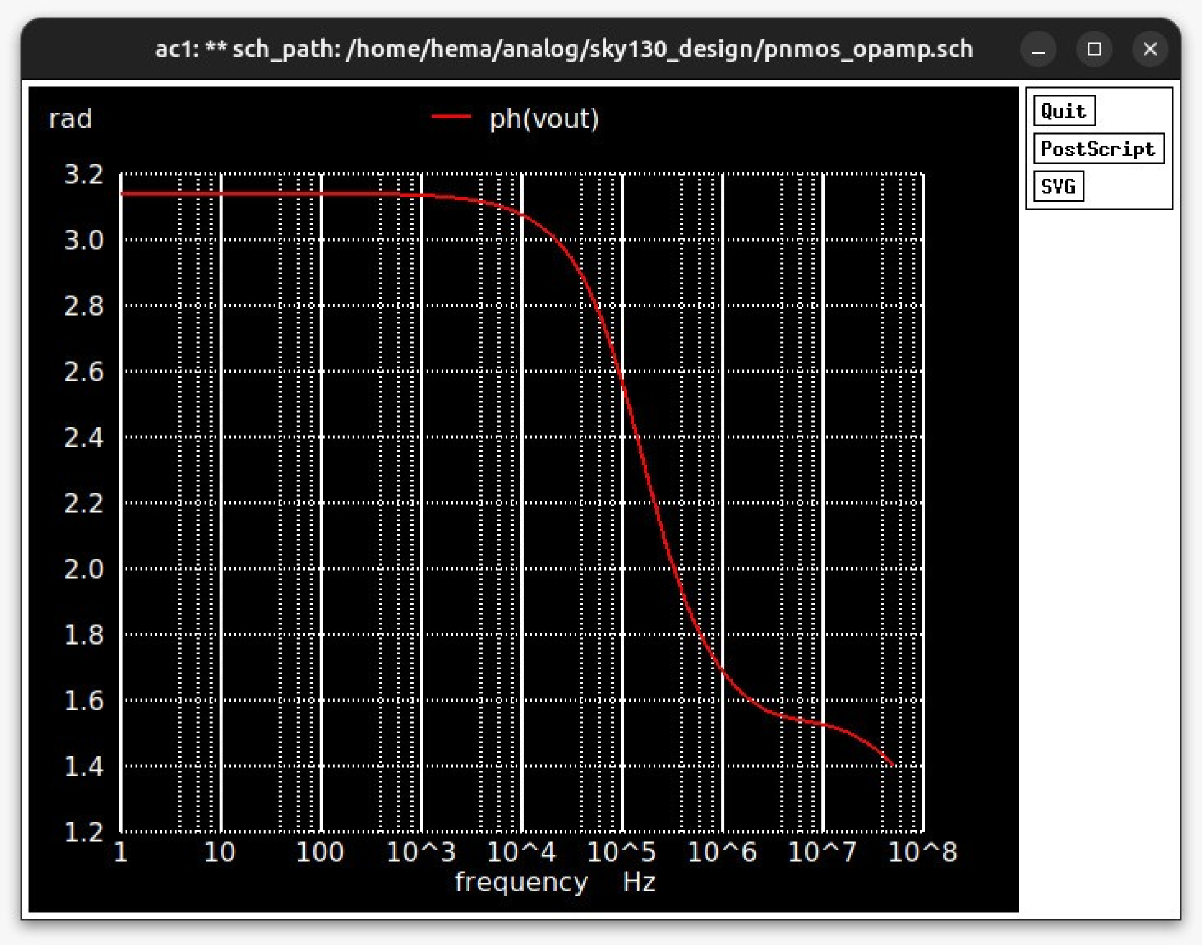
Frequency Response:

Magnitude Plot



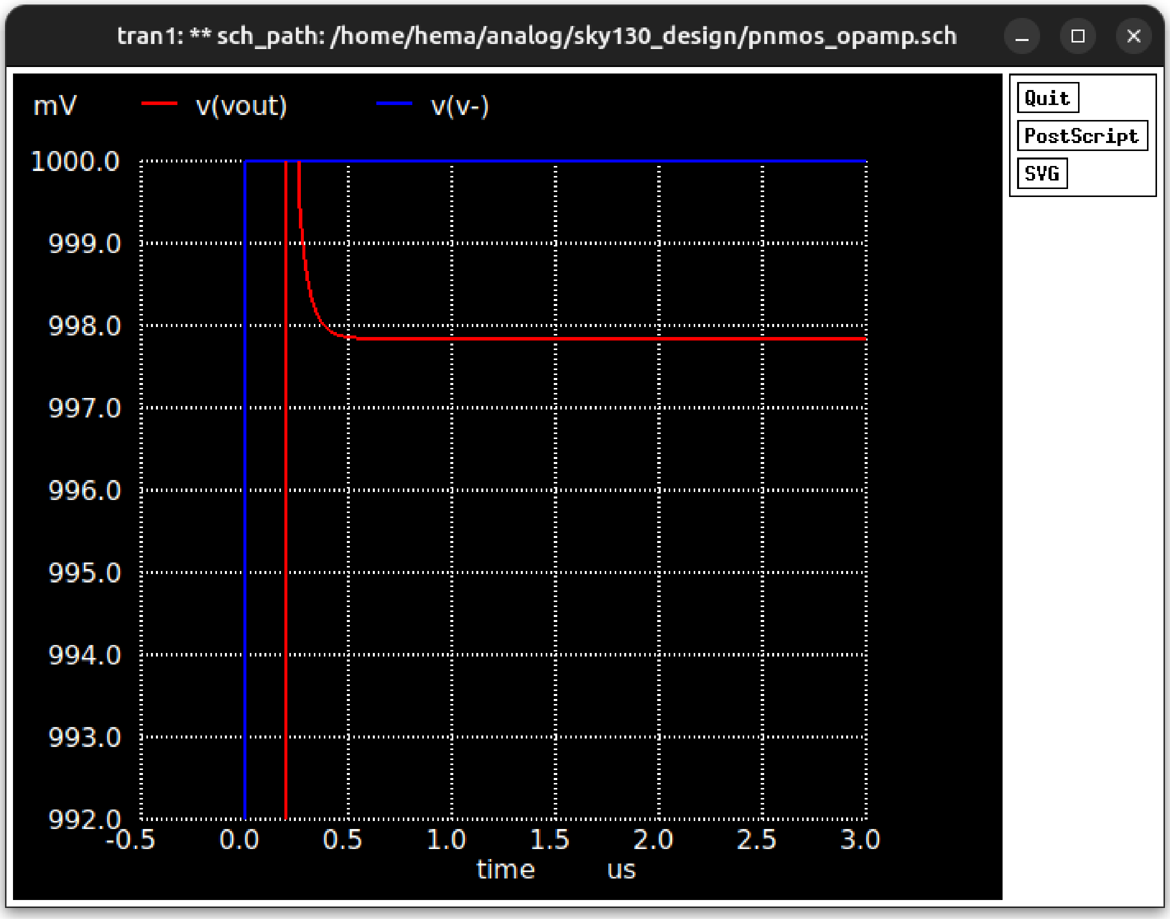
UGB=27megHz, A0=45.7db

phase-margin plot



phase margin=84.22

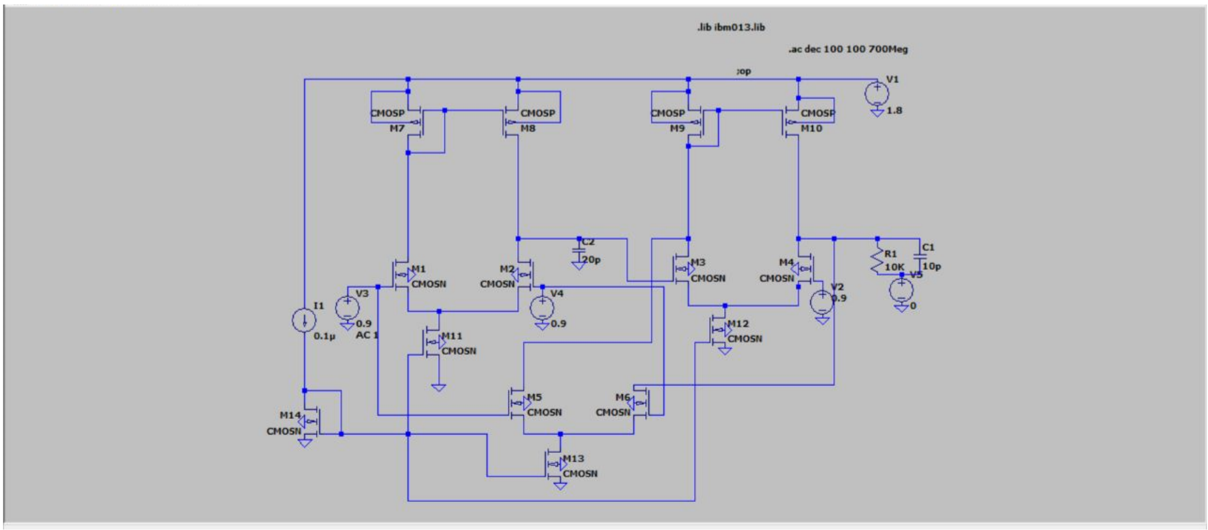
Unit-Step Response:



Weekly Report

Subject: Feed Forward Compensation of 2-Stage Op-amp

Circuit Diagram:



Block Level calculations:
DC analysis

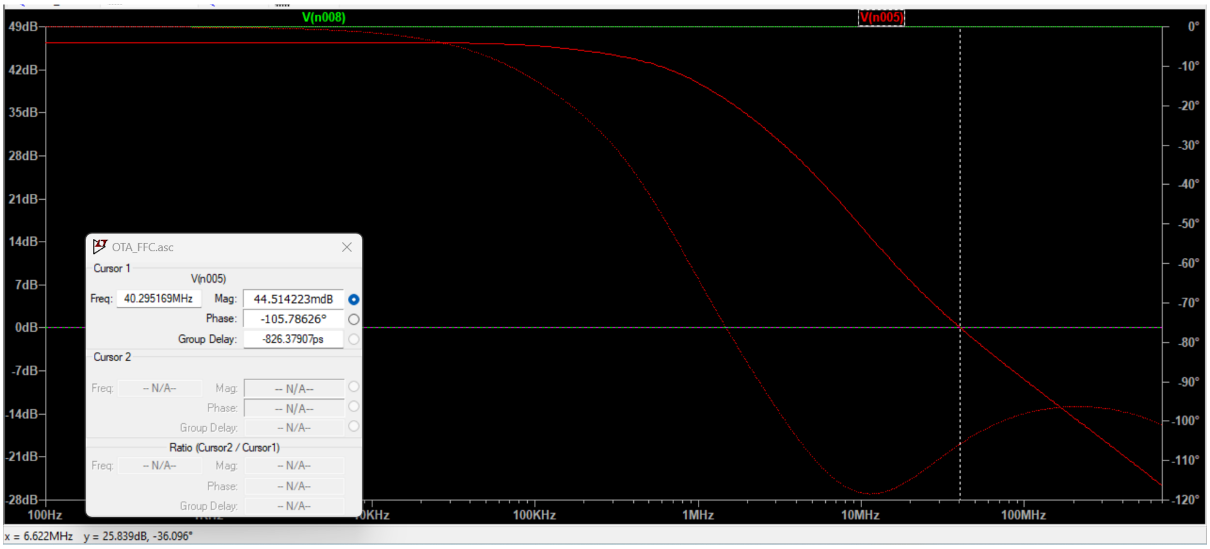
G_{M1}	2.35m	G_1	80u	UGB	41.8MHz
G_{M2}	3.18m	G_2	349.2u	Φ	61.6°
G_{M3}	2.63m	Z	22.6MHz	A_0	267.54(48db)
C_1	20p	P_1	0.63MHz	A_1	29.4
C_2	10p	P_2	5.57MHz	A_2	9.1

Look up Table:

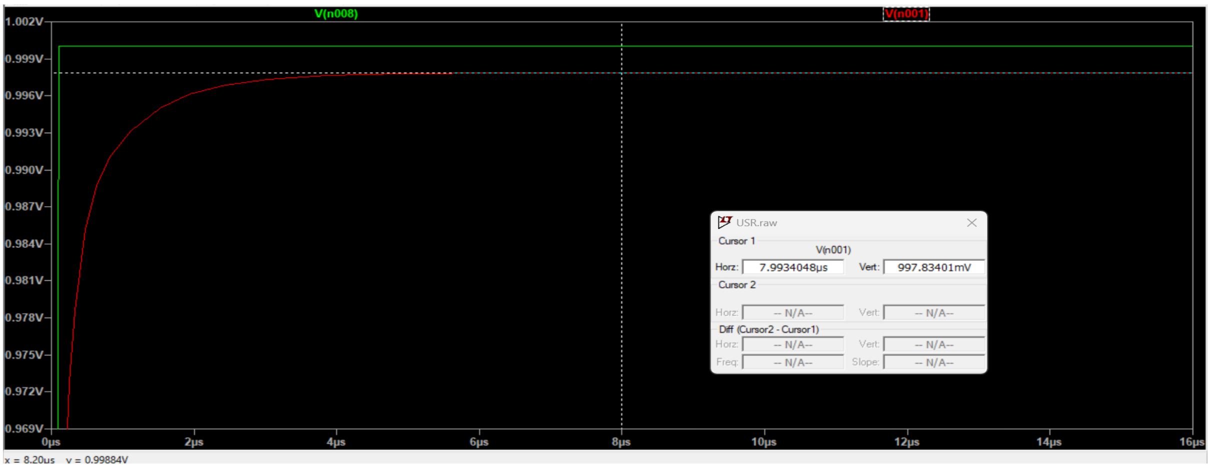
	L(nm)	W(µm)	I(µA)
$M_{1,2}$	180	20	110

$M_{3,4}$	180	143.66	127
$M_{5,6}$	180	5.7	289
$M_{7,8}$	180	1.85	110
$M_{9,10}$	180	6.7	416
M_{11}	180	35	219
M_{12}	180	33	217
M_{13}	180	97	557
M_{14}	50K	0.2	0.1

Frequency Response:



UnitStep Response:



Weekly Report

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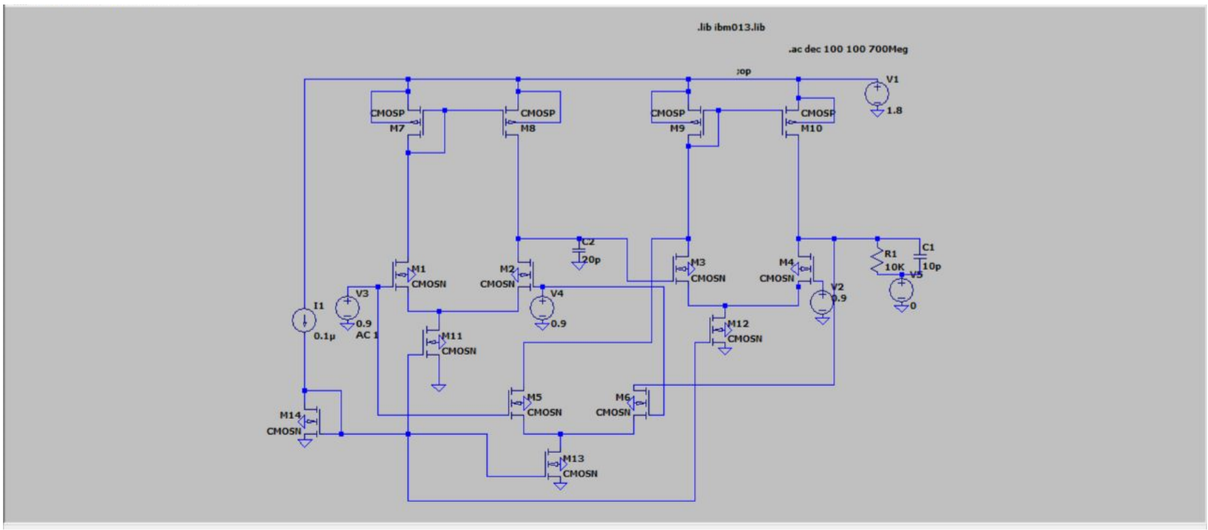

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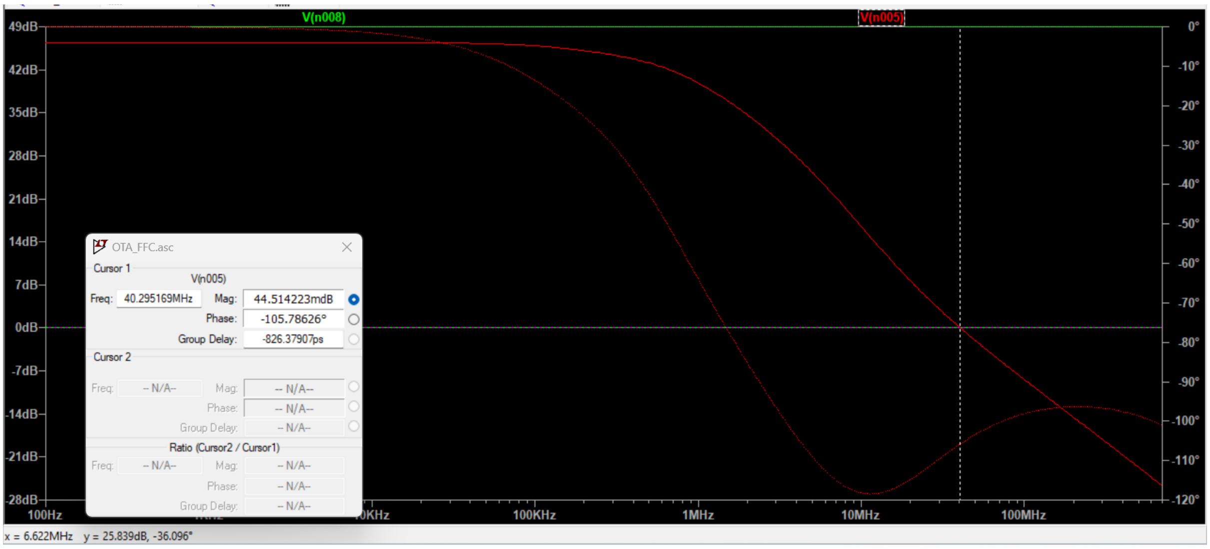

UnitStep Response: