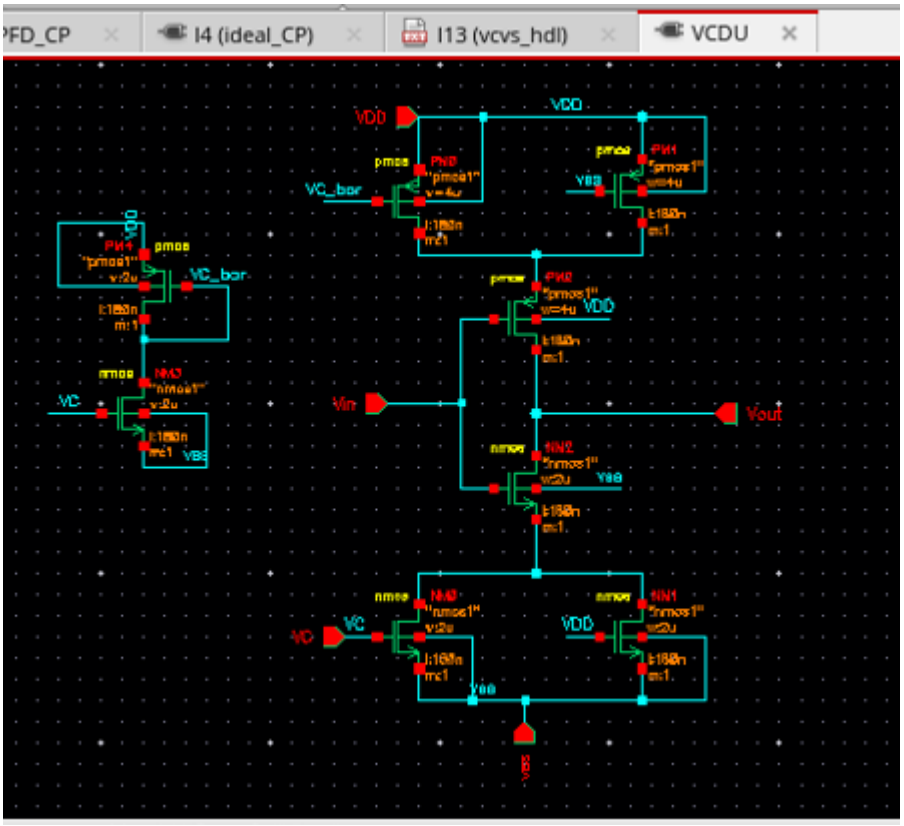
EE698G_Midterm Project

Sub: Design of DLL(Delay Locked Loop)
Technology node: gpdk180
Tool: Cadence Virtuoso

Design of VCDL:

Circuits:



Transistor sizing : W/L for nmos = 2um/180nm;
W/L for pmos = 4um/180nm

Calculations: T_O = 1.54nS , Freq = 649MHz, At V_C = 1V

Inverter: t_{pLH} = 20.238p sec = 35.923pS(With load)

Buffer: tpHL = 2*20.238p = 40.476pS(expected)

= 62.886pS(simulations)

So the number of buffers required for VCDL is = N

T_O / t_{pLH} = 24.488

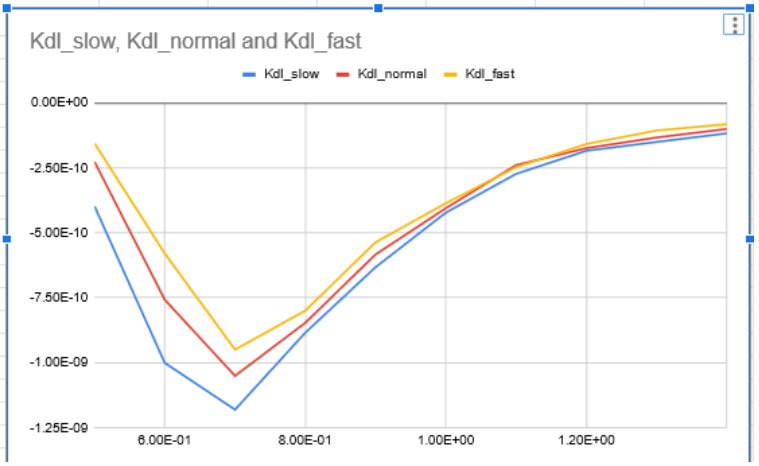
Assuming an increase of load on buffers, propagation delay increases so taking N = 24 for simulation purposes.

Delay of Output for VCDL = T_O + ΔT = 2.084ns

ΔT = 0.544ns which is supposed to be zero

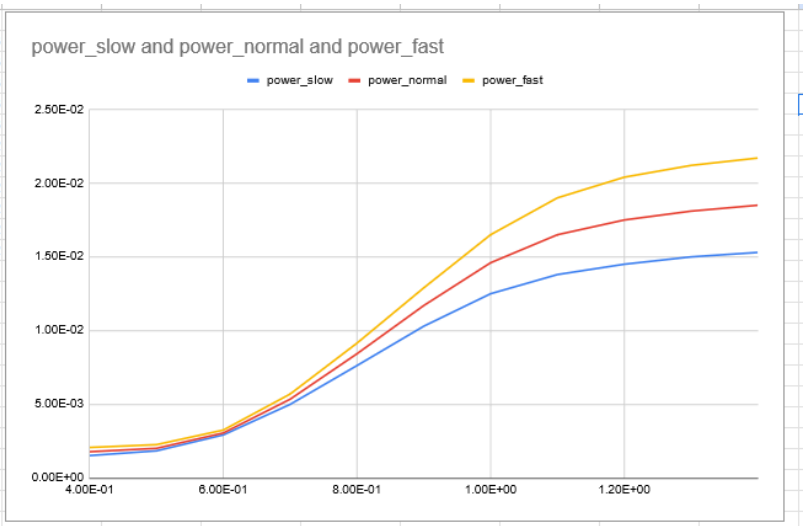
Plot of Kdl:

VC	Kdl_slow	Kdl_normal	Kdl_fast
5.00E-01	-3.97E-10	-2.26E-10	-1.55E-10
6.00E-01	-1.00E-09	-7.57E-10	-5.79E-10
7.00E-01	-1.18E-09	-1.05E-09	-9.49E-10
8.00E-01	-8.84E-10	-8.46E-10	-7.99E-10
9.00E-01	-6.32E-10	-5.83E-10	-5.36E-10
1	-4.22E-10	-4.05E-10	-3.86E-10
1.1	-2.73E-10	-2.39E-10	-2.47E-10
1.2	-1.84E-10	-1.74E-10	-1.58E-10
1.3	-1.50E-10	-1.33E-10	-1.06E-10
1.4	-1.17E-10	-1.00E-10	-8.16E-11



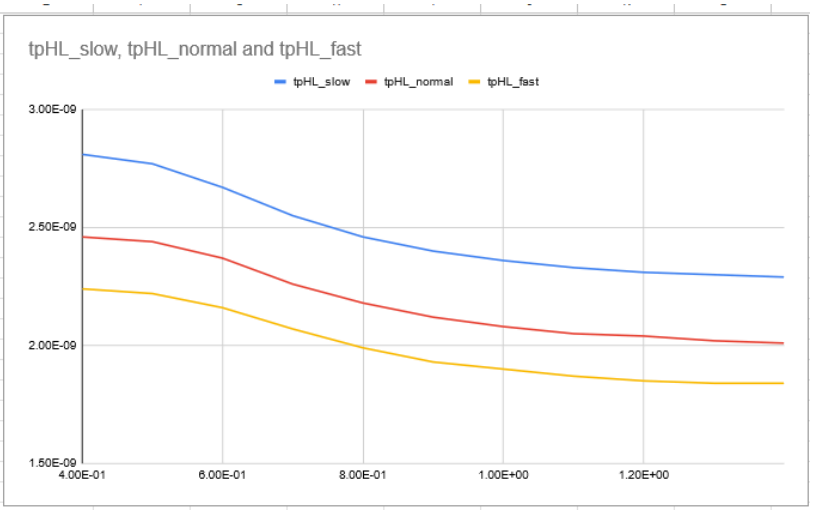
Plot of Transient power

vc	power_slow	power_normal	power_fast
4.00E-01	1.53E-03	1.79E-03	2.08E-03
5.00E-01	1.85E-03	2.02E-03	2.27E-03
6.00E-01	2.93E-03	3.06E-03	3.26E-03
7.00E-01	5.00E-03	5.35E-03	5.70E-03
8.00E-01	7.63E-03	8.43E-03	9.15E-03
9.00E-01	1.03E-02	1.17E-02	1.29E-02
1	1.25E-02	1.46E-02	1.65E-02
1.1	1.38E-02	1.65E-02	1.90E-02
1.2	1.45E-02	1.75E-02	2.04E-02
1.3	1.50E-02	1.81E-02	2.12E-02
1.4	1.53E-02	1.85E-02	2.17E-02



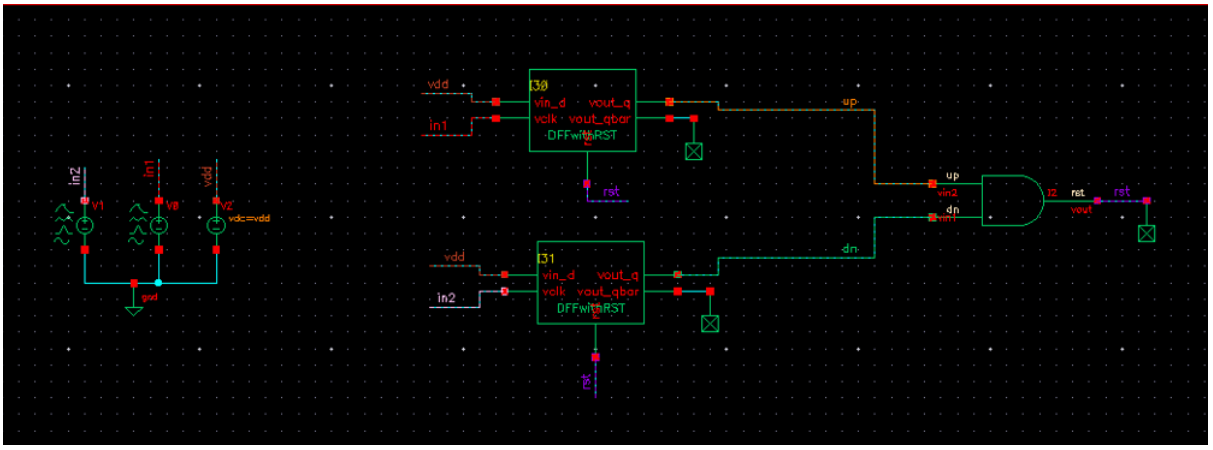
Plot of tpHL , Range = 1.84ns : 2.8ns

vc	tpHL_slow	tpHL_normal	tpHL_fast
4.00E-01	2.81E-09	2.46E-09	2.24E-09
5.00E-01	2.77E-09	2.44E-09	2.22E-09
6.00E-01	2.67E-09	2.37E-09	2.16E-09
7.00E-01	2.55E-09	2.26E-09	2.07E-09
8.00E-01	2.46E-09	2.18E-09	1.99E-09
9.00E-01	2.40E-09	2.12E-09	1.93E-09
1	2.36E-09	2.08E-09	1.90E-09
1.1	2.33E-09	2.05E-09	1.87E-09
1.2	2.31E-09	2.04E-09	1.85E-09
1.3	2.30E-09	2.02E-09	1.84E-09
1.4	2.29E-09	2.01E-09	1.84E-09

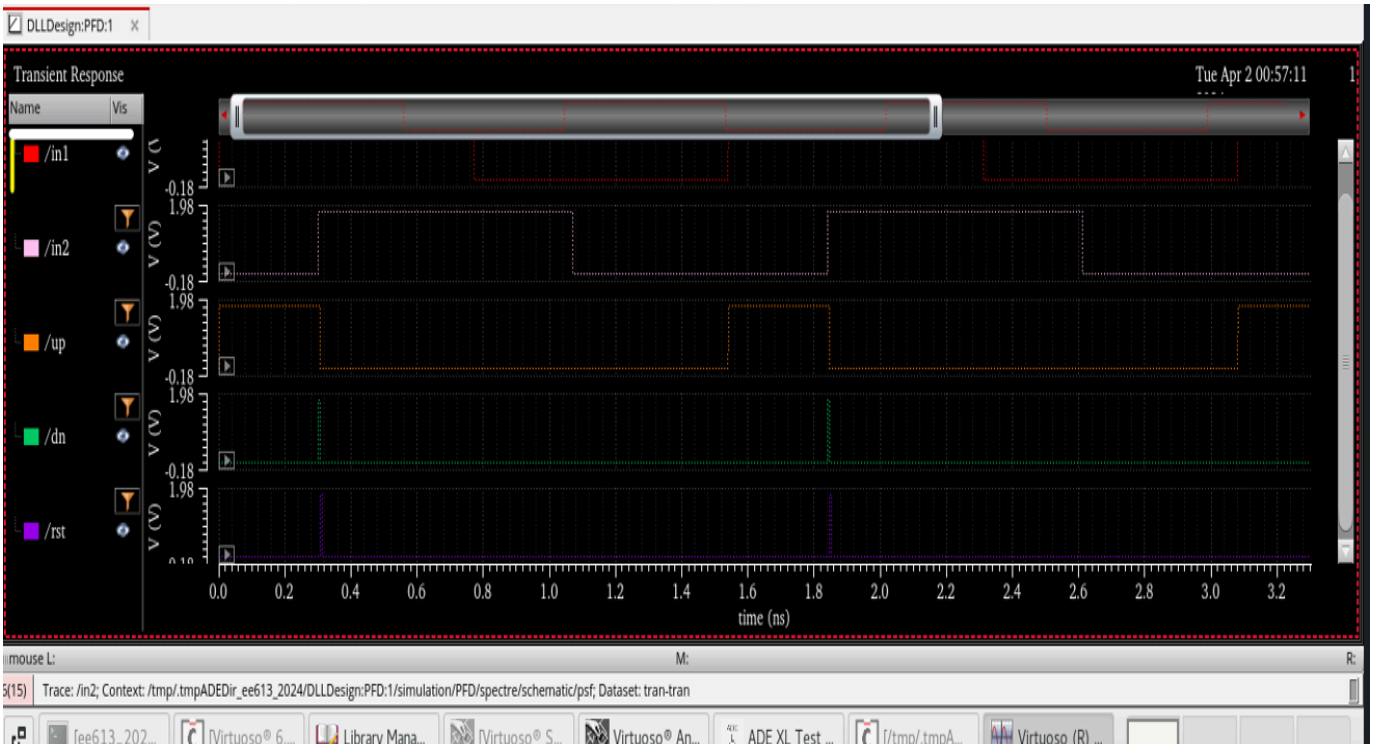


PFD(Phase Frequency Detector):

Circuit schematic

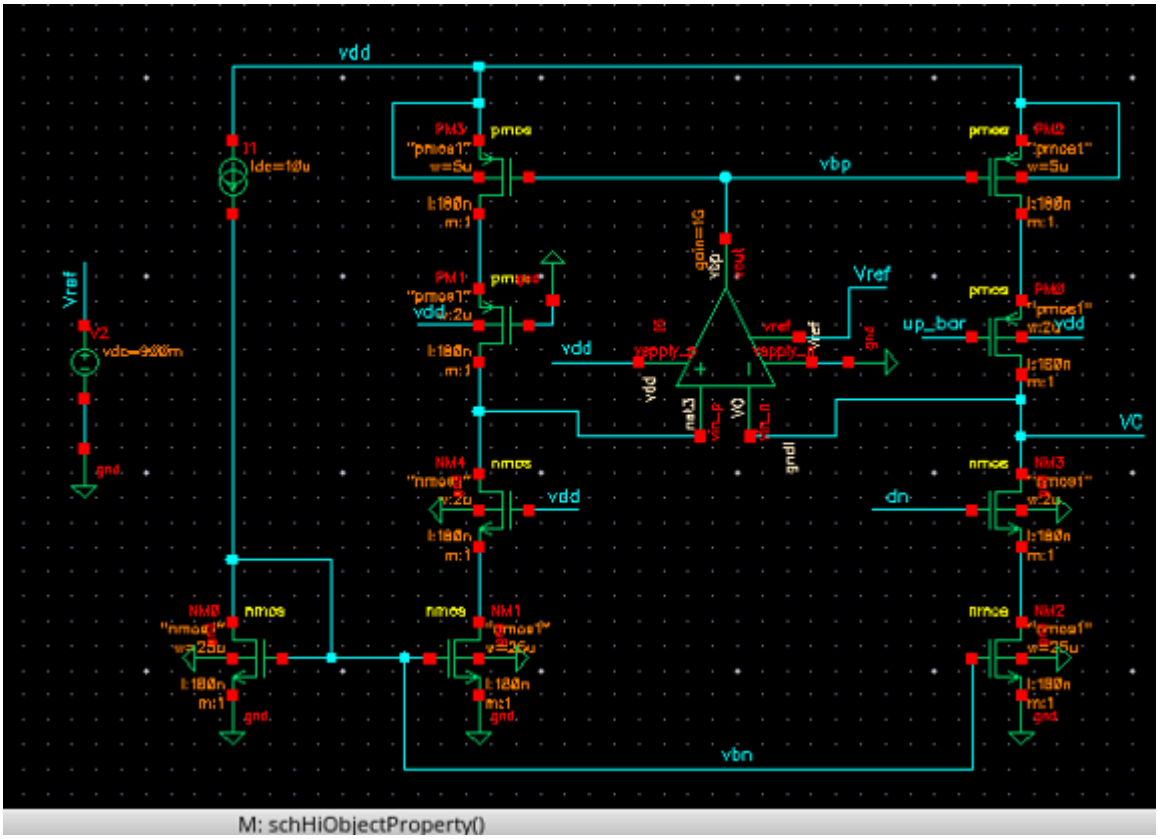


Plot



CP(charge pump**):**

Circuit Schematic:

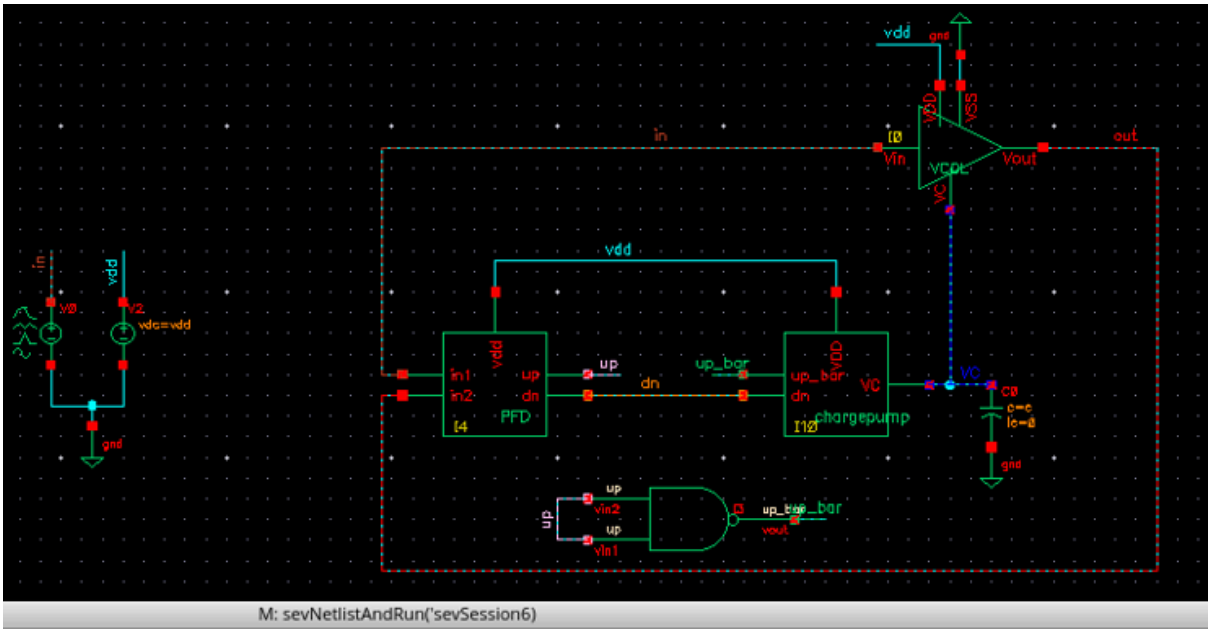


W/L of pm4, pm2 (current mirroring mos)= 5u/180m
W/L of nm0,nm1, nm2(current mirroring mos) = 25u/180m
W/L of up,dn vdd,gnd (switches) = 2u/180m
Done accordingly to equalise the up and down currents

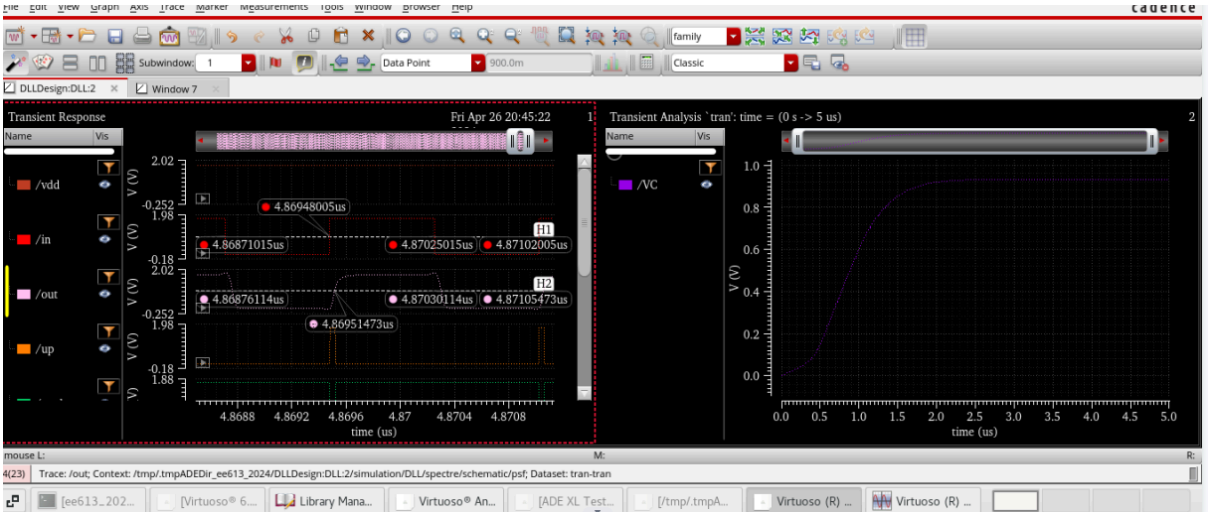
DLL:

Connect VCDL , PFD and Charge pump in a naive feedback to lock the Input signal and output signal with delay T0.

Schematic: C =10pF



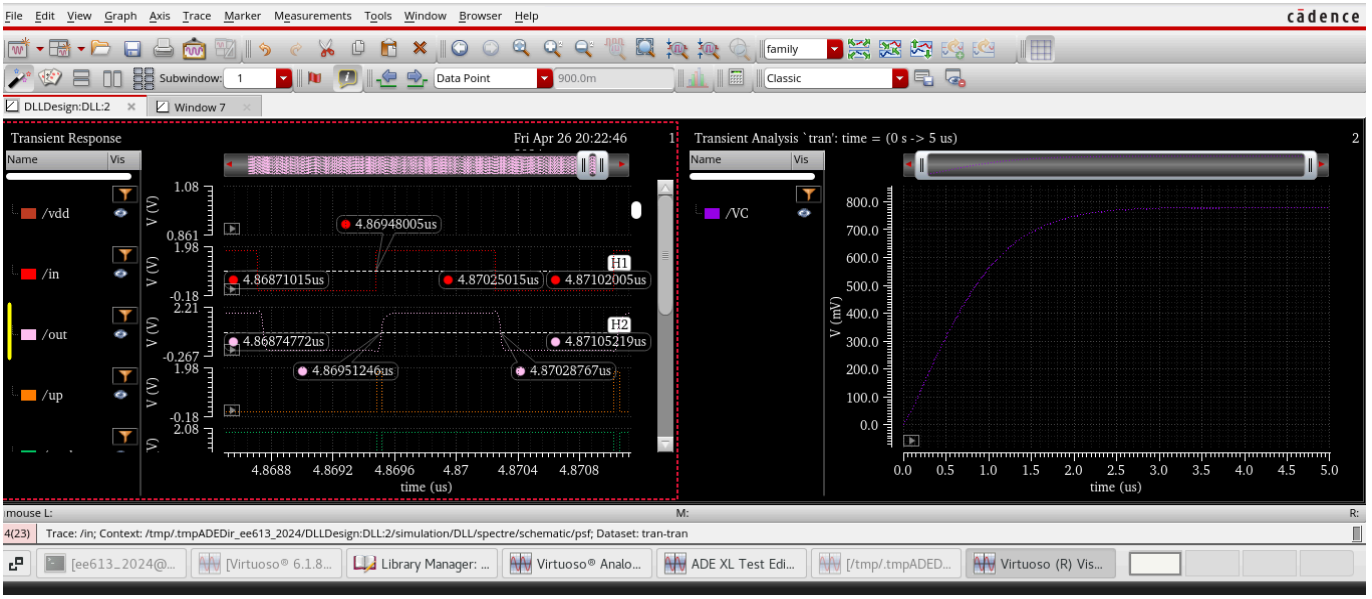
For slow corner:



Offset = 30ps , $Vc_{,Sat}$ = 0.99V

ID avg= 3.84mW Power = 1.71*3.84m =

For fast corner:



Offset = 30ps , $Vc_{,Sat}$ = 0.77V

ID avg= 3.8423mW Power = 1.89*3.842m = 7.26mW