

# EE619 Project#3

## Designing Standard cells

Tools Used : Cadence Virtuoso

Technology node used: 180nm PDK

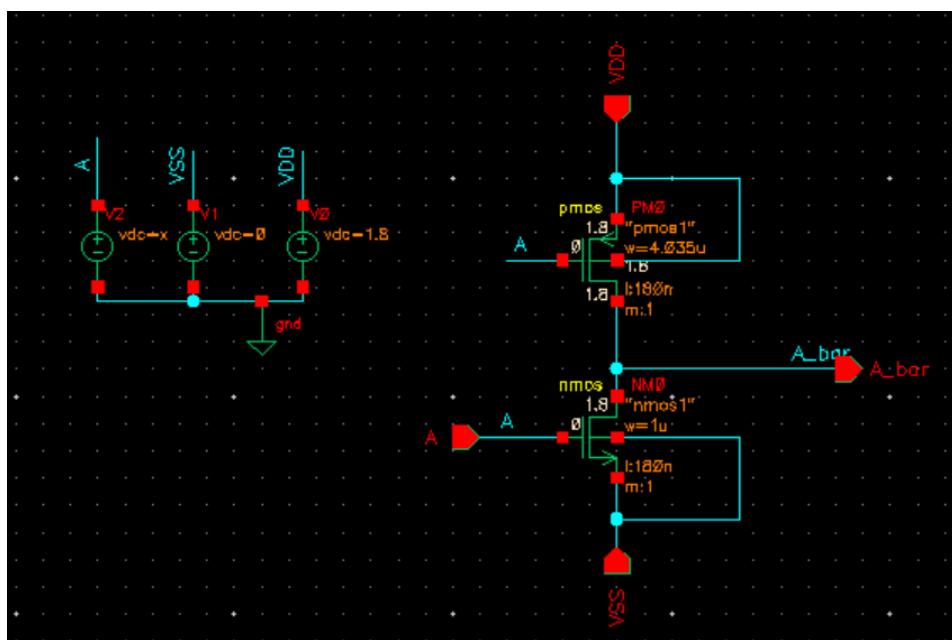
Team - Bitcoders

Group Details:

1. Sriramchandher(200744) (OR Gate)
2. Hema(200621) (AND Gate)

**CMOS Inverter :**

**Schematic**



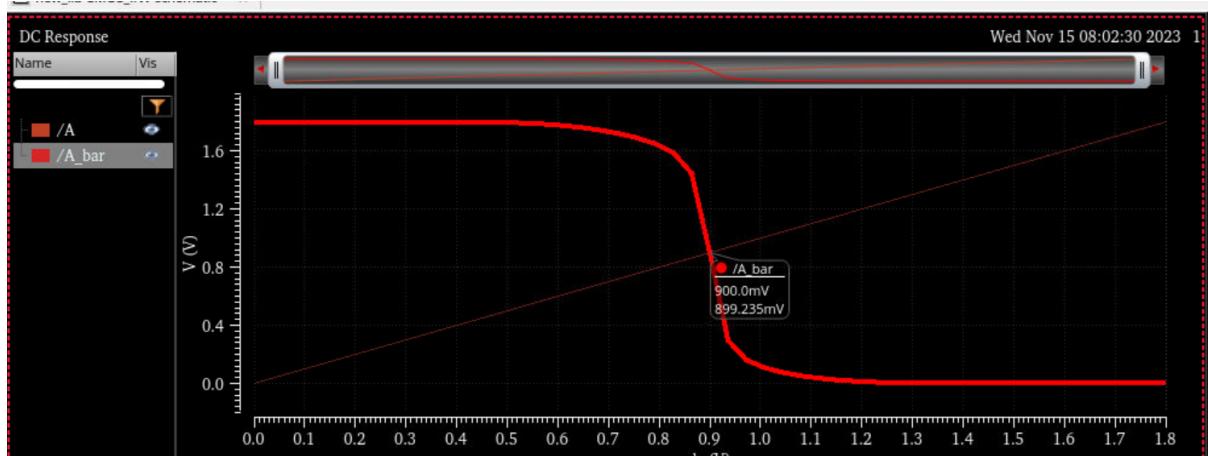
**CMOS Inverter Sizing:**

**PMOS: W = 4.035um ; L = 180nm**

**NMOS : W = 1um ; L = 180nm**

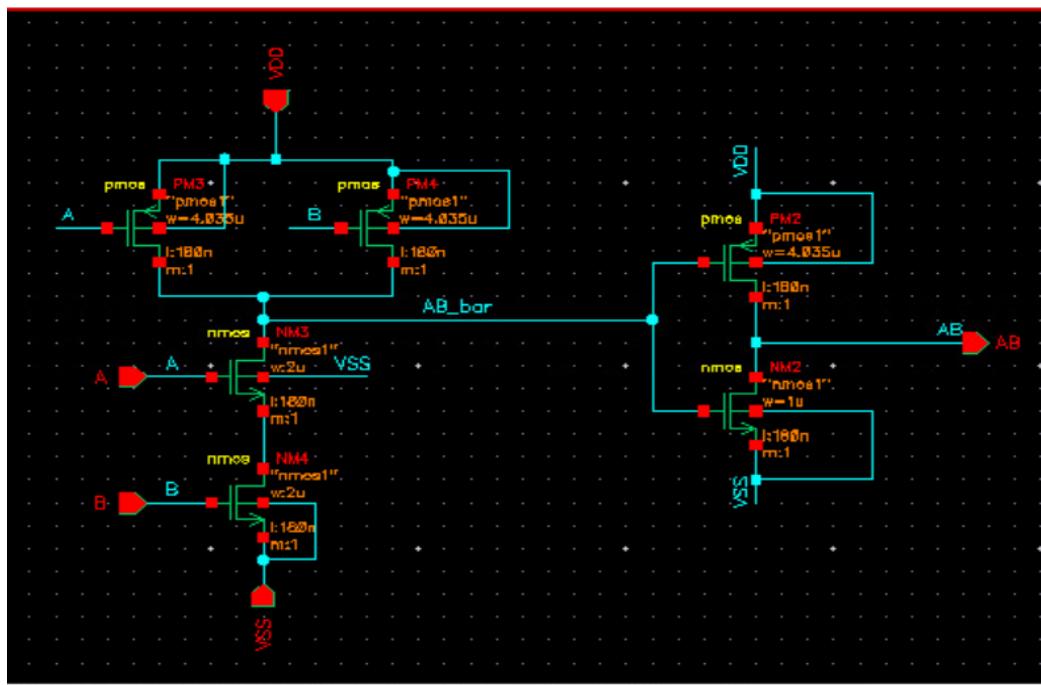
## Explanation:

Considered  $W_p$  as variable and found a point where  $V_{in}=V_{out}=V_m=VDD/2$ . So that the strength of PDN and PUN are equal when worst case is taken



## AND Gate:

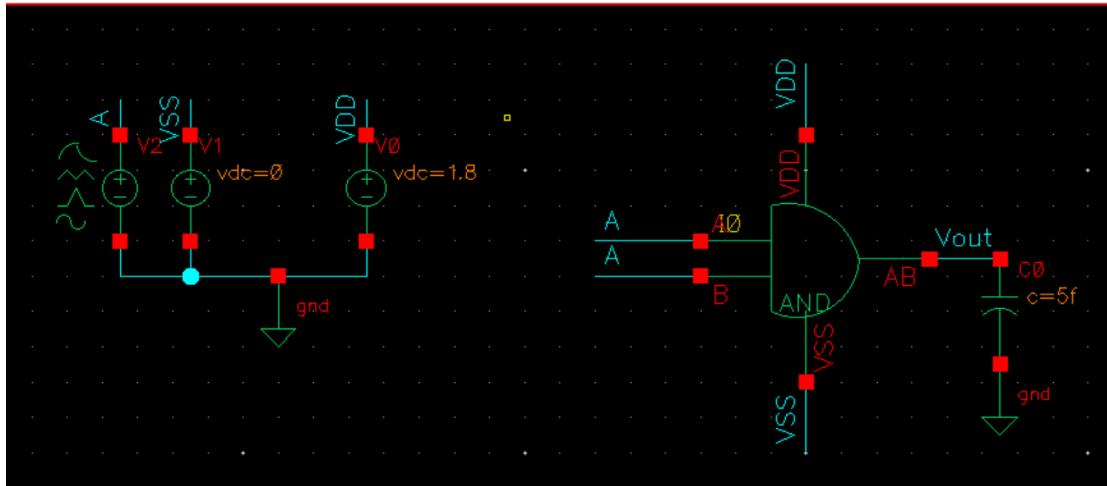
### AND Schematic



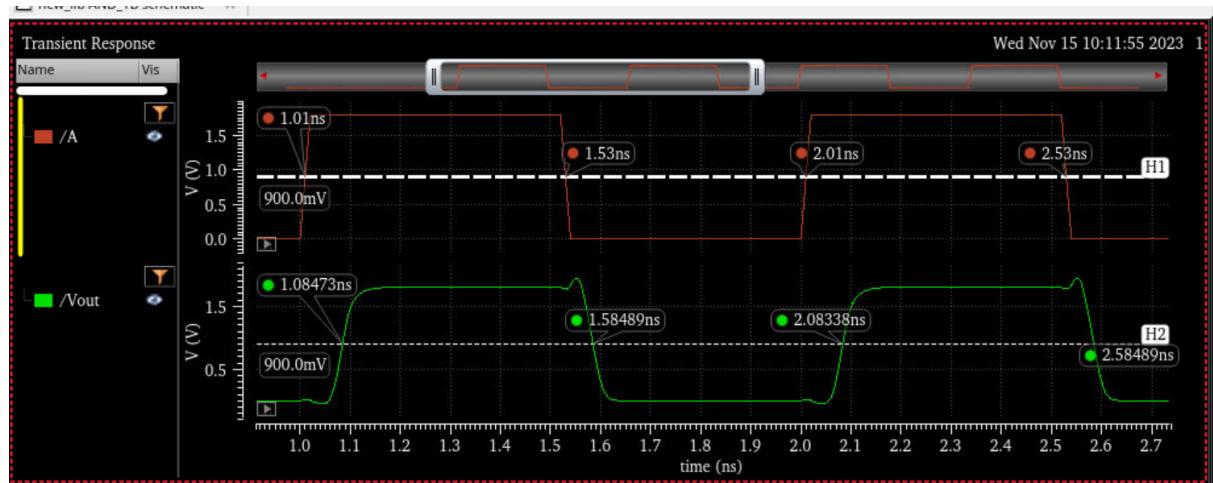
## Sizing:

PMOS : W = 4.035um, L = 180nm ; NMOS: W = 2um, L =180nm

## AND Gate TestBench



For Load Capacitance = 5fF



Raise Propagation delay:

$$T_{PLH} = 1.08473\text{ns} - 1.01\text{ns} = 0.075\text{ns}$$

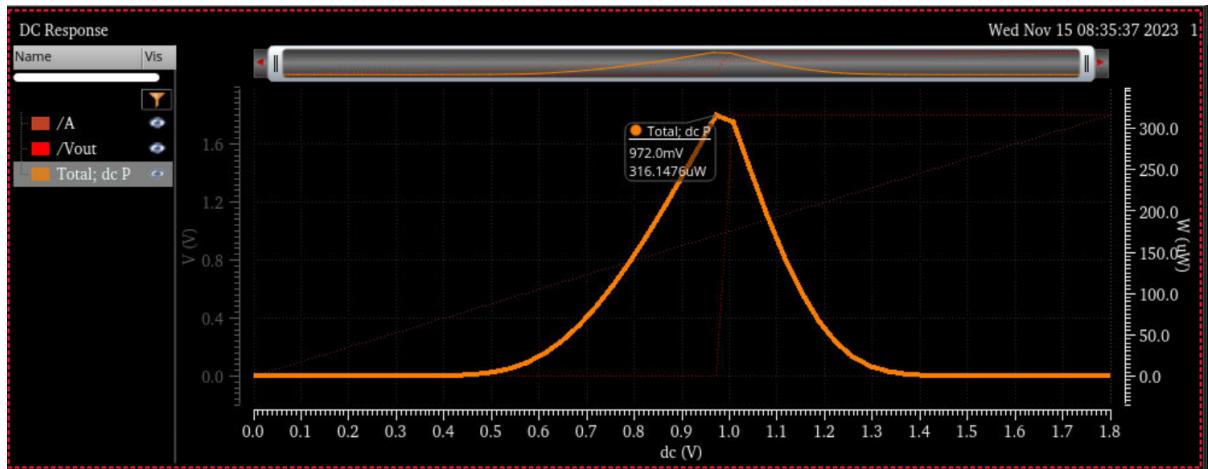
Fall Propagation delay:

$$T_{PLH} = 1.584\text{ns} - 1.53\text{ns} = 0.053\text{ns}$$

## Power consumption:

average(i"/I0/VDD" ?result "tran")	
Expression	Value
1 average(i"/I0/V...	66.73E-6

$$VDD \cdot Iavg = 1.8 \cdot 66.73E-6 = 120.114 \mu\text{Watt}$$



DC Total power graph

## For 10fF Load Capacitance:



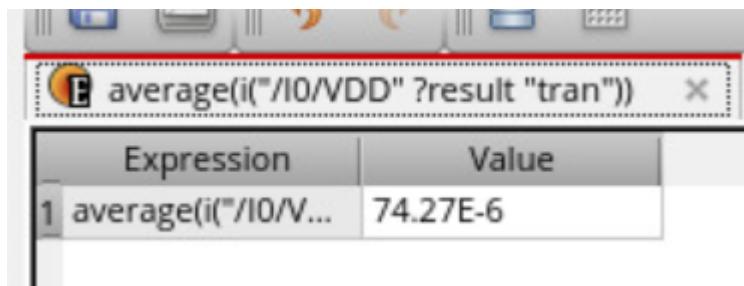
Raise Propagation Delay:

$$T_{PLH} = 1.091\text{ns} - 1.01\text{ns} = 0.09\text{ns}$$

Fall Propagation Delay:

$$T_{PHL} = 1.593\text{ns} - 1.53\text{ns} = 0.063\text{ns}$$

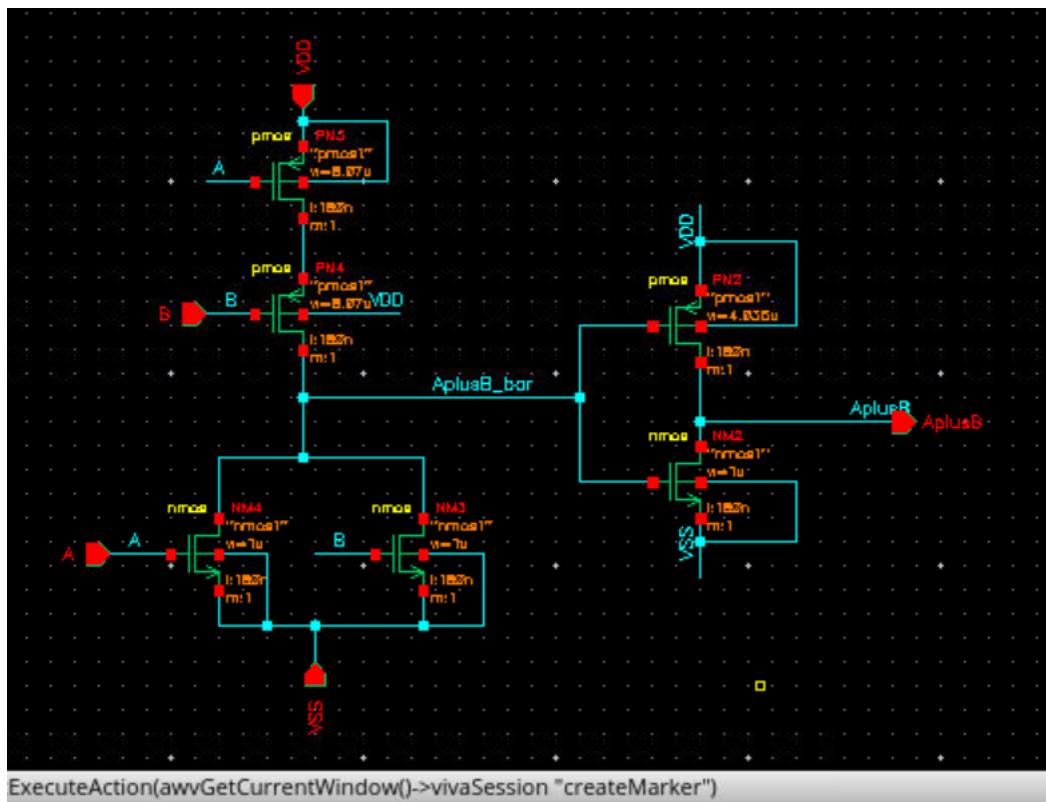
Power consumption:



$$VDD \cdot lavg = 1.8 * 74.21E-6 = 133.578\text{uWatt}$$

OR Gate:

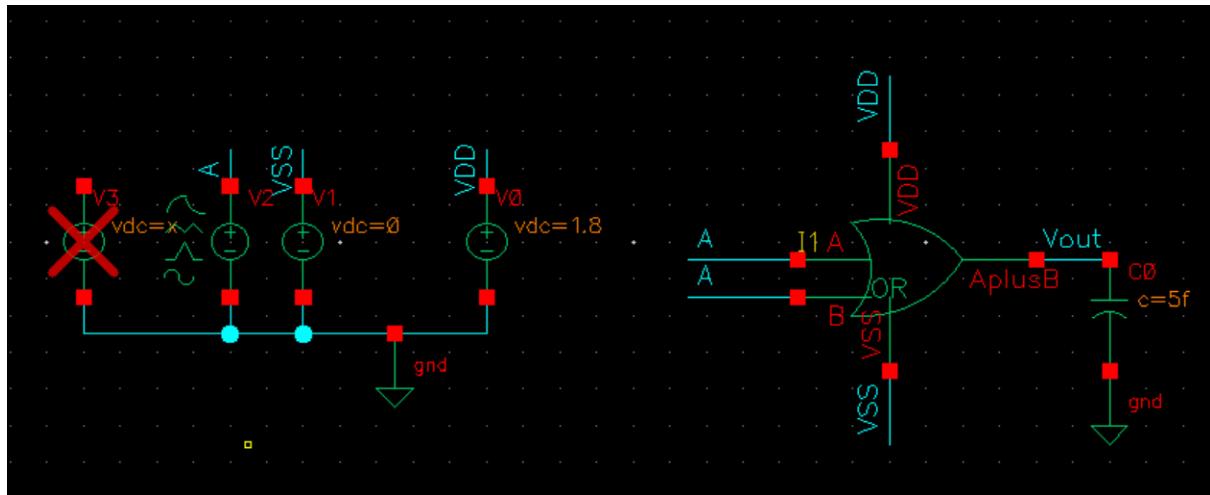
Schematic



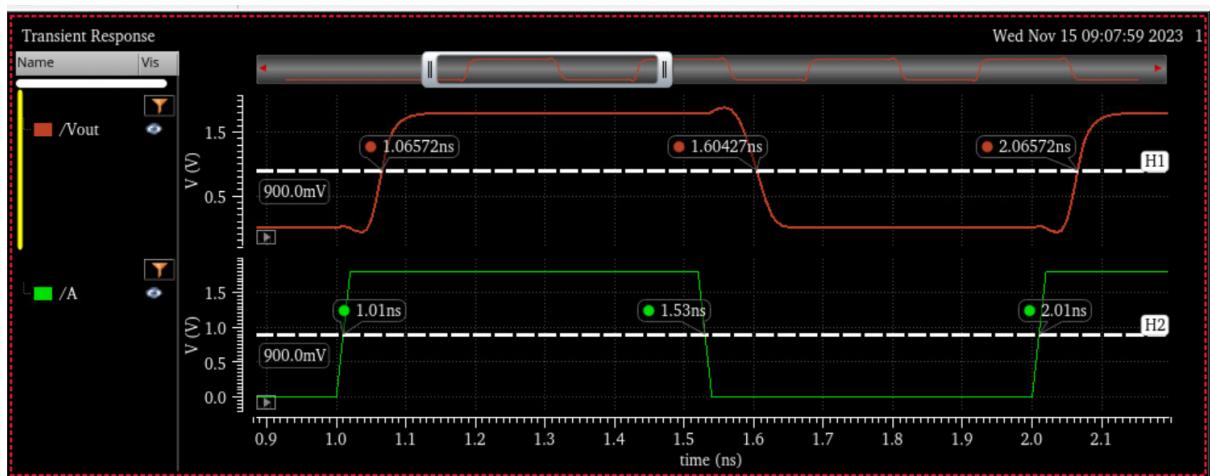
## Sizing:

PMOS : W = 8.07um, L = 180nm ; NMOS: W = 1um, L =180nm

## OR TestBench



For Load Capacitance = 5\_fF



Raise Propagation delay:

$$T_{PLH} = 1.0657\text{ns} - 1.01\text{ns} = 0.0557\text{ns}$$

Fall Propagation delay:

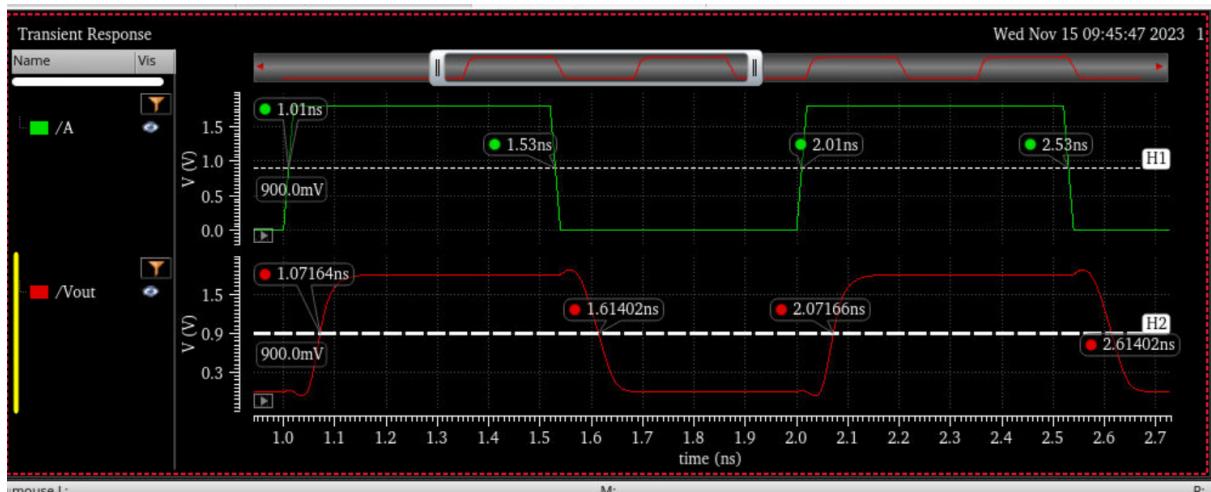
$$T_{PLH} = 1.604\text{ns} - 1.53\text{ns} = 0.074\text{ns}$$

## Power Consumption:

average(i"/I1/VDD" ?result "tran")	
Expression	Value
1 average(i"/I1/V...	72.21E-6

$$VDD \cdot I_{avg} = 1.8 \cdot 72.21E-6 = 129.978 \mu\text{Watt}$$

## For 10fF Load Capacitance:



## Raise Propagation Delay:

$$T_{PLH} = 1.0716 \text{ ns} - 1.01 \text{ ns} = 0.0616 \text{ ns}$$

## Fall Propagation Delay:

$$T_{PHL} = 1.614 \text{ ns} - 1.53 \text{ ns} = 0.084 \text{ ns}$$

## Power Consumption:

average(i"/I1/VDD" ?result "tran")	
Expression	Value
1 average(i"/I1/V...	79.43E-6

$$VDD \cdot I_{avg} = 1.8 \cdot 79.43E-6 = 142.974 \mu\text{Watt}$$

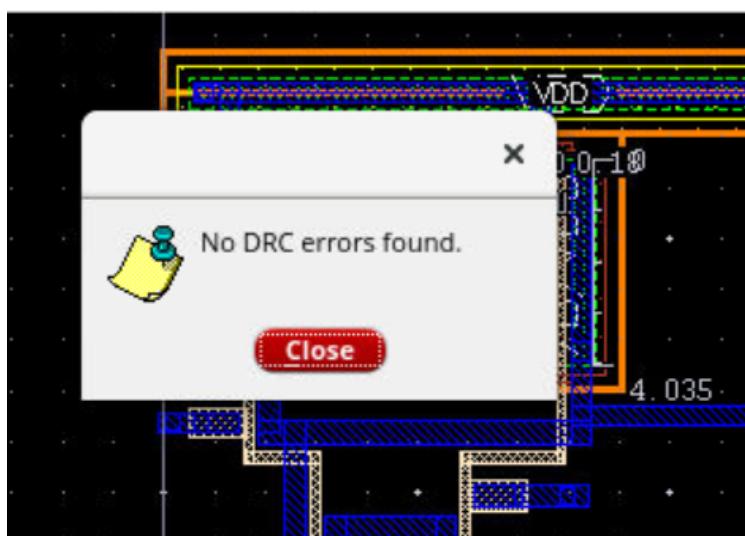
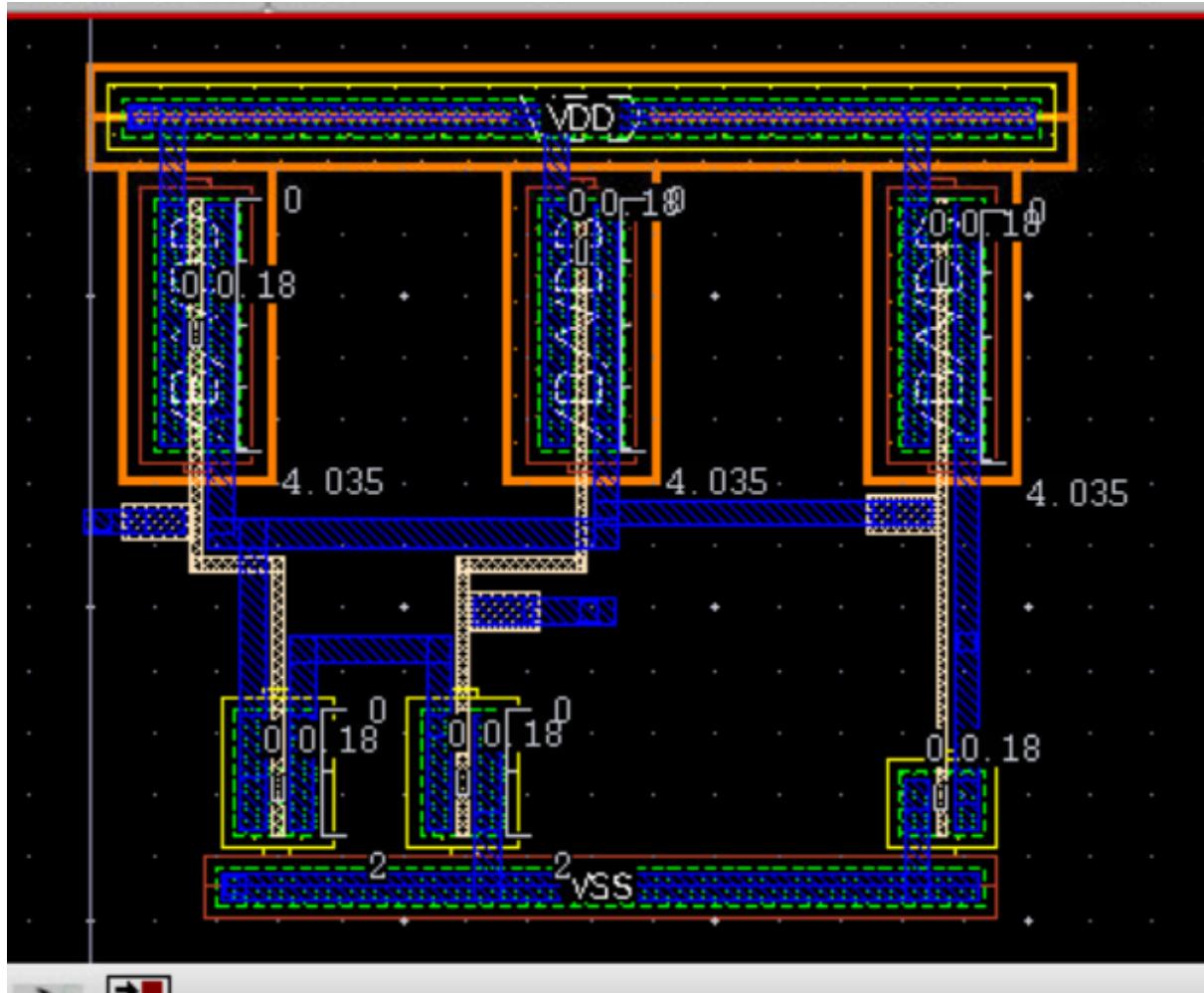
## TABULATED ALL THE VALUES

<b>Capacitor</b>		<b>AND</b>	<b>OR</b>
<b>5fF</b>	Raise Propagation delay	0.075ns	0.0557ns
	Fall Propagation delay	0.053ns	0.074ns
	Power consumption	120.114uWatt	129.978uWatt
	Power Consumption from parasitic extraction	134.55uWatt	144.09Watt
	Raise Propagation delay	0.0848ns	0.0918ns
	Fall Propagation delay	0.0617ns	0.07ns
<b>10fF</b>	Raise Propagation delay	0.09ns	0.0616ns
	Fall Propagation delay	0.063ns	0.084ns
	Power consumption	133.578uWatt	142.974uWatt
	Power Consumption from parasitic extraction	148.158uWatt	157.5uWatt
	Raise Propagation delay	0.064ns	0.0705ns
	Fall Propagation delay	0.0844ns	0.0942ns

**Input Signal Used for all the Transient analysis is  
Clock with 20ps rise and fall time and a frequency of 1GHz  
and delay time of 1ns.**

# Layouts of AND and OR Gates

## AND Gate



## Run: "AND"

X

Run: "AND" from  
/users/courses/619A\_2023/ee619\_Bit\_coders/cadence\_designs/

Schematic and Layout Match.  
You currently have an open run (project).

Do you want to close current project and view the results of new run?

### Summary of LVS Issues

### Extraction Information:



0 cells have 0 mal-formed device problems  
0 cells have 0 label short problems  
0 cells have 0 label open problems

### Comparison Information:

0 cells have 0 Net mismatches  
0 cells have 0 Device mismatches  
0 cells have 0 Pin mismatches  
0 cells have 0 Parameter mismatches

### ELW Information:

Total DRC violations: 0

**Yes**

**No**

**Help**

The image shows two windows from the Cadence Design System. The top window is a terminal-like interface displaying a log file named AND.log. The log contains error messages related to unstable devices in the design. The bottom window is a transient analysis tool showing waveforms for nodes /A and /Vout over time. The /A waveform is a digital signal with periods of 1.01ns, 1.53ns, 2.01ns, 2.53ns, 3.01ns, 3.53ns, 4.01ns, and 4.53ns. The /Vout waveform is a corresponding analog signal with similar transition times.

```

/users/courses/619A_2023/ee619_Bit_coders/cadence_designs/AND.log
cadence

( 123) unstable device for M1res_RES_7          0      0
( 125) unstable device for NWELLRES_RES_6       0      0
( 127) unstable device for PSDRES_RES_5         0      0
( 129) unstable device for ISONSDRES_RES_4       0      0
( 131) unstable device for NSDRES_RES_3         0      0
( 133) unstable device for POLYHRES_RES_2        0      0
( 135) unstable device for POLYRES_RES_1         0      0
Total errors:                                0      0

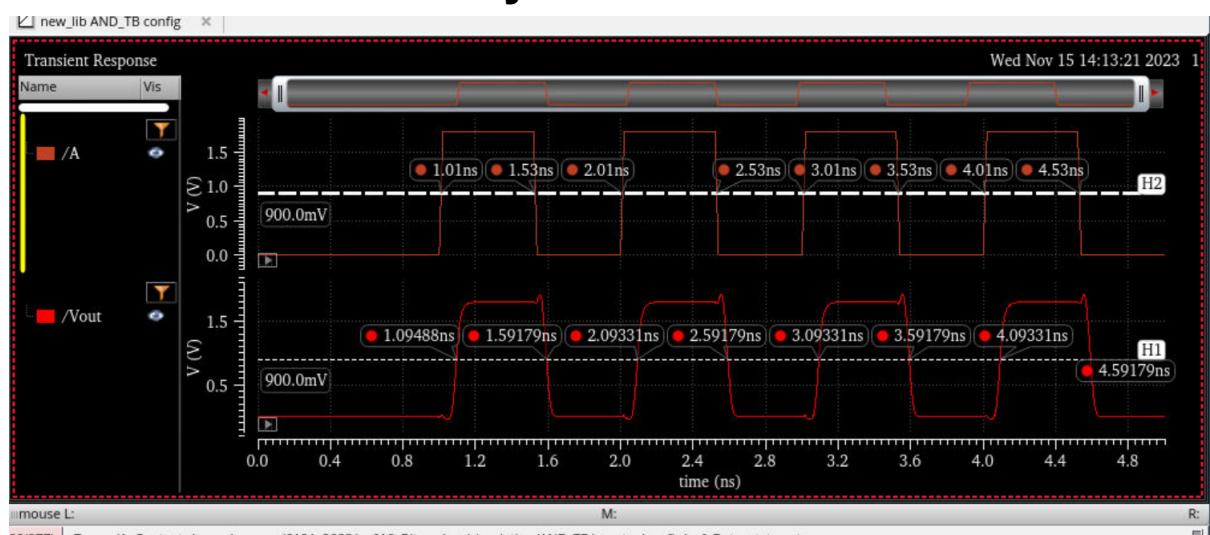
Finished creating Error Database ...
Writing Report into ./AND.err ...
avrpt cpu sec:    0.04 elapsed:    0 virtual:   93M
Finished /cad/cadence/ASSURA41_618//tools.lnx86/assura/bin/avrpt
Starting /cad/cadence/ASSURA41_618//tools.lnx86/assura/bin/avcallproc /users/courses/619A_2023/ee619_Bit_coders/cadence_designs/AND.r
250
L1,029 C1

```

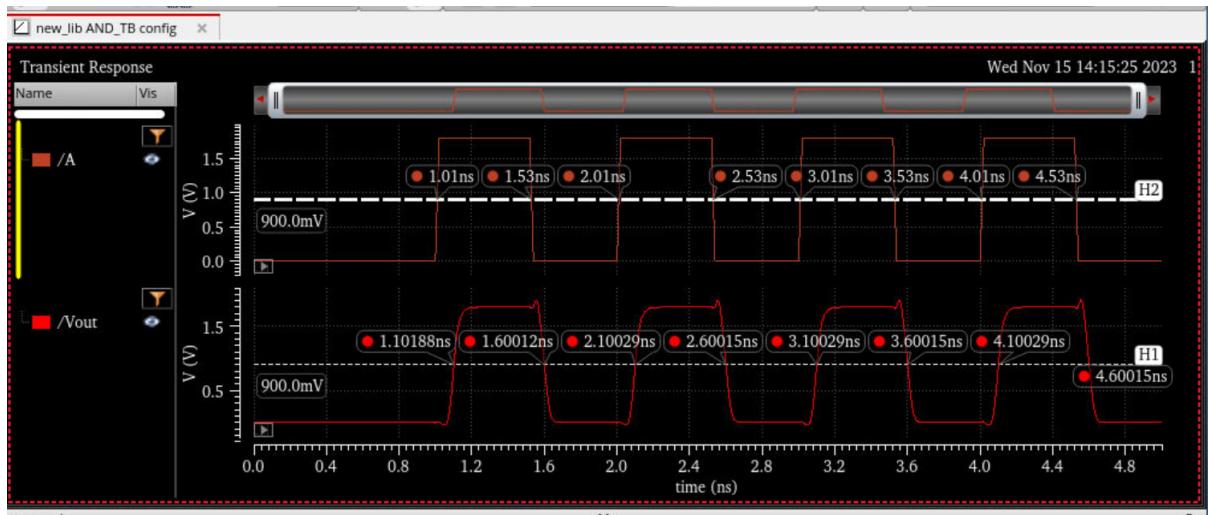
Expression	Value	Value
average(i("/I0/VDD" ?result "tran"))	74.75E-6	82.31E-6

**Power consumption = 134.55uWatt for 5fF**  
**Power consumption = 148.158uWatt for 5fF**

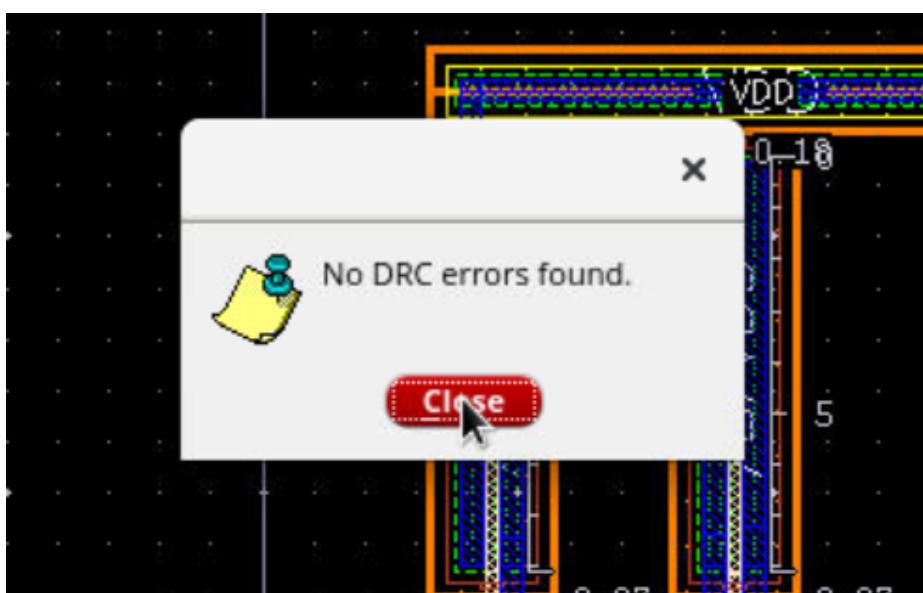
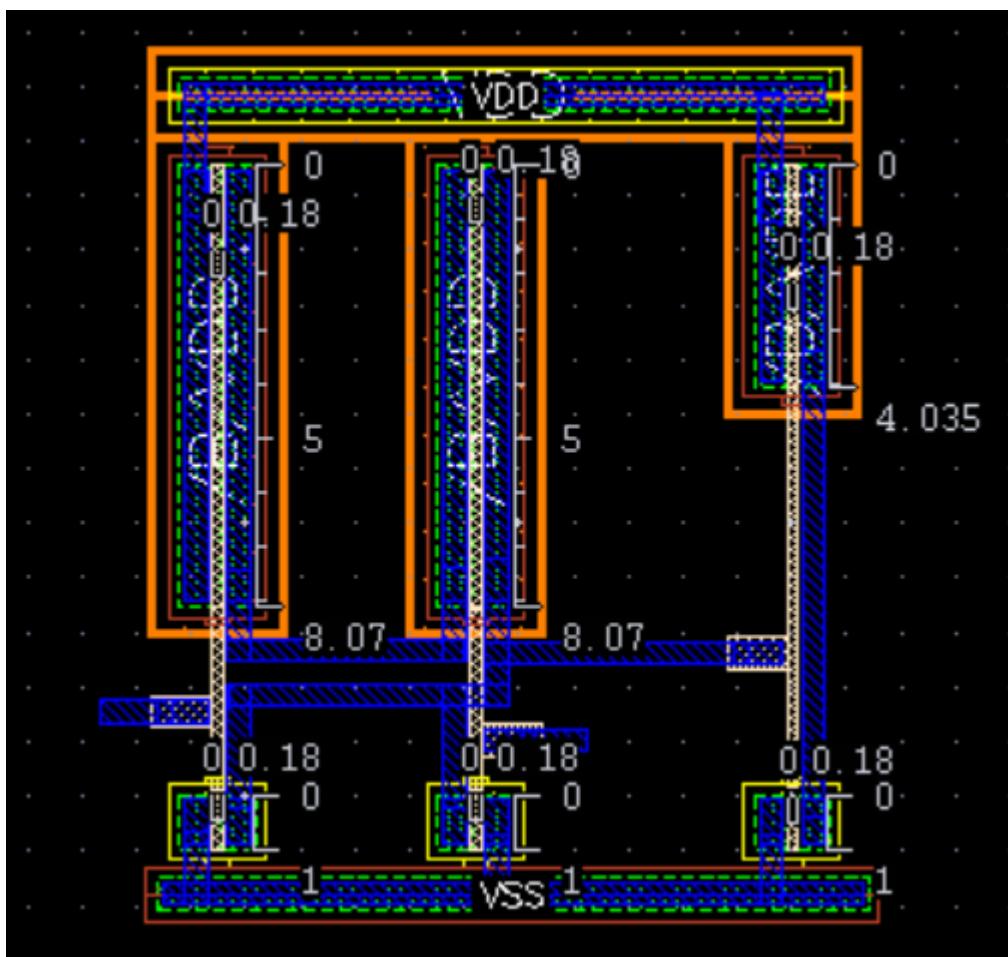
## For 5fF Transient analysis



## For 10f F



## OR Gate



## Run: "OR"

X

Run: "OR" from  
/users/courses/619A\_2023/ee619\_Bit\_coders/cadence\_designs/

ers/

Schematic and Layout Match.  
You currently have an open run (project).

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Summary of LVS Issues

Extraction Information:



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0 cells have 0 Pin mismatches  
0 cells have 0 Parameter mismatches

ELW Information:

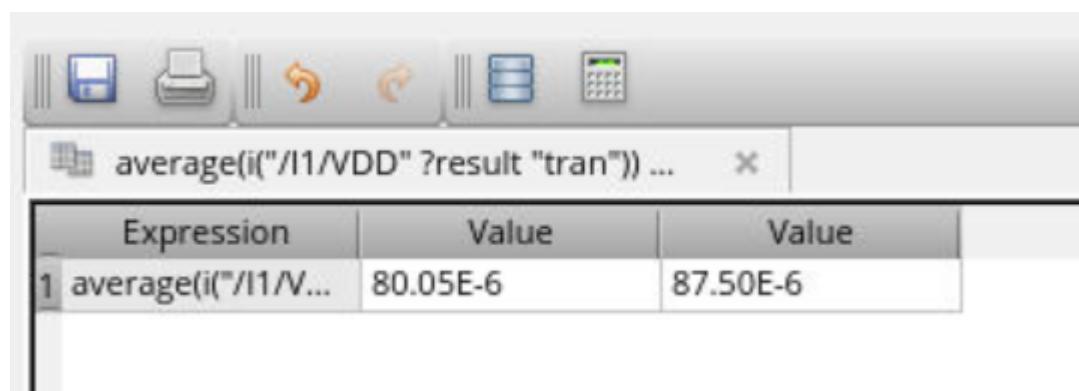
Total DRC violations: 0

Yes

No

Help

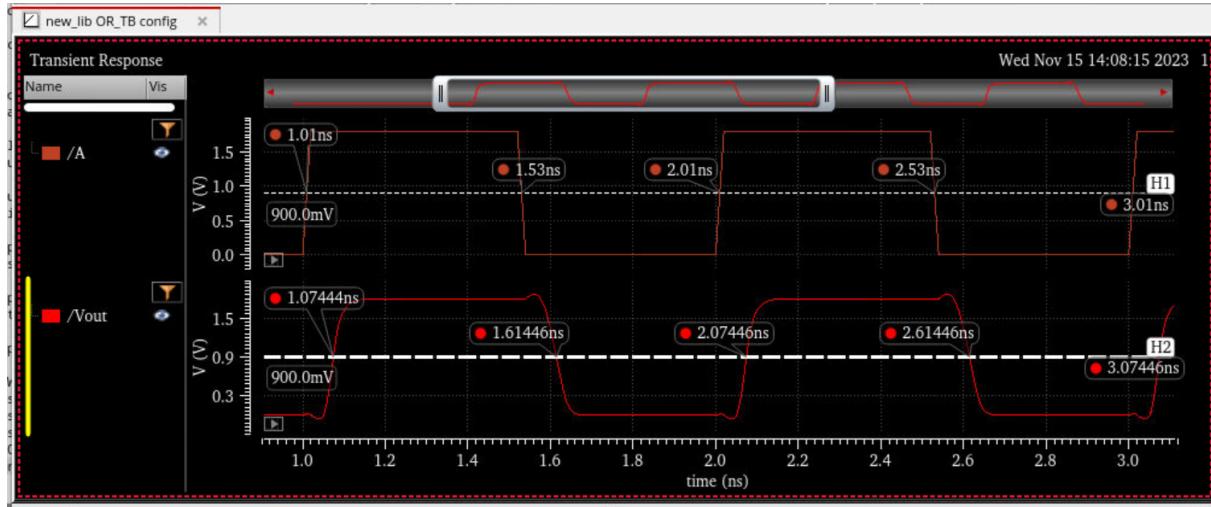
```
File Edit View Help  
n ( 123) unstable device for M1res_RES_7 0 0  
n ( 125) unstable device for NWELLRES_RES_6 0 0  
n ( 127) unstable device for PSDRES_RES_5 0 0  
n ( 129) unstable device for ISONSDRES_RES_4 0 0  
n ( 131) unstable device for NSDRES_RES_3 0 0  
n ( 133) unstable device for POLYHRES_RES_2 0 0  
n ( 135) unstable device for POLYRES_RES_1 0 0  
-----  
Total errors: 0 0  
-----  
Finished creating Error Database ...  
Writing Report into ./OR.err ...  
avrpt cpu sec: 0.05 elapsed: 0 virtual: 93M  
Finished /cad/cadence/ASSURA41_618//tools.lnx86/assura/bin/avrpt
```



**Power Consumption = 144.09uWatt for 5f F**

**Power Consumption = 157.5uWatt for 10f F**

## For 5f F Transient analysis



## For 10f F

