ELECTRONIC VOTING MACHINE (EVM)

INTRODUCTION:

This document specifies the requirements for designing a Verilog module for an Electronic Voting Machine (EVM). The EVM should handle votes for four political parties, debounce button presses, count votes, and display the winning party when the correct passkey is entered and the result display is enabled.

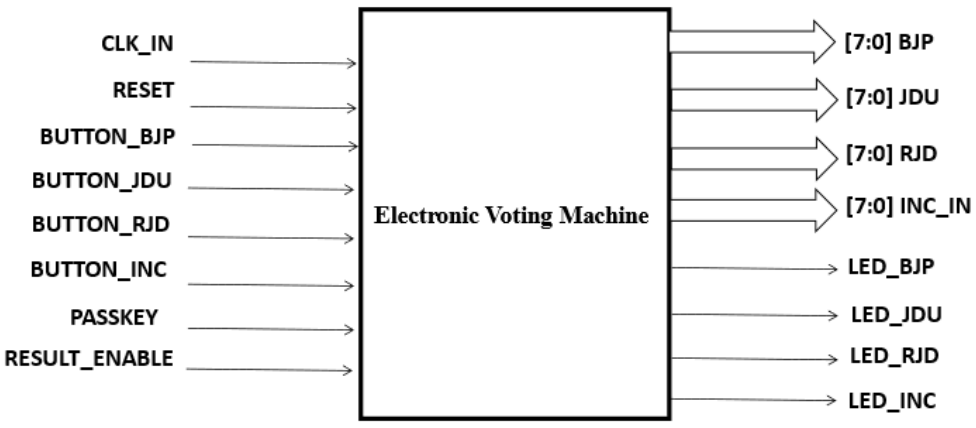
FUNCTIONAL DESCRIPTION:

Inputs:

- **Clock Signal**: Provides timing for synchronous operations.
- **Reset Signal**: Initializes all internal registers and clears ongoing operations.
- **Button Inputs**: Signals for registering votes for each political party.
- **Passkey Input**: 4-bit input for enabling the display of the winning party.
- **Result Enable Signal**: Activates the display of the winning party based on the entered passkey.

outputs:

- **Vote Count Registers**: Registers to store the count of votes received for each political party.
- **LED Indicators**: Indicate the winning party by lighting up when the result is displayed.



Block diagram of Voting Machine

Design Requirements:

1. **Initialization**
    - Upon reset, initialize all vote count registers to zero.
    - Turn off all LED indicators initially.
2. **Debouncing**
    - Implement debounce logic for each button input to prevent multiple vote registrations due to mechanical bouncing.
    - Use an appropriate method (e.g., shift register) to filter out noise and ensure accurate vote counting.
3. **Vote Counting**
    - Increment the respective party's vote count register on a valid button press.
4. **Result Display**
    - Compare the entered passkey with a predefined correct passkey.
    - If the passkey matches and result display is enabled:
        - Determine the party with the highest vote count.
        - Light up the LED corresponding to the winning party.
        - Handle ties by prioritizing parties in a specified order.

Example Test Cases

1. **Vote Count Verification**:
    - Press buttons for each party and verify the respective vote counts increment correctly.
2. **Debouncing Validation**:
    - Simulate noisy signals on button inputs and ensure only one vote is registered per press.
3. **Result Display Testing**:
    - Enter the correct passkey and activate result display, confirm the LED lights up for the party with the highest vote count.
4. **Reset Functionality**:
    - Assert reset signal and observe all counts and LEDs reset to initial states.

conclusion:

In conclusion, this specification document provides a thorough outline for designing an Electronic Voting Machine (EVM) module in Verilog. The module aims to manage voting for four political parties, debounce button inputs, count votes accurately, and display the winning party based on a correct passkey entry and result enablement. Key functional requirements include initializing registers on reset, implementing debounce logic for reliable button presses, and using combinational logic to determine and display the winning party's LED indicator.