UNIT 2

8086 Microprocessors

Dr. Ujjaval Patel

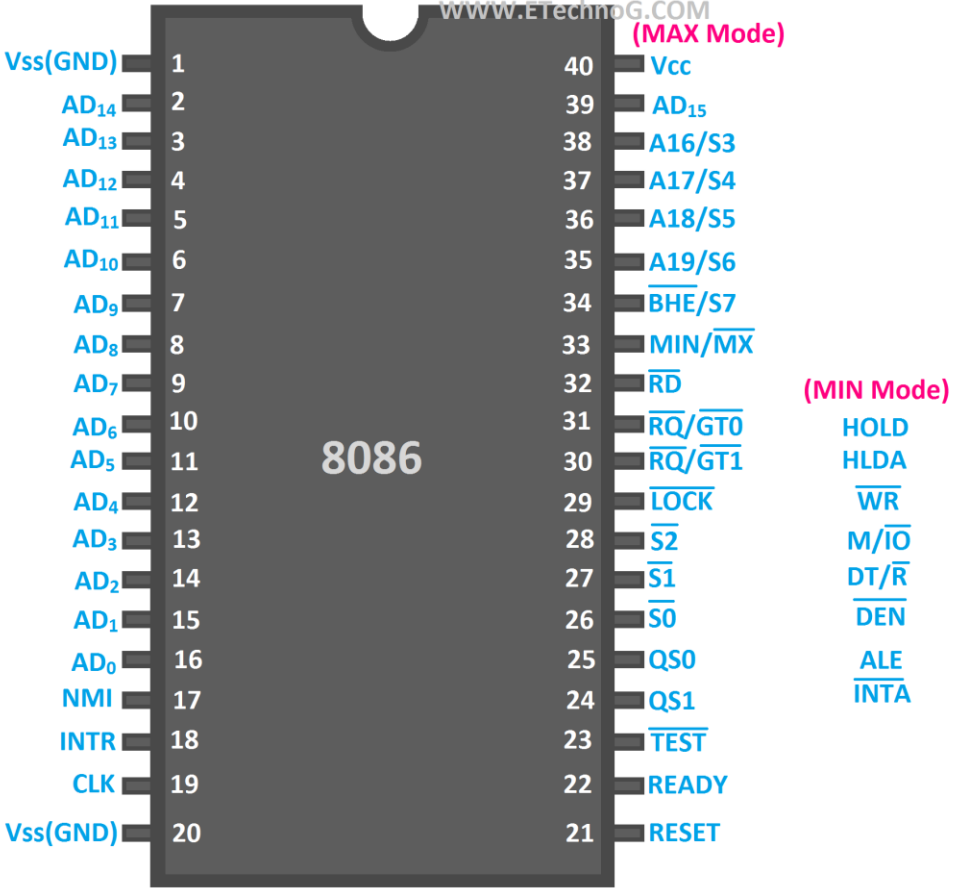
What is Microprocessor?

"Microprocessor is a programmable electronic device that controls interpretation and execution of the instructions. It is called as CPU of the computer". The word micro in the microprocessor refers to its small size and the processor refers to the device that performs computational and control operations.

Salient features of 8086

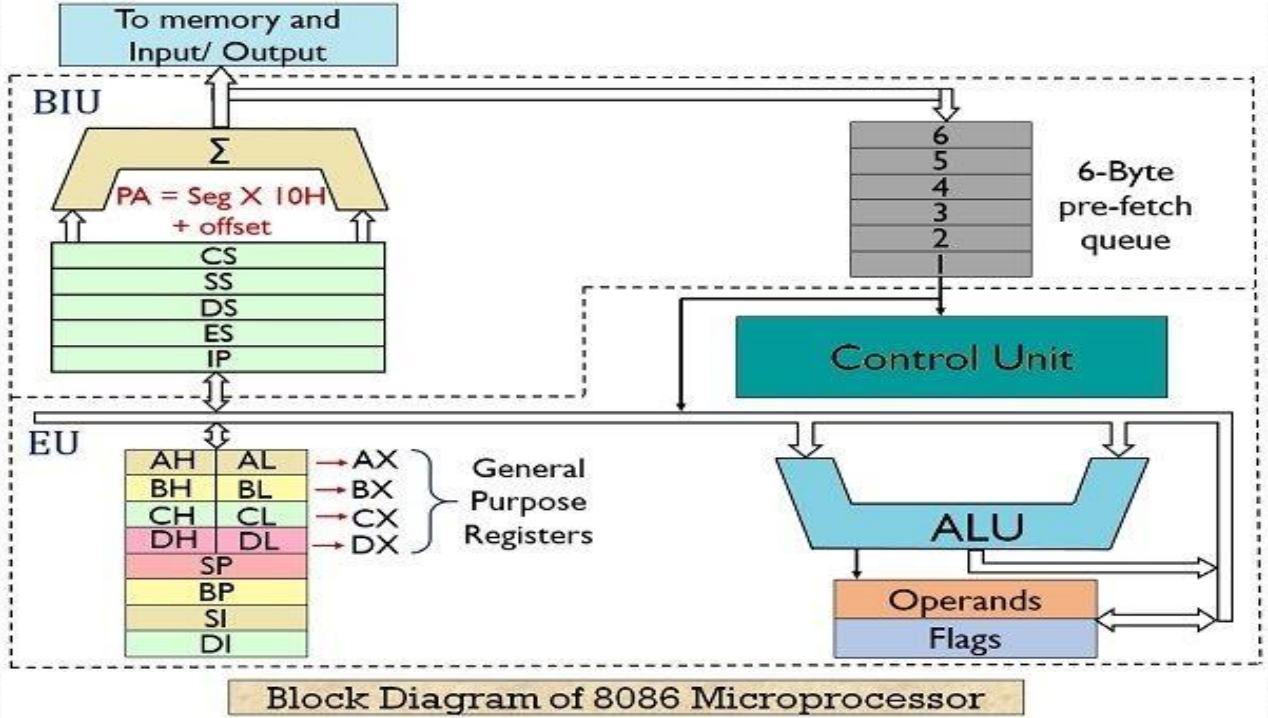
1. The Intel 8086 is a 16-bit microprocessor.
2. It contains approximately 29,000 transistors.
3. The number of address pins is 20 and hence the memory addressing capacity is 2^{20}= 1 megabyte.
4. The 8086 has 20 address pins, 16 of which are also used as data pins. The use of pins for both addresses and data means that both an address and data cannot be sent to the system bus at the same time.
5. This multiplexing of addresses and data reduces the number of pins needed.
6. The 8086 requires only one supply voltage, + 5 V, and one clock phase whose frequency can be up to 5 MHz.
7. There are 16 control lines for various control operations.

8086 Pin Diagram



Microprocessor 8086 Pinout Diagram

8086 Internal Architecture



Block Diagram of 8086 Microprocessor

8086 Internal Architecture

The 8086 internal architecture is divided into two functional units.

They are,

1. Bus Interface Units(BIU)
2. Execution Unit (EU)

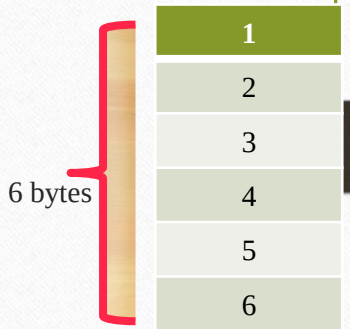
Bus Interface Units(BIU)

- It is responsible of transfer of instructions, addresses and data on the system bus to the execution unit.
- It handles the transfer of the data to the processor with memory and I/O devices.
- It includes instruction fetch, data fetch, address transfer and computation of effective address of the memory.
- The functional parts of BIU are,

1. Instruction Queue (IQ)
2. Segment Registers
3. Instruction Pointer (IP)

Instruction Queue

- The instruction queue is of six bytes in length and is used to speed up the execution of programs, by perfecting six instruction bytes in advance from the memory.
- The prefetched instructions are stored in a group of high speed registers known as the **INSTRUCTION QUEUE.**
- The BIU(Bus Interface Unit) works in parallel with the EU(Execution Unit). The BIU fetches the instruction bytes while the EU is executing an instruction.
- The process of fetching the next instruction in advance while the EU is executing the current instruction is known as **PIPELINING.**



Segment Registers

There are the additional 16-bit registers to generate memory address when combined with the other registers in the microprocessors.

There are four segment registers.

1. Code Segment Registers (CS)
2. Data Segment Registers (DS)
3. Stack Segment Registers (SS)
4. Extra Segment Registers (ES)

Code Segment Register

1. The code segment is a section of a memory that holds the code (programs and procedures) used by the microprocessor.
2. The CS register defines the starting address (Upper 16 bits of the 20-bit starting address of the segment) of the section of memory holding code. The code segment is limited to 64 KB.

Data Segment Register

1. The data segment is a section of memory that contains most data used by a program. Data are accessed in the data segment by an offset address or the contents of other registers that hold the offset address.
2. The data segment is limited to 64 KB.

Stack Segment Register

1. The stack segment defines the area of the memory used for the stack. The stack pointer (SP) determines the location of the current entry point in the stack segment.
2. The BP register also addresses (Access) data within the stack segment. .

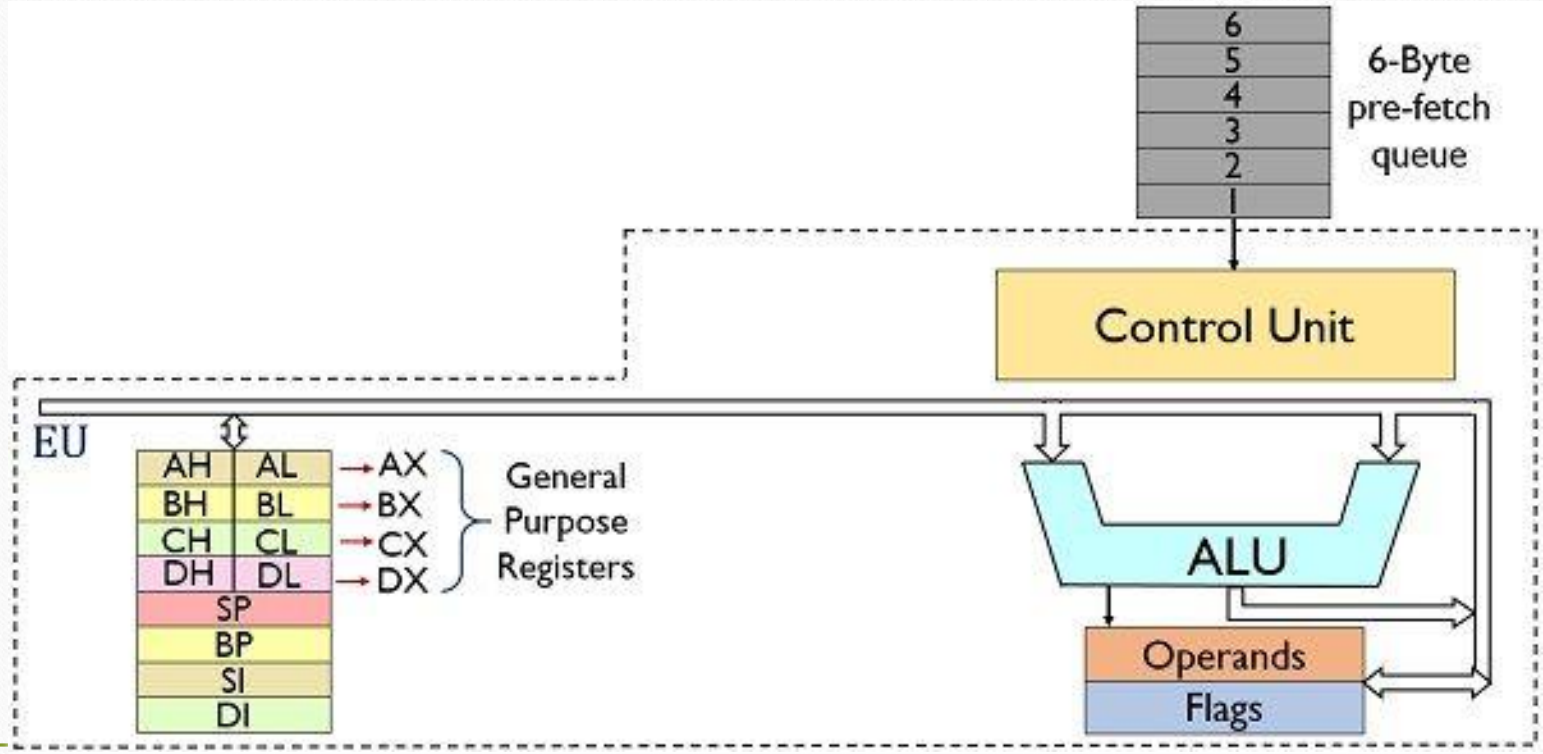
Extra Segment Register

The extra segment is an additional data segment used by some of the string instructions to hold the destination data. The extra segment is limited to 64 KB.

IP (Instruction Pointer)

1. It is designated as IP.
2. The instruction pointer, which points to the next instruction in a program, is used by the microprocessor to find the next sequential instruction in a program located with in the code segment.
3. It is also called as program counter in the microprocessor.

Execution Unit

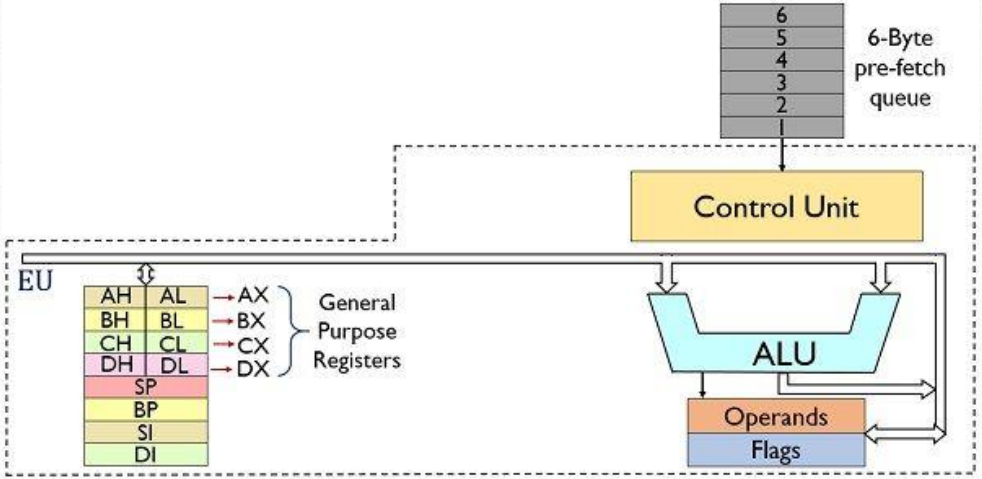


Execution Unit

1. The execution unit works parallel with Bus Interface Unit
2. It informs the BIU the location at which the next instruction or data is to be fetched.
3. The instruction consists of different phases. i.e Fetch, Execute, Decode and Write phases.
4. The Fetch Phase performs the fetching of instructions.
5. The Execution Phase performs actual operation on data.
6. The Decode Phase perform the decoding of instructions.
7. The Write Phase performs the operation of storing the result at destination.

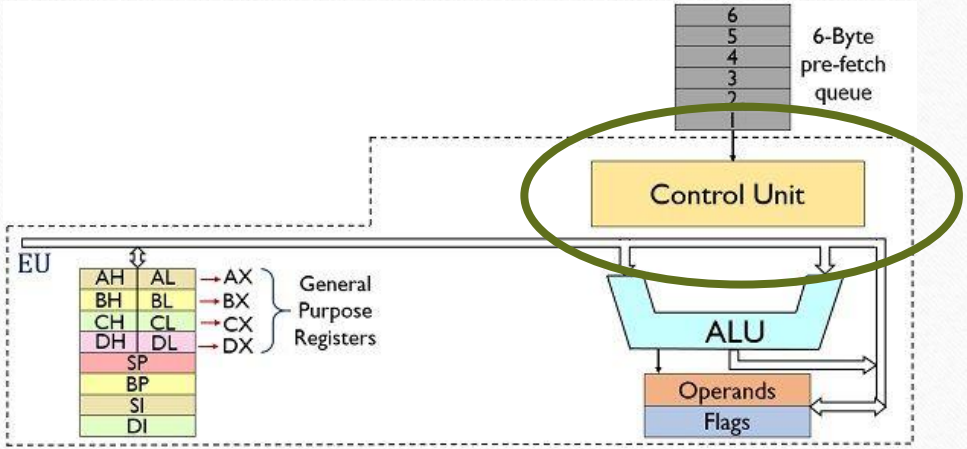
EU Functional Parts:

1. Control system and Instruction Decode
2. Arithmetic and Logic Unit
3. Flag Register
4. General Purpose Registers
5. Stack Pointer Register
6. Pointer and Index registers



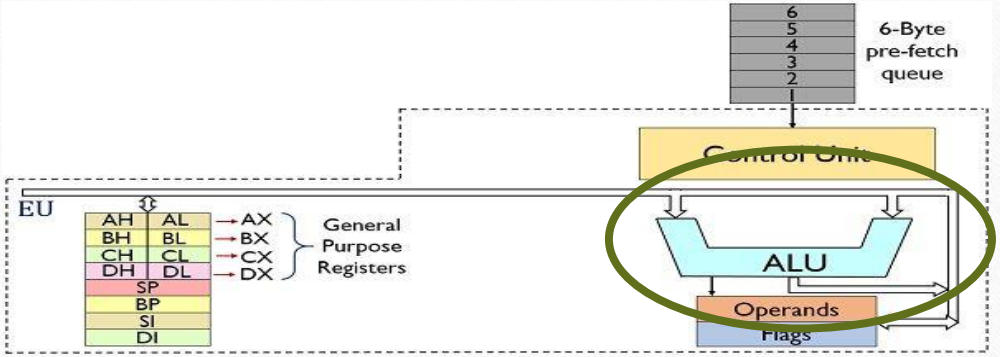
Control system and Instruction Decode

1. It directs all the internal operation of the processor.
2. The instruction in the EU translate the instruction fetched from the memory into a series of actions carried out by the EU.



Arithmetic and Logic Unit

1. It is one of the components of EU.
2. It performs 8-bit or 16-bit mathematical operations such as addition, subtraction, multiplication, division, data conversion and logical operations like NOT, OR, AND.
3. It also performs register increment and decrement and shift operations.



Flag Register:

Processor Status Word (PSW):

1. The register that holds current status of the processor.
2. 8086's PSW contains 16 bits, but 7 of them are not used. Each bit in the PSW is called a ***flag.***

Types of Flags

- Conditional Flag
- Control Flags

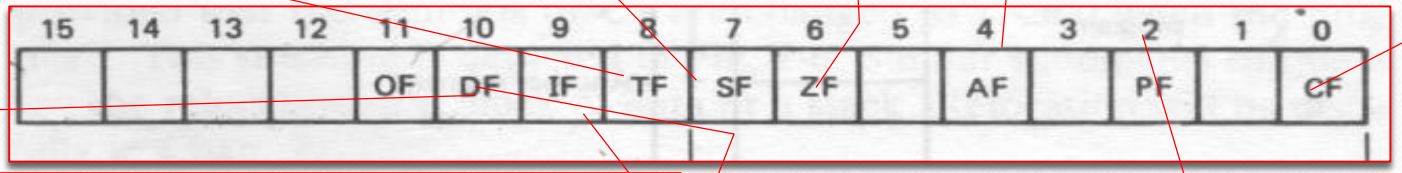
Sign Flag
Is equal to MSB of the result. Negative numbers have a1 in MSB and Non negative numbers then bit is Zero.

Auxiliary Carry Flag
This is set, if there is a carry out of bit 3 during the addition or barrow by bit 3 during subtraction.

Tarp Flag
If this flag is set, the processor enters the single step execution mode by generating internal interrupts after the execution of each instruction

Zero Flag
This flag is set, if the result of the computation or comparison performed by an instruction is zero

Carry Flag
This flag is set, when there is a carry out of MSB in case of addition or a borrow in case of subtraction.



Over flow Flag
This flag is set, if an overflow occurs, i.e, if the result of a signed operation is large enough to accommodate in a destination register. The result is of more than 7-bits in size in case of 8-bit signed operation and more than 15-bits in size in case of 16-bit sign operations, then the overflow will be set.

Parity Flag
This flag is set to 1, if the lower byte of the result contains even number of 1's ; for odd number of 1's set to zero.

Direction Flag
This is used by string manipulation instructions. If this flag bit is '0', the string is processed beginning from the lowest address to the highest address, i.e., auto incrementing mode. Otherwise, the string is processed from the highest address towards the lowest address, i.e., auto incrementing mode.

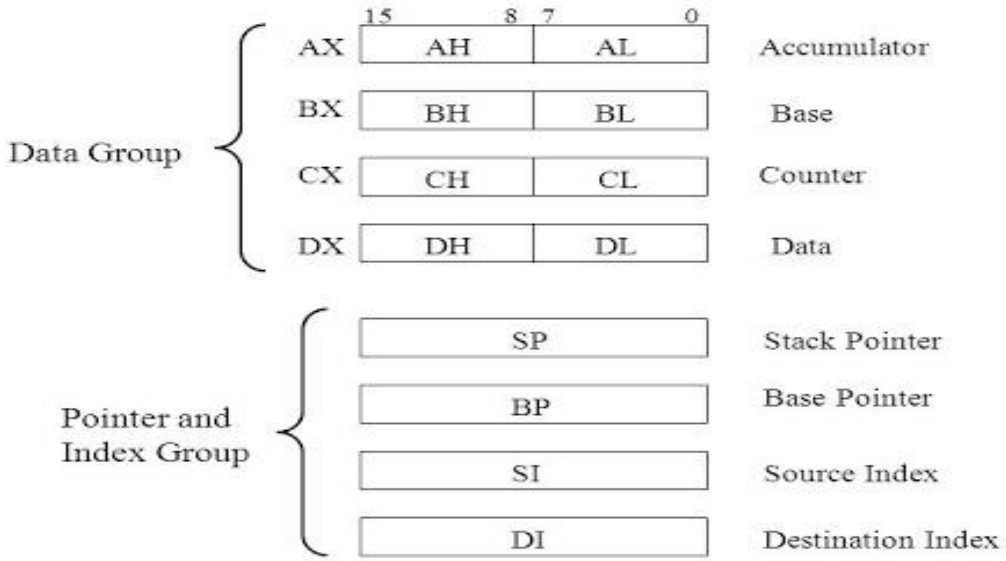
Interrupt Flag
If, set certain type of interrupt is recognised by the CPU, otherwise, these interrupts are ignored.

Consider the following example, if the instruction performed the addition.

```
   0 0 1 0   0 0 1 1   0 1 0 0   0 1 0 1
+  0 0 1 1   0 0  1 1   0 0 0 1  1 0 0 1
-------------------------------------------
   0 1 0 1   0 1 1 0   0 1 0 1   1 1 1 0
-------------------------------------------
```

Then, SF = 0 ZF = 0 PF = 0 CF = 0 AF = 0 OF = 0

1. General Purpose Registers



General Purpose Registers

- ✓ The 8086 processor has four 16- bit general purpose registers.
- ✓ They are, AX, BX, CX, DX
- ✓ Again it can be divided into the two 8-bit registers distinguished as high and low order bytes, referenced as AH, AL,BH, BL, CH, CL and DH, DL.

Accumulator Register (AX)

- ✓ Consists of two 8-bit registers AL and AH, which can be combined together and used as a 16-bit register AX.
- ✓ AL in this case contains the low order byte of the word, and AH contains the high-order byte.
- ✓ Multiplication and Division instructions also use the AX or AL.

Base Register (BX)

- ✓ Consists of two 8-bit registers BL and BH, which can be combined together and used as a 16-bit register BX.
- ✓ It is used to hold the offset address of a location in the memory system.

Count Register (CX)

- ✓ Consists of two 8-bit registers CL and CH, which can be combined together and used as a 16-bit register CX.
- ✓ When combined, CL register contains the low order byte of the word, and CH contains the high-order byte.
- ✓ Instructions such as SHIFT, ROTATE and LOOP use the contents of CX as a counter.

Data Register (DX)

- ✓ It is a general purpose register that holds the port address during certain IN and OUT instruction.

Stack Pointer (SP) and Base Pointer (BP)

- ✓ Both SP and BP registers are 16- bit registers.
- ✓ The register SP points to the current stack of the stack.
- ✓ Where as BP points to the memory location for memory data transfers and also access the data within the stack segment.

Source Index (SI) and Destination Index (DI)

- ✓ Used in indexed addressing.
- ✓ Instructions that process data strings use the SI and DI registers together with DS and ES respectively in order to distinguish between the source and destination addresses.

Source Index (SI) and Destination Index (DI)

- ✓ Used in indexed addressing.
- ✓ Instructions that process data strings use the SI and DI registers together with DS and ES respectively in order to distinguish between the source and destination addresses.

Thank you