Connections (how bord) Memory mapped port mappact PAM+MOV / FEDER TRAM / MPU / ROM device -> Range of addresses (bose + offset ) Supplicities anyphi register > TRM: "Technical reference manual Was Care digital design I Jeis as to ola specs: Memory map: base, and address Il Paripherals Singister.

Peripherals Il april 12 registers Il act, offsots II -> Bus Bridges .. Says Mo s M & Bus System Bus lle rate Il Moi ilie DMAT TAND Bridge (AHB) SIS WELLS INC. JAN AXT II

(AXI >AHB) AXI we go, I AHB ( moster won't mully Peripheral player i lisae it ing peripherals - on complegate Jego act & granter was one > HW Ports Two ty Des Protocal type AYY AHR ABB CHI mester slave ivitate transaction > W pras HR (Address, data, size) 10 M - my Allges Slave 11 money IFU

=> AMBA. "ARM Advanced Microcontroller Bus Architecture" standard -> reveability 1 Bus -> B.W -> Frax magh = (4) > Laterray MCU Clocks CLX -> 80 MHZ - 1320 => Clock Tree TRM TRM Suprison water Missi jusain al Pariphoralsasses wir Power consumption Il Frequency 11600; ald F & P بحتاع ترد قلل فله أفيه باور في الفامي 0) Egical lobian 1000 Power, clock moragement no Ju Ju Mc Steen Winiti Co Peripherals 11 St By default alger Je clk 16 (Roset and clock control) RCC and ARM Ilia Bripland in line atmega 11 5; - it MC air ( Peripherals ) (i) CLK Il is a line Jobbalalia joji CLK No RCC acienção > General topology of the CIK Arch. (SYSCIK) clock maragement unit fre com WI MC 11 JO cla Min CPU D 7 Flash Clock Crystal E cerouse 3 JGPIO