LAB4 – preparation report

FPGA based Digital Design

Omri Raz – 318671120

Eyal Rothschild – 318793882

Introduction:

• Understanding of digital system synthesis.

• FPGA design as a target HW.

• we will learn to use the Quartus program.

In this laboratory we will synthesize a Synchronic Digital System based on Lab1 in addition to PWM unit.

Performance Test Case:

In this test case, we will test the performance, area, and functionality of a **digital system.**
in order to check the ALU from lab 1, we add 2 registers – one before the ALU unit and one after the ALU unit.
we did it because the ALU from lab 1 is an a-synchronic unit, without a clock.

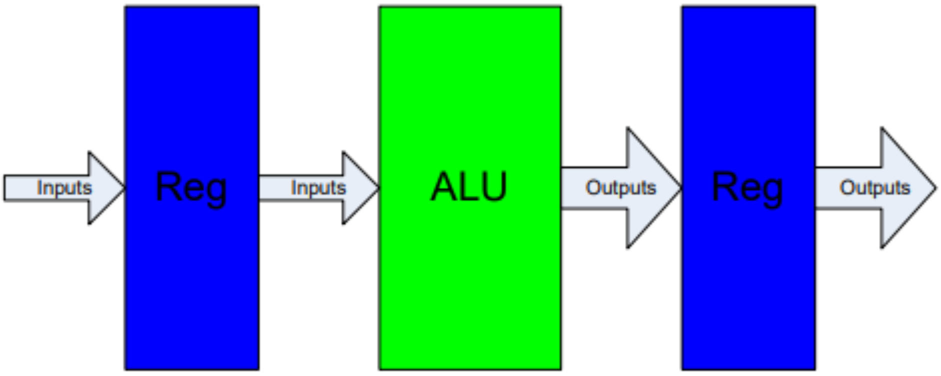
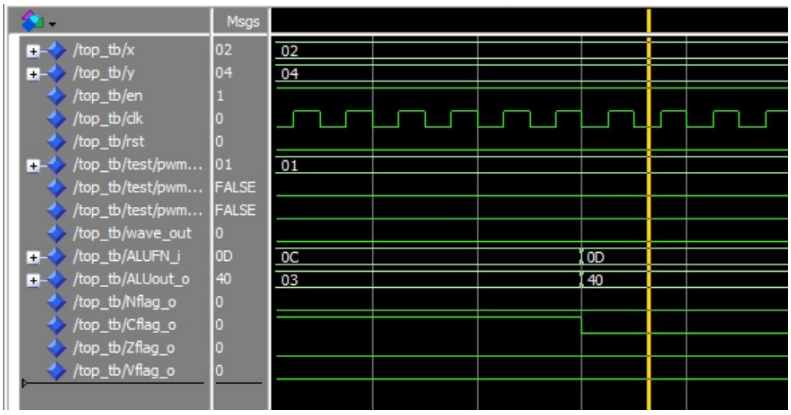


Figure 1 : Test Case in case of pure logic system as ALU

ModelSim simulation:

We will present a few of our test.

We tested our ALU and PWM units separately and the whole system as a hole.



	Msgs
/top_tb/x	02
/top_tb/y	04
/top_tb/en	1
/top_tb/clk	0
/top_tb/rst	0
/top_tb/test/pwm...	01
/top_tb/test/pwm...	FALSE
/top_tb/test/pwm...	FALSE
/top_tb/wave_out	0
/top_tb/ALUFN_i	0D
/top_tb/ALUout_o	40
/top_tb/Nflag_o	0
/top_tb/Cflag_o	0
/top_tb/Zflag_o	0
/top_tb/Vflag_o	0

Figure 2 – ALU test

here we tested our ALU unit, we did a simple test:
we tested the “Y-1” function and the “swap” function.
as we can see the test was asuccess.

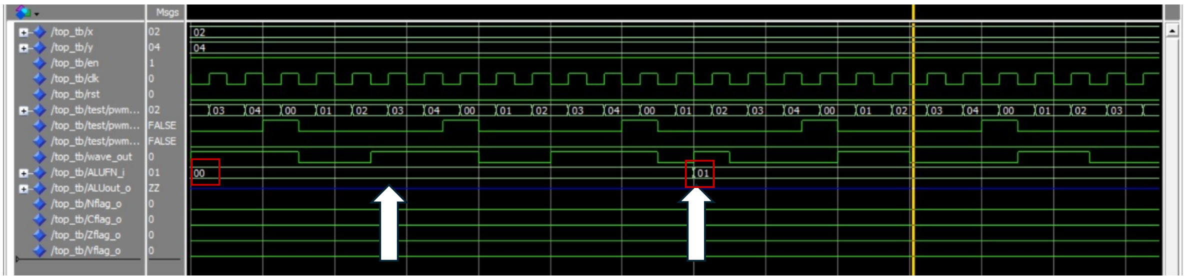
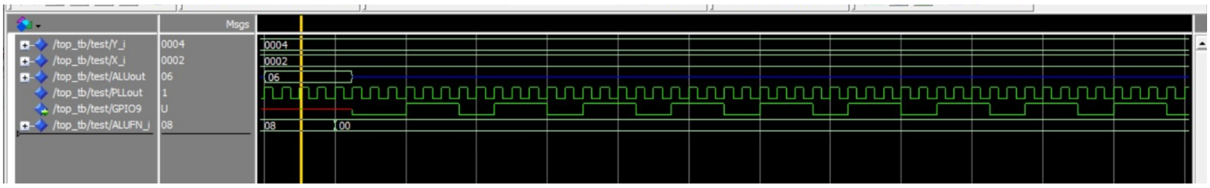


Figure 3 – PWM test

Here we can see our test for the PWM – the critical point is the change of the “ALUFN” from 0 to 1, and the change of our wave respectively.

Worked wonderfully!



	Msgs
/top_tb/test/Y_i	0004
/top_tb/test/X_i	0002
/top_tb/test/ALUout	06
/top_tb/test/PLLout	1
/top_tb/test/GPIO9	U
/top_tb/test/ALUFN_i	08

Figure 4 – Top test

Now we can see the test for the top.

We did 2 simple tests:

First, we tested the ALU and checked the add function 4+2 = 6 then we checked the PWM in mode 0.

The test was successful.

Finding the maximal frequency:

In order to find the maximal frequency of the system we enveloped the ALU module with synchronous objects.

In addition, we have found the maximal frequency of each component separately.

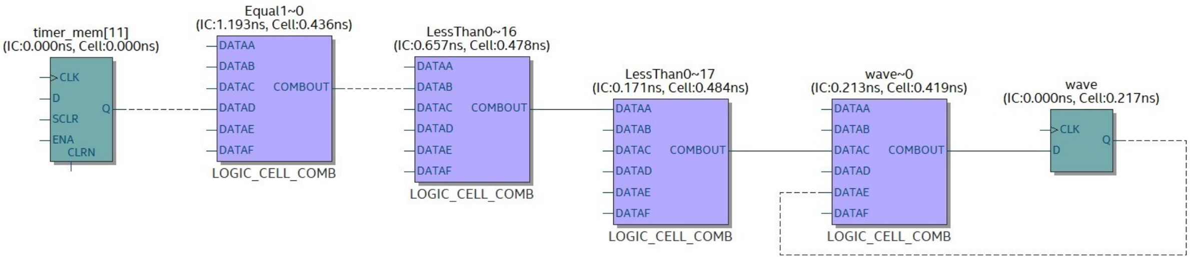


Figure 5 – critical PWM ALU

This is the critical path of the PWM unit.

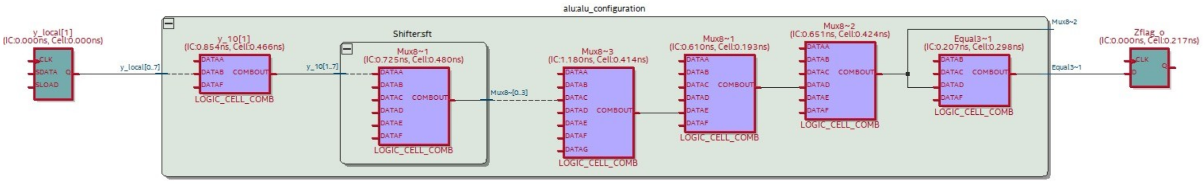
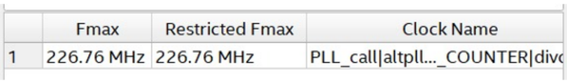


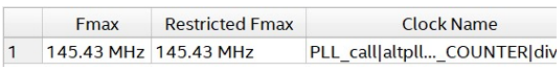
Figure 6 – critical path Top

This is the critical path of the Top, we can see that the path is going through the ALU unit, through the shifter.



	Fmax	Restricted Fmax	Clock Name
1	226.76 MHz	226.76 MHz	PLL_call|altpll..._COUNTER|divc

Figure 7 – Fmax PWM



	Fmax	Restricted Fmax	Clock Name
1	145.43 MHz	145.43 MHz	PLL_call|altpll..._COUNTER|div

Figure 8 – Fmax Top

As we can see our Fmax of the system is determine from the ALU Fmax, without the ALU the Fmax of PWM unit is much larger (the system is faster) then when we add the ALU to the system.

Explanation of the system:

We will explain our system.

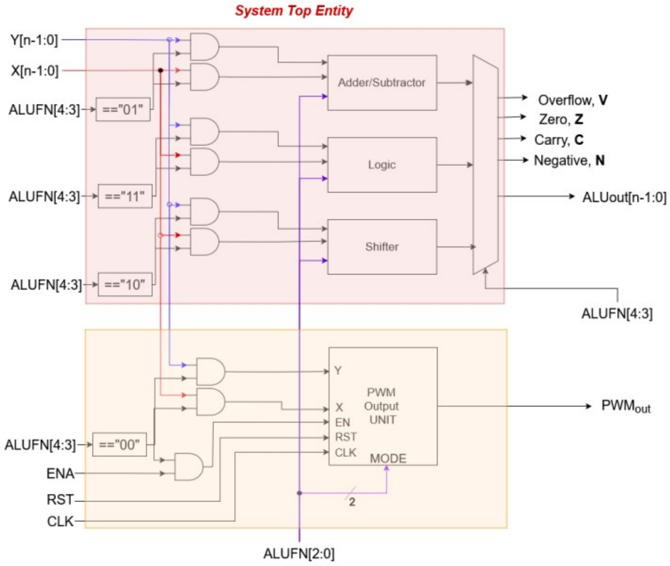
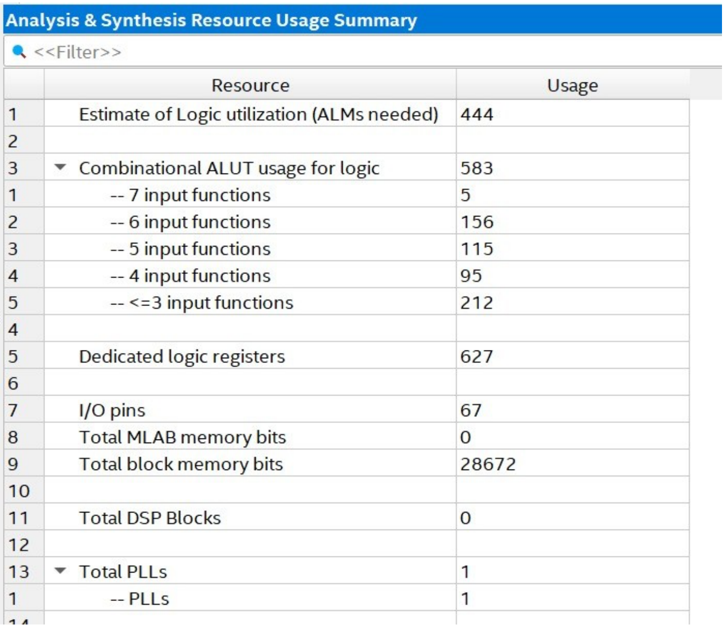


Figure 9 – System Top Entity

Our system is built from 2 units – the ALU and the PWM.
This is the resource usage:



Analysis & Synthesis Resource Usage Summary

<<Filter>>

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	444
2		
3	Combinational ALUT usage for logic	583
1	-- 7 input functions	5
2	-- 6 input functions	156
3	-- 5 input functions	115
4	-- 4 input functions	95
5	-- <=3 input functions	212
4		
5	Dedicated logic registers	627
6		
7	I/O pins	67
8	Total MLAB memory bits	0
9	Total block memory bits	28672
10		
11	Total DSP Blocks	0
12		
13	Total PLLs	1
1	-- PLLs	1
14		

Figure 10 – Resource usage summary

ALU:

Our ALU component is built from several sub systems, its goal is to perform arithmetic and logical operations according to the user requirements.

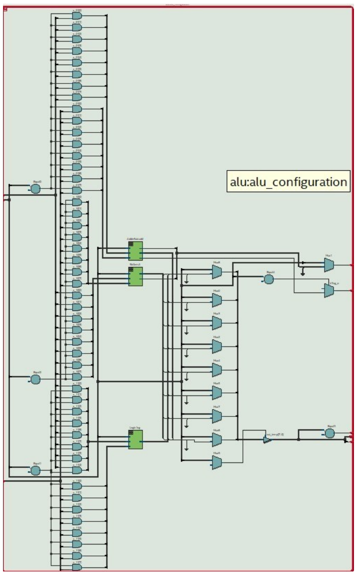


Figure 11-ALU RTL

Here we can see the RTL of the ALU.

The ALU is built from several sub-components

AdderSub:

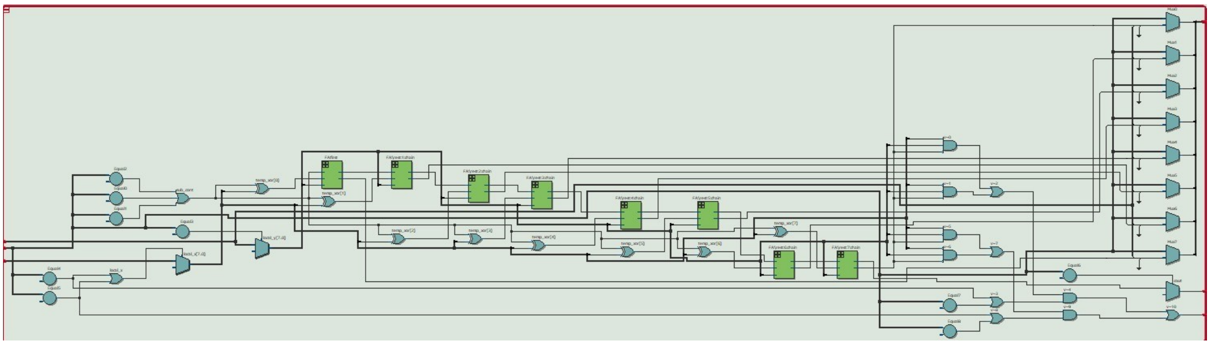


Figure 12 - AdderSub RTL

Logic unit:

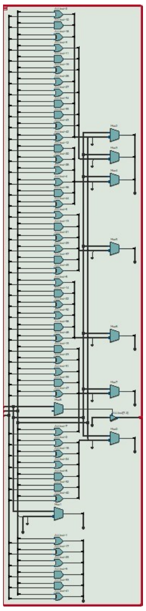


Figure 13 -Logic RTL

Shifter:

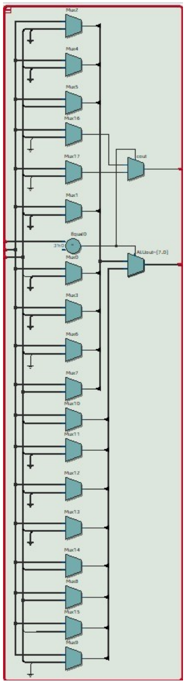


Figure 14 -Shifter RTL

- Most of the units are explained in prep for lab1.

PWM:

The goal of this unit is to create a wave according to the demand of the user, as explained in the task.

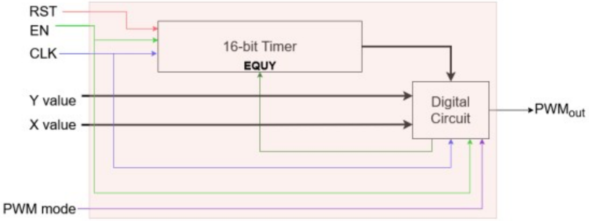


Figure 15 –PWM subparts

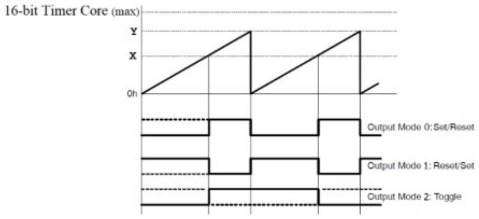


Figure 16 –PWM output unit

Our PWM unit is built exactly the way we were asked to in the task:

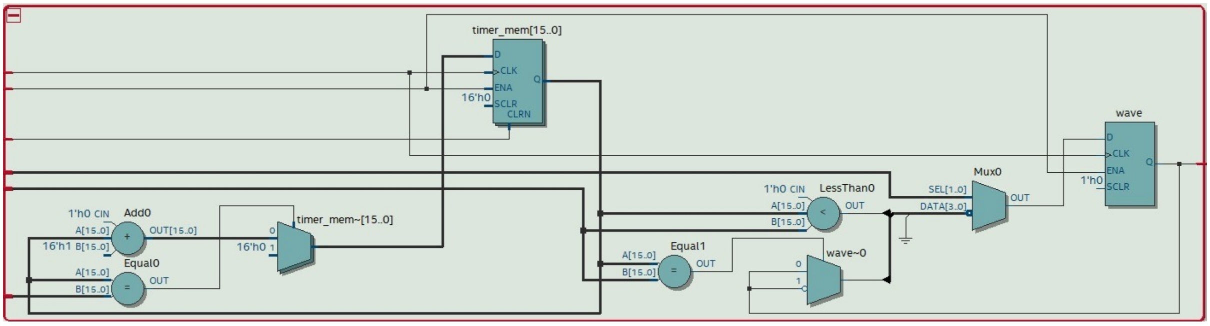


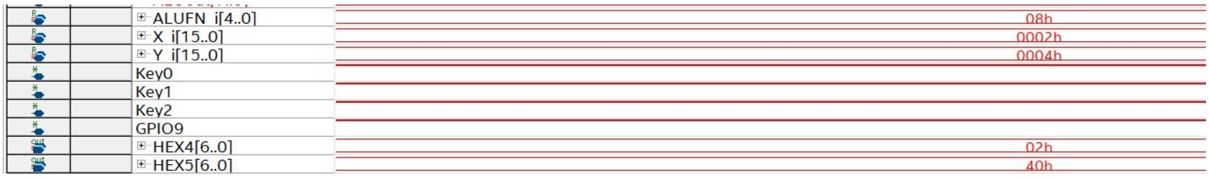
Figure 17 - PWM RTL

This is the RTL of the PWM unit.

Signal tap:

We performed the verification of the system via the signal tap function in the quartus software.

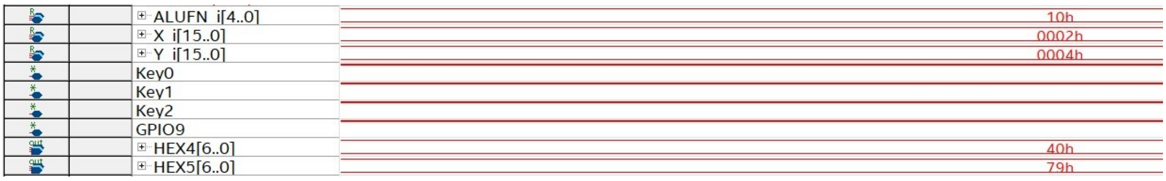
We decide to test few functions in the verification stage.
first we tested “add” and “shift” left functions in the ALU:



ALUFN_i[4..0]	08h
X_i[15..0]	0002h
Y_i[15..0]	0004h
Key0	
Key1	
Key2	
GPIO9	
HEX4[6..0]	02h
HEX5[6..0]	40h

Figure 18 – signal tap add function

This is signal tap simulation for add function.



ALUFN_i[4..0]	10h
X_i[15..0]	0002h
Y_i[15..0]	0004h
Key0	
Key1	
Key2	
GPIO9	
HEX4[6..0]	40h
HEX5[6..0]	79h

Figure 19 – signal tap shift left function

Signal tap simulation for shift left function.

Then we tested the PWM :

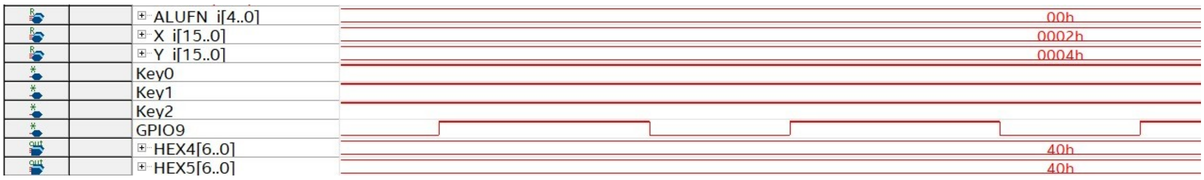


Figure 20 – signal tap PWM