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| Light  Separator | **Digital Design and Logical Synthesis for**  **Computer Engineering (36113611)**  **Course Project** |
| **Digital High Level Design**  **Version 0.1** |

Version 0.1 4 June 2007

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**Revision Log**

|  |  |  |  |  |  |
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**Table of Content**

[LISt of figures 5](#_Toc172279519)

[List of tables 6](#_Toc172279520)

[1. Verification Plan 20](#_Toc172279564)

[1.1 Verification Test Objectives 20](#_Toc172279565)

[1.2 Test Bench Architecture and Functionality 20](#_Toc172279566)

[1.3 Test Bench Input & Output 20](#_Toc172279567)

[2. Verification Results 21](#_Toc172279568)

[3. Appendix 24](#_Toc172279572)

[3.1 Terminology 24](#_Toc172279573)

[3.2 References 24](#_Toc172279574)

# LISt of figures

[Figure 1: Test Bench Block Diagram 9](#_Toc181935849)

[Figure 2 – Code coverage percentage results. 10](#_Toc181935849)

[Figure 3 – Coverage results 11](#_Toc181935849)

[Figure 4 – WaveForms 11](#_Toc181935849)

[Figure 5 - Matlab golden model comparison 11](#_Toc181935849)

# List of tables

[Table 1: Test Plan Functionality 10](#_Toc181935851)

[Table 2: Test Plan FunctionalCheckers 12](#_Toc181935852)

# Verification Plan

This section will describe the design verification strategy that we took as a basis for defining the testbenches.  
This paper will include:

1. Test name/number.
2. Functionality tested.
3. Test data set.
4. Expected results.
5. Any observations from the actual simulation of the design mode under test.

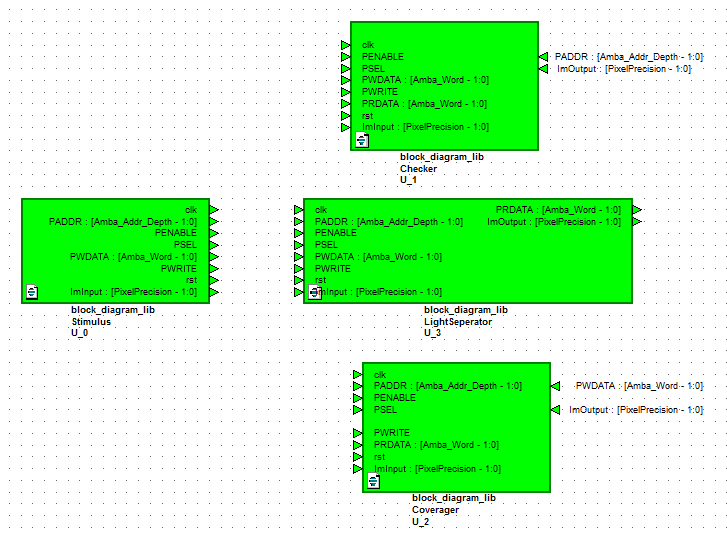
## Verification Test Objectives

The objective of the testing is to create verification test for part 1 of our final project. We created verification plane using deferent scenarios: standard, extreme and forbidden.

## Test Bench Architecture and Functionality

The testbench is following the APB protocol to test the light separator by the following steps.

1. Read data of B from the register bank
2. Read the pictures data
3. Calculate the output image
4. Send out the output image



1. Test Bench Block Diagram

## Functional Coverage

In this section, we will present the functional coverage for few deferent standard and extreme scenarios.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **FUNCTION** | **EVENT** | **COVERAGE POINT** | **BINS** | **Scenario** |
| **Reset\_value** | **Rst** | **Rst** | **0, 1** | **Standard** |
| **Pixel\_input\_value** | **Posedge clock** | **ImInput** | **[0 : ]** | **Standard** |
| **Pixel\_output\_value** | **Posedge clock** | **ImOutput** | **[0 : ]** | **Standard** |
| **PADDR\_value** | **Posedge clock** | **PADDR** | **[0 : ]** | **standard** |
| **PENABLE\_value** | **Posedge clock** | **PENABLE** | **0, 1** | **standard** |
| **PSEL\_value** | **Posedge clock** | **PSEL** | **0, 1** | **standard** |
| **PWDATA** | **Posedge clock** | **PWDATA** | **[0 : ]** | **standard** |
| **PWRITE\_value** | **Posedge clock** | **PWRITE** | **0, 1** | **standard** |
| **PRDATA\_value** | **Posedge clock** | **PRDATA** | **[0 : ]** | **standard** |
| **Output less then 0** | **Posedge clock** | **ImOutput** | **0** | **Extreme** |
|  |  |  |  |  |
| **ADDR more then 8** | **Posedge clock** | **ADDR** | **2,4,8** | **Forbidden** |

Table 1: Test Plan Functional Coverage

## Test Bench Functional Checkers

In this section' we will present the functional checkers that implemented in the project.

We have cover reset, write/read from internal registers and AMBA APB protocol state machine.

|  |  |  |  |
| --- | --- | --- | --- |
| **Event** | **Condition** | **Expected Result** | **Scenario** |
| **Reset Active** | **Rst==0** | **PRDATA== & ImOutput==0** | **Standard** |
| **Setup to acces read state** | **Posedge clock, PENABLE==0, PWRITE==1, PSEL==1** | **|-> PSEL==1 & PENABLE==1** | **Standard** |
| **Setup to acces write state** | **Posedge clock, PENABLE==0, PWRITE==0, PSEL==1** | **|-> PSEL==1 & PENABLE==1** | **standard** |
| **Acces to setup state** | **Posedge clock, PENABLE==1, PSEL==1** | **|-> PENABLE==0 & PSEL==1 &** | **Standard** |
| **Acces to idle stae** | **Posedge clock, PENABLE==1, PSEL==1** | **|-> PENABLE==0 & PSEL==0** | **standard** |

Table 2: Test Plan Functional Checkers

# Verification results

In this section, we will show some of the results of our verification.

* In figure (2) we can see the code coverage percentage results.
* In figure (3) we can see the checker results
* In figure (4) we can see the WaveForm of the LightSeperator internal and external ports and registers.
* In figure (5) we can see the comparison between our design to the matlab golden model. The parameters in the golden model are: Amba\_Addr\_Depth = 4, Amba\_Word = 32, N = 4, PixelPrecision  = 8, Row = 1, Col = 1.

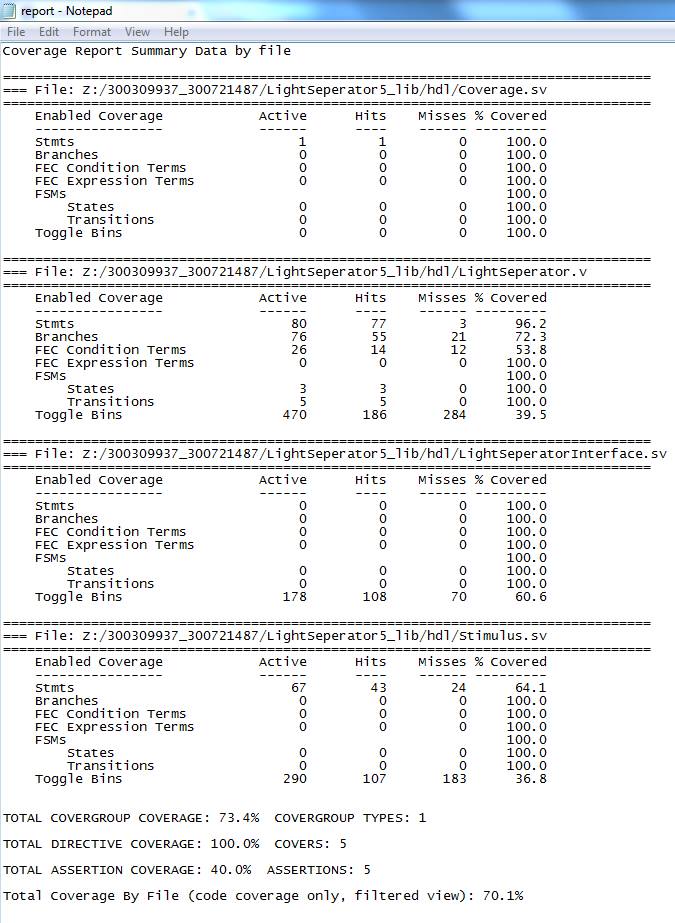


Figure 2 – Code coverage percentage results.

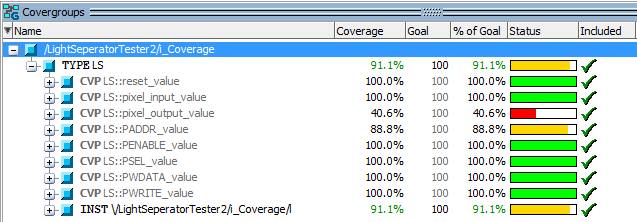


Figure 3 – Coverage results

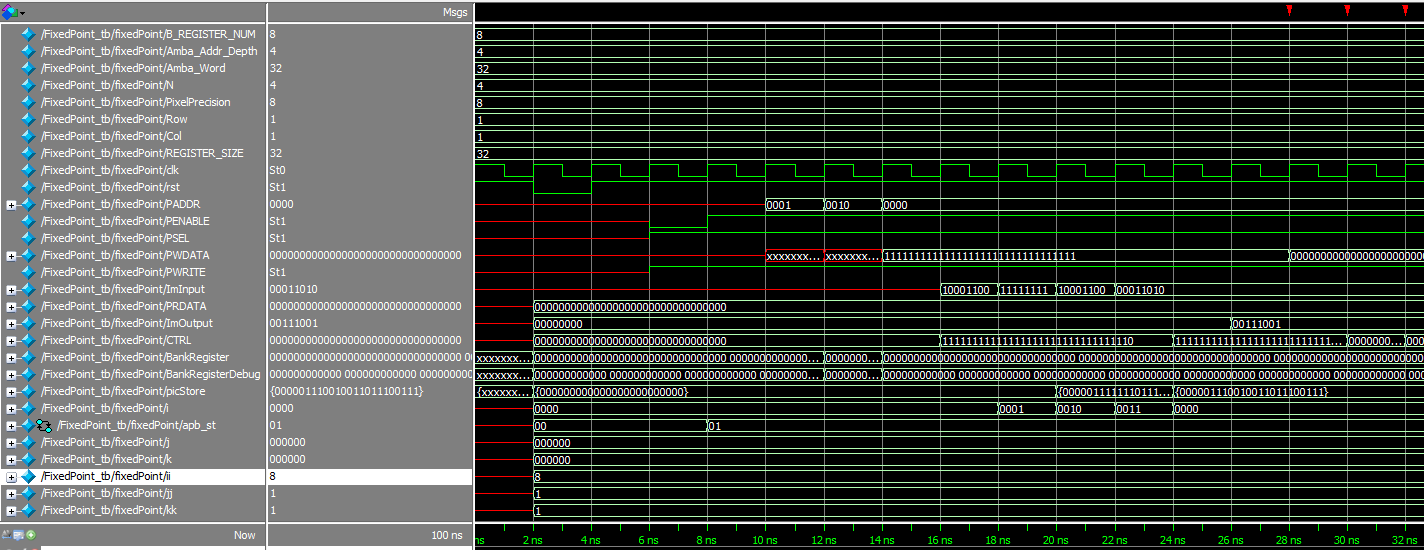
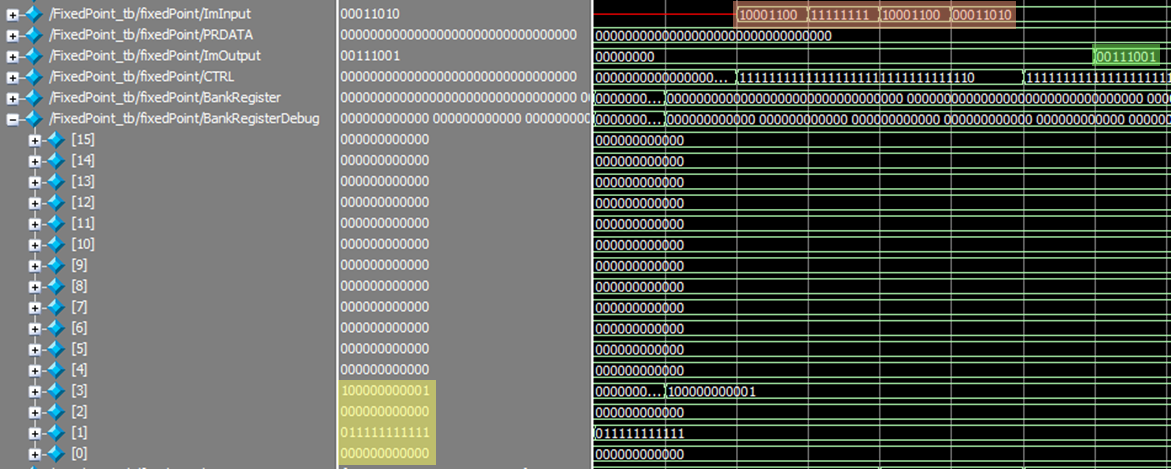
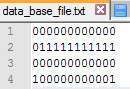


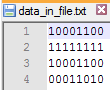
Figure 4 – WaveForms

ImInput





ImOutput



Coefficients



Figure 5 - Matlab golden model comparison

# Appendix

## Terminology

**LSB** - Least Significant Bit

**TBR** - To Be Reviewed

**TBD** - To Be Defined

## References

[1] AMBA™ Specification, (Rev 2.0), by ARM, 1999.