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| Shadow Remover |  |
| **Digital Design and Logical Synthesis (361113611) Course Project**  **Design Synthesis**  **Version 0.1** |
|  |  |

# Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| **Rev** | **Change Description** | **Done By** | **Date** |
| 0.1 | Initial document | Eyar Gilad, Lierez Tzur | 13,Jan,2015 |

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# Unit FSM

Figure 1 Unit FSM

Since part 2 we transited to view the unit as an FSM machine which its state is represented by its CTRL register and operates as shown in Figure 1. This new perspective helped us to better understand and redesign the unit.

# Design Constraints

|  |  |
| --- | --- |
| Constraint type | Description |
| Clock period | At least 30Mhz |
| Clock Max External Latency | 0.2 ns |
| Clock Max Internal Latency | 0.1 |
| Clock uncertainty | 0.6 ns |
| Clock transition time | 0.7 ns |
| input delay | 2.5 ns |
| output delay | 1 ns |
| design area | Smallest |
| driving cell | Smallest not gate |
| output load | load of biggest DFF |
| Input transition | 0.1 |
| wire load model | tsmc18\_wl50 |

Table 1 General Larger Design Timing Constraints.

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| False Path | | | | | | | | | | | | |
| From Pin/Port | Through Pin | | | | To Pin/Port | | | | Comments | | | |
|  |  | | | |  | | | |  | | | |
| Clock Definitions | | | | | | | | | | | | | |
| Constraint Name | | | | clk | | | | Comment | | | | | |
| Period [Nano Seconds] | | | | 20 | | | |  | | | | | |
| Rising edge [Nano Seconds] | | | | 0 | | | |  | | | | | |
| Falling edge [Nano Seconds] | | | | 10 | | | |  | | | | | |
| Pin/Port name | | | | clk | | | |  | | | | | |
| Uncertainty | | | | 0.6 ns | | | |  | | | | | |
| Transition | | | | 0.7 ns | | | |  | | | |  | |
| External Delay [Nano Seconds] | | | | | | | | | | | | |
| Pin name | | | | Value | | | | | | | Comment | | |
| \*All\* Input pins | | | | 2.5 ns | | | | | | | clk, rst, ImInput, PSEL, PWDATA, PWRITE, PADDR, PENABLE | | |
| Load [Pico Farads] | | | | | | | | | | | | | |
| Pin name | | | |  | | | | | | |  | | |
| \*All\* Output pins | | | | 0.0038 [Pico Farads]  (DFFX4) | | | | | | | ImOutput, PRDATA | | |
| External Driver | | | | | | | | | | | | | |
| Pin name | | | Standard Cell Name | | | | Cell Port name | | | | Comment | | |
|  | | | INVXL | | | | Input – A  Output - Y | | | |  | | |
| Multi-cycle Path | | | | | | | | | | | | | | |
| From Pin/Port | | Through Pin | | | | To Pin/Port | | | | Comments | | | | |
|  | |  | | | |  | | | |  | | | | |

Table 2 Timing Constraints by pin names.

# Design summary

# Design area report

Number of ports: 89

Number of nets: 1597

Number of cells: 1097

Number of combinational cells: 795

Number of sequential cells: 267

Number of macros/black boxes: 0

Number of buf/inv: 180

Number of references: 84

Combinational area: 94483.067079

Buf/Inv area: 4201.243314

Noncombinational area: 20387.505524

Macro/Black Box area: 0.000000

Net Interconnect area: 1969809.924728

Total cell area: 114870.572602

Total area: 2084680.497331

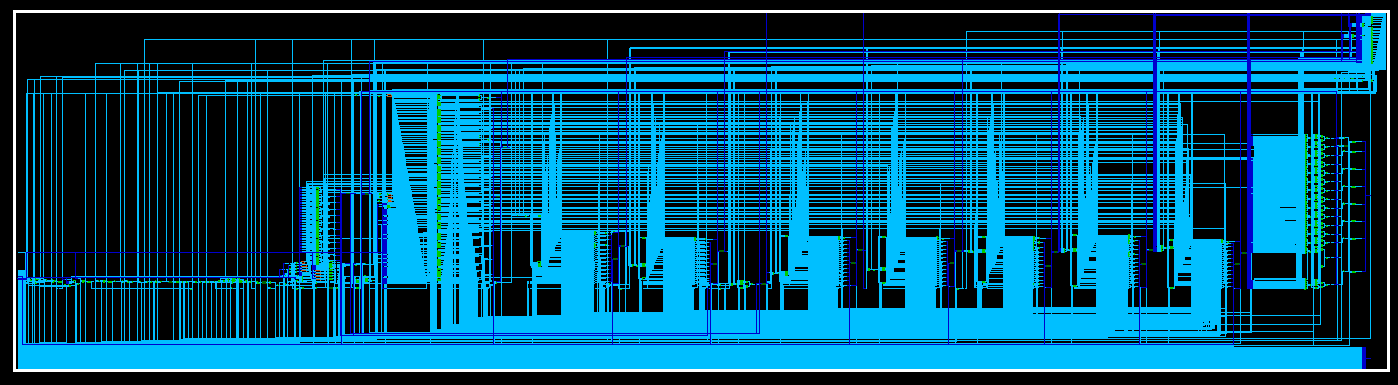


Figure 2 Top Level Area Demonstration

# Timing analysis

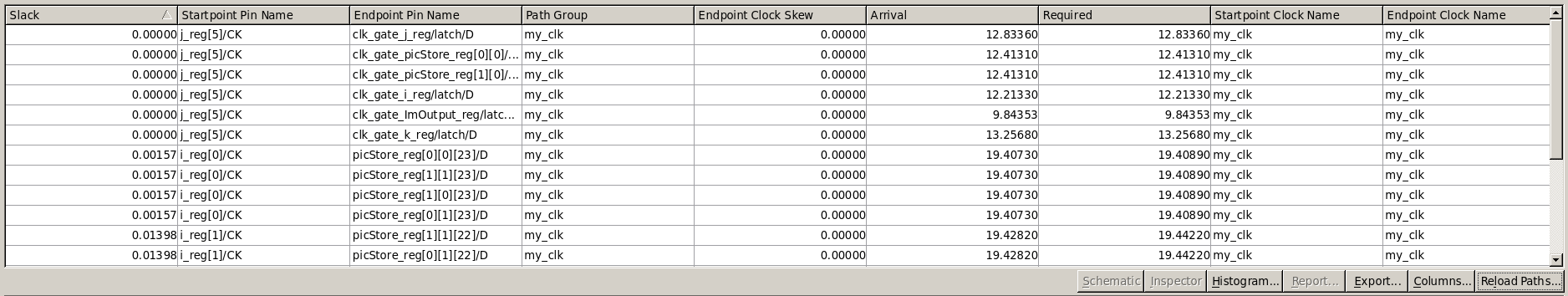


Figure 3 Timing Report

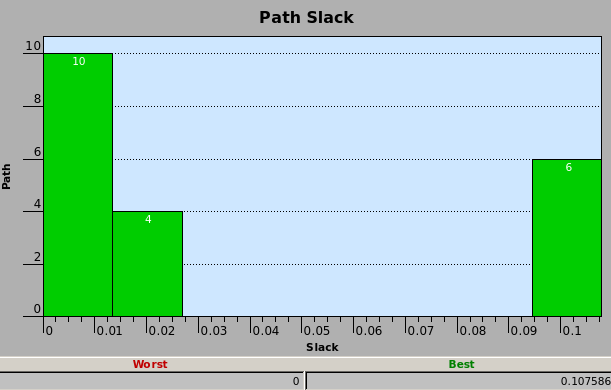


Figure 4 Bar Graph Analysis

Longest Path

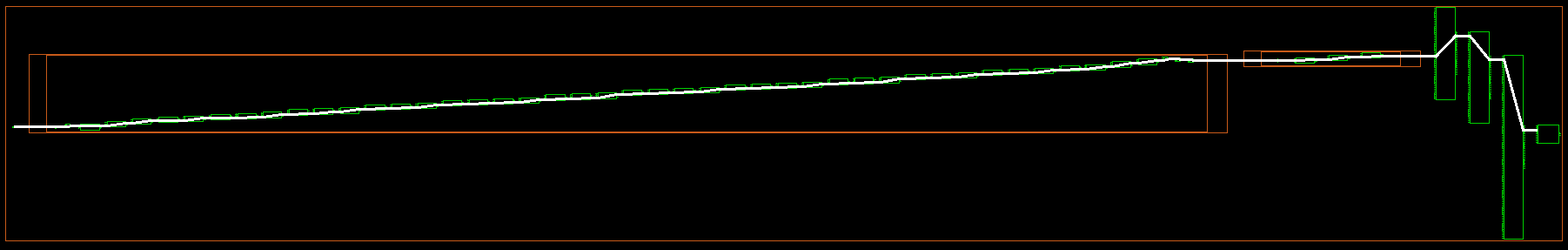


Figure 5 Longest Path



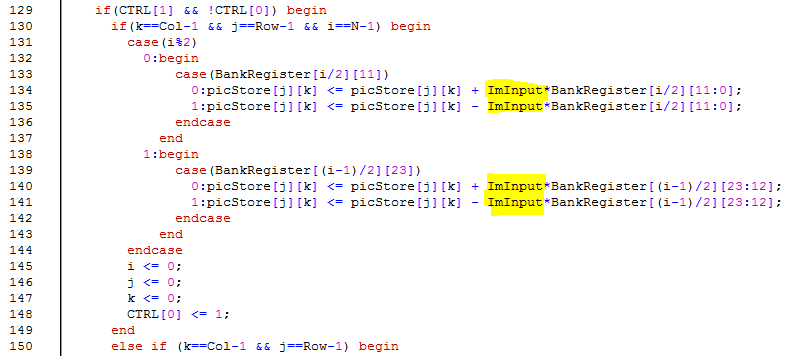
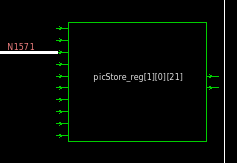


Figure 6+7 Top: Start of Longest Path, Bottom: RTL code of that path



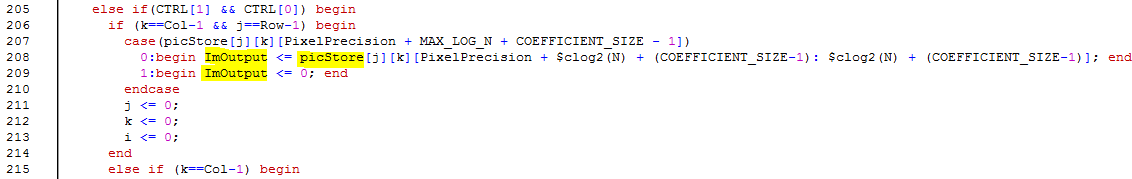


Figure 8+9 Top: End of Longest Path, Bottom: RTL code of that path

Note that with Clock Gating longest path changes and becomes a clock path.

* library setup time -0.19

# Power refinement

|  |  |
| --- | --- |
| **without the SAIF input file and without gated clock** | **with the SAIF input file and without gated clock** |
| Cell Internal Power = 1.2281 mW (59%)  Net Switching Power = 848.2385 uW (41%)  ---------  Total Dynamic Power = 2.0764 mW (100%)  Cell Leakage Power = 6.9955 uW | Cell Internal Power = 1.2470 mW (82%)  Net Switching Power = 282.9717 uW (18%)  ---------  Total Dynamic Power = 1.5300 mW (100%)  Cell Leakage Power = 4.3459 uW |
| **without the SAIF input file and with clock gating** | **with the SAIF input file with clock gating** |
| Cell Internal Power = 63.5619 uW (24%)  Net Switching Power = 201.7793 uW (76%)  ---------  Total Dynamic Power = 265.3412 uW (100%)  Cell Leakage Power = 4.8844 uW | Cell Internal Power = 195.3765 uW (28%)  Net Switching Power = 490.7158 uW (72%)  ---------  Total Dynamic Power = 686.0923 uW (100%)  Cell Leakage Power = 3.7102 uW |

Explanation: Clock gating obviously saves a lot of power as it saves toggle operations of timely unused FFs. The SAIF file tells the compiler real runtime example and given it is a decent run the results should and do improve. Oddly, using both of them combined shows a little less good result than each separately but it's still a lot better than running with neither.

# Gate level simulation

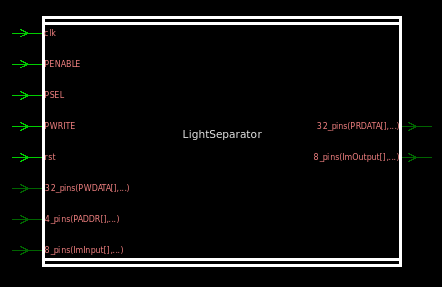


Figure 10 Gate Level Top View

## Input to simulator

Initial Errors were caused mainly due to unit naming differences. After we passed that, Gate Level ran but produced unexpected waves. That was solved firstly by using a clock that is closer to the one we stated in our constraints file (original testbench clock changed every 1 ns). But that wasn't enough, in our initial testbench we set up values that were samples precisely on rising edge of the clock. Obviously Gate Level delays caused sampling unwanted values. We therefor changed giving values at falling edge giving the unit 50% value uptime to sample it. After that change we got identical values in the RTL and GLV simulations.

## Waveform Comparison

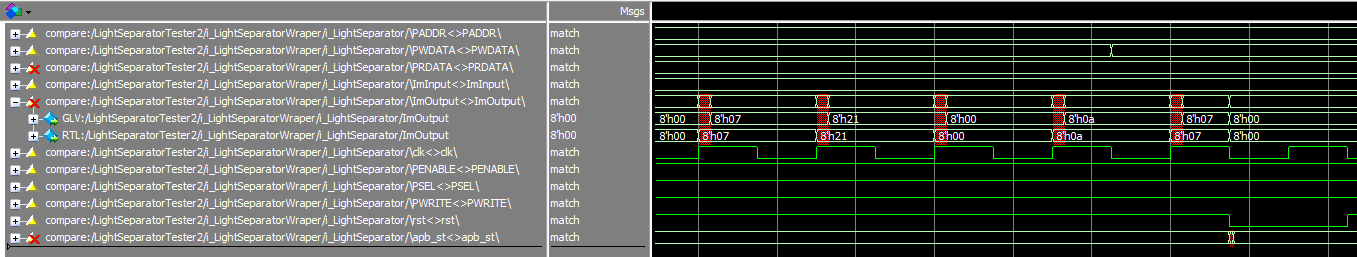


Figure 11 Wavform Comparison

We can see that the output is identical in both wavforms with delay in the GLV wave that is the result of simulating real delays.

# Comparison to the **Golden** Model

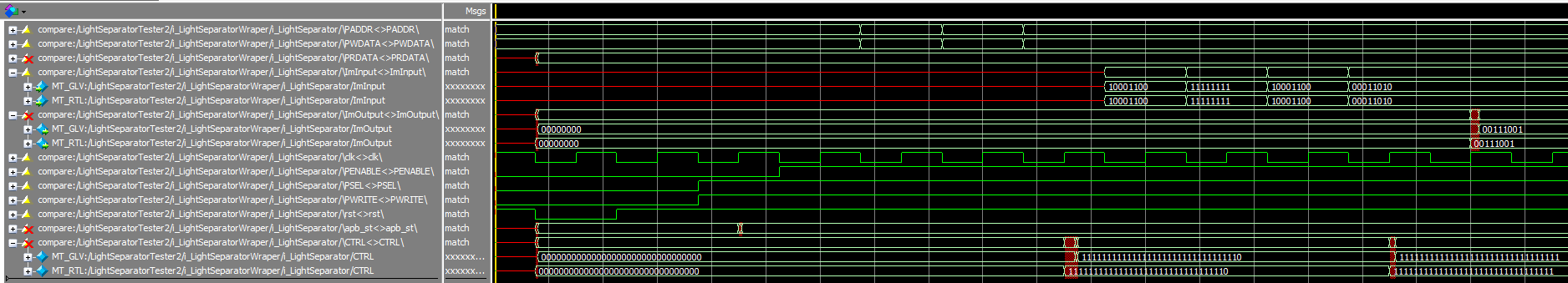


Figure 12 Comparison to the Golden Model

As shown Comparison between GLV and RTL of Golden Model input is similar to the previous comparison as the operation of the unit is identical for both models with delay in the GLV model.

# Ignored Policy Rules

1. FSM does not have a default handling for transitions. – Unexpected behavior for non '0' or '1' values
2. Net 'BankRegisterDebug[15:0]' is unused. – These wires were added for debug purpose and thus aren't used
3. Case item statement is not reachable. – Line 139, unclear why we receive this error when this statement is provably reached.   
   Case statement does not have a 'default' branch. – The explanation is the same as 1.  
   Case statement is not full. – The error is about a repeating line starting at line 195. It is a modulo 2 statement and thus '0' and '1' cases should cover the case in full.