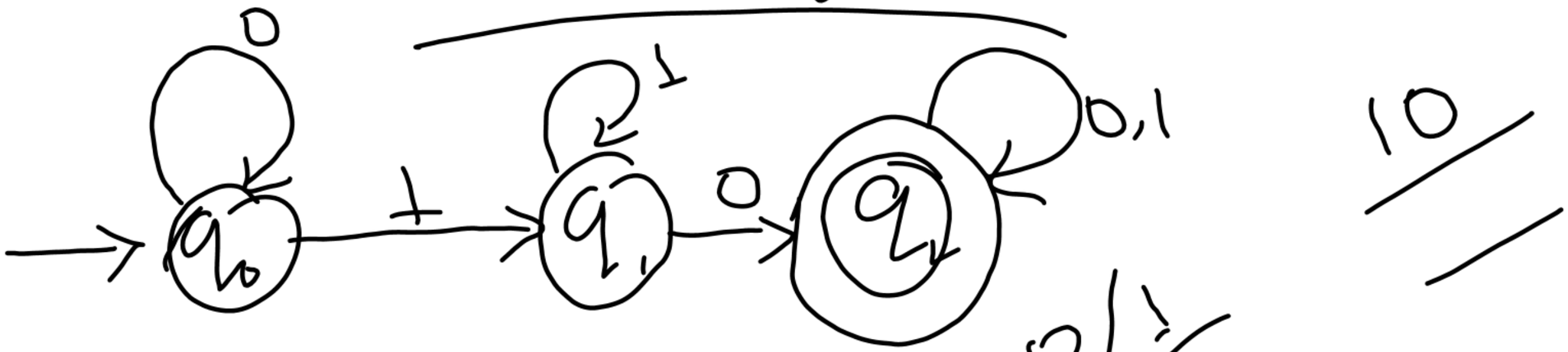
State Diagram



0^*

$0^* 1 \rightarrow q_1 \rightarrow 1$

$1\,1$

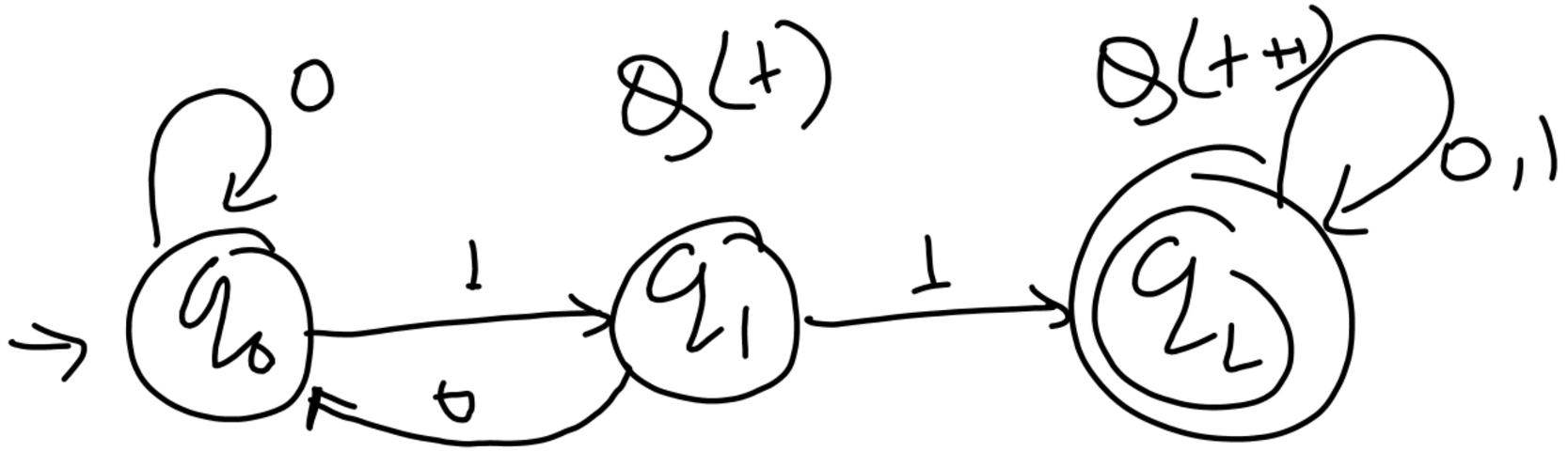
$0\,1^*$

$q_2 \rightarrow 1\,0$

$0 \rightarrow$

10

11



$q_0 \rightarrow 0 \;.\; 1$

q_1

$q_1 \rightarrow 10 \;.\; 0$

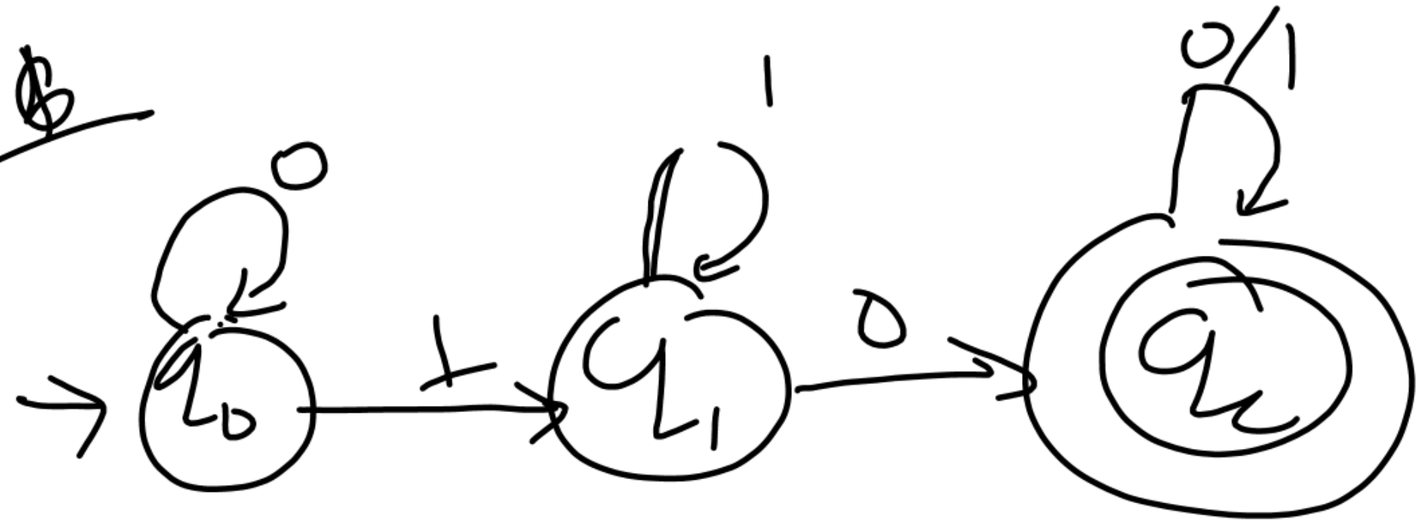
101

$q_1 \rightarrow 10 \rightarrow q_0$

$101 \rightarrow q_1$

1011

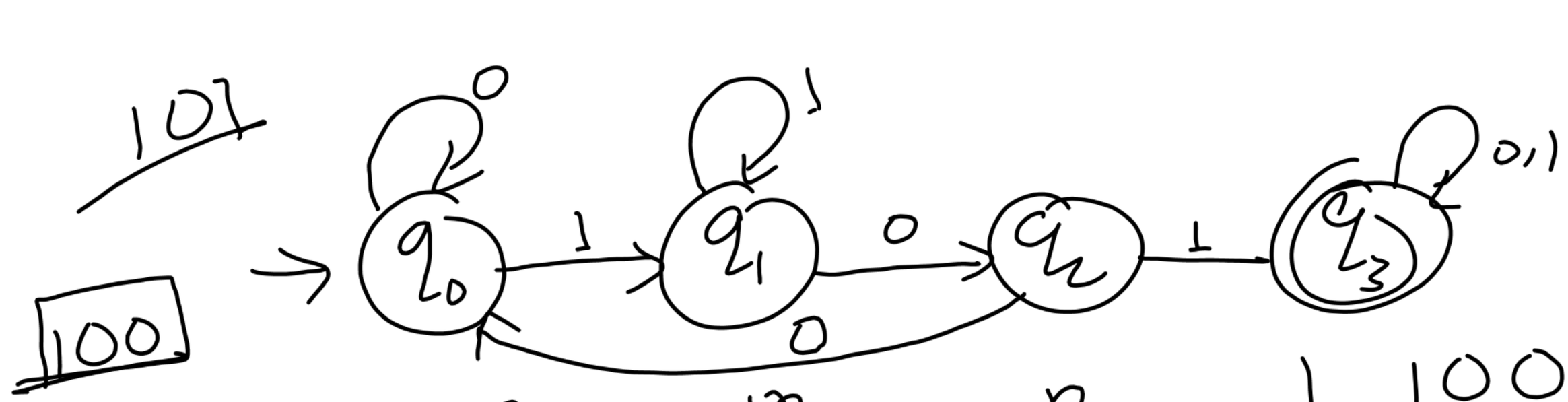
10$



1 $q_1 \rightarrow 0/1$

10

11-0



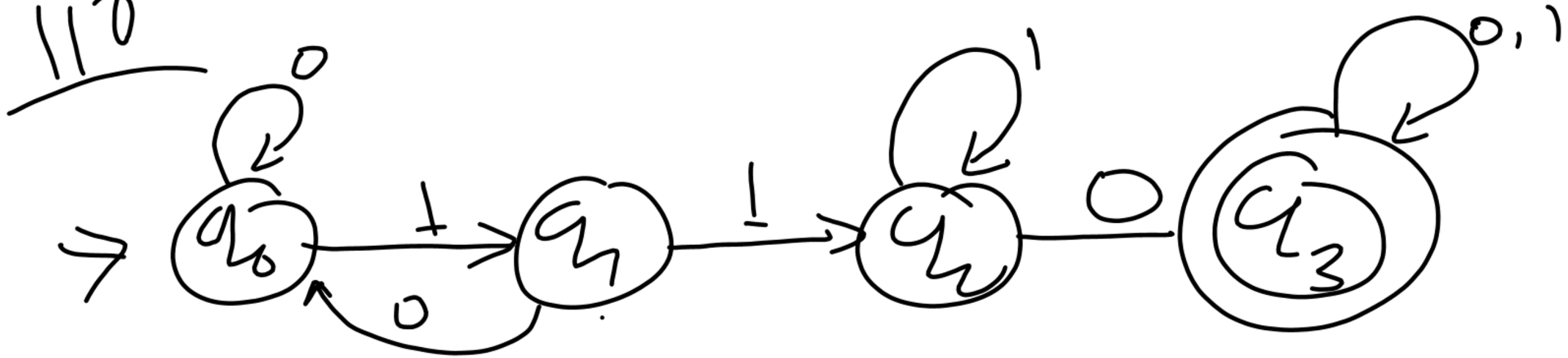
101

01

c	in	n
q_0	—	0/1	q_1
q_1	1	0	q_2 (10)
q_2	10	1	q_3
		0	q_0
		1	q_3

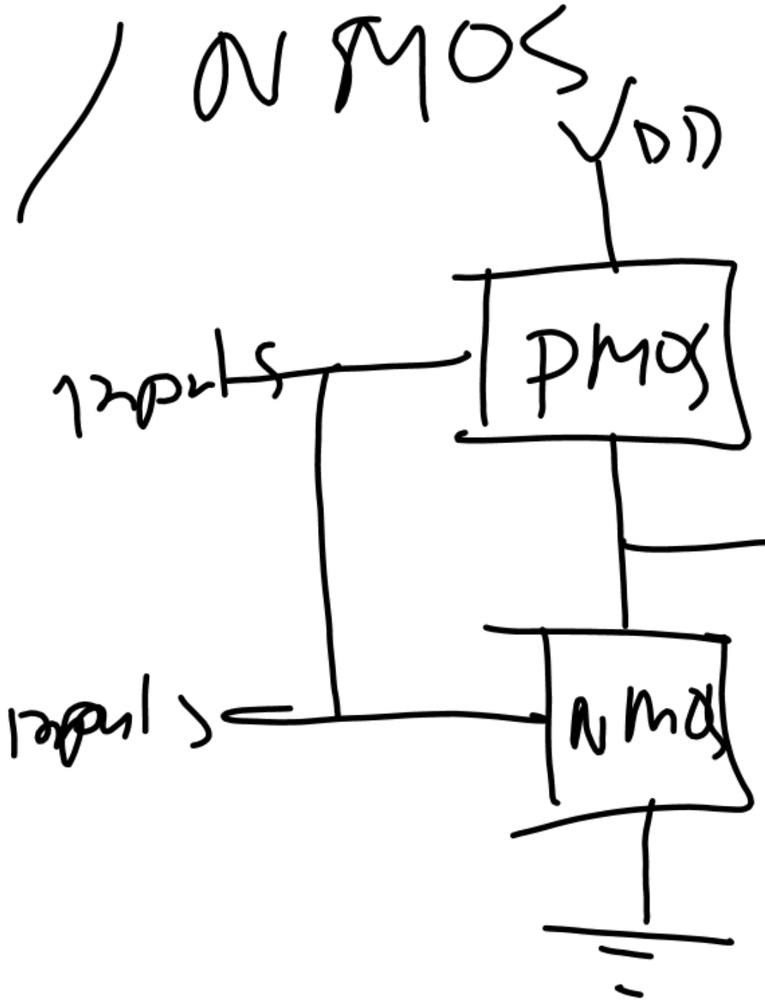
100 → q_0

110

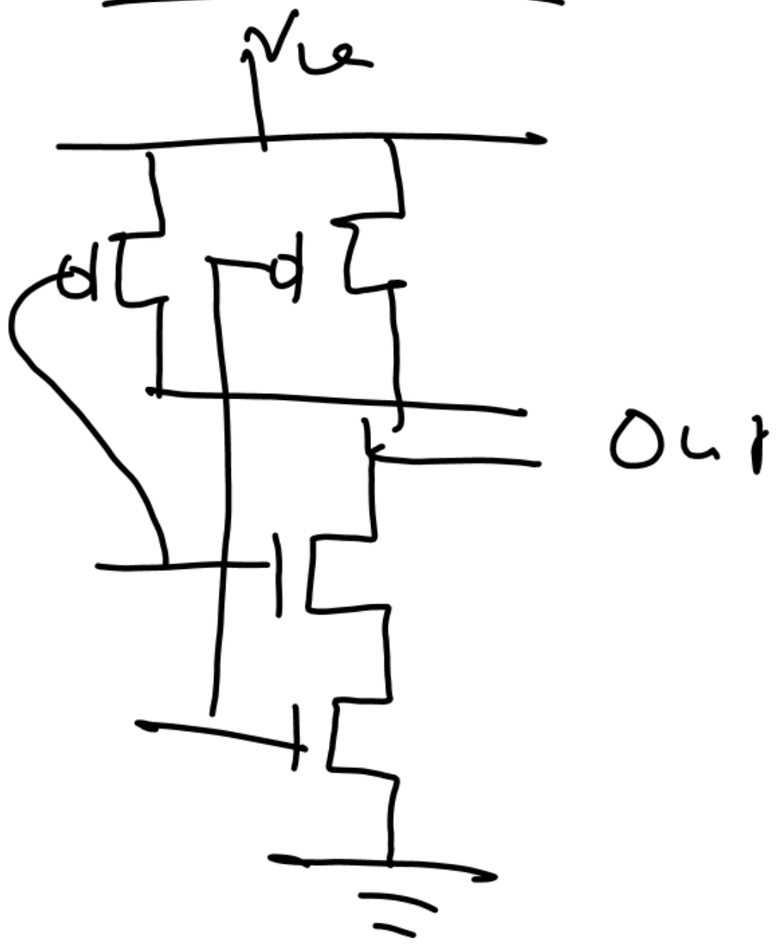


$q_0 \to 0 \to q_0 \to 1 \to q_1 \to 0 \to q_0$

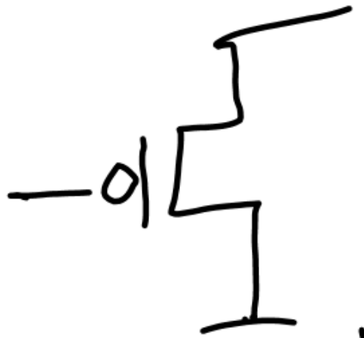
PMOS / NMOS



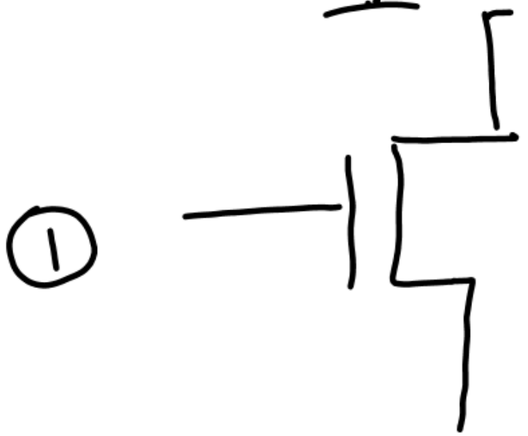
CMOS



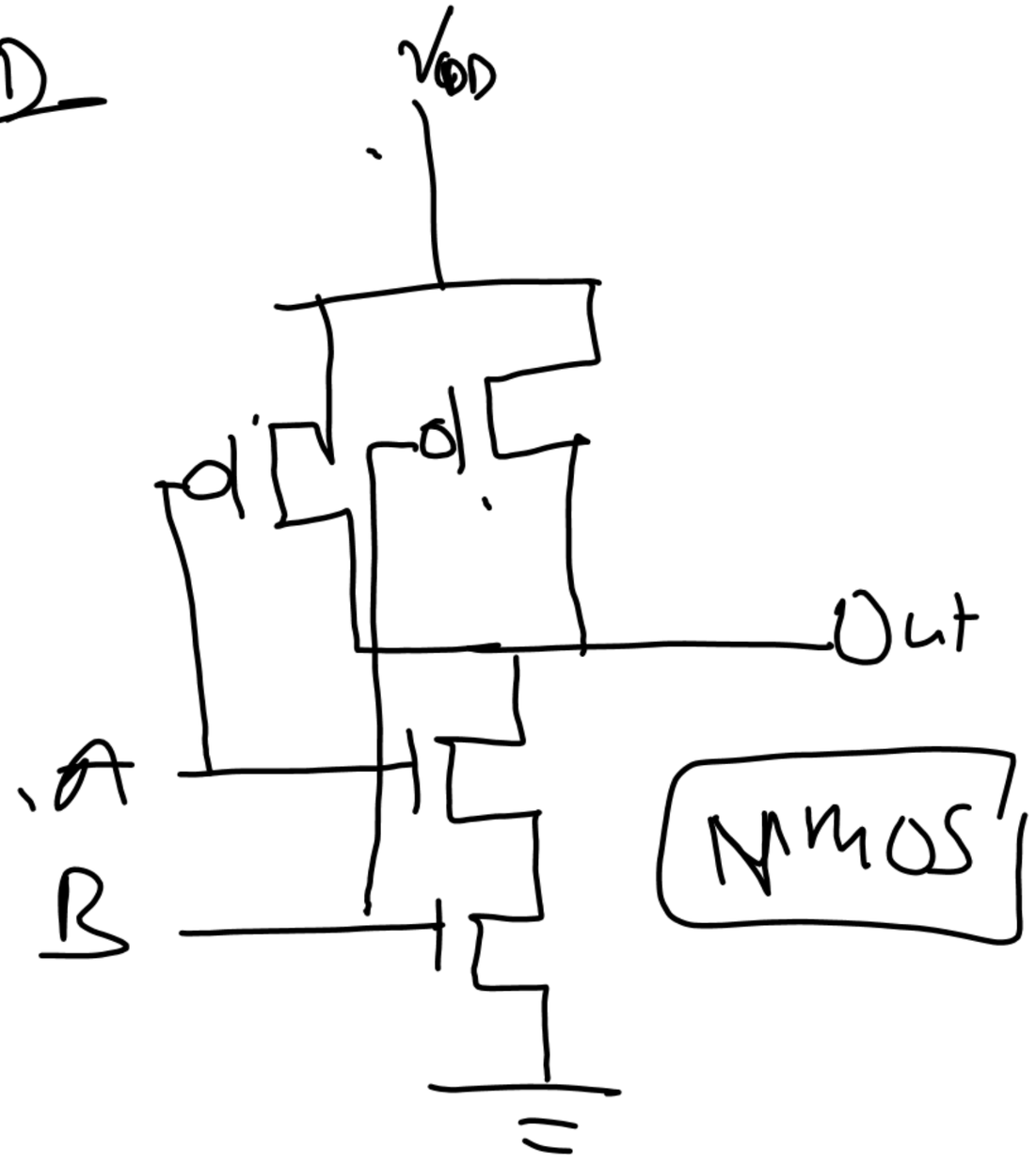
PMOS



NMOS

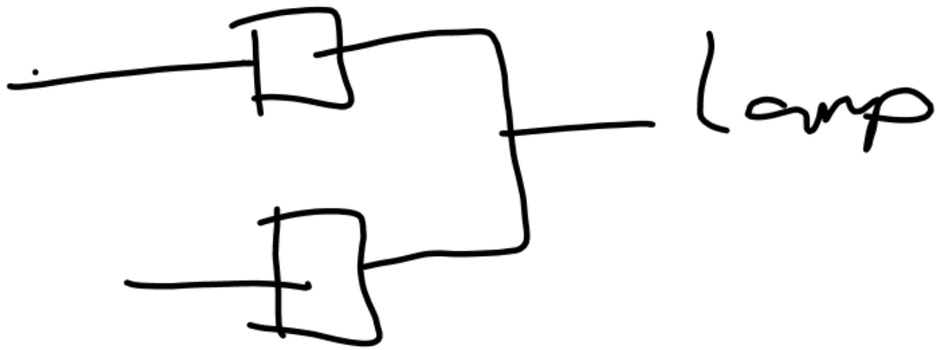


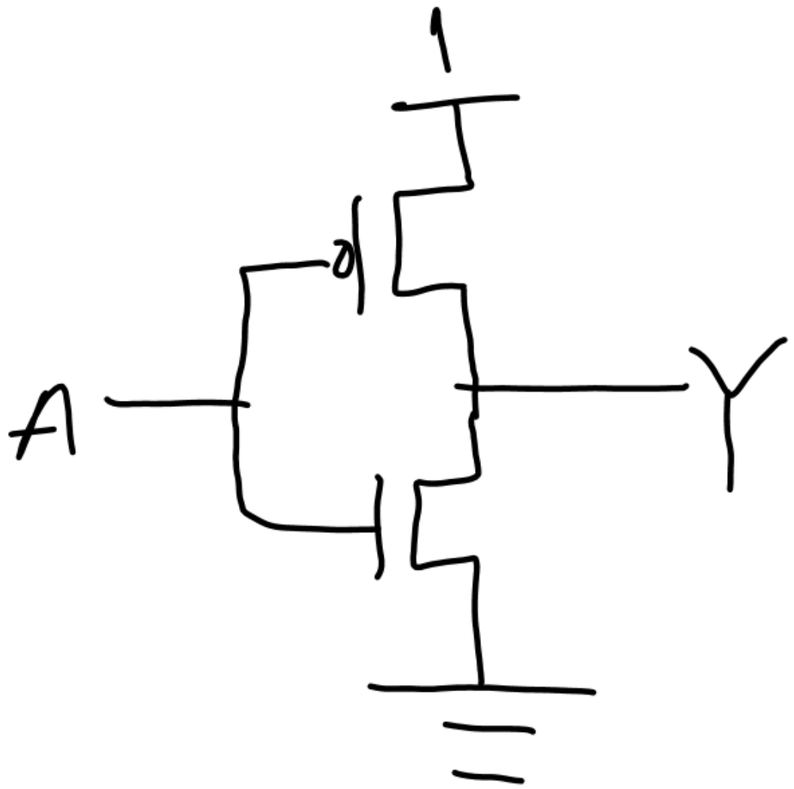
NAND



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0


Lamp


lamp



A	Y
0	1
1	0

PMOS

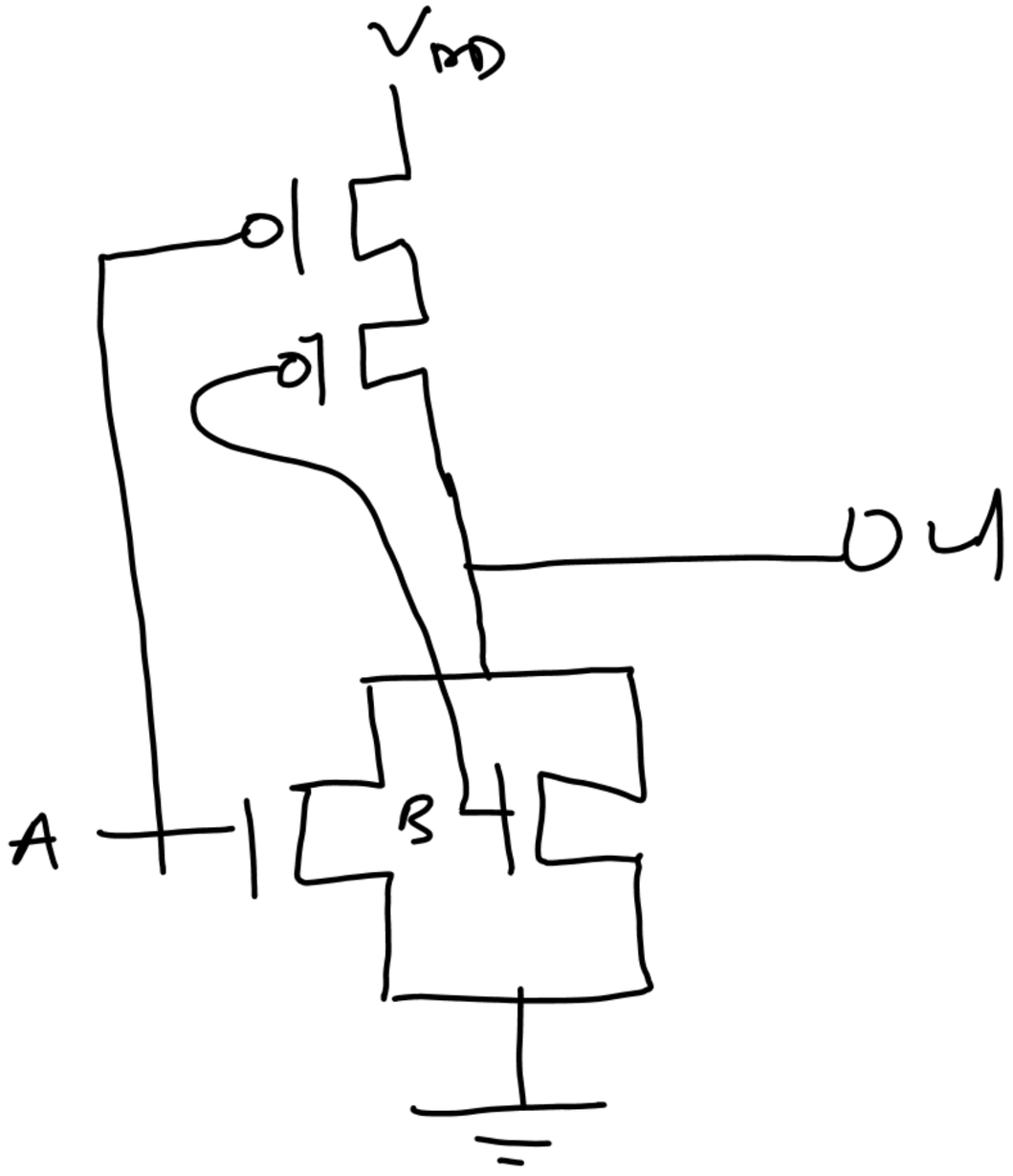
input → 0

output → 1 (V_{DD})

NMOS

input → 1

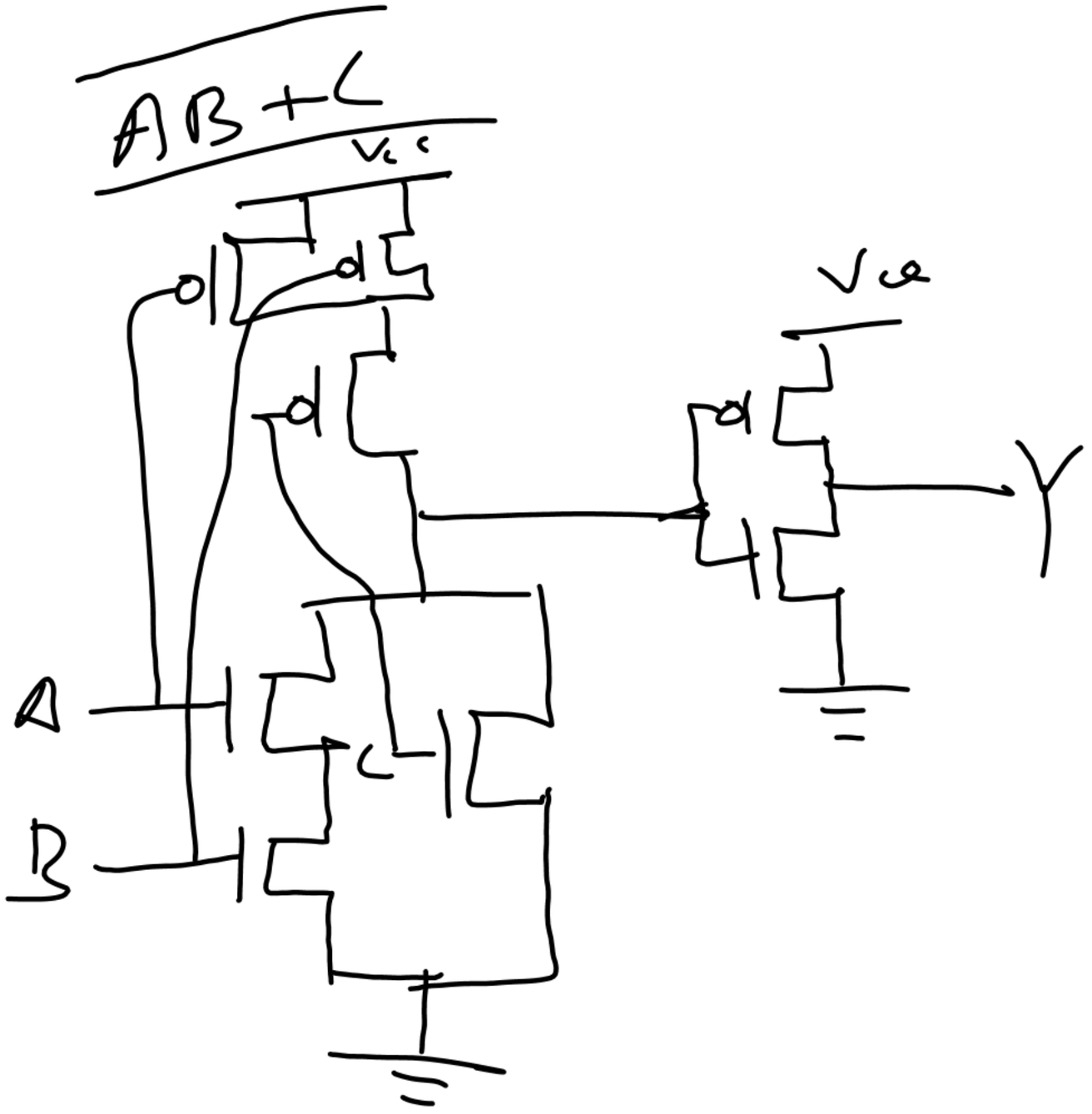
output → 0 (GND)



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

A+B

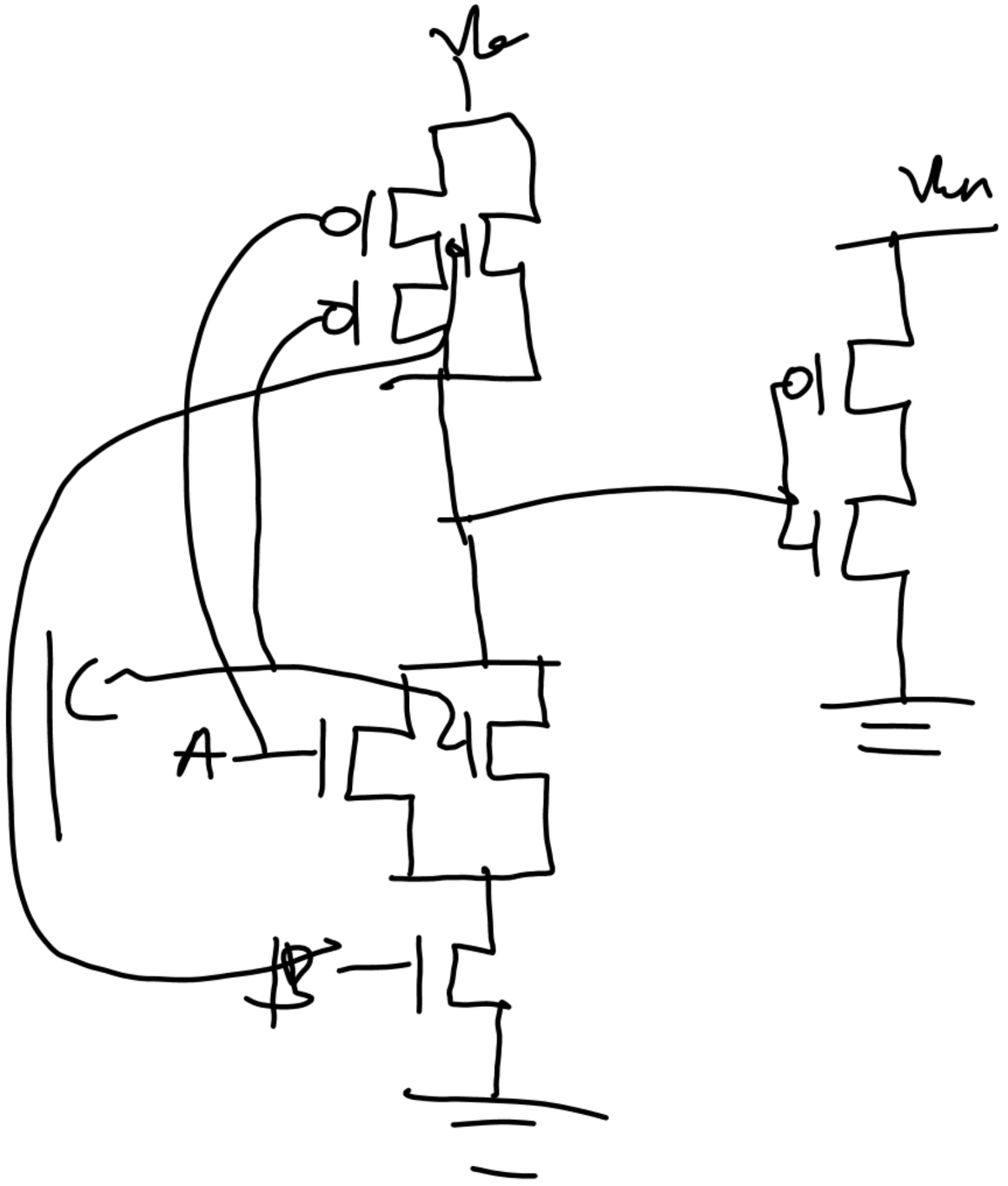
AB+C



A	B	
0	0	0 1
0	1	0 1
1	0	0 1
1	1	1 0

$AB + BC$

$B(A + C)$



$\overline{AB}$