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Parity Generator and Parity Check

April 5, 2021 By [Ravi Teja\(https://www.electronicshub.org/author/raviteja/\)](https://www.electronicshub.org/author/raviteja/)

Majority of modern communication is Digital in nature i.e., it is a combination of 1's and 0's. The digital data is transmitted either through wires (in case of wired communication) or wireless. Even in an advanced mode of communication, there will be errors while transmitting data (due to noise).

The simplest of errors is corruption of a bit i.e., a 1 may be transmitted as a 0 or vice-versa. To confirm whether the received data is the intended data or not, we should be able to detect errors at the receiver.

In this tutorial, we will learn about Parity Bit, Even Parity, Odd Parity, Parity Generator and Parity Checker with a practical example and practical circuit.

Outline



What is Parity Bit?

The parity generating technique is one of the most widely used error detection techniques for the data transmission. In digital systems, when binary data is transmitted and processed, data may be subjected to noise so that such noise can alter 0s (of data bits) to 1s and 1s to 0s.

Hence, a Parity Bit is added to the word containing data in order to make number of 1s either even or odd. The message containing the data bits along with parity bit is transmitted from transmitter to the receiver.

At the receiving end, the number of 1s in the message is counted and if it doesn't match with the transmitted one, it means there is an error in the data. Thus, the Parity Bit is used to detect errors, during the transmission of binary data.

Parity Generator and Checker

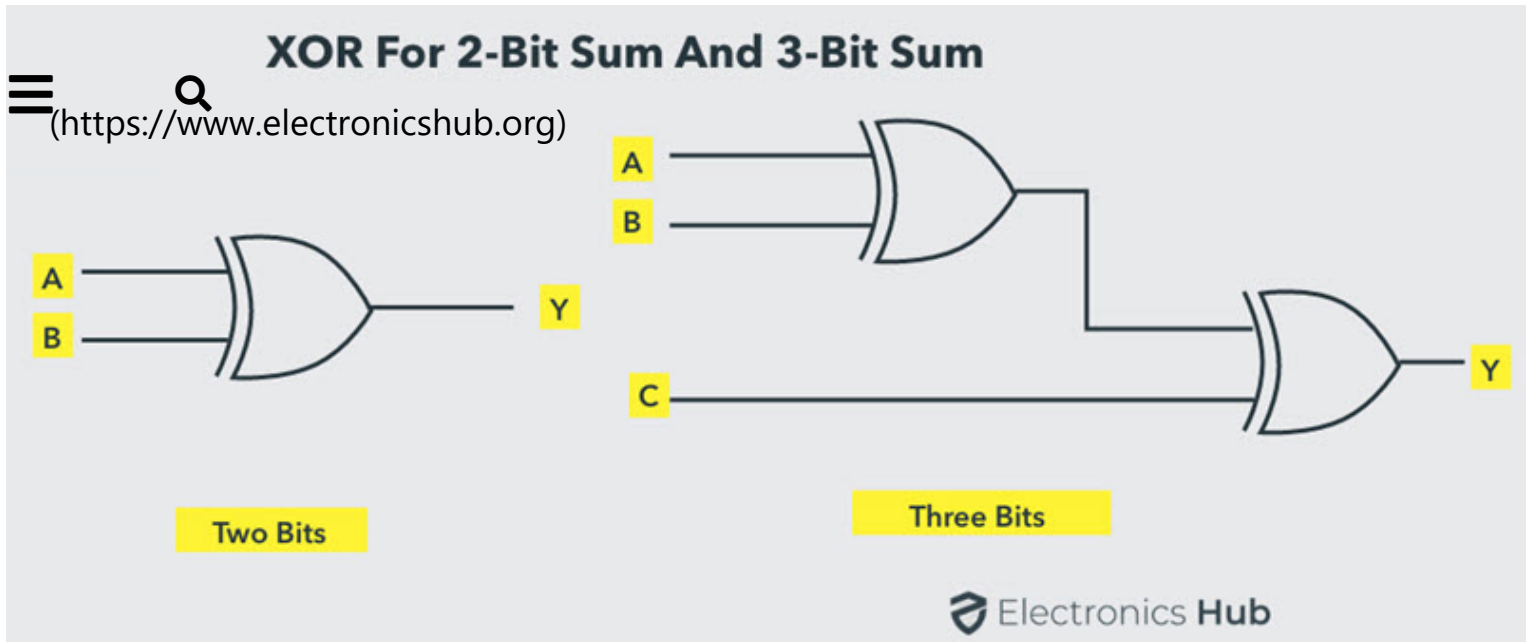
A Parity Generator is a combinational logic circuit that generates the parity bit in the transmitter. On the other hand, a circuit that checks the parity in the receiver is called Parity Checker. A combined circuit or device of parity generators and parity checkers are commonly used in digital systems to detect the single bit errors in the transmitted data.

Even Parity and Odd Parity

The sum of the data bits and parity bits can be even or odd. In even parity, the added parity bit will make the total number of 1s an even number, whereas in odd parity, the added parity bit will make the total number of 1s an odd number.

The basic principle involved in the implementation of parity circuits is that sum of odd number of 1s is always 1 and sum of even number of 1s is always 0. Such error detecting and correction can be implemented by using Ex-OR gates (since Ex-OR gate produce zero output when there are even number of inputs).

To produce two bits sum, one Ex-OR gate is sufficient whereas for adding three bits, two Ex-OR gates are required as shown in below figure.



(<https://www.electronicshub.org/wp-content/uploads/2021/04/XOR-Gate-for-2-bit-and-3-bit-Sum.jpg>)

Parity Generator

It is combinational circuit that accepts an $n-1$ bit data and generates the additional bit that is to be transmitted with the bit stream. This additional or extra bit is called as a Parity Bit.

In even parity bit scheme, the parity bit is '0' if there are even number of 1s in the data stream and the parity bit is '1' if there are odd number of 1s in the data stream.

In odd parity bit scheme, the parity bit is '1' if there are even number of 1s in the data stream and the parity bit is '0' if there are odd number of 1s in the data stream. Let us discuss both even and odd parity generators.

Even Parity Generator

Let us assume that a 3-bit message is to be transmitted with an even parity bit. Let the three inputs A, B and C are applied to the circuit and output bit is the parity bit P. The total number of 1s must be even, to generate the even parity bit P.

The figure below shows the truth table of even parity generator in which 1 is placed as parity bit in order to make all 1s as even when the number of 1s in the truth table is odd.
(<https://www.electronicshub.org>)

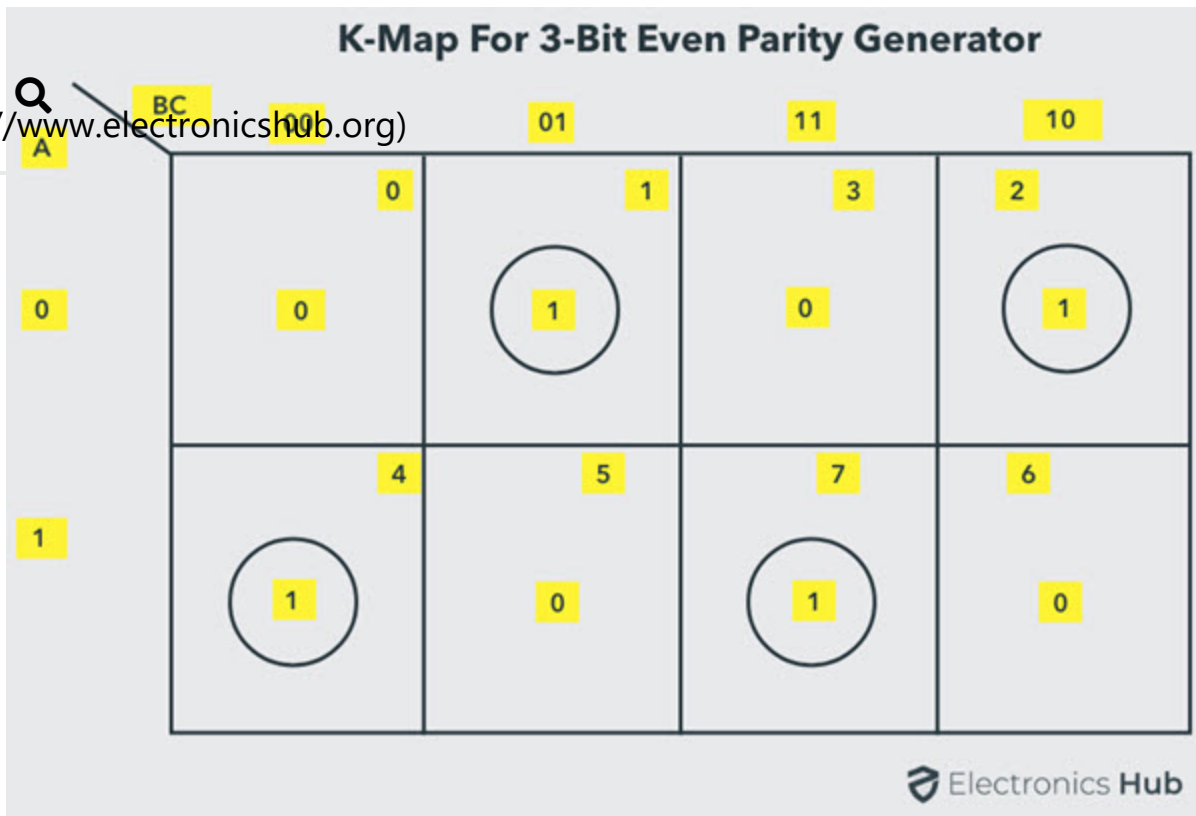
3-bit message			Even parity bit generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(<https://www.electronicshub.org/wp-content/uploads/2015/07/Even-Parity-Generator-Truth-Table.jpg>)

The K-map simplification for 3-bit message even parity generator is



(<https://www.electronicshub.org>)



(<https://www.electronicshub.org/wp-content/uploads/2021/04/K-Map-for-3-bit-Even-Parity-Generator.jpg>)

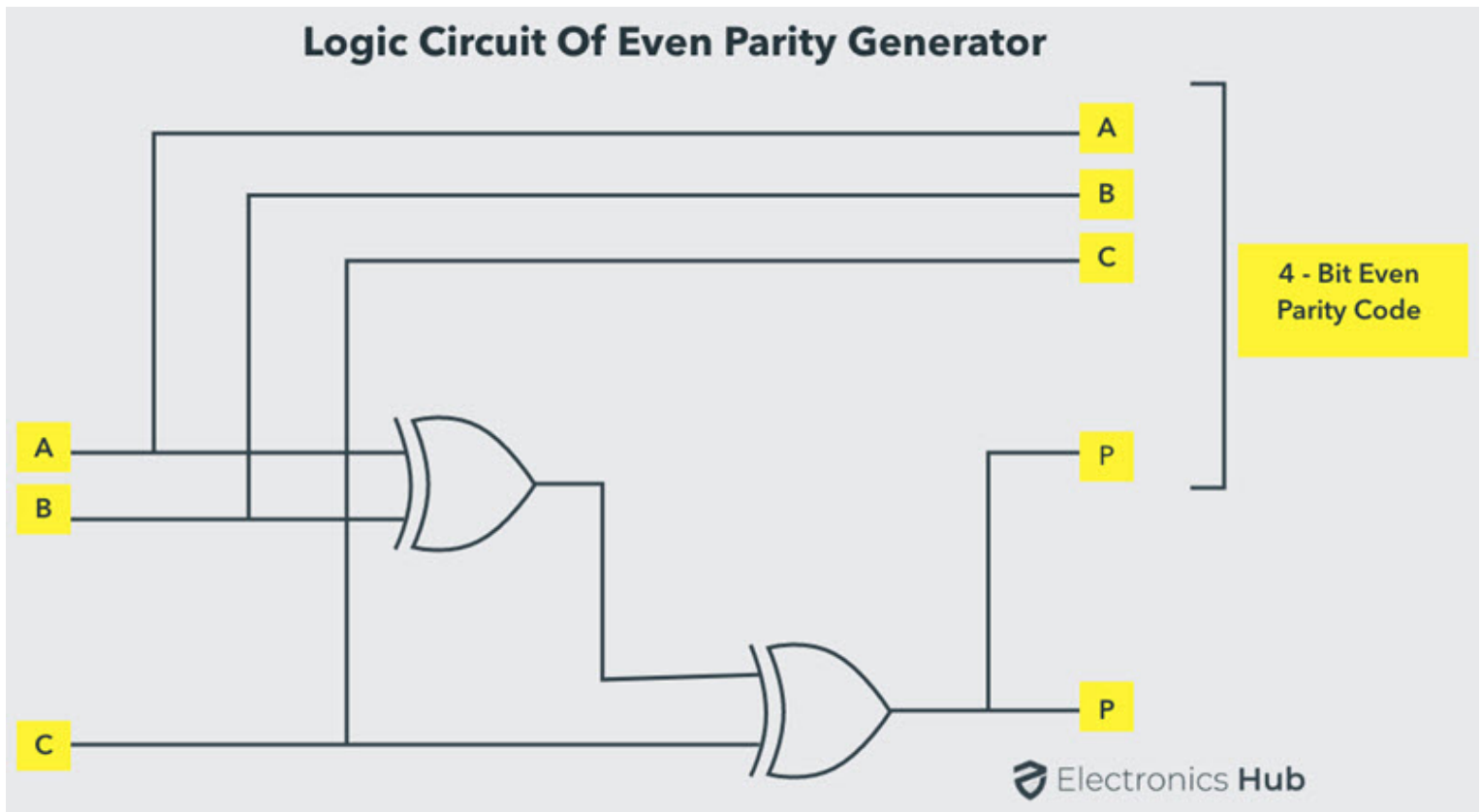
From the above truth table, the simplified expression of the parity bit can be written as

$$\begin{aligned}
 P &= \bar{A} \bar{B} C + \bar{A} B \bar{C} + A \bar{B} \bar{C} + A B C \\
 &= \bar{A} (\bar{B} C + B \bar{C}) + A (\bar{B} \bar{C} + B C) \\
 &= \bar{A} (B \oplus C) + A (\overline{B \oplus C}) \\
 P &= A \oplus B \oplus C
 \end{aligned}$$

(<https://www.electronicshub.org/wp-content/uploads/2015/07/even-parity-generator-exp.jpg>)

The above expression can be implemented by using two Ex-OR gates. The logic diagram of even parity generator with two Ex – OR gates is shown below. The three bit message along with the parity generated by this circuit which is transmitted to the receiving end where parity checker circuit checks whether any error is present or not.

To generate the even parity bit for a 4-bit data, three Ex-OR gates are required to add the 4-bits and their sum will be the parity bit.
(<https://www.electronicshub.org>)



(<https://www.electronicshub.org/wp-content/uploads/2021/04/Logic-Circuit-of-Even-Parity-Generator.jpg>)

Odd Parity Generator

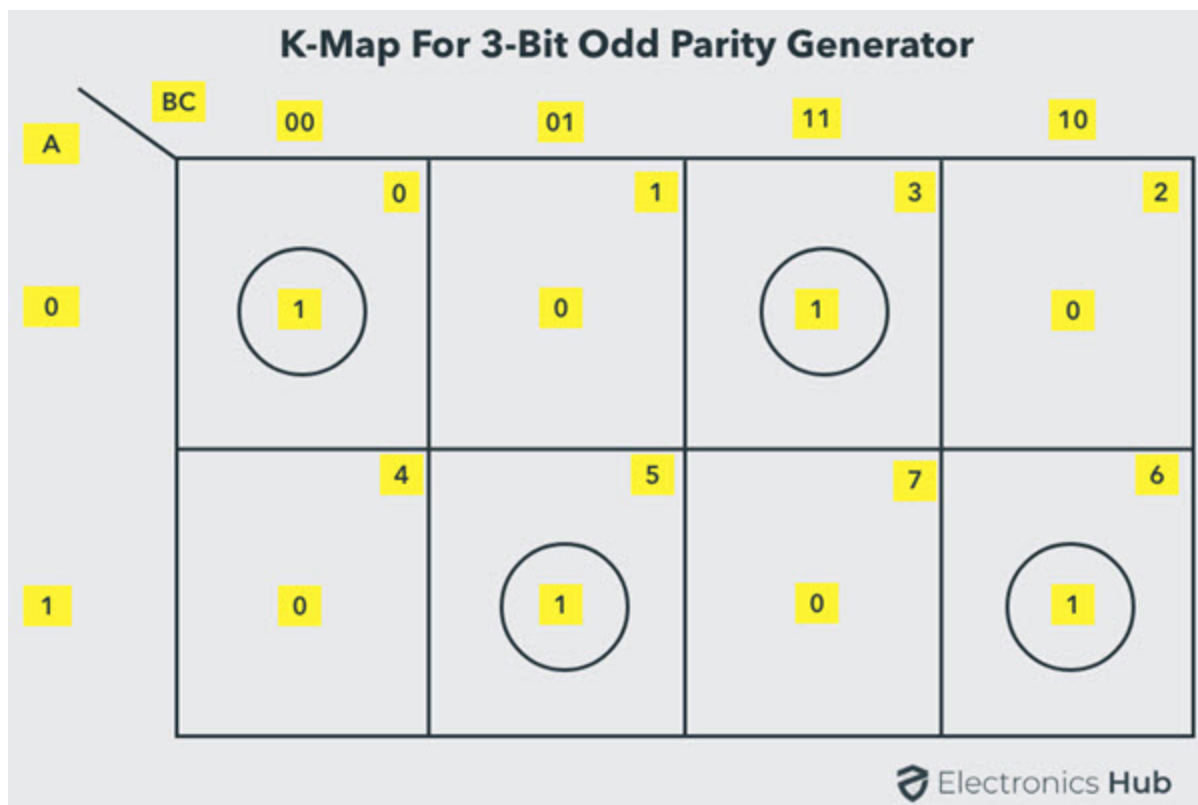
Let us consider that the 3-bit data is to be transmitted with an odd parity bit. The three inputs are A, B and C and P is the output parity bit. The total number of bits must be odd in order to generate the odd parity bit.

In the given truth table below, 1 is placed in the parity bit in order to make the total number of bits odd when the total number of 1s in the truth table is even.

3-bit message			Odd parity bit generator (P)
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

(<https://www.electronicshub.org/wp-content/uploads/2015/07/Odd-Parity-Generator-Truth-Table.jpg>)

The truth table of the odd parity generator can be simplified by using K-map as



(<https://www.electronicshub.org/wp-content/uploads/2021/04/K-Map-for-3-bit-Odd-Parity-Generator.jpg>)

The output parity bit expression for this generator circuit is obtained as

 
(<https://www.electronicshub.org>)

$$P = A \oplus (B \oplus \overline{C})$$

The above Boolean expression can be implemented by using one Ex-OR gate and one Ex-NOR gate in order to design a 3-bit odd parity generator.

The logic circuit of this generator is shown in below figure, in which two inputs are applied at one Ex-OR gate, and this Ex-OR output and third input is applied to the Ex-NOR gate, to produce the odd parity bit. It is also possible to design this circuit by using two Ex-OR gates and one NOT gate.

(<https://www.electronicshub.org/wp-content/uploads/2021/04/Logic-Circuit-of-Odd-Parity-Generator.jpg>)

Parity Check

It is a logic circuit that checks for possible errors in the transmission. This circuit can be an even parity checker or odd parity checker depending on the type of parity generated at the transmission end. When this circuit is used as even parity checker, the number of input bits must always be even.

Even Parity Checker



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Consider that three input message along with even parity bit is generated at the transmitting end. These 4 bits are applied as input to the parity checker circuit, which checks the possibility of error on the data. Since the data is transmitted with even parity, four bits received at circuit must have an even number of 1s.

If any error occurs, the received message consists of odd number of 1s. The output of the parity checker is denoted by PEC (Parity Error Check).

The below table shows the truth table for the Even Parity Checker in which $PEC = 1$ if the error occurs, i.e., the four bits received have odd number of 1s and $PEC = 0$ if no error occurs, i.e., if the 4-bit message has even number of 1s.

(<https://www.electronicshub.org/wp-content/uploads/2015/07/Even-Parity-Checker-Truth-Table.jpg>)

The above truth table can be simplified using K-map as shown below.



(<https://www.electronicshub.org>)

(<https://www.electronicshub.org/wp-content/uploads/2021/04/K-Map-for-3-bit-Even-Parity-Checker.jpg>)

(<https://www.electronicshub.org/wp-content/uploads/2015/07/Even-Parity-Checker-Boolean.jpg>)

The above logic expression for the even parity checker can be implemented by using three Ex-OR gates as shown in figure. If the received message consists of five bits, then one more Ex-OR gate is required for the even parity checking.

<https://www.electronicshub.org/wp-content/uploads/2021/04/Logic-Circuit-of-Even-Parity-Checker.jpg>

Odd Parity Checker

Consider that a three bit message along with odd parity bit is transmitted at the transmitting end. Odd parity checker circuit receives these 4 bits and checks whether any error are present in the data.

If the total number of 1s in the data is odd, then it indicates no error, whereas if the total number of 1s is even then it indicates the error since the data is transmitted with odd parity at transmitting end.

The below figure shows the truth table for odd parity generator where PEC = 1 if the 4-bit message received consists of even number of 1s (hence the error occurred) and PEC = 0 if the message contains odd number of 1s (that means no error).

(<https://www.electronicshub.org/wp-content/uploads/2015/07/Odd-Parity-Checker-Truth-Table.jpg>)

The expression for the PEC in the above truth table can be simplified by K-map as shown below.

(<https://www.electronicshub.org/wp-content/uploads/2021/04/K-Map-for-3-bit-Odd-Parity-Checker.jpg>)

After simplification, the final expression for the PEC is obtained as

$$PEC = (A \text{ Ex-NOR } B) \text{ Ex-NOR } (C \text{ Ex-NOR } P)$$

The expression for the odd parity checker can be designed by using three Ex-NOR gates as shown below.

<https://www.electronicshub.org/wp-content/uploads/2021/04/Logic-Circuit-of-Odd-Parity-Checker.jpg>

Parity Generator/Checker ICs

There are different types of parity generator /checker ICs are available with different input configurations such as 5-bit, 4-bit, 9-bit, 12-bit, etc. One of the most commonly used and standard type of parity generator/checker IC is 74180.

It is a 9-bit parity generator or checker used to detect errors in high speed data transmission or data retrieval systems. The figure below shows the pin diagram of 74180 IC.

This IC can be used to generate a 9-bit odd or even parity code or it can be used to check for odd or even parity in a 9-bit code (8 data bits and one parity bit).

18 Responses

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Trupalsinh says:

Superb..!!!! All informations are covered....

Reply

aditi says:

awesome...

Reply

(<https://www.electronicshub.org/wp-content/uploads/2021/04/Parity-Generator-Checker-IC-74180.jpg>)

naveen reddy says:

This IC consists of eight parity inputs from A through H and two cascading inputs. There are two outputs even sum and odd sum. In implementing generator or checker circuits, unused parity bits must be tied to logic zero and the cascading inputs must not be equal.

Reply

If this IC is used as an Even Parity Checker and when a parity error occurs, the 'sum even' output goes low and 'sum odd' output goes high. If this IC is used as an Odd Parity Checker, the number of input bits should be odd, but if an error occurs the 'sum odd' output goes low and 'sum even' output goes high.

It is covered all topics. Very help full for me.

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Is exor or exor or both In the odd parity generator. It is confusing with sentence and figure
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tarun says:

tell some important applications

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jui says:

if it is said to design a parity generator to generate an odd parity for four bit word does that mean the parity generator is of 5 bit

Reply

Atul Patare says:

Odd Parity Generator diagram is wrong. Correct itLook at equation and then at Diagram..
And Thanks for the notes. Appreciate.

Reply



jdkks says:
(<https://www.electronicshub.org>)

There is a huge,mistake, The figure for odd parity generator is actually odd parity checker.

Reply

Anjali Rai says:

Thank you superb knowledge shared

Reply

rubina says:

can u post the difference between parity checker and parity generator

Reply

Pratik says:

For 4 bit parity generator which ic is required and it's circuit dig plzz tell me

Reply

Sasi says:

Not bad

Reply



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Anusha says:

Sir plz present proper applications of parity

Reply

pravalika says:

nice explanation

Reply

anonymous says:

For 4 bit parity generator which ic is required ?

Reply

Kushal Basnet says:

Thank you very much

Reply

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