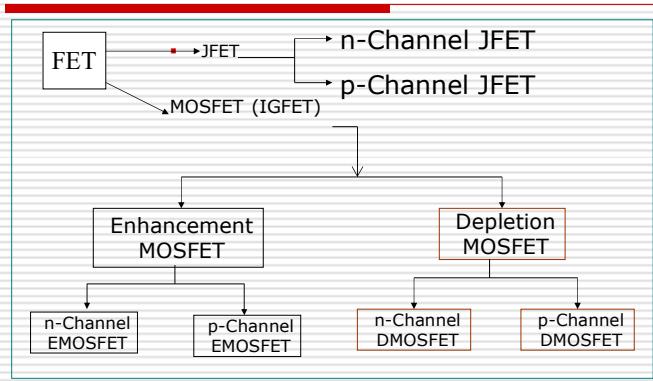


Field Effect Transistor

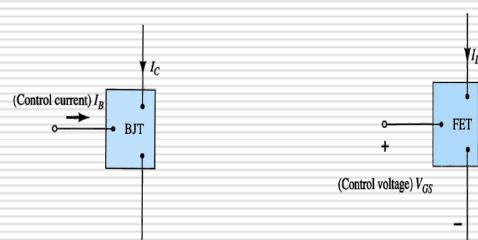
Introduction (FET)

- Field-effect transistor (FET) are important devices such as BJTs
- Also used as amplifier and logic switches
- Types of FET:
 - MOSFET (metal-oxide-semiconductor field-effect transistor)
 - Depletion-mode MOSFET
 - JFET (junction field-effect transistor)
- What is the difference between JFET and MOSFET?

Types of Field Effect Transistors (The Classification)



Output controlling variable

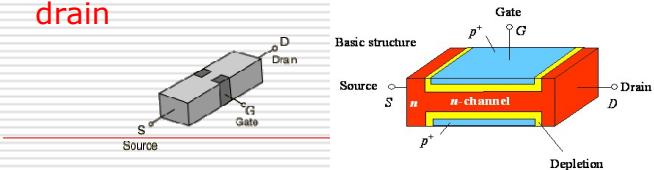


BJT:-Current-controlled device

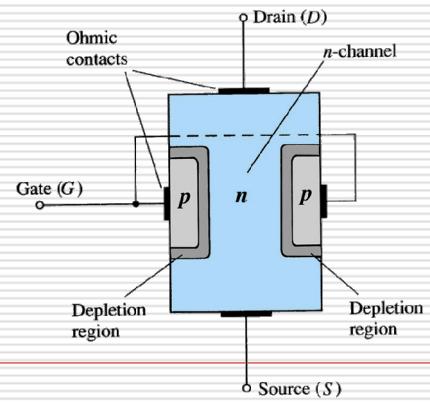
FET -voltage controlled device

Junction FETs (JFETs)

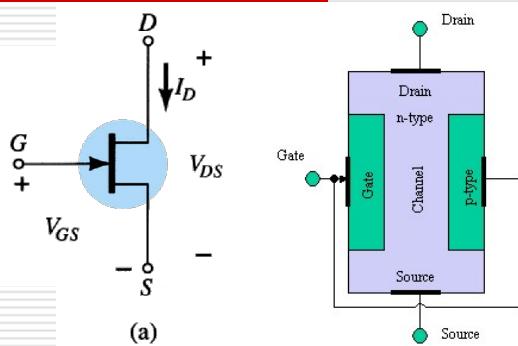
- JFETs consists of a piece of high-resistivity semiconductor material (usually Si) which constitutes a **channel** for the majority carrier flow.
- Conducting semiconductor channel between two ohmic contacts – **source & drain**



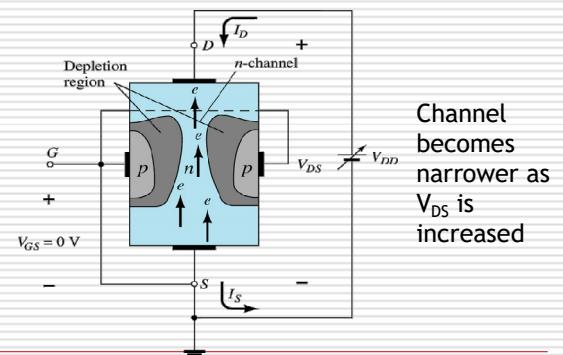
Junction field-effect transistor (JFET)



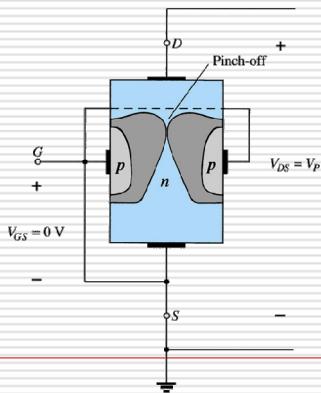
N-channel JFET..



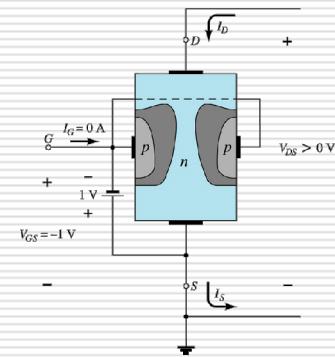
JFET for $V_{GS} = 0 \text{ V}$ and $0 < V_{DS} < |V_p|$



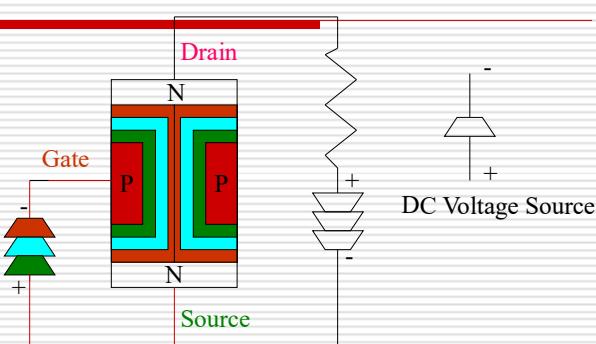
Pinch-off ($V_{GS} = 0 \text{ V}$, $V_{DS} = V_P$).



Application of a negative voltage to the gate of a JFET.



Operation of a JFET



Operation of JFET at Various Gate Bias Potentials

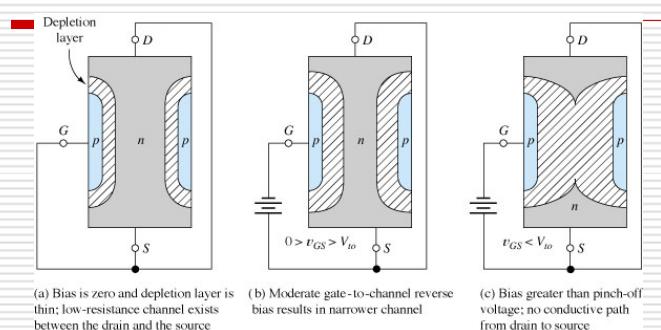
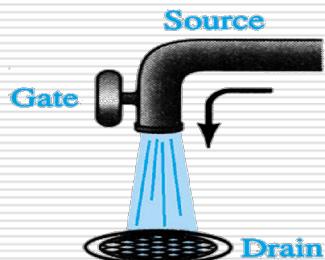
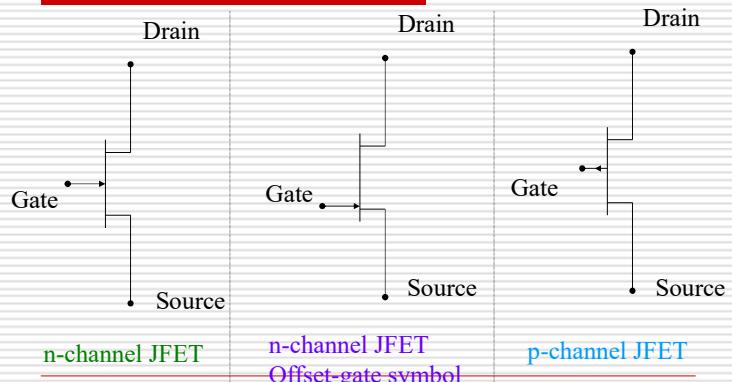


Figure: The nonconductive depletion region becomes broader with increased reverse bias.
(Note: The two gate regions of each FET are connected to each other.)

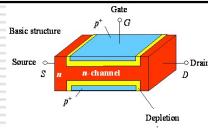
Water analogy for the JFET control mechanism



SYMBOLS



Junction FETs



- ❑ JFET is a high-input resistance device, while the BJT is comparatively low.
- ❑ If the channel is doped with a **donor impurity**, n-type material is formed and the channel current will consist of electrons.
- ❑ If the channel is doped with an **acceptor impurity**, p-type material will be formed and the channel current will consist of holes.
- ❑ N-channel devices have greater conductivity than p-channel types, since electrons have higher mobility than do holes; **thus n-channel JFETs are approximately twice as efficient conductors compared to their p-channel counterparts.**

N-channel JFET

❑ N channel JFET:

- Major structure is **n-type material (channel)** between embedded **p-type material** to form 2 p-n junctions.
- In the normal operation of an n-channel device, the **Drain (D)** is positive with respect to the **Source (S)**. Current flows into the Drain (D), through the channel, and out of the Source (S).
- Because the resistance of the channel depends on the **gate-to-source voltage (V_{GS})**, the **drain current (I_D)** is controlled by that voltage

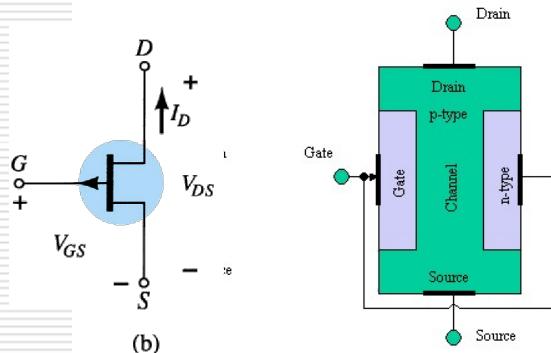
Introduction.. (Advantages of FET)

- High input impedance ($M\Omega$)
(Linear AC amplifier system)
- Temperature stable than BJT
- Smaller than BJT
- Can be fabricated with fewer processing
- BJT is bipolar – conduction both hole and electron
- FET is unipolar – uses only one type of current carrier
- Less noise compare to BJT
- Usually use as logic switch

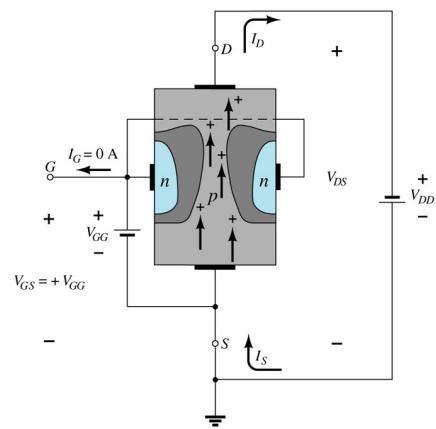
Disadvantages of FET

- Easy to damage compare to BJT
- ???

P-channel JFET..



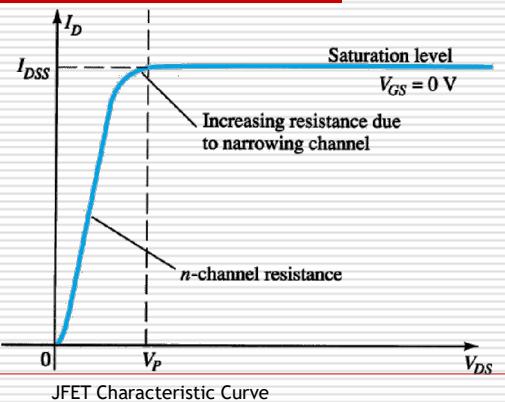
p-Channel JFET



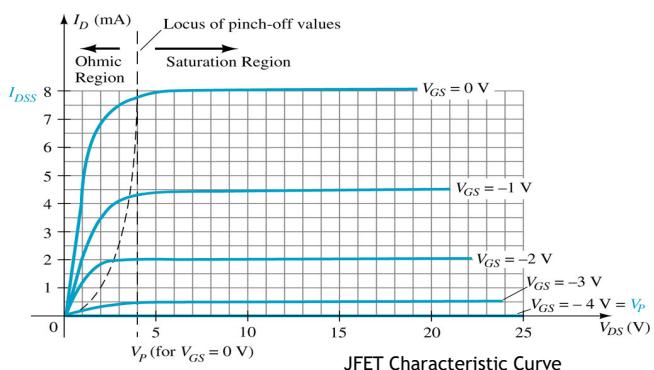
JFET Characteristic Curve

- To start, suppose $V_{GS}=0$
- Then, when V_{DS} is increased, I_D increases. Therefore, I_D is proportional to V_{DS} for small values of V_{DS}
- For larger value of V_{DS} , as V_{DS} increases, the depletion layer become wider, causing the resistance of channel increases.
- After the pinch-off voltage (V_p) is reached, the I_D becomes nearly constant (called as I_D maximum, I_{DSS} -Drain to Source current with Gate Shorted)

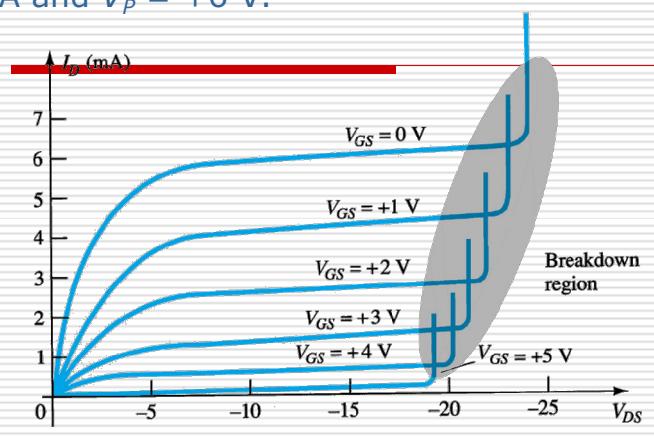
I_D versus V_{DS} for $V_{GS} = 0$ V.



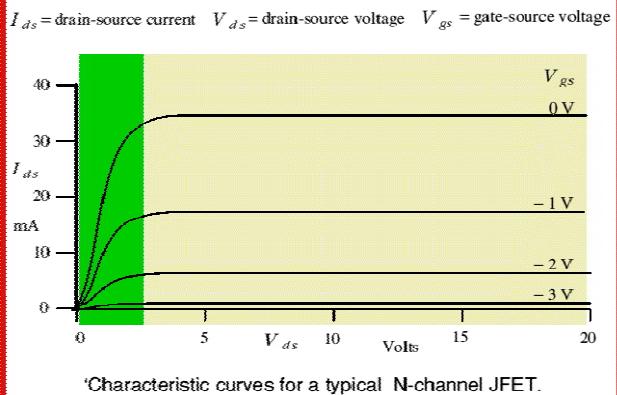
n-Channel JFET characteristics curve with $I_{DSS} = 8$ mA and $V_p = -4$ V.



p-Channel JFET characteristics with $I_{DSS} = 6$ mA and $V_p = +6$ V.



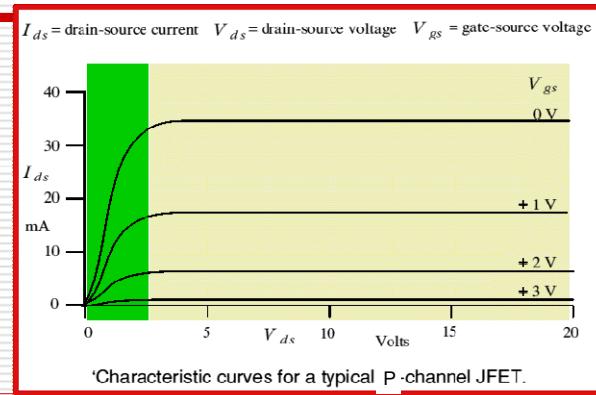
Characteristics for n-channel JFET



JFET Characteristic Curve..

- For negative values of V_{GS} , the gate-to-channel junction is reverse biased even with $V_{DS}=0$
- Thus, the initial channel resistance is higher (in which the initial slope of the curves is smaller for values of V_{GS} closer to the pinch-off voltage (V_P)
- The resistance value is under the control of V_{GS}
- If V_{GS} is less than pinch-off voltage, the resistance becomes an open-circuit ;therefore the device is in cutoff ($V_{GS}=V_{GS(off)}$)
- The region where I_D constant – The saturation/pinch-off region
- The region where I_D depends on V_{DS} is called the linear/triode/ohmic region

Characteristics for p-channel JFET



Operation of n-channel JFET

- JFET is biased with two voltage sources:
 - V_{DD}
 - V_{GG}
- V_{DD} generate voltage bias between Drain (D) and Source (S) – V_{DS}
- V_{DD} causes drain current, I_D flows from Drain (D) to Source (S)
- V_{GG} generate voltage bias between Gate (G) and Source (S) with negative polarity source is connected to the Gate Junction (G) – reverse-biases the gate; therefore gate current, $I_G = 0$.
- V_{GG} is to produce depletion region in N channel so that it can control the amount of drain current, I_D that flows through the channel

Transfer Characteristics

The input-output transfer characteristic of the JFET is not as straight forward as it is for the BJT. In BJT:

$$I_C = \beta I_B$$

which β is defined as the relationship between I_B (input current) and I_C (output current).

Transfer Characteristics..

In JFET, the relationship between V_{GS} (input voltage) and I_D (output current) is used to define the transfer characteristics. It is called as Shockley's Equation:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2 \quad V_p = V_{GS(\text{off})}$$

The relationship is more complicated (and not linear)

As a result, FET's are often referred to as square law devices

Transfer Characteristics...

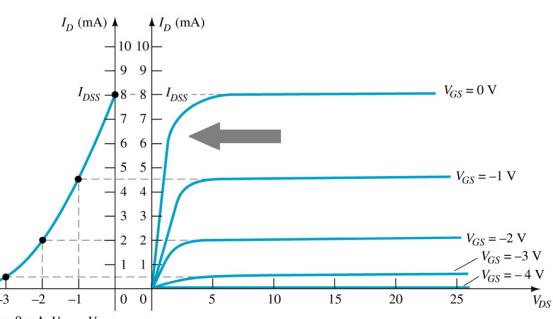
Defined by Shockley's equation:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2 \quad V_p = V_{GS(\text{off})}$$

Relationship between I_D and V_{GS} .

Obtaining transfer characteristic curve axis point from Shockley:

- When $V_{GS} = 0 \text{ V}$, $I_D = I_{DSS}$
- When $V_{GS} = V_{GS(\text{off})}$ or V_p , $I_D = 0 \text{ mA}$



JFET Transfer Characteristic Curve

JFET Characteristic Curve

Exercise 1

Sketch the transfer defined by
 $I_{DSS} = 12 \text{ mA}$ dan $V_{GS(\text{off})} = -6$

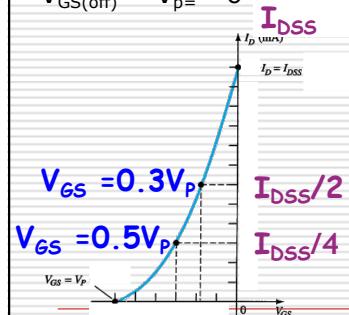
V_{GS}	I_D
0	I_{DSS}
$0.3V_p$	$I_{DSS}/2$
$0.5V_p$	$I_{DSS}/4$
V_p	0 mA

$$V_{GS} = V_p \left(1 - \sqrt{\frac{I_D}{I_{DSS}}} \right)$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

Exercise 1

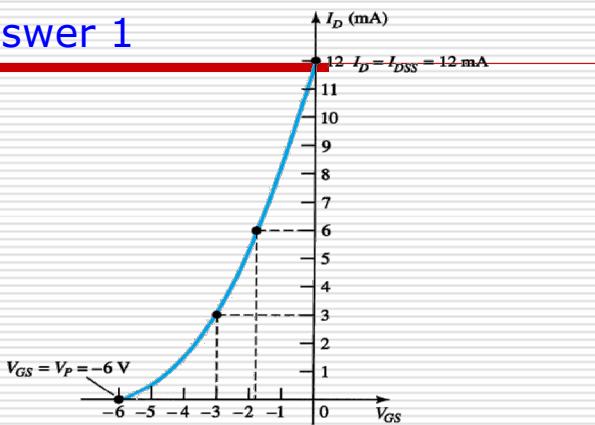
Sketch the transfer defined by $I_{DSS} = 12 \text{ mA}$ dan
 $V_{GS(\text{off})} = V_p = -6$



$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

$$V_{GS} = V_p \left(1 - \sqrt{\frac{I_D}{I_{DSS}}} \right)$$

Answer 1



Exercise 2

Sketch the transfer defined by
 $I_{DSS} = 4 \text{ mA}$ dan $V_{GS(\text{off})} = 3 \text{ V}$

V_{GS}	I_D
0	I_{DSS}
$0.3V_p$	$I_{DSS}/2$
$0.5V_p$	$I_{DSS}/4$
V_p	0 mA

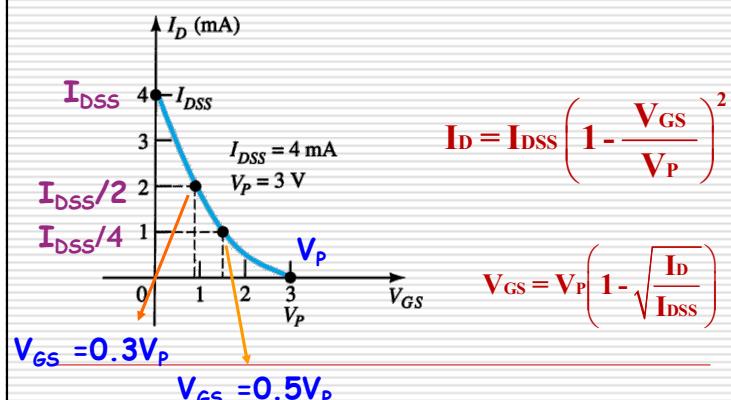
$$V_{GS} = V_p \left(1 - \sqrt{\frac{I_D}{I_{DSS}}} \right)$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

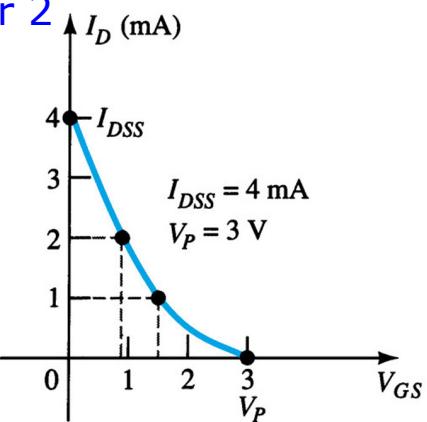
Exercise 2

Sketch the transfer defined by

$$I_{DSS} = 4 \text{ mA} \text{ dan } V_{GS(\text{off})} = 3V$$



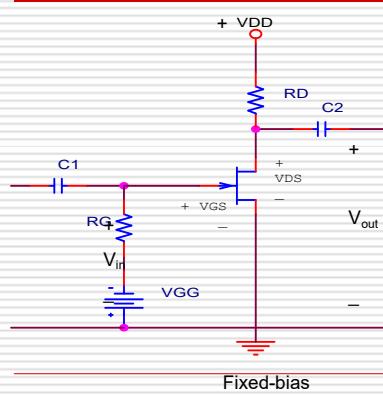
Answer 2



DC JFET Biasing

- Just as we learned that the BJT must be biased for proper operation, the JFET also must be biased for operation point (I_D , V_{GS} , V_{DS})
- In most cases the ideal Q-point will be at the **middle** of the transfer characteristic curve, which is **about half of the I_{DSS}** .
- 3 types of DC JFET biasing configurations :
 - Fixed-bias
 - Self-bias
 - Voltage-Divider Bias

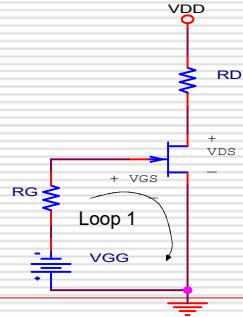
Fixed-bias



- Use two voltage sources: V_{GG} , V_{DD}
- V_{GG} is reverse-biased at the Gate - Source (G-S) terminal, thus no current flows through R_G ($I_G = 0$).

Fixed-bias..

- DC analysis
 - All capacitors replaced with open-circuit



Fixed-bias...

1. Input Loop

□ By using KVL at loop 1:

$$V_{GG} + V_{GS} = 0$$

$$V_{GS} = -V_{GG}$$

- For graphical solution, use $V_{GS} = -V_{GG}$ to draw the load line
- For mathematical solution, replace $V_{GS} = -V_{GG}$ in Shockley's Eq., therefore:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right)^2 = I_{DSS} \left(1 + \frac{V_{GG}}{V_{GS(\text{off})}} \right)^2$$

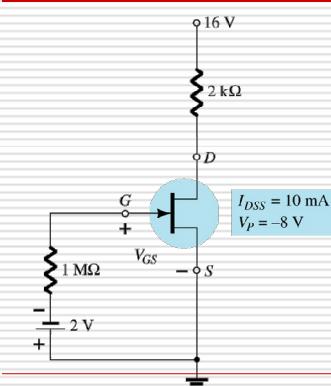
2. Output loop

$$-V_{DD} + I_D R_D + V_{DS} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

3. Then, plot transfer characteristic curve by using Shockley's Equation

Example : Fixed-bias



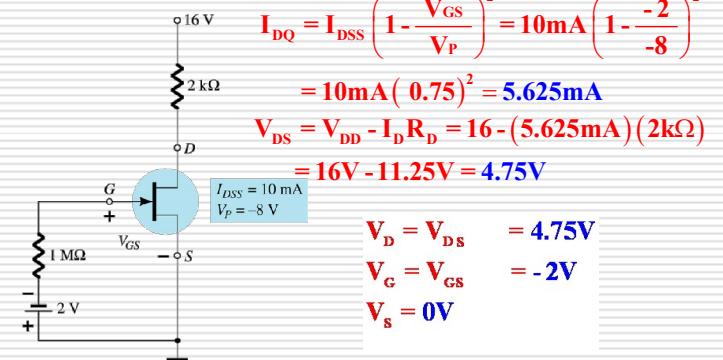
Determine the following network:

1. V_{GSQ}
2. I_{DQ}
3. V_D
4. V_G
5. V_S

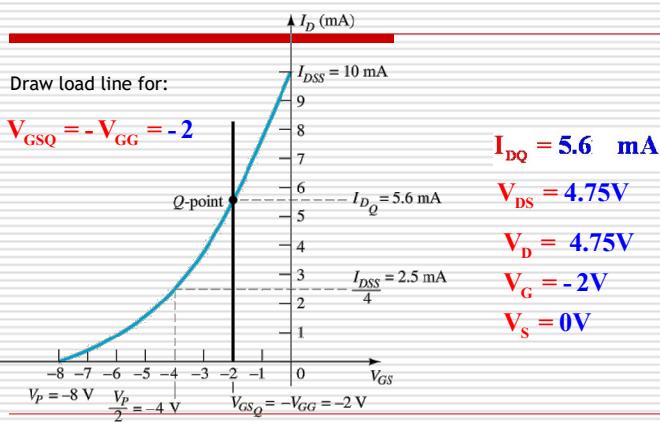
$$ID = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

Mathematical Solutions

$$V_{GSQ} = -V_{GG} = -2$$

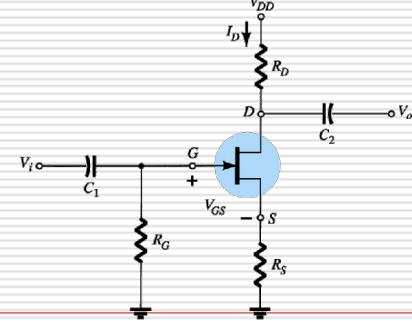


Graphical solution for the network

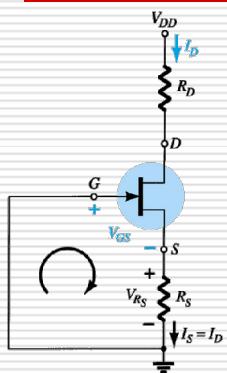


Self-bias

Using only one voltage source



DC analysis of the self-bias configuration.



Since $I_G \approx 0 \text{ A}$, $V_{RG} = I_G R_G$
thus $V_{RG} = 0 \text{ A}$,

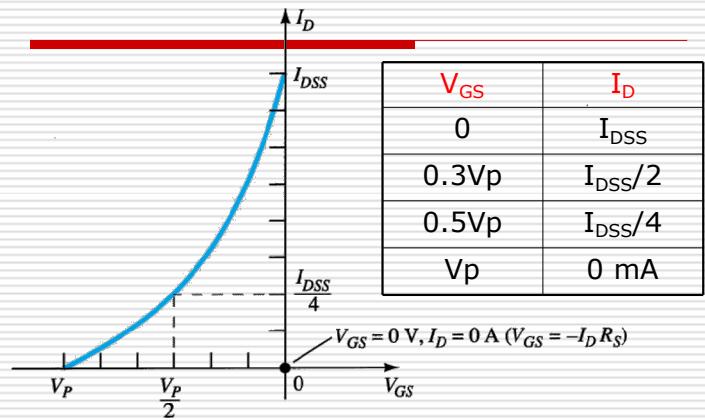
$$V_{RS} = I_D R_S$$

$$V_{GS} + V_{RS} = 0$$

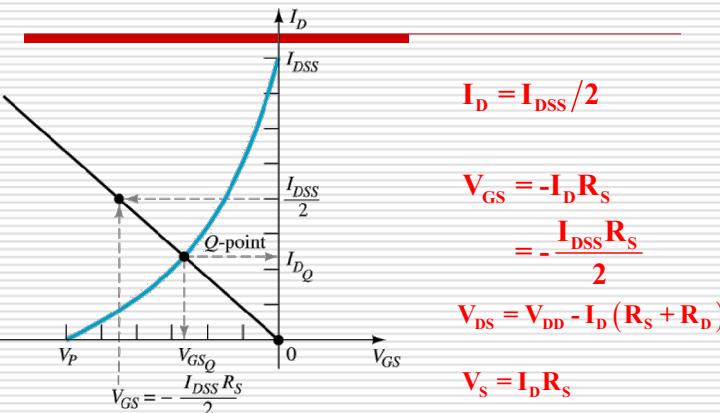
$$V_{GS} = -V_{RS} \\ = -I_D R_S$$

Q point for V_{GS}

Graphical Solutions: Defining a point on the self-bias line.



Graphical Solutions: Sketching the self-bias line.



Mathematical Solutions:

□ Replace $V_{GS} = -I_D R_S$ in the Shockley's Equation:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2 \quad V_p = V_{GS(\text{off})}$$

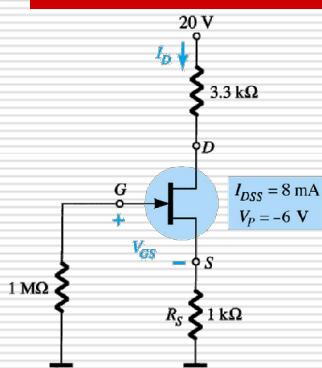
therefore;

$$I_D = I_{DSS} \left(1 - \frac{(-I_D R_S)}{V_p} \right)^2$$

□ By using, quadratic equation and formula, choose value of I_D that relevant within the range (0 to I_{DSS}): nearly to $I_{DSS}/2$

□ Find V_{GS} by using $V_{GS} = -I_D R_S$; also choose V_{GS} that within the range (0 to V_p)

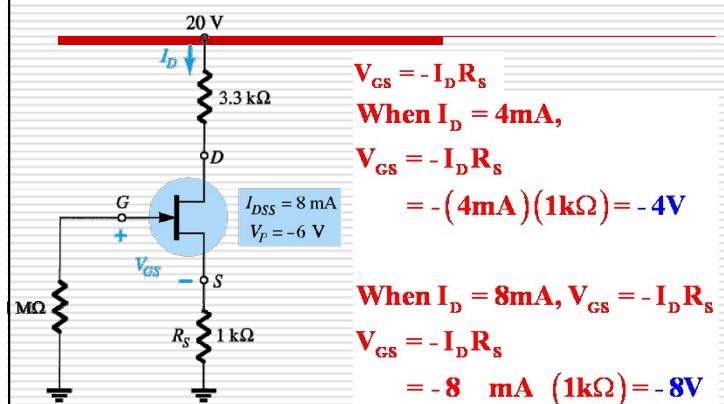
Example : Self-bias configuration



Determine the following for the network

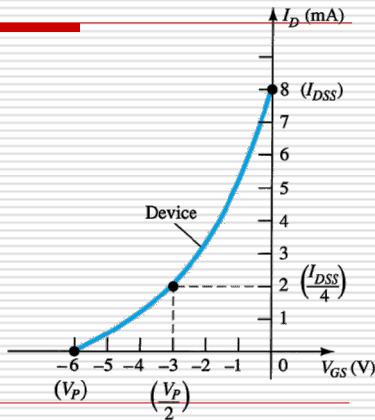
1. V_{GSQ}
2. I_{DQ}
3. V_D
4. V_G
5. V_S

Graphical Solutions:

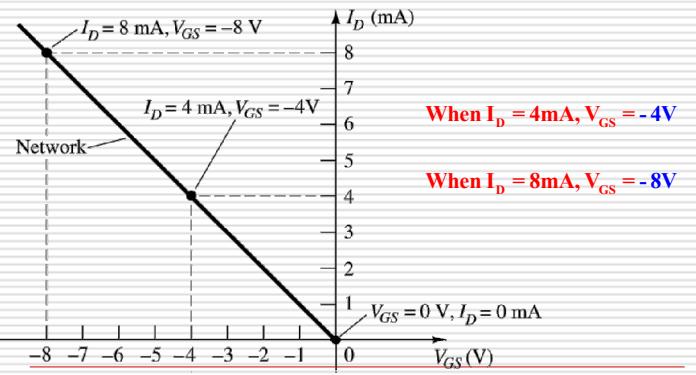


Sketching the transfer characteristics curve

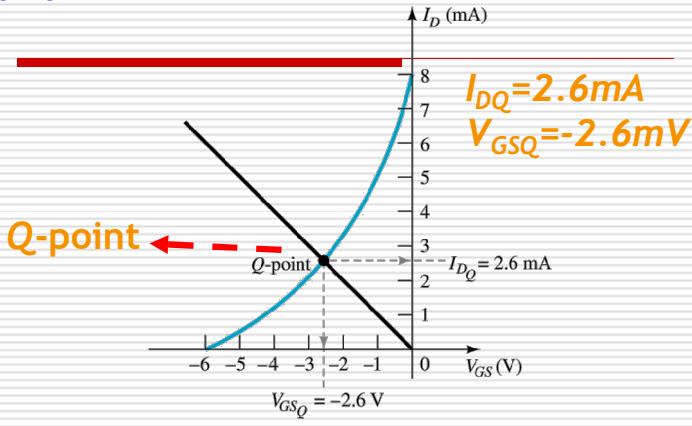
V _{gs}	I _D
0	I _{DSS}
0.3V _p	I _{DSS} /2
0.5V _p	I _{DSS} /4
V _p	0 mA



Sketching the self-bias line



Graphical Solutions: Determining the Q-point



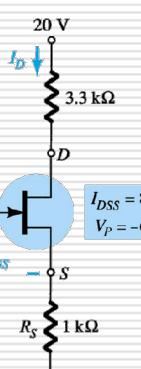
Mathematical Solutions

$$\begin{aligned}
 I_D &= I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2 \quad \text{recall} \quad V_{GS} = -I_D R_S \\
 &= I_{DSS} \left(1 - \frac{(-I_D R_S)}{V_p} \right)^2 \\
 I_D &= 8m \left(1 + \frac{I_D (1k)}{-6} \right)^2 = 8m \left(\frac{-6 + I_D (1k)}{-6} \right)^2 \\
 &= \frac{8m}{36} (36 - 6I_D - 6kI_D + 1mI_D^2) \\
 36I_D &= 0.288 - 96I_D + 8kI_D^2 \\
 8kI_D^2 - 132I_D + 0.288 &= 0 \\
 I_{D_1} &= 13.9 \text{ mA} \quad I_{D_{2i}} = 2.588 \text{ mA} \\
 V_{GS} &= -I_D R_S \quad V_{GS} = -I_D R_S \\
 &= -13.9 \text{ mA} (1k) \quad = -2.588 \text{ mA} (1k) \\
 &= -13.9V \quad = -2.6V \\
 \text{therefore ; choose } I_D &= 2.588 \text{ mA and } V_{GS} = -2.6V
 \end{aligned}$$

Solutions

$$V_{GSQ} = -2.6V$$

$$I_{DQ} = 2.6mA$$



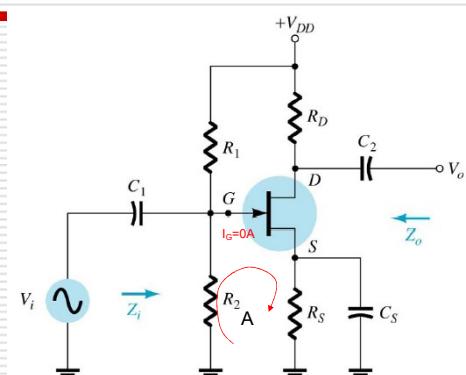
$$I_D = I_S$$

$$\begin{aligned} V_{DS} &= V_{DD} - I_D (R_D + R_S) \\ &= 20V - 2.6mA (4.3k\Omega) \\ &= 8.82V \end{aligned}$$

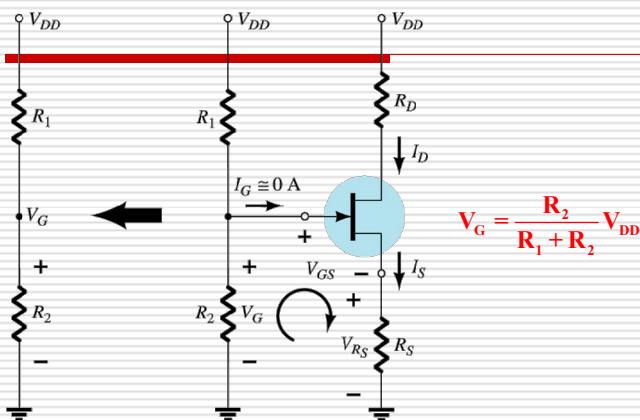
$$\begin{aligned} V_s &= I_S R_s = (2.6mA)(1k\Omega) \\ &= 2.6V \end{aligned}$$

$$\begin{aligned} V_G &= V_{GS} + V_s = 0V \\ V_D &= V_{DS} + V_s \text{ or } V_D = V_{DD} - I_D R_D \\ &= V_{DS} + V_s = 8.82V + 2.6V = 11.42V \end{aligned}$$

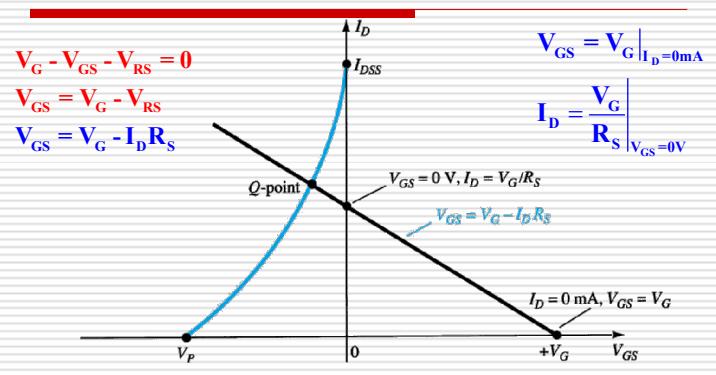
Voltage-divider bias



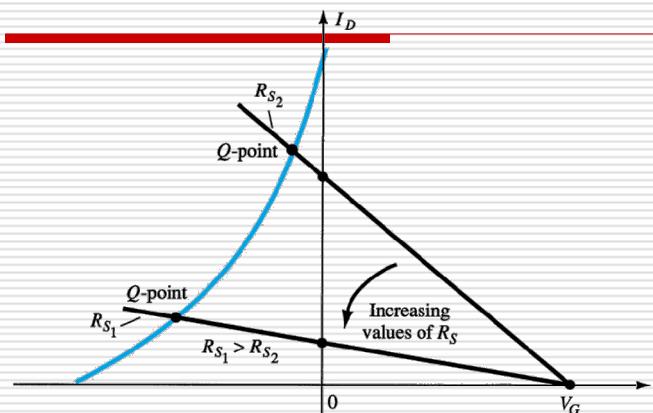
Redrawn network



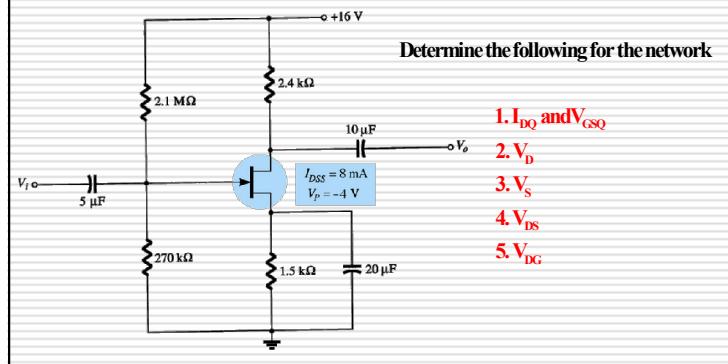
Sketching the network equation for the voltage-divider configuration.



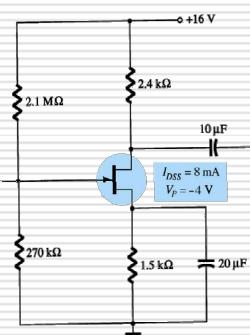
Effect of R_S on the resulting Q-point.



Example : Voltage-divider bias



Solutions



$$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$= \frac{(270\text{k}\Omega)(16\text{V})}{2.1\text{M}\Omega + 0.27\text{M}\Omega} V_{DD}$$

$$= 1.82\text{V}$$

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82\text{V} - 8\text{mA} (1.5\text{k}\Omega)$$

When $I_D = 0\text{mA}$, $V_{GS} = +1.82\text{V}$

$$\text{When } V_{GS} = 0\text{V}, I_D = \frac{+1.82\text{V}}{1.5\text{k}\Omega} = 1.21\text{mA}$$

Determining the Q-point for the network

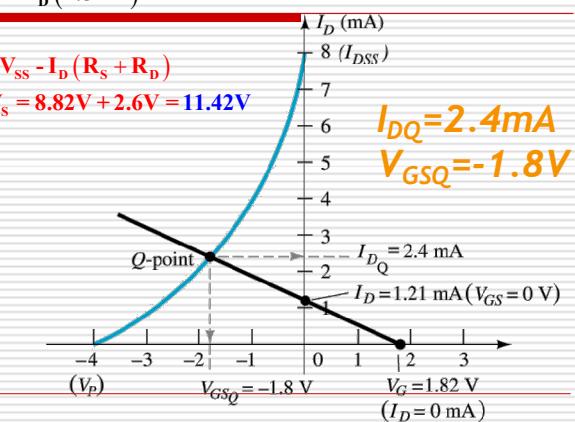
$$V_{GS} = 1.82\text{V} - I_D (1.5\text{k}\Omega)$$

$$V_{DS} = V_{DD} + V_{SS} - I_D (R_S + R_D)$$

$$= V_{DS} + V_S = 8.82\text{V} + 2.6\text{V} = 11.42\text{V}$$

$$I_{DQ} = 2.4\text{mA}$$

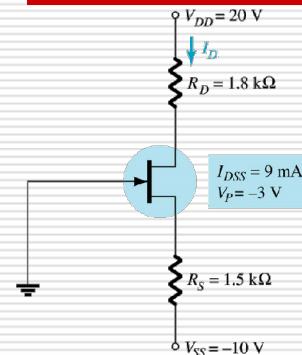
$$V_{GSQ} = -1.8\text{V}$$



Mathematical solutions

- How to get I_{DS} , V_{GS} and V_{DS} for voltage-divider bias configuration by using mathematical solutions?

Exercise 3:



Determine the following for the network

1. I_{DQ} and V_{GSQ}
2. V_{DS}
3. V_D
4. V_S

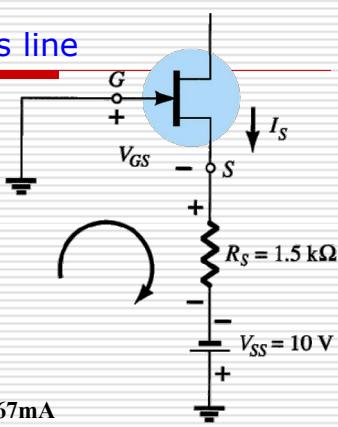
Drawing the self bias line

$$V_{GS} + I_D R_S - 10V = 0$$

$$V_{GS} = 10V - I_D (1.5k\Omega)$$

When $I_D = 0mA$, $V_{GS} = 10V$

$$\text{When } V_{GS} = 0V, I_D = \frac{10V}{1.5k\Omega} = 6.67mA$$



Determining the Q-point

$$I_{DQ} = 6.9mA$$

$$V_{GSQ} = -0.35V$$

$$V_{DS} = V_{DD} - (V_{SS}) - I_D (R_S + R_D)$$

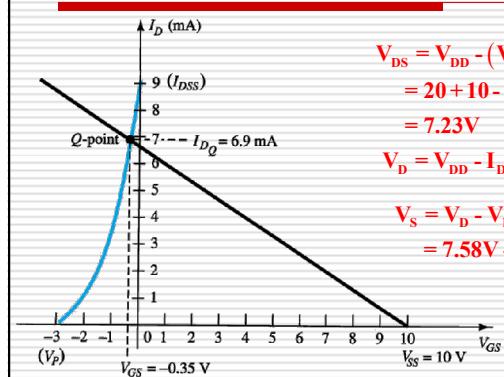
$$= 20 + 10 - (6.9mA)(1.8k\Omega + 1.5k\Omega)$$

$$= 7.23V$$

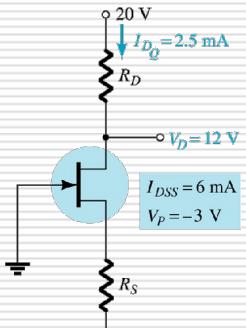
$$V_D = V_{DD} - I_D (R_D) = 7.58V$$

$$V_S = V_D - V_{DS}$$

$$= 7.58V - 7.23V = 0.35V$$



Exercise 4



Determine the required values of R_D and R_S

Determining V_{GSQ} for the network

