CMPE 240 Spring 2022 Experiment 6
Preliminary Question

Experiment 6 (Register-Transfer Level Design)

Aim

In this experiment, you will design a system using the RTL design method.

Problem

In this experiment, you will design a module that will be used to find the index of the maximum element from an 8 element array containing 8-bit values in signed 2s complement representation using the RTL design method.

A **start** input will be given for a single clock cycle signifying that the input array is ready, so you can start the operation. The operation may take multiple clock cycles and when it is done, along the **index of the maximum element**, you must also give an output **completed** for a single clock cycle which signifies that the operation is complete.

Another single bit input **reset** will be used to reset the outputs of the module, so that a new array can be given. The index output can be in unsigned/signed form, it is up to you.

Preliminary Work

You should prepare the following materials for the preliminary work:

1. **Capture a high-level state machine:** Describe the system's desired behavior as a high-level state machine.
2. **Construct a datapath:** Construct a datapath to carry out the data operations of the high-level state machine.
3. **Connect the datapath to a controller:** Connect the datapath to a controller block. Connect external boolean inputs and outputs to the controller block.
4. **Derive the controller's FSM:** Convert the high-level state machine to a finite-state machine for the controller, by replacing data operations with settings and reading of control signals to and from the datapath.

5. **Write code:** Write the behavioural level Verilog code for the module.

6. **Write testbench:** Write a testbench in Verilog to test some cases of the module to make sure it works the way you intended.

Submit your code and report considering the submission rules described in Lab Handbook. One submission per group is required.

Lab Work

1. Repeat all the procedures done in the preliminary work for the problem given in the lab section. Fill the report, write the Verilog code, and demonstrate your implementation to the assistants.