ECE 20002: Electrical Engineering Fundamentals II

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Lecture notes for Purdue's ECE 20002.

Contents

Course Introduction

Continuation of Electrical Engineering Fundamentals I. The course addresses mathematical and computational foundations of circuit analysis (differential equations, Laplace Transform techniques) with a focus on application to linear circuits having variable behavior as a function of frequency, with emphasis on filtering. Variable frequency behavior is considered for applications of electronic components through single-transistor and operational amplifiers. The course ends with a consideration of how circuits behave and may be modeled for analysis at high frequencies.

Learning Objectives:

1. Analyze 2nd order linear circuits with sources and/or passive elements
2. Compute responses of linear circuits with and without initial conditions via one-sided Laplace transform techniques
3. Compute responses to linear circuits using transfer function and convolution techniques
4. Analyze and design transistor amplifiers at low, mid and high frequencies

Field-Effect Transistor Devices

MOSFETs

Let us begin where ECE 20001 ended, with metal-oxide semiconductor field-effect transistors (MOSFETs). The rectangle below represent a wafer of silicon. The p - Si label indicates that the the wafer is primarily doped with boron and the primary carrier type is holes. The two n^+ rectangles designate regions of phosphorus doping. The grey rectangles above the wafer are dielectric layers of silicon dioxide. The black rectangles are ohmic metals that allow for connecting our phosphorus regions to other components. To these metal contacts we attach a source, a gate, and a drain. The source is the source of electron, and the drain is how the electrons exit. The gate will define a pathway between the source and drain. Since the phosphorus re-

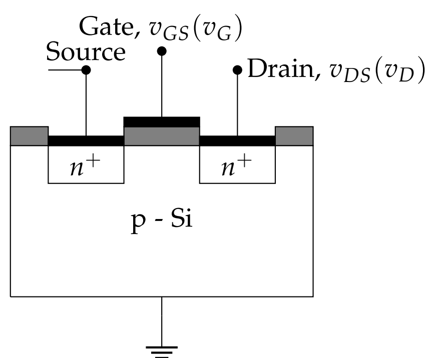

Figure 1: nMOSFET diagram

gions are n-type and ergo have free electrons, the primary carrier of this MOSFET are electrons. The way we allow current to flow from source to drain is by increasing the voltage of the gate v_{GS} to attract an inversion layer underneath the dielectric separating the gate from the silicon wafer. If the voltage of the gate is high enough ($v_{GS} > V_T$) then enough electrons will be attracted to that area for current to flow between source and drain.

We could create a similar MOSFET by inverting the n-type and p-type regions, as in figure 2. In this case the primary current carrier will be holes.

In the case of the nMOSFET in figure 1, a negative gate voltage will attract holes in the semiconductor, forming two oppositely charged areas separated by a distance x. This establishes an electric field within the oxide layer given by the equation for a parallel plate capacitor

$$\mathcal{E}_x = -\frac{dV}{dx} \tag{1}$$

Likewise, a positive gate voltage *that is less than* V_T will attract elec-

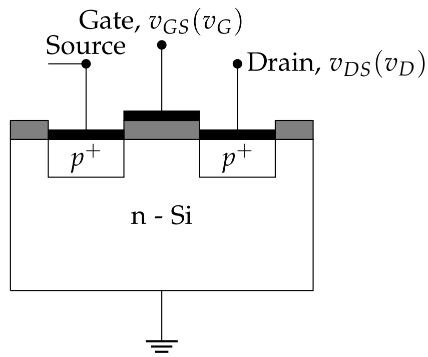

Figure 2: pMOSFET diagram

trons in the semiconductor. This also forms a capacitance of C_{ox} in the oxide layer, but because the semiconductor is n-type, the electrons will be spread out over a wider area and have their own capacitance C_d. Thus the total capacitance across the oxide and depletion region C given by

$$\frac{1}{C} = \frac{1}{C_o x} + \frac{1}{C_d} \tag{2}$$

If $0 < V_T < v_{GS}$, then $C = f\omega$, where ω is the frequency of our probe.

Figure 3 displays the capacitance-voltage graph of a p-type metal-oxide semiconductor. The capacitance is constant when gate voltage is negative, then falls at the *flat-band voltage* $V_{GS} = 0V$, then rapidly rises again after the threshold voltage is reached.

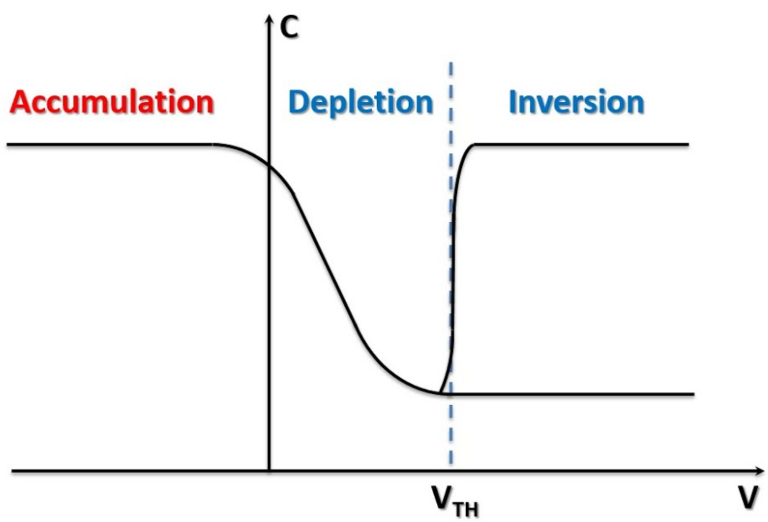

Figure 3: p-type MOS capacitance-voltage characteristic

The resistivity of the inversion channel created by the gate's bias is given by

$$\frac{1}{\rho} = (n\mu_e + p\mu_h)q \tag{3}$$

where n is the concentration of electrons, p is the concentration of holes, μ_e is the mobility of electrons, μ_h is the mobility of holes, and q is the charge of an electron. The higher the gate voltage, the higher the current between source and drain. Below the threshold voltage there is no current flow because no channel is formed. This relationship is linear provided the drain voltage is less than 150 mV, but above 0.3 V becomes nonlinear. That's because the channel is no longer a regular shape, but narrows in the region of the drain. Below 150 mV, however, this distortion can be assumed negligible. Recall that

$$R = \frac{\rho L}{A} \tag{4}$$

Whereas for small v_{DS} the area is almost constant, when $v_{DS} > 0.15V$ the area A decreases enough that the resistance R is significantly increased. When the area has decreased to zero at the drain, we reach the *pinch-off* and the drain voltage is at saturation $v_{DS(sat)}$. The current still flows constantly for all drain voltage above saturation, however. Before saturation is reached and after the gate voltage is above the threshold, we are in the triode region. In the triode region, the current is given by

$$i_{D(triode)} = \mu C_{ox} \frac{W}{L}((v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}) \tag{5}$$

Sometimes, the constant terms are wrapped up into one constant, like so:

$$i_{D(triode)} = k_n((v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}) \tag{6}$$

In the saturation region,

$$i_{D(sat)} = \mu C_{ox} \frac{W}{L} \frac{(v_{GS} - V_T)^2}{2} \tag{7}$$

$$= k_n \frac{v_{DS(sat)}^2}{2} \tag{8}$$

When we are far away from saturation, the resistance of the channel is given by

$$R_{on} = \frac{\partial v_{DS}}{\partial i_D} \tag{9}$$

$$= \frac{1}{\mu C_{ox} \frac{W}{L}(v_{GS} - V_T)} \tag{10}$$

Figure 4 shows a family of i_D-v_{DS} curves with differing values of v_{GS}. Also show as a dashed green line is the saturation current as a function of gate voltage. Let's look at the impact the threshold voltage has by plotting the i_D-v_{GS} curve for differing values of V_T in figure 5. Now the green dashed curve corresponds to a threshold voltage of

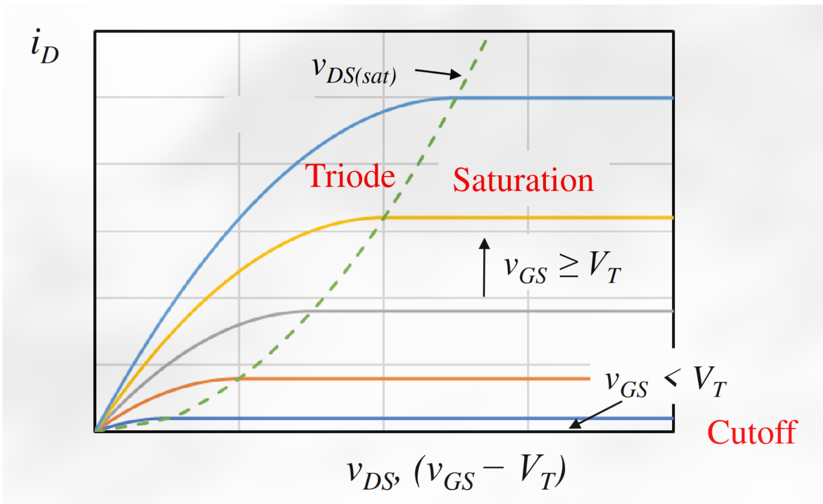

Figure 4: Transfer characteristics of nMOSFETs

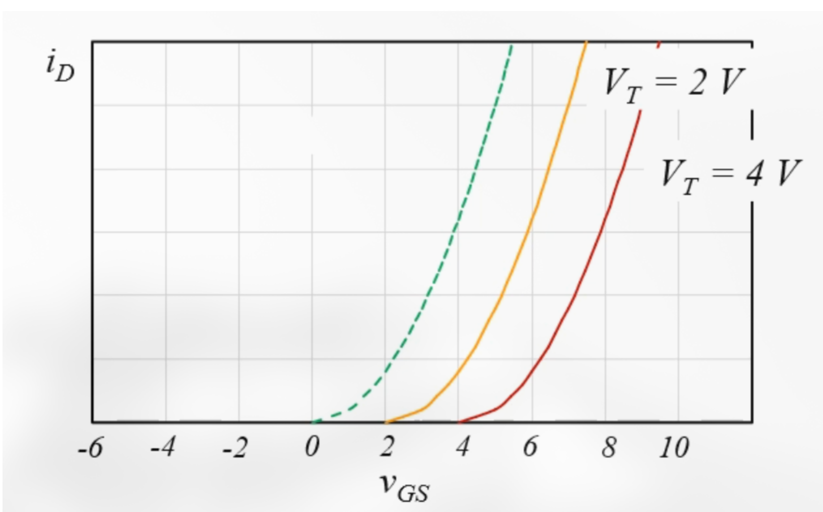

Figure 5: i_D-v_{GS} curve for select values of V_T

zero. Recall that the threshold voltage is intrinsic to the semiconductor wafer. Doping variations, defect, and shape can all affect the threshold voltage. If we build a depletion-mode nMOSFET, then we allow for negative threshold voltages.

A normally off like in figure 1 has the symbol shown in 6 and is said to be in enhancement mode. If the nMOSFET has an n-channel

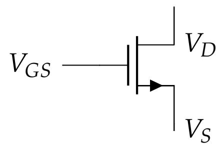

Figure 6: nMOSFET schematic

between the source and drain, as shown in figure 7, then it is normally

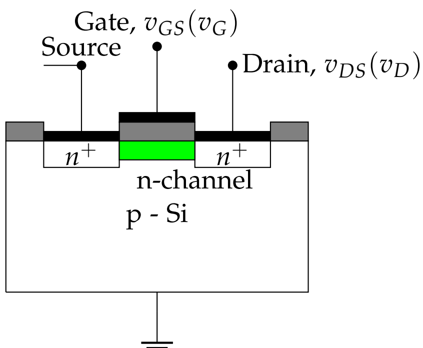

Figure 7: Normally on nMOSFET diagram

on and its symbol is as seen in figure 8. This kind of nMOSFET is said to be in depletion mode. Note the thicker line between source and

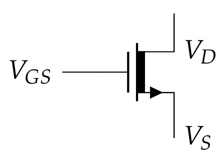

Figure 8: Schematic of normally on nMOSFET

drain representing the n-channel.

Similarly, the pMOSFET shown in figure 2 is a normally off, enhancement mode pMOSFET. A pMOSFET with a p-channel is normally on and in depletion mode.

Let's look at the transfer characteristics of the different types of MOSFETs. figure 4 shows these characteristics for a normally off, enhancement mode nMOSFET. For a normally on, depletion mode nMOSFET the graph is exactly the same, except that the current can flow even when the gate bias is zero since the fabricated channel allows the flow of electrons from source to drain. The output characteristics for a normally off, enhancement mode pMOSFET are shown in figure 9. A negative bias on the gate will induce a channel of pos-

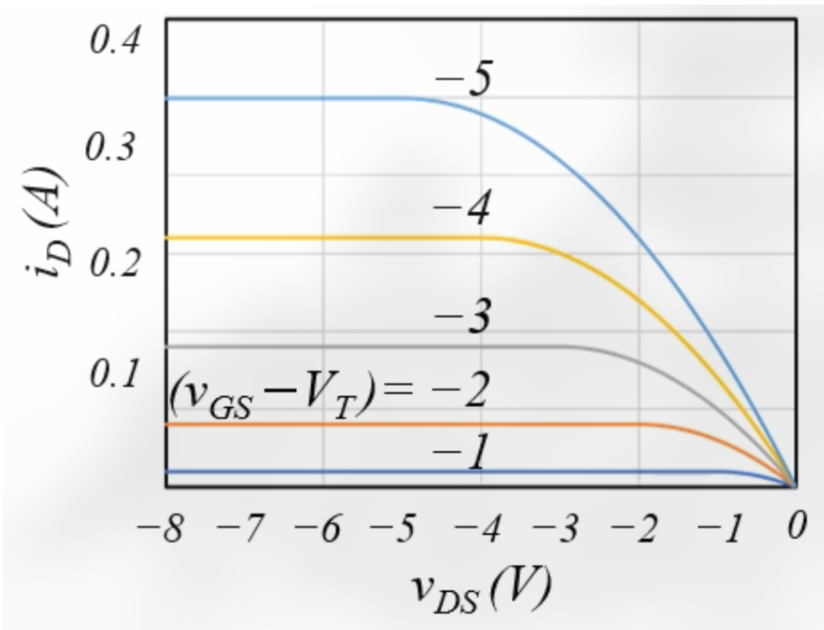

Figure 9: i_D-v_{DS} curve for select values of $v_{GS} - V_T$

itive holes in the semiconductor, making the threshold voltage for a pMOSFET negative. Again, the normally on depletion mode pMOSFET graph has the same shape, but since there is an existing channel for current it will flow even for some positive values of v_{GS}. We need to deplete the channel by pushing away all the holes in it with the bias on the gate in order to turn it off.

To review, there for four kinds of MOSFETs in which we are interested:

- normally off, enhancement mode nMOSFETs
- normally on, depletion mode nMOSFETs
- normally off, enhancement mode pMOSFETs
- normally on, depletion mode pMOSFETs

Transconductance

Now, let us move on the the topic of transconductance. In the triode region, the transconductance is defined as

$$g_m = \frac{i_D}{v_{GS}}|_{Q_{pt}} \tag{11}$$

where

$$Q_{pt} = (I_D, V_{DS}). \tag{12}$$

If we recall equation 5, and substitute for i_D in equation 11, then we obtain

$$g_m = \mu C_{ox} \frac{W}{L} v_{DS} \tag{13}$$

$$= \frac{i_{D(triode)}}{(v_{GS} - v_T) - \frac{v_{DS}}{2}} \tag{14}$$

In the saturation region,

$$g_m = \frac{di_D}{dv_{GS}}|_{Q_{pt}} \tag{15}$$

and

$$i_{D(sat)} = \mu C_{ox} \frac{W}{L} \frac{(v_{GS} - V_T)^2}{2}. \tag{16}$$

Again combining these two equations,

$$g_m = \mu C_{ox} \frac{W}{L} (v_{GS} - V_T) \tag{17}$$

$$= \frac{2 i_{D(sat)}}{(v_{GS} - V_T)} \tag{18}$$

The larger the transconductance, the larger the gain of an amplifier circuit that uses the transistor.

Channel length modulation

By adjusting the voltage of the drain, we can modulate the channel length. Specifically,

$$i_{D(sat)} \propto \frac{1}{L - \Delta L} \tag{19}$$

$$\equiv \frac{1}{L} \left(1 + \frac{\Delta L}{L}\right). \tag{20}$$

And

$$\Delta L \propto (v_{DS} - v_{DS(sat)}) \tag{21}$$

means that

$$i_{D(sat)} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (v_{GS} - V_T)^2 \left[1 + \lambda(v_{DS} - v_{DS(sat)})\right] \tag{22}$$

where λ is the empirically determined channel length modulation parameter. The output resistance at the drain is given by

$$r_0 = \left[\frac{\partial i_{D(sat)}}{\partial v_{DS}}\right]^{-1} \tag{23}$$

$$= \left[\lambda \frac{1}{2} k_n (v_{GS} - V_T)^2\right]^{-1} \tag{24}$$

$$= \frac{1}{\lambda I_{D(sat)}} \tag{25}$$

$$\approx \frac{V_A}{I_{D(sat)}} \tag{26}$$

Channel length modulation is not important when channel length is relatively large, but it is important on modern transistors where are on the order of nanometers.

MOSFETs in DC circuits

Consider a circuit with two enhancement mode pMOSFETs. Notice

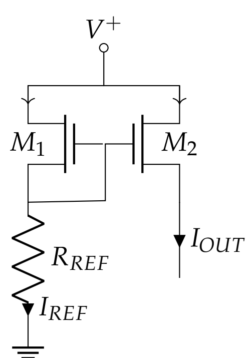

Figure 10: MOSFET DC circuit

that in figure 10, the drain of M_1 is directly attached to the gate. From this we have

$$v_{DS1} = v_{GS1} \tag{27}$$

$$= v_{GS2} \tag{28}$$

We are told M_1 is in saturation. If these are two identical transistors, then

$$I_{REF} = I_{D(sat)} \tag{29}$$

$$= \frac{1}{2} k_{p1} (v_{GS1} - V_{T1})^2 \tag{30}$$

$$= I_{OUT}. \tag{31}$$

From this, we learn that the reference current is mirrored by the drain current if $k_{p1} = k_{p2}$ and $v_{GS1} = v_{GS2}$.

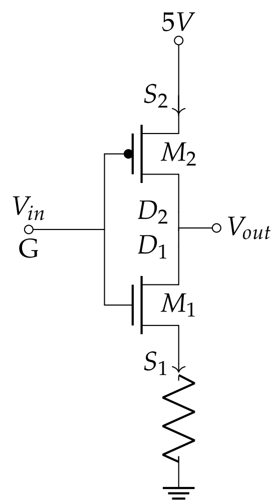

Figure 11: Inverter

Let us now look at the inverter shown in figure 11. Let's try to find V_{out} for $V_{in} = 0V$ and $V_{in} = 5V$. We are told that $V_{T(M1)} = 1V$ and $V_{T(M2)} = -1V$, because M1 is an enhancement mode nMOSFET and M2 is an enhancement mode pMOSFET. When $V_{in} = 0V$, M1 is off because $v_{GS1} < V_{T(M1)}$. Likewise, M2 is on because $v_{GS2} < V_{T(M2)}$ (recall that M2 is a pMOSFET). Since M1 is off, no current flows and $V_{out} = 5V$. For $V_{in} = 5V$, M1 flips on while M2 is off. Since M2 is off, no current flows. That means that $V_{out} = 5V$.

Transistors as amplifiers

The circuit shown in figure 12 has both AC and DC voltage sources.

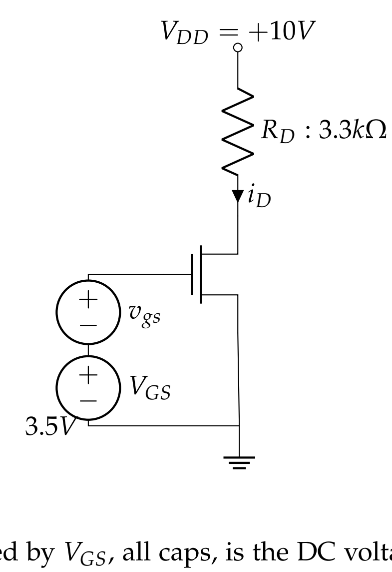

Figure 12: Common-source nMOSFET amplifier circuit

The source labelled by V_{GS}, all caps, is the DC voltage. The source v_{gs}, all lowercase, is the AC. This is not to be confused with v_{GS}, the total gate bias. The mix of cases indicates we have both AC and DC bias in consideration. The cool thing about this circuit is a small oscillation in the AC input induces a much larger oscillation in the output, hence calling it an amplifier. The output signal is going to be phase shifted by 180°. We can calculate the gain with eq. 32

$$A_v = \frac{v_{ds}}{v_{gs}} \tag{32}$$

In this instance,

$$\begin{aligned} A_v &= \frac{v_{ds}}{v_{gs}} && (33) \\ &= \frac{4.17\angle 180^\circ}{1\angle 0^\circ} && (34) \\ &= -4.17 && (35) \end{aligned}$$

This gain, however, will be somewhat distorted. To reduce distortion we need that $|v_{gs}| << 2(V_{GS} - V_T)$. The exact value of the "much less" symbol $<<$ will depend on the application, but it's common to require $|v_{gs}| < 0.2(V_{GS} - V_T)$. If we assume the small signal condition and no channel length modulation, then the transconductance of the amplifier is

$$g_m = \sqrt{2k_n I_{D(sat)}} \tag{36}$$

Figure 13 shows the small signal equivalent circuit of a common source amplifier. Notice the two voltage sources, one AC signal and

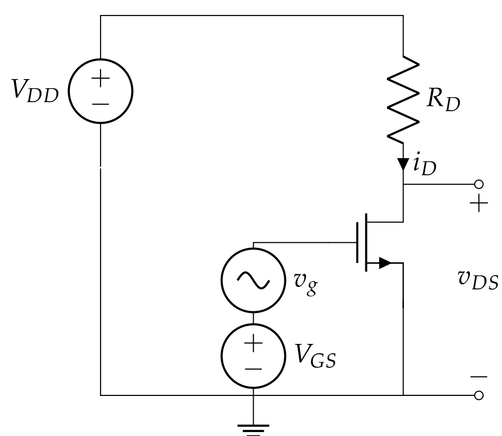

Figure 13: Small signal equivalent circuit

one DC bias at the gate. The total input signal is given by

$$v_{GS}(t) = v_{gs}(t) + V_{GS} \tag{37}$$

$$v_{DS}(t) = v_{ds}(t) + V_{DS} \tag{38}$$

The drain current for such a circuit when channel length modulation is accounted for is given by

$$\begin{aligned} i_{D(clm)} = \frac{1}{2}k_n \left[v_{gs}^2 + 2(V_{GS} - V_T)v_{gs} + (V_{GS} - V_T)^2\right] \\ \times \left[1 + \lambda(V_{DS} - (V_{GS} - V_T)) + \lambda(v_{ds} - v_{gs})\right] \end{aligned}$$

When channel length modulation can be ignored, the current reduces to

$$i_{D(sat)} = \frac{1}{2}k_n \left[v_{gs}^2 + 2(V_{GS} - V_T)v_{gs} + (V_{GS} - V_T)^2\right] \tag{39}$$

For finite output resistance r_0,

$$\begin{aligned} \frac{1}{r_0} &= \left[\frac{\partial i_{D(clm)}}{\partial v_{DS}}\right] && (40) \\ &= \frac{\partial}{\partial v_{DS}} \left\{\frac{k_n}{2}(v_{GS} - V_T)^2 \left[1 + \lambda(v_{DS} - v_{DS(sat)})\right]\right\} && (41) \\ &= \frac{k_n}{2}(v_{GS} - V_T)^2 \frac{\partial}{\partial v_{DS}} \left[1 + \lambda(v_{DS} - v_{DS(sat)})\right] && (42) \\ &= \lambda \frac{k_n}{2}(v_{GS} - V_T)^2 && (43) \\ &= \lambda I_{D(sat)}. && (44) \end{aligned}$$

We then define the *intrinsic voltage gain of a MOSFET* as

$$\begin{aligned} \mu_f &= g_m r_0 && (45) \\ &= \sqrt{2k_n I_{D(sat)}} \left(\frac{1}{\lambda I_{D(sat)}}\right) && (46) \\ &= \frac{1}{\lambda}\sqrt{\frac{2k_n}{I_{D(sat)}}} && (47) \end{aligned}$$

We can greatly simplify circuit analysis by breaking the circuit up into AC and DC. To find the DC equivalent circuit, follow these steps:

1. Replace all capacitors with open circuits
2. Replace all inductors with short circuits
3. Deactivate AC sources
4. Find the Q-point using the DC equivalent circuit

To find the AC equivalent circuit,

1. Replace all capacitors with short circuits at operational frequency
2. Replace all inductors with open circuits at operational frequency
3. Deactivate DC voltages and replace with short circuits
4. Deactivate DC current sources and replace with open circuits
5. Replace the transistor with its small-signal model

Amplifier topologies

There are three different nMOSFET amplifier topologies we will consider in this class, starting with the common-source amplifier shown in figure 14. The common-source amplifier's input is taken

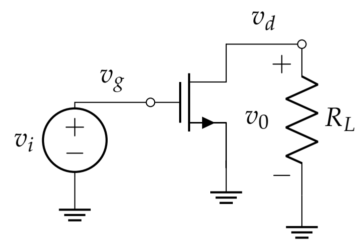

Figure 14: Common-source amplifier

through the gate, the output is taken through the drain, and the terminal that is common to output and input is the source.

The second topology is the common-gate amplifier shown in figure 15. Here we see that the AC voltage source is applied to the source,

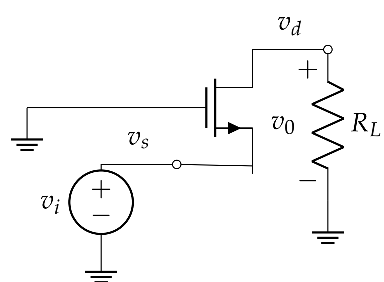

Figure 15: Common-source amplifier

while the output is taken at the drain and the common terminal is at the gate.

The previous two amplifiers suggest a third, the common-drain amplifier in figure 16. As may be expected, here the common terminal

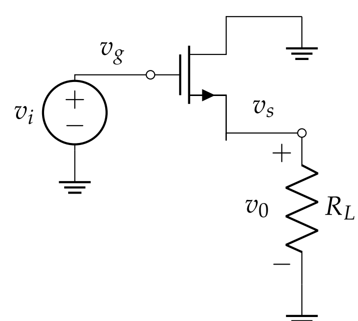

Figure 16: Common-source amplifier

is the drain, the input is at the gate, and the output is at the source.

You may be thinking: "what happens if the input and output are swapped? Will the circuit still work as an amplifier?" No.

The voltage gain in a common-drain amplifier is given by

$$A_V = \frac{g_m R_L'}{1 + g_m R_L'} \left(\frac{R_G}{R_I + R_G} \right) \tag{48}$$

where $R_L' = (r_0 || R_6 || R_3)$. For a MOSFET where $r_0 >> R_L$,

$$A_V \approx \frac{R_G}{R_I + R_G} \tag{49}$$

When this is true, the MOSFET is acting as a *voltage follower*.

Figure 17 shows the small-signal model for an nMOSFET called a hybrid-pi model. This model is excellent for common-source and common-drain amplifiers. For the common-gate amplifier, the alternative T-model shown in figure 18 is more useful. The voltage gain in a common-gate amplifier is given by

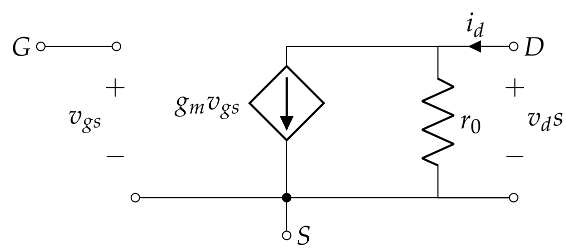

Figure 17: Hybrid-pi model

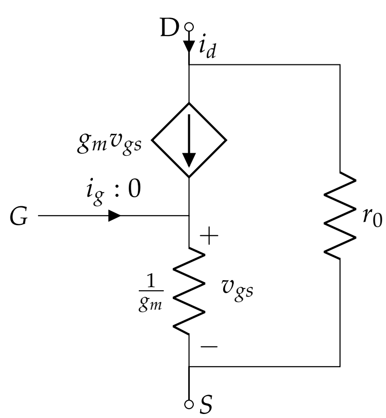

Figure 18: T-model

$$A_V = \frac{g_m R_L}{1 + g_m (R_I || R_6)} \left(\frac{R_6}{R_I + R_6} \right) \tag{50}$$

Let's recap our three kinds of amplifiers. For the inverting common-source amplifier,

$$A_V = -\frac{g_m R_L}{1 + g_m R_S} \left(\frac{R_G}{R_I + R_G} \right). \tag{51}$$

Additionally,

$$R_{in} = \infty \tag{52}$$
$$R_{out} = R_L \tag{53}$$

For the non-inverting common-gate amplifier,

$$A_V = \frac{g_m R_L}{1 + g_m (R_I || R_6)} \left(\frac{R_6}{R_I + R_6} \right) \tag{54}$$

with

$$R_{in} = \frac{1}{g_m} \tag{55}$$
$$R_{out} = R_L \tag{56}$$

For the follower common-drain amplifier,

$$A_V = \frac{g_m R_L}{1 + g_m R_L} \left(\frac{R_G}{R_I + R_G} \right) \tag{57}$$
$$\approx \left(\frac{R_G}{R_I + R_G} \right). \tag{58}$$

Here,

$$R_{in} = \infty \tag{59}$$
$$R_{out} = \frac{1}{g_m} \tag{60}$$

The *lower-frequency cutoff* for an amplifier circuit is defined as the ω_L where the gain A_V is $\frac{1}{\sqrt{2}}$ the maximum gain. The *higher-frequency cutoff* ω_H is also defined as the frequency where the gain A_V is $\frac{1}{\sqrt{2}}$ the maximum gain, but the higher of the two values. The bandwidth of useable frequencies is $\omega_H - \omega_L$.

In addition to the intrinsic capacitances C_{ox} and C_d, there are also parasitic capacitances. The junction capacitance C_J forms between the source/drain and the semiconductor, while the overlap capacitance C_{ov} forms between the source/drain and the metal contact on the gate.

Reference

Region	Conditions
Cut-off	$v_{GS} < V_T$
Triode	$v_{DS} > v_{DS(sat)}$
Saturation	$v_{DS} \leq v_{DS(sat)}$

Figure 19: nMOSFET regions of operation

Region	Conditions
Cut-off	$v_{GS} > V_T$
Triode	$v_{DS} \leq v_{DS(sat)}$
Saturation	$v_{DS} > v_{DS(sat)}$

Figure 20: pMOSFET regions of operation

	nMOSFET	pMOSFET
Cutoff	$v_{GS} < 0$	$v_{GS} > 0$
Triode	$v_{GS} > 0$	$v_{GS} < 0$
Saturation	$v_{GS} > 0$	$v_{GS} < 0$
Enhancement	$V_T > 0$	$V_T < 0$
Depletion	$V_T < 0$	$V_T > 0$

Figure 21: Differences between pMOSFET and nMOSFET

Equation	Use	Reference
$v_{DS(sat)} = v_{GS} - V_T$	MOSFET	
$i_{D(cutoff)} = 0$	MOSFET	
$i_{D(triode)} = \mu C_{ox} \frac{W}{L}((v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2})$ $= k_n((v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2})$ $= \frac{k_n}{2}(2v_{DS(sat)} - v_{DS})v_{DS}$	MOSFET	eq. 5
$i_{D(sat)} = \mu C_{ox} \frac{W}{L} \frac{(v_{GS}-V_T)^2}{2}$ $= k_n \frac{v_{DS(sat)}^2}{2}$	MOSFET	eq. 7
$A_v = \frac{v_{out}}{v_{in}}$	Amplifying transistor	eq. 32
$g_m = \sqrt{2k_n I_{D(sat)}}$	Amplifying transistor	eq. 36
$i_{D(clm)} = \frac{1}{2}k_n \left[v_{gs}^2 + 2(V_{GS} - V_T)v_{gs} + (V_{GS} - V_T)^2\right]$ $\times \left[1 + \lambda(V_{DS} - (V_{GS} - V_T)) + \lambda(v_{ds} - v_{gs})\right]$	CLM active	eq. 39

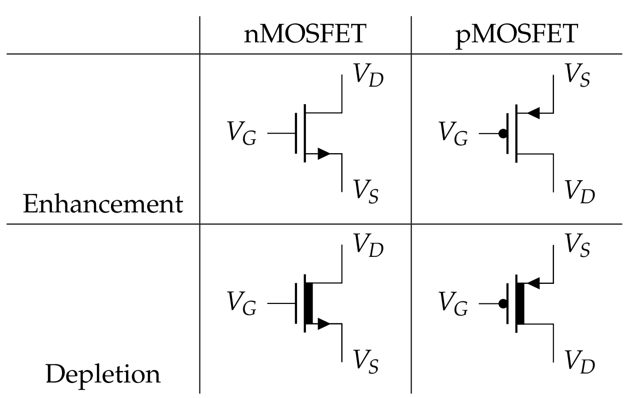

Figure 22: MOSFET schema

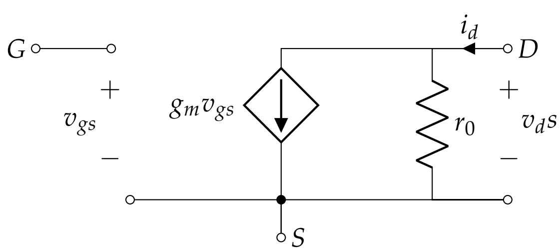

Figure 23: Hybrid-pi model