ECE 20002: Electrical Engineering Fundamentals II

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Lecture notes for Purdue's ECE 20002.

Contents

Course Introduction

Continuation of Electrical Engineering Fundamentals I. The course addresses mathematical and computational foundations of circuit analysis (differential equations, Laplace Transform techniques) with a focus on application to linear circuits having variable behavior as a function of frequency, with emphasis on filtering. Variable frequency behavior is considered for applications of electronic components through single-transistor and operational amplifiers. The course ends with a consideration of how circuits behave and may be modeled for analysis at high frequencies.

Learning Objectives:

1. Analyze 2nd order linear circuits with sources and/or passive elements
2. Compute responses of linear circuits with and without initial conditions via one-sided Laplace transform techniques
3. Compute responses to linear circuits using transfer function and convolution techniques
4. Analyze and design transistor amplifiers at low, mid and high frequencies

Field-Effect Transistor Devices

Let us begin where ECE 20001 ended, with metal-oxide semiconductor field-effect transistors (MOSFETs). The rectangle below represent a wafer of silicon. The p - Si label indicates that the the wafer is primarily doped with boron and the primary carrier type is holes. The two n^+ rectangles designate regions of phosphorus doping. The grey rectangles above the wafer are dielectric layers of silicon dioxide. The black rectangles are ohmic metals that allow for connecting our phosphorus regions to other components. To these metal contacts we attach a source, a gate, and a drain. The source is the source of electron, and the drain is how the electrons exit. The gate will define a pathway between the source and drain. Since the phosphorus regions are n-type and ergo have free electrons, the primary carrier of this MOSFET are electrons. The way we allow current to flow from source to drain is by increasing the voltage of the gate v_{GS} to attract an inversion layer underneath the dielectric separating the gate from the silicon wafer. If the voltage of the gate is high enough ($v_{GS} > V_T$) then enough electrons will be attracted to that area for current to flow between source and drain.

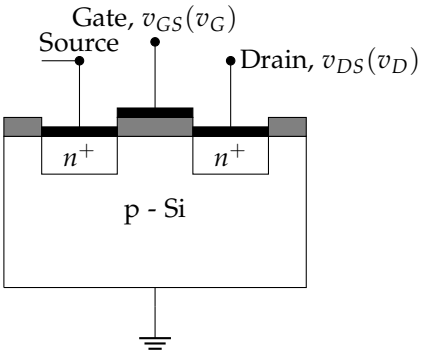

Figure 1: nMOSFET diagram

We could create a similar MOSFET by inverting the n-type and p-type regions, as in figure 2. In this case the primary current carrier will be holes.

In the case of the nMOSFET in figure **??**, a negative gate voltage will attract holes in the semiconductor, forming two oppositely charged areas separated by a distance x. This establishes an electric field within the oxide layer given by the equation for a parallel plate capacitor

$$\mathcal{E}_x = -\frac{dV}{dx} \tag{1}$$

Likewise, a positive gate voltage *that is less than* V_T will attract electrons in the semiconductor. This also forms a capacitance of C_{ox} in

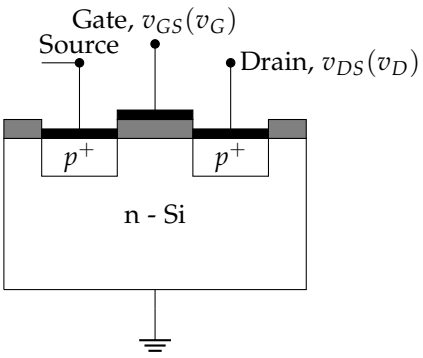

Figure 2: pMOSFET diagram

the oxide layer, but because the semiconductor is n-type, the electrons will be spread out over a wider area and have their own capacitance C_d. Thus the total capacitance across the oxide and depletion region C given by

$$\frac{1}{C} = \frac{1}{C_o x} + \frac{1}{C_d} \tag{2}$$

If $0 < V_T < v_{GS}$, then $C = f\omega$, where ω is the frequency of our probe.

Figure 3 displays the capacitance-voltage graph of a p-type metal-oxide semiconductor. The capacitance is constant when gate voltage is negative, then falls at the *flat-band voltage* $V_{GS} = 0V$, then rapidly rises again after the threshold voltage is reached.

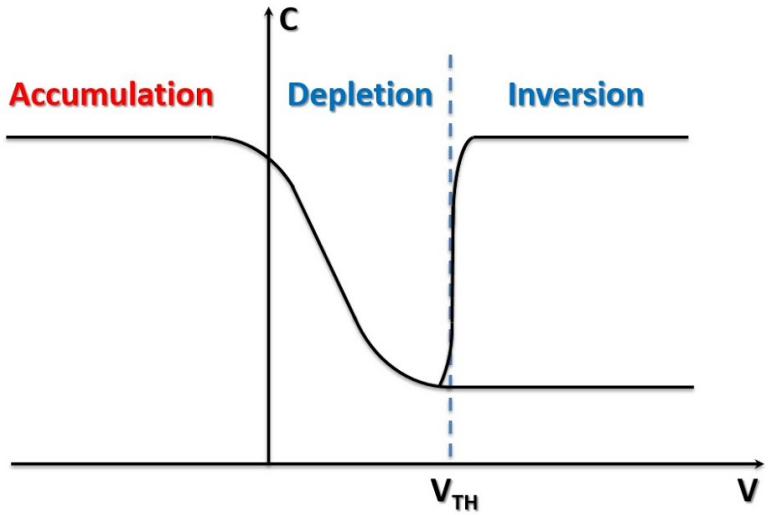

Figure 3: p-type MOS Capacitance-Voltage Characteristic

The resistivity of the inversion channel created by the gate's bias is given by

$$\frac{1}{\rho} = (n\mu_e + p\mu_h)q \tag{3}$$

where n is the concentration of electrons, p is the concentration of holes, μ_e is the mobility of electrons, μ_h is the mobility of holes, and q

is the charge of an electron. The higher the gate voltage, the higher the current between source and drain. Below the threshold voltage there is no current flow because no channel is formed. This relationship is linear provided the drain voltage is less than 150 mV, but above 0.3 V becomes nonlinear. That's because the channel is no longer a regular shape, but narrows in the region of the drain. Below 150 mV, however, this distortion can be assumed negligible. Recall that

$$R = \frac{\rho L}{A} \tag{4}$$

Whereas for small v_{DS} the area is almost constant, when $v_{DS} > 0.15V$ the area A decreases enough that the resistance R is significantly increased. When the area has decreased to zero at the drain, we reach the *pinch-off* and the drain voltage is at saturation $v_{DS(sat)}$. The current still flows constantly for all drain voltage above saturation, however. Before saturation is reached and after the gate voltage is above the threshold, we are in the triode region. In the triode region, the current is given by

$$i_{D(triode)} = \mu C_{ox} \frac{W}{L}((v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}) \tag{5}$$

Sometimes, the constant terms are wrapped up into one constant, like so:

$$i_{D(triode)} = k_n((v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}) \tag{6}$$

In the saturation region,

$$i_{D(sat)} = \mu C_{ox} \frac{W}{L} \frac{(v_{GS} - V_T)^2}{2} \tag{7}$$

$$= k_n \frac{v_{DS(sat)}^2}{2} \tag{8}$$

When we are far away from saturation, the resistance of the channel is given by

$$R_{on} = \frac{\partial v_{DS}}{\partial i_D} \tag{9}$$

$$= \frac{1}{\mu C_{ox} \frac{W}{L}(v_{GS} - V_T)} \tag{10}$$