ECE 20002: Electrical Engineering Fundamentals II

Zeke Ulrich

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Lecture notes for Purdue's ECE 20002.

Contents

Course Introduction

Continuation of Electrical Engineering Fundamentals I. The course addresses mathematical and computational foundations of circuit analysis (differential equations, Laplace Transform techniques) with a focus on application to linear circuits having variable behavior as a function of frequency, with emphasis on filtering. Variable frequency behavior is considered for applications of electronic components through single-transistor and operational amplifiers. The course ends with a consideration of how circuits behave and may be modeled for analysis at high frequencies.

Learning Objectives:

1. Analyze 2nd order linear circuits with sources and/or passive elements
2. Compute responses of linear circuits with and without initial conditions via one-sided Laplace transform techniques
3. Compute responses to linear circuits using transfer function and convolution techniques
4. Analyze and design transistor amplifiers at low, mid and high frequencies

Field-Effect Transistor Devices

MOSFETs

Let us begin where ECE 20001 ended, with metal-oxide semiconductor field-effect transistors (MOSFETs). The rectangle below represent a wafer of silicon. The p - Si label indicates that the the wafer is primarily doped with boron and the primary carrier type is holes. The two n^+ rectangles designate regions of phosphorus doping. The grey rectangles above the wafer are dielectric layers of silicon dioxide. The black rectangles are ohmic metals that allow for connecting our phosphorus regions to other components. To these metal contacts we attach a source, a gate, and a drain. The source is the source of electron, and the drain is how the electrons exit. The gate will define a pathway between the source and drain. Since the phosphorus re-

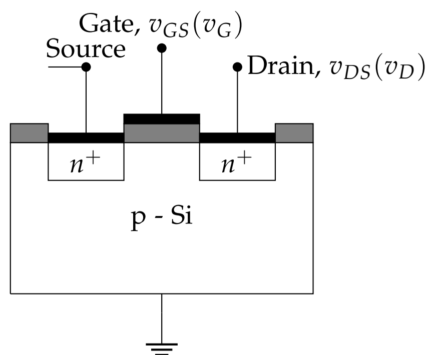

Figure 1: nMOSFET diagram

gions are n-type and ergo have free electrons, the primary carrier of this MOSFET are electrons. The way we allow current to flow from source to drain is by increasing the voltage of the gate v_{GS} to attract an inversion layer underneath the dielectric separating the gate from the silicon wafer. If the voltage of the gate is high enough ($v_{GS} > V_T$) then enough electrons will be attracted to that area for current to flow between source and drain.

We could create a similar MOSFET by inverting the n-type and p-type regions, as in figure 2. In this case the primary current carrier will be holes.

In the case of the nMOSFET in figure 1, a negative gate voltage will attract holes in the semiconductor, forming two oppositely charged areas separated by a distance x. This establishes an electric field within the oxide layer given by the equation for a parallel plate capacitor

$$\mathcal{E}_x = -\frac{dV}{dx} \tag{1}$$

Likewise, a positive gate voltage *that is less than* V_T will attract elec-

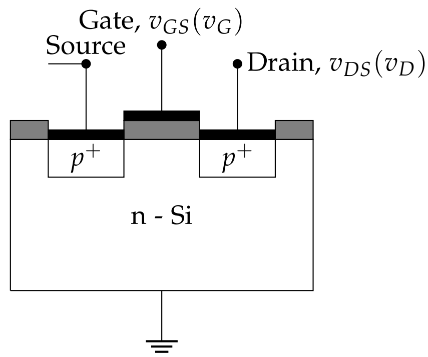

Figure 2: pMOSFET diagram

trons in the semiconductor. This also forms a capacitance of C_{ox} in the oxide layer, but because the semiconductor is n-type, the electrons will be spread out over a wider area and have their own capacitance C_d. Thus the total capacitance across the oxide and depletion region C given by

$$\frac{1}{C} = \frac{1}{C_o x} + \frac{1}{C_d} \tag{2}$$

If $0 < V_T < v_{GS}$, then $C = f\omega$, where ω is the frequency of our probe.

Figure 3 displays the capacitance-voltage graph of a p-type metal-oxide semiconductor. The capacitance is constant when gate voltage is negative, then falls at the *flat-band voltage* $V_{GS} = 0V$, then rapidly rises again after the threshold voltage is reached.

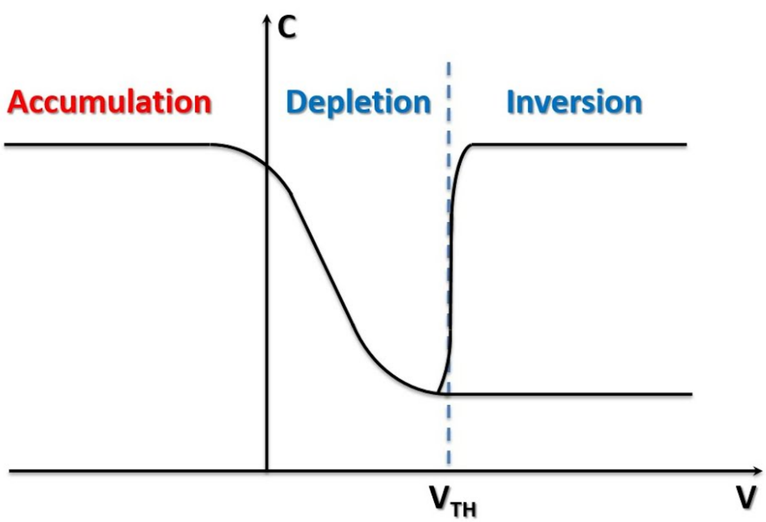

Figure 3: p-type MOS capacitance-voltage characteristic

The resistivity of the inversion channel created by the gate's bias is given by

$$\frac{1}{\rho} = (n\mu_e + p\mu_h)q \tag{3}$$

where n is the concentration of electrons, p is the concentration of holes, μ_e is the mobility of electrons, μ_h is the mobility of holes, and q is the charge of an electron. The higher the gate voltage, the higher the current between source and drain. Below the threshold voltage there is no current flow because no channel is formed. This relationship is linear provided the drain voltage is less than 150 mV, but above 0.3 V becomes nonlinear. That's because the channel is no longer a regular shape, but narrows in the region of the drain. Below 150 mV, however, this distortion can be assumed negligible. Recall that

$$R = \frac{\rho L}{A} \tag{4}$$

Whereas for small v_{DS} the area is almost constant, when $v_{DS} > 0.15V$ the area A decreases enough that the resistance R is significantly increased. When the area has decreased to zero at the drain, we reach the *pinch-off* and the drain voltage is at saturation $v_{DS(sat)}$. The current still flows constantly for all drain voltage above saturation, however. Before saturation is reached and after the gate voltage is above the threshold, we are in the triode region. In the triode region, the current is given by

$$i_{D(triode)} = \mu C_{ox}\frac{W}{L}((v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}) \tag{5}$$

Sometimes, the constant terms are wrapped up into one constant, like so:

$$i_{D(triode)} = k_n((v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2}) \tag{6}$$

In the saturation region,

$$\begin{aligned} i_{D(sat)} &= \mu C_{ox}\frac{W}{L}\frac{(v_{GS} - V_T)^2}{2} && (7) \\ &= k_n\frac{v_{DS(sat)}^2}{2} && (8) \end{aligned}$$

When we are far away from saturation, the resistance of the channel is given by

$$\begin{aligned} R_{on} &= \frac{\partial v_{DS}}{\partial i_D} && (9) \\ &= \frac{1}{\mu C_{ox}\frac{W}{L}(v_{GS} - V_T)} && (10) \end{aligned}$$

Figure 4 shows a family of i_D-v_{DS} curves with differing values of v_{GS}. Also show as a dashed green line is the saturation current as a function of gate voltage. Let's look at the impact the threshold voltage has by plotting the i_D-v_{GS} curve for differing values of V_T in figure 5. Now the green dashed curve corresponds to a threshold voltage of

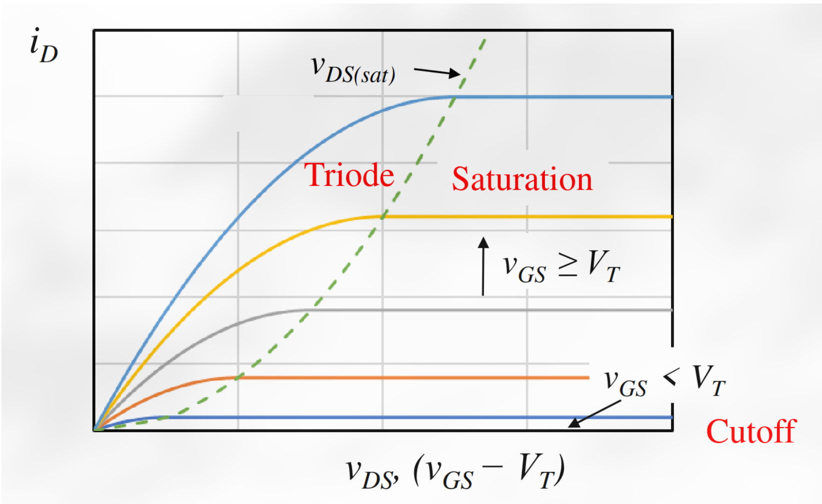

Figure 4: Transfer characteristics of nMOSFETs

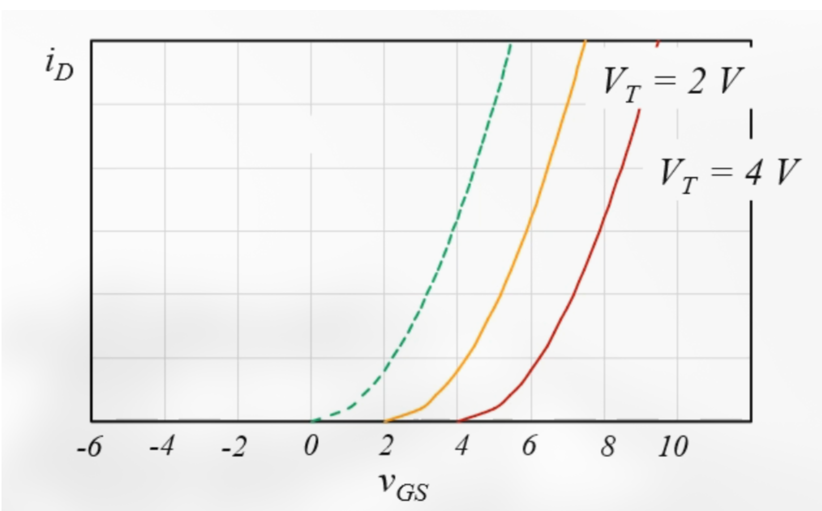

Figure 5: i_D-v_{GS} curve for select values of V_T

zero. Recall that the threshold voltage is intrinsic to the semiconductor wafer. Doping variations, defect, and shape can all affect the threshold voltage. If we build a depletion-mode nMOSFET, then we allow for negative threshold voltages.

A normally off like in figure 1 has the symbol shown in 6 and is said to be in enhancement mode. If the nMOSFET has an n-channel

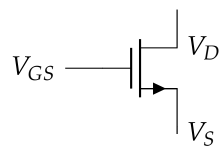

Figure 6: nMOSFET schematic

between the source and drain, as shown in figure 7, then it is normally

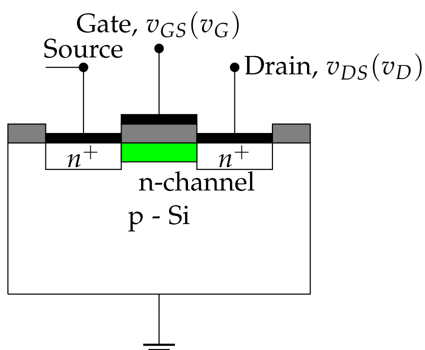

Figure 7: Normally on nMOSFET diagram

on and its symbol is as seen in figure 8. This kind of nMOSFET is said to be in depletion mode. Note the thicker line between source and

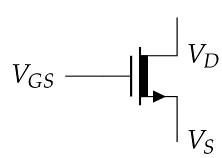

Figure 8: Schematic of normally on nMOSFET

drain representing the n-channel.

Similarly, the pMOSFET shown in figure 2 is a normally off, enhancement mode pMOSFET. A pMOSFET with a p-channel is normally on and in depletion mode.

Let's look at the transfer characteristics of the different types of MOSFETs. figure 4 shows these characteristics for a normally off, enhancement mode nMOSFET. For a normally on, depletion mode nMOSFET the graph is exactly the same, except that the current can flow even when the gate bias is zero since the fabricated channel allows the flow of electrons from source to drain. The output characteristics for a normally off, enhancement mode pMOSFET are shown in figure 9. A negative bias on the gate will induce a channel of pos-

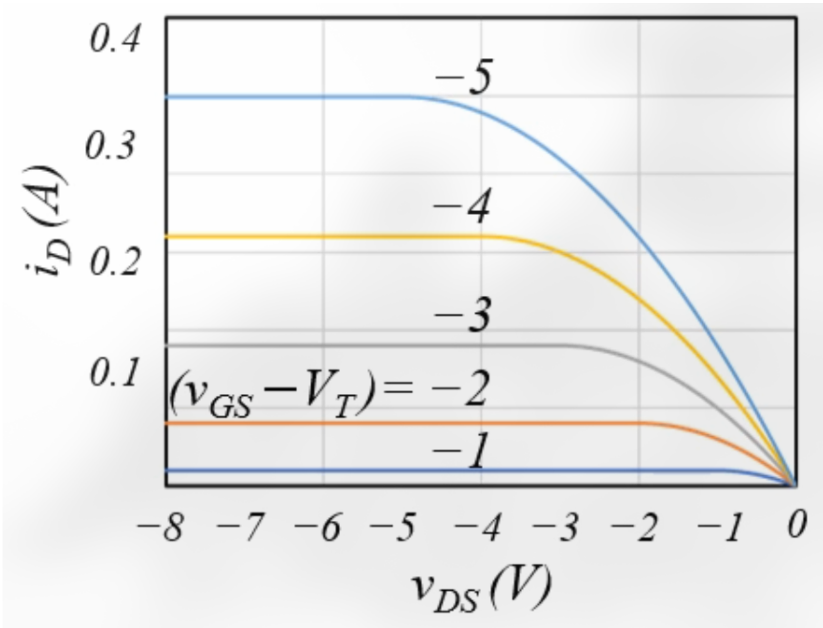

Figure 9: i_D-v_{DS} curve for select values of $v_{GS} - V_T$

itive holes in the semiconductor, making the threshold voltage for a pMOSFET negative. Again, the normally on depletion mode pMOSFET graph has the same shape, but since there is an existing channel for current it will flow even for some positive values of v_{GS}. We need to deplete the channel by pushing away all the holes in it with the bias on the gate in order to turn it off.

To review, there for four kinds of MOSFETs in which we are interested:

- normally off, enhancement mode nMOSFETs
- normally on, depletion mode nMOSFETs
- normally off, enhancement mode pMOSFETs
- normally on, depletion mode pMOSFETs

Transconductance

Now, let us move on the the topic of transconductance. In the triode region, the transconductance is defined as

$$g_m = \frac{i_D}{v_{GS}}|_{Q_{pt}} \tag{11}$$

where

$$Q_{pt} = (I_D, V_{DS}). \tag{12}$$

If we recall equation 5, and substitute for i_D in equation 11, then we obtain

$$g_m = \mu C_{ox} \frac{W}{L} v_{DS} \tag{13}$$

$$= \frac{i_{D(triode)}}{(v_{GS} - v_T) - \frac{v_{DS}}{2}} \tag{14}$$

In the saturation region,

$$g_m = \frac{di_D}{dv_{GS}}|_{Q_{pt}} \tag{15}$$

and

$$i_{D(sat)} = \mu C_{ox} \frac{W}{L} \frac{(v_{GS} - V_T)^2}{2}. \tag{16}$$

Again combining these two equations,

$$g_m = \mu C_{ox} \frac{W}{L} (v_{GS} - V_T) \tag{17}$$

$$= \frac{2 i_{D(sat)}}{(v_{GS} - V_T)} \tag{18}$$

The larger the transconductance, the larger the gain of an amplifier circuit that uses the transistor.

Channel length modulation

By adjusting the voltage of the drain, we can modulate the channel length. Specifically,

$$i_{D(sat)} \propto \frac{1}{L - \Delta L} \tag{19}$$

$$\equiv \frac{1}{L} \left(1 + \frac{\Delta L}{L}\right). \tag{20}$$

And

$$\Delta L \propto (v_{DS} - v_{DS(sat)}) \tag{21}$$

means that

$$i_{D(sat)} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (v_{GS} - V_T)^2 \left[1 + \lambda (v_{DS} - v_{DS(sat)})\right] \tag{22}$$

where λ is the empirically determined channel length modulation parameter. The output resistance at the drain is given by

$$r_0 = \left[\frac{\partial i_{D(sat)}}{\partial v_{DS}}\right]^{-1} \tag{23}$$

$$= \left[\lambda \frac{1}{2} k_n (v_{GS} - V_T)^2\right]^{-1} \tag{24}$$

$$= \frac{1}{\lambda I_{D(sat)}} \tag{25}$$

$$\approx \frac{V_A}{I_{D(sat)}} \tag{26}$$

Channel length modulation is not important when channel length is relatively large, but it is important on modern transistors where are on the order of nanometers.

MOSFETs in DC circuits

Consider a circuit with two enhancement mode pMOSFETs. Notice

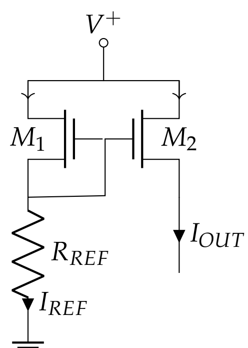

Figure 10: MOSFET DC circuit

that in figure 10, the drain of M_1 is directly attached to the gate. From this we have

$$v_{DS1} = v_{GS1} \tag{27}$$

$$= v_{GS2} \tag{28}$$

We are told M_1 is in saturation. If these are two identical transistors, then

$$I_{REF} = I_{D(sat)} \tag{29}$$

$$= \frac{1}{2} k_{p1} (v_{GS1} - V_{T1})^2 \tag{30}$$

$$= I_{OUT}. \tag{31}$$

From this, we learn that the reference current is mirrored by the drain current if $k_{p1} = k_{p2}$ and $v_{GS1} = v_{GS2}$.

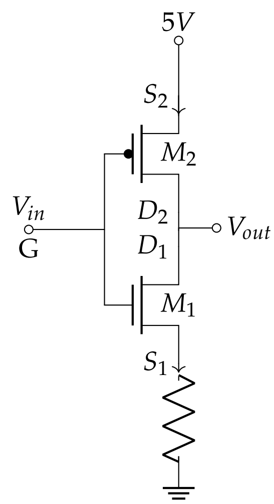

Figure 11: Inverter

Let us now look at the inverter shown in figure 11. Let's try to find V_{out} for $V_{in} = 0V$ and $V_{in} = 5V$. We are told that $V_{T(M1)} = 1V$ and $V_{T(M2)} = -1V$, because M1 is an enhancement mode nMOSFET and M2 is an enhancement mode pMOSFET. When $V_{in} = 0V$, M1 is off because $v_{GS1} < V_{T(M1)}$. Likewise, M2 is on because $v_{GS2} < V_{T(M2)}$ (recall that M2 is a pMOSFET). Since M1 is off, no current flows and $V_{out} = 5V$. For $V_{in} = 5V$, M1 flips on while M2 is off. Since M2 is off, no current flows. That means that $V_{out} = 5V$.

Transistors as amplifiers

The circuit shown in figure 12 has both AC and DC voltage sources.

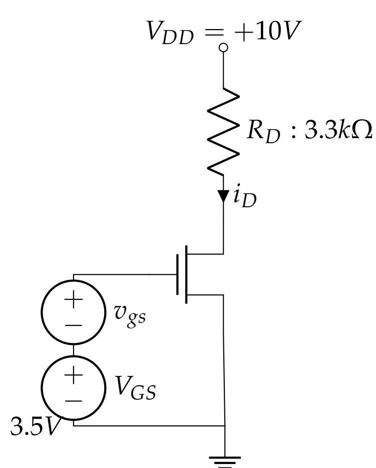

Figure 12: Common-source nMOSFET amplifier circuit

The source labelled by V_{GS}, all caps, is the DC voltage. The source v_{gs}, all lowercase, is the AC. This is not to be confused with v_{GS}, the total gate bias. The mix of cases indicates we have both AC and DC bias in consideration. The cool thing about this circuit is a small oscillation in the AC input induces a much larger oscillation in the output, hence calling it an amplifier. The output signal is going to be phase shifted by 180°. We can calculate the gain with eq. 32

$$A_v = \frac{v_{ds}}{v_{gs}} \tag{32}$$

In this instance,

$$\begin{aligned} A_v &= \frac{v_{ds}}{v_{gs}} && (33) \\ &= \frac{4.17\angle 180^\circ}{1\angle 0^\circ} && (34) \\ &= -4.17 && (35) \end{aligned}$$

This gain, however, will be somewhat distorted. To reduce distortion we need that $|v_{gs}| << 2(V_{GS} - V_T)$. The exact value of the "much less" symbol $<<$ will depend on the application, but it's common to require $|v_{gs}| < 0.2(V_{GS} - V_T)$. If we assume the small signal condition and no channel length modulation, then the transconductance of the amplifier is

$$g_m = \sqrt{2k_n I_{D(sat)}} \tag{36}$$

Figure 13 shows the small signal equivalent circuit of a common source amplifier. Notice the two voltage sources, one AC signal and

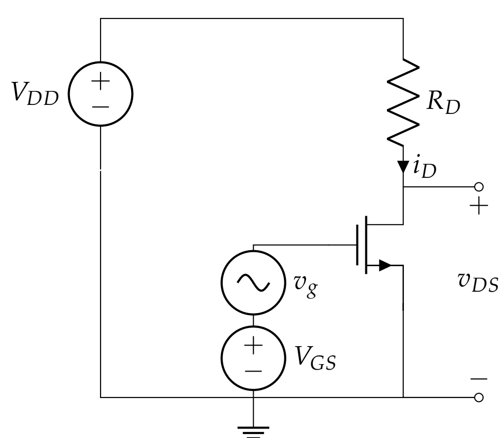

Figure 13: Small signal equivalent circuit

one DC bias at the gate. The total input signal is given by

$$\begin{aligned} v_{GS}(t) &= v_{gs}(t) + V_{GS} && (37) \\ v_{DS}(t) &= v_{ds}(t) + V_{DS} && (38) \end{aligned}$$

The drain current for such a circuit when channel length modulation is accounted for is given by

$$\begin{aligned} i_{D(clm)} &= \frac{1}{2}k_n\left[v_{gs}^2 + 2(V_{GS} - V_T)v_{gs} + (V_{GS} - V_T)^2\right] \\ &\times \left[1 + \lambda(V_{DS} - (V_{GS} - V_T)) + \lambda(v_{ds} - v_{gs})\right] \end{aligned}$$

When channel length modulation can be ignored, the current reduces to

$$i_{D(sat)} = \frac{1}{2}k_n\left[v_{gs}^2 + 2(V_{GS} - V_T)v_{gs} + (V_{GS} - V_T)^2\right] \tag{39}$$

For finite output resistance r_0,

$$\begin{aligned} \frac{1}{r_0} &= \left[\frac{\partial i_{D(clm)}}{\partial v_{DS}}\right] && (40) \\ &= \frac{\partial}{\partial v_{DS}}\left\{\frac{k_n}{2}(v_{GS} - V_T)^2\left[1 + \lambda(v_{DS} - v_{DS(sat)})\right]\right\} && (41) \\ &= \frac{k_n}{2}(v_{GS} - V_T)^2\frac{\partial}{\partial v_{DS}}\left[1 + \lambda(v_{DS} - v_{DS(sat)})\right] && (42) \\ &= \lambda\frac{k_n}{2}(v_{GS} - V_T)^2 && (43) \\ &= \lambda I_{D(sat)}. && (44) \end{aligned}$$

We then define the *intrinsic voltage gain of a MOSFET* as

$$\begin{aligned} \mu_f &= g_m r_0 && (45) \\ &= \sqrt{2k_n I_{D(sat)}}\left(\frac{1}{\lambda I_{D(sat)}}\right) && (46) \\ &= \frac{1}{\lambda}\sqrt{\frac{2k_n}{I_{D(sat)}}} && (47) \end{aligned}$$

We can greatly simplify circuit analysis by breaking the circuit up into AC and DC. To find the DC equivalent circuit, follow these steps:

1. Replace all capacitors with open circuits
2. Replace all inductors with short circuits
3. Deactivate AC sources
4. Find the Q-point using the DC equivalent circuit

To find the AC equivalent circuit,

1. Replace all capacitors with short circuits at operational frequency
2. Replace all inductors with open circuits at operational frequency
3. Deactivate DC voltages and replace with short circuits
4. Deactivate DC current sources and replace with open circuits
5. Replace the transistor with its small-signal model

Amplifier topologies

There are three different nMOSFET amplifier topologies we will consider in this class, starting with the common-source amplifier shown in figure 14. The common-source amplifier's input is taken

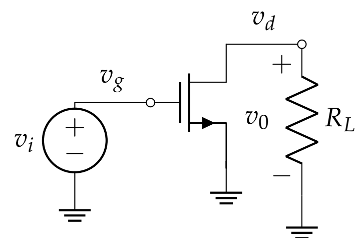

Figure 14: Common-source amplifier

through the gate, the output is taken through the drain, and the terminal that is common to output and input is the source.

The second topology is the common-gate amplifier shown in figure 15. Here we see that the AC voltage source is applied to the source,

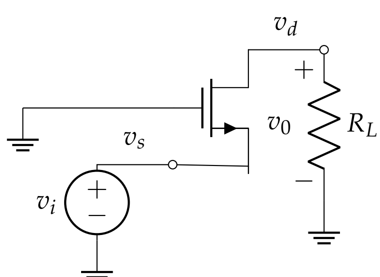

Figure 15: Common-gate amplifier

while the output is taken at the drain and the common terminal is at the gate.

The previous two amplifiers suggest a third, the common-drain amplifier in figure 16. As may be expected, here the common terminal

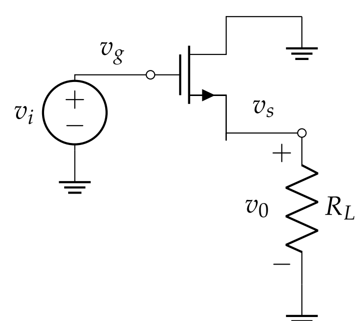

Figure 16: Common-drain amplifier

is the drain, the input is at the gate, and the output is at the source.

You may be thinking: "what happens if the input and output are swapped? Will the circuit still work as an amplifier?" No.

The voltage gain in a common-drain amplifier is given by

$$A_V = \frac{g_m R_L'}{1 + g_m R_L'} \left(\frac{R_G}{R_I + R_G} \right) \tag{48}$$

where $R_L' = (r_0||R_6||R_3)$. For a MOSFET where $r_0 >> R_L$,

$$A_V \approx \frac{R_G}{R_I + R_G} \tag{49}$$

When this is true, the MOSFET is acting as a *voltage follower*.

Figure 17 shows the small-signal model for an nMOSFET called a hybrid-pi model. This model is excellent for common-source and common-drain amplifiers. For the common-gate amplifier, the alternative T-model shown in figure 18 is more useful. The voltage gain in a common-gate amplifier is given by

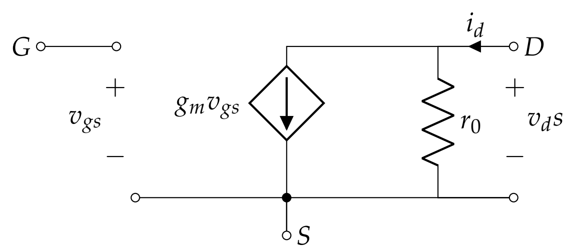

Figure 17: Hybrid-pi model

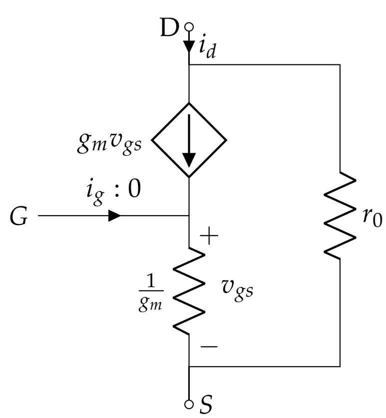

Figure 18: T-model

$$A_V = \frac{g_m R_L}{1 + g_m (R_I||R_6)} \left(\frac{R_6}{R_I + R_6} \right) \tag{50}$$

Let's recap our three kinds of amplifiers. For the inverting common-source amplifier,

$$A_V = -\frac{g_m R_L}{1 + g_m R_S} \left(\frac{R_G}{R_I + R_G} \right). \tag{51}$$

Additionally,

$$R_{in} = \infty \tag{52}$$
$$R_{out} = R_L \tag{53}$$

For the non-inverting common-gate amplifier,

$$A_V = \frac{g_m R_L}{1 + g_m(R_I||R_6)} \left(\frac{R_6}{R_I + R_6} \right) \tag{54}$$

with

$$R_{in} = \frac{1}{g_m} \tag{55}$$
$$R_{out} = R_L \tag{56}$$

For the follower common-drain amplifier,

$$A_V = \frac{g_m R_L}{1 + g_m R_L} \left(\frac{R_G}{R_I + R_G} \right) \tag{57}$$
$$\approx \left(\frac{R_G}{R_I + R_G} \right). \tag{58}$$

Here,

$$R_{in} = \infty \tag{59}$$
$$R_{out} = \frac{1}{g_m} \tag{60}$$

Frequency range for FET amplifiers

The *lower-frequency cutoff* for an amplifier circuit is defined as the ω_L where the gain A_V is $\frac{1}{\sqrt{2}}$ the maximum gain. We are told that

$$\omega_L = \frac{1}{\tau} \tag{61}$$
$$= \frac{1}{r_{eq}C}. \tag{62}$$

If there are multiple capacitors in the circuit, find r_{eq} for each, calculate all possible values of ω_L, and pick the largest. The *higher-frequency cutoff* ω_H is also defined as the frequency where the gain A_V is $\frac{1}{\sqrt{2}}$ the maximum gain, but the higher of the two values. For a common-source amplifier,

$$\omega_H = \frac{1}{(R_S||R_1||R_2)C_{gs}} \tag{63}$$

The bandwidth of useable frequencies is $\omega_H - \omega_L$.

The higher-cutoff frequency is defined by capacitors within the amplifier circuit, C_{gs} and C_{gd}. We do not explore this relation within

C_{gs} is the capacitance between the gate and channel at a point nearer the source, while C_{gd} is the same but for a point nearer the drain.

this course. However, we are told the following equations are valid in the triode region:

$$C_{gc} = WLC_{ox} \tag{64}$$

$$C_{gd} = \frac{C_{gc}}{2} + C_{gdo}X_{do} \tag{65}$$

$$C_{gs} = \frac{C_{gc}}{2} + C_{gso}X_{so} \tag{66}$$

In the saturation region,

C_{gso} is the capacitance of oxide overlapping source, C_{gdo} is the capacitance of oxide overlapping drain, X_{so} is the length of oxide overlap on source, and X_{do} is the length of oxide overlap on drain.

$$C_{gd} = C_{gdo}X_{do} \tag{67}$$

$$C_{gs} = \frac{2}{3}C_{gc} + C_{gso}X_{so} \tag{68}$$

Typically C_{gd} is so much smaller than C_{gs} as to be insignificant.

The maximum useful linear frequency of a transistor is

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gc}} \tag{69}$$

$$= \frac{1}{2\pi}\frac{\mu}{L^2}(v_{gs} - V_T) \tag{70}$$

In addition to the intrinsic capacitances C_{ox} and C_d, there are also parasitic capacitances. The junction capacitance C_J forms between the source/drain and the semiconductor, while the overlap capacitance C_{ov} forms between the source/drain and the metal contact on the gate.

Reference

Region	Conditions
Cut-off	$v_{GS} < V_T$
Triode	$v_{DS} \leq v_{DS(sat)}$
Saturation	$v_{DS} > v_{DS(sat)}$

Figure 19: nMOSFET regions of operation

Region	Conditions
Cut-off	$v_{GS} > V_T$
Triode	$v_{DS} \geq v_{DS(sat)}$
Saturation	$v_{DS} < v_{DS(sat)}$

Figure 20: pMOSFET regions of operation

	nMOSFET	pMOSFET
Cutoff	$v_{GS} < 0$	$v_{GS} > 0$
Triode	$v_{GS} > 0$	$v_{GS} < 0$
Saturation	$v_{GS} > 0$	$v_{GS} < 0$
Enhancement	$V_T > 0$	$V_T < 0$
Depletion	$V_T < 0$	$V_T > 0$

Figure 21: Differences between pMOSFET and nMOSFET

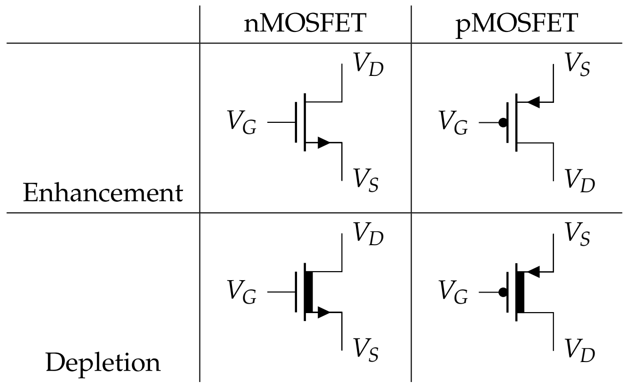

Figure 22: MOSFET schema

Equation	Condition	Reference
$v_{DS(sat)} = v_{GS} - V_T$	MOSFET	
$i_{D(cutoff)} = 0$	MOSFET	
$i_{D(triode)} = \mu C_{ox}\frac{W}{L}((v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2})$ $= k_n((v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2})$ $= \frac{k_n}{2}(2v_{DS(sat)} - v_{DS})v_{DS}$	MOSFET	eq. 5
$i_{D(sat)} = \mu C_{ox}\frac{W}{L}\frac{(v_{GS}-V_T)^2}{2}$ $= k_n\frac{v_{DS(sat)}^2}{2}$	MOSFET	eq. 7
$A_v = \frac{v_{out}}{v_{in}}$	Amplifying transistor	eq. 32
$g_m = \sqrt{2k_n I_{D(sat)}}$	Amplifying transistor	eq. 36
$i_{D(clm)} = \frac{1}{2}k_n\left[v_{gs}^2 + 2(V_{GS} - V_T)v_{gs} + (V_{GS} - V_T)^2\right]$ $\times\left[1 + \lambda(V_{DS} - (V_{GS} - V_T)) + \lambda(v_{ds} - v_{gs})\right]$	CLM active	eq. 39
$\omega_L = \frac{1}{\tau}$ $= \frac{1}{r_{eq}C}$	Amplifier	eq. 61
$\omega_H = \frac{1}{(R_S\|\|R_1\|\|R_2)C_{gs}}$	Common-source amplifier	eq. 63

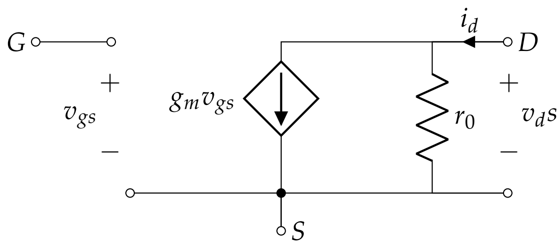

Figure 23: Hybrid-pi model

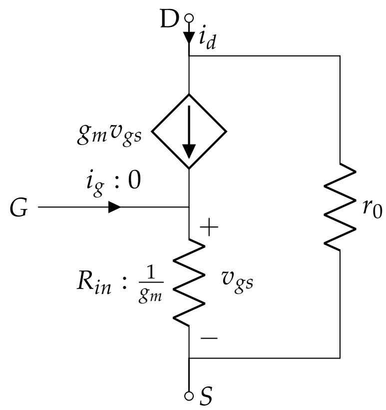

Figure 24: T-model

Operational Amplifier

The *operational amplifier* (op-amp) is a high voltage gain amplifier with a differential input. It can perform mathematical operations, but it's also commonly used in industrial and consumer products. On any op-amp pinout are eight terminals:

1. offset null
2. inverting input
3. noninverting input
4. negative power supply
5. offset null
6. output
7. positive power supply
8. no connection

The symbol for an op-amp is given in figure 25. We have a potential at the inverting terminal of v_-, and a potential at the noninverting terminal of v_+. V_- and V_+ are the negative and positive power supplies,

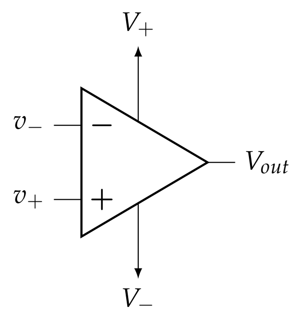

Figure 25: amplifier symbol

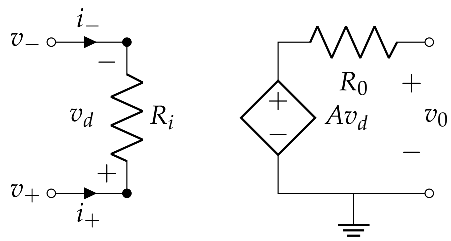

Figure 26: amplifier model

respectively. We can model the op-amp as in figure 26. The open-loop gain A is typically $O(10^4)$, but can be higher or lower. The input signal is voltage, not current, so we typically make R_i large to avoid loss of signal. The maximum and minimum possible voltages are clipped to V_+ and V_-, respectively.

In an ideal op-amp, $A = \infty$ and R_i is also ∞.

Consider the feedback loop shown in figure 27. Here, $x_o = Ax_i$

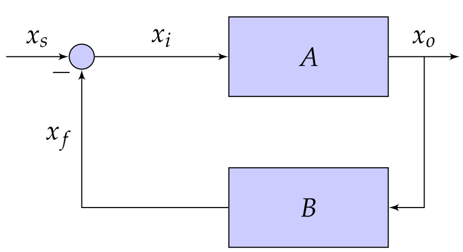

Figure 27: Feedback loop

and $x_f = Bx_o$. At the summing circle, the feedback x_f is subtracted from x_s to yield x_i: $x_i = x_s - x_f$. We define the closed-loop gain as

$$A_f = \frac{x_o}{x_s} \tag{71}$$

$$= \frac{A}{1 + AB} \tag{72}$$

The product AB is the *loop gain*, and $1 + AB$ is the *amount of feedback*. When $AB >> 1$, $A_f \approx \frac{1}{B}$. Consider the inverting op-amp shown in figure 28. Because the potential of the noninverting and inverting

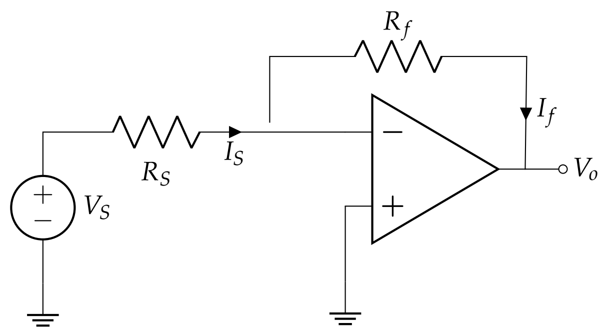

Figure 28: Inverting op-amp

terminals of an op-amp are equal, we know that $V_- = 0$. Ergo,

$$I_S = \frac{V_S}{R_S} \tag{73}$$

With a little more algebra that makes a useful exercise for the reader, we obtain

$$A_f = -\frac{R_f}{R_S} \tag{74}$$

Hence why this setup is called an inverting op-amp.

Reference

Ideal op-amp features:

- $v_+ = v_-$
- $A = \infty$
- $R_o = 0$
- $i_- = i_+ = 0$

Circuit Analysis

Differential Equations

An important function in circuit analysis is the exponential function

$$e^x = \sum_{k=0}^{\infty} \frac{x^k}{k!} \tag{75}$$

Any function can be expressed as a linear combination of exponential functions. Recall also that $\int e^x dx = e^x + C$ and $\frac{d}{dx}e^x = e^x$. An *ordinary differential equation* (ODE) is given by

$$y(t) = \sum_{k=0}^{n} A_k \frac{d^k x(t)}{dt^k} \tag{76}$$

$y(t)$ is the forcing function, our objective is to find $x(t)$ that matches $y(t)$. The process for this is to first solve the specific case when $y(t) = 0$, the homogeneous ODE. We then find the particular solution that matches $y(t)$. In the case of exponential circuit analysis, the homogeneous case corresponds to analyzing our circuit absent any excitations from forcing functions. To make this clear, we want to solve

$$0 = \sum_{k=0}^{n} A_k \frac{d^k x(t)}{dt^k}. \tag{77}$$

We assume a solution of the form

$$x_h(t) = Ae^{\lambda t}. \tag{78}$$

Let's consider an example. Say

$$y(t) = 2x(t) + 3\frac{dx(t)}{dt}. \tag{79}$$

We take

$$0 = 2x_h(t) + 3\frac{dx_h(t)}{dt}. \tag{80}$$

If $x_h(t) = Ae^{\lambda t}$, then

$$0 = 2Ae^{\lambda t} + 3A\lambda e^{\lambda t}. \tag{81}$$

Cancelling out $Ae^{\lambda t}$ from both sides, we obtain

$$0 = 2 + 3\lambda. \tag{82}$$

This is the *characteristic equation* of the circuit. Solving this characteristic equation will provide the *natural frequency* λ for the homogeneous ODE solution. Returning to our example, say $y(t) = 4e^{-t}$. We can reasonably assume that $x_p(t) = Be^{-t}$. Plugging this in, we find that

λ is called the natural frequency because it's what we get without any external excitation.

$$y(t) = 2x(t) + 3\frac{dx(t)}{dt} \tag{83}$$

$$4e^{-t} = 2Be^{-t} + 3(-1)Be^{-t} \tag{84}$$

$$B = -4 x_p(t) = -4e^{-t}. \tag{85}$$

The complete solution is the superposition of the homogeneous and particular solutions,

$$x(t) = x_h(t) + x_p(t). \tag{86}$$

Recall that although we found λ for the homogenous solution, we have not yet found A. To do so we require an initial condition. Say in this case the initial condition is given as $x(0) = 2$. Then

$$x(0) = 2 \tag{87}$$

$$= -4e^0 + Ae^0 \tag{88}$$

$$A = 6. \tag{89}$$

So the complete solution becomes

$$x(t) = -4r^{-t} + 6e^{-\frac{2}{3}t} \tag{90}$$

RC and RL Circuits

This isn't a differential equations class, this is a circuits class. The reason we care about ODEs is because they arise in circuits. For example, consider the circuit in figure 29. Remember that

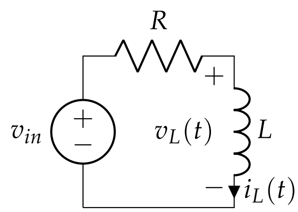

Figure 29: RL circuit

$$v_L = L\frac{di_L(t)}{dt}. \tag{91}$$

Via KVL, we have that

$$v_{in}(t) = v_L(t) + Ri_L(t). \tag{92}$$

Putting the two together,

$$v_{in}(t) = L\frac{di_L(t)}{dt} + Ri_L(t). \tag{93}$$

This is a first-order ODE. Solving it is left as an exercise to the reader. A similar process applies to the RC circuit shown in figure 30. In both

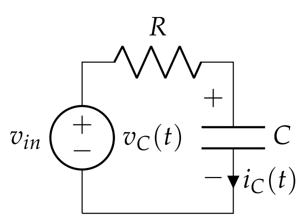

Figure 30: RC circuit

the RC and RL cases, solving the ODE will yield the formulas for $v_C(t)$ and $v_L(t)$ with which we are familiar from ECE 20001.

Note that both the inductor and capacitor are non-ideal elements, and if we are to accurately model circuits we must account for this. Specifically, inductors behave non-ideally in the following ways:

- The wire that makes up the coil of the inductor has intrinsic resistance
- The spacing between the wire has intrinsic capacitance
- Hysteresis or eddy currents in the ferrite core have intrinsic resistance

Capacitors have the following non-idea characteristics:

- The wire connected to the capacitor has intrinsic inductance
- The wire connected to the capacitor has intrinsic resistance
- The insulating dielectric between the plates of the capacitor has a large but finite resistance, and leakage current can therefore flow from one plate to another

The inductor is less ideal than the capacitor, since it necessarily has more non-ideal components than the capacitor. Therefore, for the capacitor, we can comfortably neglect the effects of the non-ideal wire. Figures 31 and 32 show the non-ideal models for inductor and capacitor used in this course.

In real life, the effects of the wire can be minimized by using chip capacitors, which have very short wires.

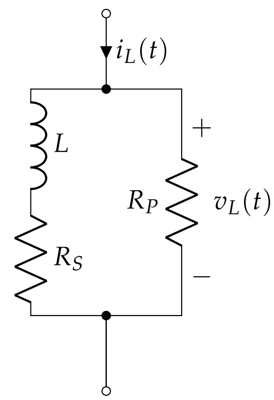

Figure 31: Non-ideal inductor

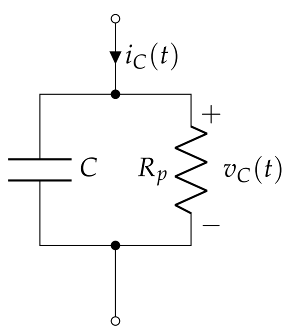

Figure 32: Non-ideal capacitor

Switched Circuits

The current through an inductor is continuous, even when the voltage across it is not. Likewise, voltage across a capacitor is continuous even if current is not. Recall from ECE 20001 that the time it takes a variable of interest, inductor current or capacitor voltage, to go from $x(t_1)$ to $x(t_2)$ in its respective circuit is given by

$$t_2 - t_1 = \tau \ln\left(\frac{x(t_1) - x(\infty)}{x(t_2) - x(\infty)}\right). \tag{94}$$

If switched events are associated with $x(t)$, then eq. 94 can be used to find the time for which a certain circuit configuration is valid.

Consider the circuit in figure 33. We are told that the switch is

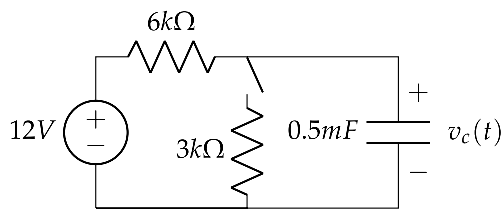

Figure 33: Switched circuit

initially open as shown and closes when $v_c(t) = 9V$. The switch opens again when $v_c(t) = 5V$. $v_c(0^+) = 0V$. We wish to find an expression for $v_c(t)$ from $t = 0$ to the third time the switch flips. Let's start by recalling the helpful equation in eq. 95.

$$x(t) = x(\infty) + [x(t_0) - x(\infty)]\, e^{-\left(\frac{t-t_0}{\tau}\right)} \tag{95}$$

Ergo,

$$v_c(t) = v_c(\infty) + [v_c(t_0) - v_c(\infty)]\, e^{-\left(\frac{t-t_0}{\tau}\right)} \tag{96}$$

For an RC circuit such as this one, $\tau = RC$.

$$v_c(t) = v_c(\infty) + [v_c(t_0) - v_c(\infty)]\, e^{-\left(\frac{t-t_0}{RC}\right)} \tag{97}$$

We know from our conditions that $v_c(t_0) = 0$, so eq. 97 simplifies to

$$v_c(t) = v_c(\infty) - v_c(\infty)e^{-\frac{t}{RC}} \tag{98}$$

In the open configuration, $v_c(\infty) = 12V$ and $R = 6k\Omega$. We know that, but our circuit from $t = 0$ until $v_c(t) = 9V$ doesn't. Therefore,

$$t_2 - t_1 = \tau \ln\left(\frac{x(t_1) - x(\infty)}{x(t_2) - x(\infty)}\right) \tag{99}$$

$$= \tau \ln\left(\frac{v_c(t_1) - v_c(\infty)}{v_c(t_2) - v_c(\infty)}\right) \tag{100}$$

$$t_2 = RC \ln\left(\frac{0 - 12}{9 - 12}\right) \tag{101}$$

$$= 3 \ln\left(\frac{-12}{-3}\right) \tag{102}$$

$$\approx 4.16 \tag{103}$$

and

$$v_c(t) = v_c(\infty) - v_c(\infty)e^{-\frac{t}{RC}} \tag{104}$$
$$= 12 - 12e^{-\frac{t}{3}} \tag{105}$$

Now, let's consider what happens after the switch closes. Now $R = 6k\Omega || 3k\Omega = 2k\Omega$, and $v_c(t) = 4V$. This time around, $v_c(t_0) = 9V$. We therefore have

$$t_2 - t_1 = \tau \ln\left(\frac{x(t_1) - x(\infty)}{x(t_2) - x(\infty)}\right) \tag{106}$$
$$t_2 - 4.16 = \ln\left(\frac{9-4}{5-4}\right) \tag{107}$$
$$t_2 \approx 4.16 + 1.61 \tag{108}$$
$$= 5.77 \tag{109}$$

and

$$v_c(t) = v_c(\infty) + [v_c(t_0) - v_c(\infty)]\, e^{-\left(\frac{t-t_0}{\tau}\right)} \tag{110}$$
$$= 4 + [9-4]\, e^{-\left(\frac{t-4.16}{1}\right)} \tag{111}$$
$$= 4 + 5e^{-(t-4.16)} \tag{112}$$

Finally, the switch opens again.

$$t_2 = 5.77 + 3\ln\left(\frac{5-12}{9-12}\right) \tag{113}$$
$$= 8.31 \tag{114}$$

and

$$v_c(t) = 12 - 7e^{\left(-\frac{t-5.77}{3}\right)} \tag{115}$$

Therefore, our complete function is

$$v_c(t) = \begin{cases} 0 & t \leq 0 \\ 12 - 12e^{-\frac{t}{3}} & 0 \leq t \leq 4.16 \\ 4 + 5e^{-(t-4.16)} & 4.16 \leq t \leq 5.77 \\ 12 - 7e^{\left(-\frac{t-5.77}{3}\right)} & 5.77 \leq t \leq 8.31 \end{cases}$$

Second-order Differential Equations

Consider the circuit shown in figure 34. By KVL, we see that

$$v_{in}(t) = v_C(t) + v_L(t) \tag{116}$$

and we also know, because i is the current through a capacitor,

$$i = C\frac{dv_C(t)}{dt} \tag{117}$$

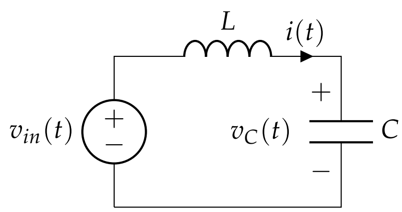

Figure 34: LC circuit

But wait! The voltage through the inductor is

$$
\begin{aligned}
v_L(t) &= L\frac{di(t)}{dt} && (118)\\
&= L\left(\frac{d}{dt}C\frac{dv_C(t)}{dt}\right) && (119)\\
&= LC\frac{d^2v_C(t)}{dt^2}. && (120)
\end{aligned}
$$

That means

$$v_{in}(t) = LC\frac{d^2v_C(t)}{dt^2} + v_C(t). \tag{121}$$

Yikes. This is a second order homogeneous equation. We can still solve it by assuming a homogenous solution of the form

$$v_{ch} = Ae^{\lambda t}, \tag{122}$$

But now substitution and cancellation yields

$$0 = LC\lambda^2 + 1 \tag{123}$$

as a characteristic equation, meaning

$$\lambda = \pm j\frac{1}{\sqrt{LC}}. \tag{124}$$

Well, this is no problem for us. To make things a little cleaner let's define $\omega_o = \frac{1}{\sqrt{LC}}$ as the *natural frequency* of the LC circuit. Now what we have for a homogenous equation is

$$v_{ch} = A_1e^{j\omega_o t} + A_2e^{-j\omega_o t} \tag{125}$$

Via Eurler's formula

$$e^{j\theta} = \cos(\theta) + j\sin(\theta), \tag{126}$$

we have that

$$v_{ch}(t) = A_1\left(\cos(\omega_o t) + j\sin\omega_o t\right) + A_2\left(\cos(-\omega_o t) + j\sin(-\omega_o t)\right). \tag{127}$$

It's incredible how often Euler's formula arises in the natural world, isn't it?

With a little bit of algebraic manipulation, we find

$$v_{ch}(t) = B_1\cos(\omega_o t) + B_2\sin(\omega_o t). \tag{128}$$

What that means for our circuit is that the capacitor's voltage will oscillate back and forth sinusoidally, which is a pretty cool result.

RLC circuits

Let's now introduce a resistor to the LC circuit. Consider figure 35, where resistor, inductor, and capacitor are in parallel. We can also

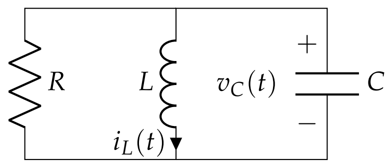

Figure 35: RLC parallel circuit

align the components in parallel, like in figure 36. In either case, the

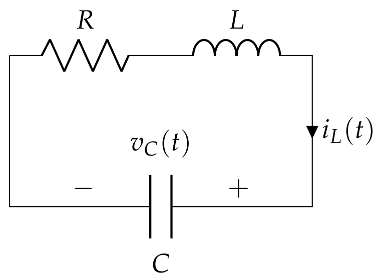

Figure 36: RLC series circuit

resistor dampens the sinusoidal response of the LC circuit. In the case of the parallel circuit of figure 35, as the resistance goes to infinity, the circuit starts to resemble just a plain LC circuit. In the case of the series circuit of 36, as the resistance goes to zero the circuit start to look more like an LC circuit. Deriving an ODE for both of these circuits is a wonderful exercise, give it a try and compare your result to the following expression.

$$F = \frac{d^2x(t)}{dt^2} + \frac{1}{\tau}\frac{dx(t)}{dt} + \frac{x(t)}{LC} \tag{129}$$

where $\tau = \frac{L}{R}$ for series RLC circuits and $\tau = RC$ for parallel. Finding the solution to the differential is another great exercise. Here is the characteristic equation:

Consider how R affects the differential equation in both the series and parallel cases.

$$0 = \lambda^2 + \frac{1}{\tau}\lambda + \frac{1}{LC} \tag{130}$$

and here is the general solution to the homogenous equation:

$$x_h(t) = A_1e^{\lambda_1 t} + A_2e^{\lambda_2 t} \tag{131}$$

Now the specific values of λ become very relevant, and give us three cases.

Case 1: λ real When λs are real and distinct, the circuit is *overdamped*. There is no oscillation, and the function simply goes to zero and stops.

Case 2: both λ identical When $\lambda_1 = \lambda_2$, the circuit is *critically damped*. The signal in the circuit decays exponentially to zero.

Case 3: λ complex When λ are complex, they will be conjugates of one another and the circuit is *underdamped*. If λ is imaginary, then the circuit has no dissipation and will oscillate forever. If $\lambda_1 = -\sigma_p \pm j\omega_d$ and $\lambda_2 = -\sigma_p \mp j\omega_d$, then we say σ_p is the attenuation factor and ω_p is the dampened resonance frequency.

Figure 37 shows each case plotted on the complex plane.

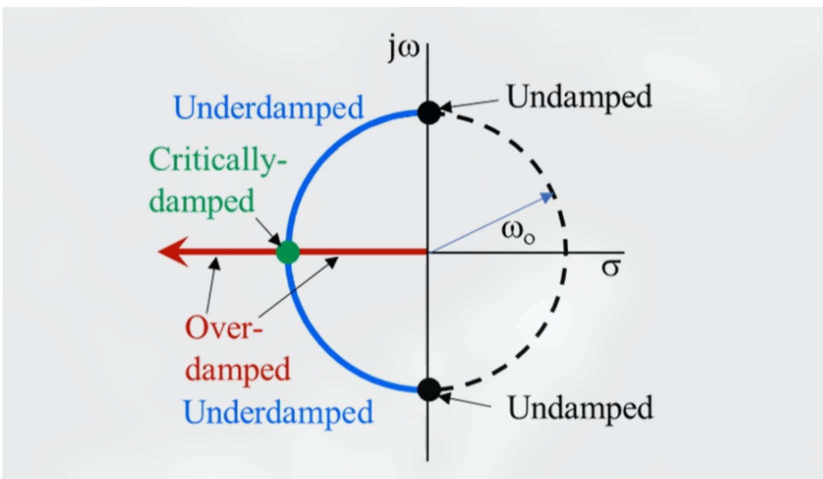

Figure 37: Damping cases on complex plane

Convolution

Given two functions, $f(t)$ and $g(t)$, their *convolution* is

$$f(t) * g(t) = \int_{-\infty}^{\infty} f(\tau)g(t-\tau)d\tau.$$

A notable property of the Dirac delta function $\delta(t)$ is that

$$f(t) * \delta(t) = \int_{-\infty}^{\infty} f(\tau)\delta(t-\tau)d\tau \quad (132)$$

$$= f(t) \quad (133)$$

Additionally,

$$f(t) * \delta(t-T) = \int_{-\infty}^{\infty} f(\tau)\delta(t-T-\tau)d\tau \quad (134)$$

$$= f(t-T) \quad (135)$$

It may seem a bit odd to convolve a function when you can just compute it, but soon we shall find examples where convolution is actually easier than finding the function $f(t)$, and then we will be glad for eqs. 132 and 134. If we convolve $f(t)u(t)$ with $u(t)$, we obtain

$$f(t)u(t) * u(t) = \int_{-\infty}^{\infty} f(\tau)\delta(\tau)u(t-\tau)d\tau \tag{136}$$

$$= \int_{0}^{t} f(\tau)d\tau \tag{137}$$

which is simply the integral of $f(t)$. Convolution is, as can be shown with a bit of elbow grease, commutative, associative, and distributive over addition.

Linear Time Invariant Systems

Again, however, this is an electrical engineering class, not a math class. How does this relate to circuits? For the purposes, of this class, it allows us to relate outputs to inputs using functions that describe a linear network. Specifically, we can model *linear time invariant* (LTI) systems, which produce output signals that are related to inputs in a linear and time invariant manner. Recall that linear means the differential equation has the form

$$b(x) = a_0(x)y + a_1(x)\frac{dy}{dx} + a_2\frac{d^2y}{dx^2} + \cdots + a_n(x)\frac{d^ny}{dx}.$$

The *degree* of this differential equation is n, but it's linear because $b(x)$ is a linear combination of derivatives of y. Likewise,

$$\frac{1}{L}\frac{dv_{in}(t)}{dt} = \frac{d^2i_L(t)}{dt^2} + \frac{R}{L}\frac{di_L(t)}{dt} + \frac{1}{LC}i_L(t)$$

is linear, even though its *order* is two. That's the linear part of linear time invariant. The time invariant part means that whether we apply an input to the system now or T seconds from now, the output will be identical except for a time delay of T seconds. That is, if the output due to input $x(t)$ is $y(t)$, then the output due to input $x(t-T)$ is $y(t-T)$. Hence, the system is time invariant because the output does not depend on the particular time the input is applied.

Suppose we have some LTI system, where the input is $x(t)$ and the output is $y(t)$. The relationship betwen them is given by $x(t) * h(t) = y(t)$. $h(t)$ is the *impulse response*. Consider the case of the RC circuit in figure 38. For convenience, let $R = 1\omega$ and $C = 1F$. Let the circuit also be at rest at $t_0 = 0$. We know that for an RC circuit,

$$v_c(t) = v_c(\infty) + [v_c(t_0) - v_c(\infty)]e^{-\frac{t-t_0}{RC}}$$

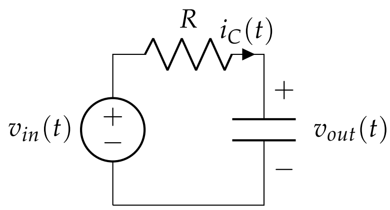

Figure 38: RC circuit as an LTI system

In this case, $v_C(t) = v_{out}(t)$, $v_{out}(t_0) = 0V$, and by inspection $v_C(\infty) = v_{in}(t)$. Our equation becomes

$$v_{out}(t) = v_{in}(t) - v_{in}(t)e^{-t}.$$

Let's let $v_{in}(t) = u(t)$. Then

$$u(t) = (1 - e^{-t})u(t).$$

If we differentiate both sides, then we have that

$$\begin{aligned}
\frac{d}{dt}u(t) &= \frac{d}{dt}u(t) - \frac{d}{dt}e^{-t}u(t) && (138)\\
\delta(t) &= \delta(t) - (e^{-t}\delta(t) - e^{-t}u(t)) && (139)\\
&= e^{-t}u(t) && (140)\\
&= h(t) && (141)
\end{aligned}$$

The response of the circuit to a Dirac impulse excitation is found by taking the time derivative of the unit-step response. That's important: the impulse response is the derivative of the step response.

Laplace Transformations

I don't know about you, but my idea of a good time isn't sitting down to solve integro-differential equations. Luckily there's a better way to solve circuits. If we can move from the time domain to the frequency domain our math gets a lot easier and we'll have time for more important things, such as literally anything else. Enter the one-sided *Laplace transform*. This is big kid math and you should be excited because it turns nasty differential equations into nice algebraic ones. Eq. 142 shows the guts of the Laplace transform.

$$\begin{aligned}
\mathcal{L}\left\{f(t)\right\} &= F(s) && (142)\\
&= \int_0^\infty f(t)e^{-st}dt && (143)
\end{aligned}$$

The Laplace transform turns a function of time t into a function of frequency s by integrating time away. Eq. 144 shows why that's useful.

$$\mathcal{L}\left\{\frac{d}{dt}f(t)\right\} = \int_0^\infty \frac{d}{dt}f(t)e^{-st}dt \tag{144}$$
$$= e^{-st}f(t)|_{t=0}^{\infty} - \int_0^\infty -sf(t)e^{-st}dt \tag{145}$$
$$= s\mathcal{L}\{f(t)\} - f(0) \tag{146}$$

Did you catch that? We transformed a differential equation into an algebraic one. With the help of a table like table 1, we can transform back into the time domain too.

Technically, you don't need a table. The inverse Laplace transform is defined as $\mathcal{L}^{-1}\{F(s)\}(t) = \frac{1}{2\pi i}\lim_{T\to\infty}\int_{\gamma-iT}^{\gamma+iT} e^{st}F(s)\,ds$, but like, gross.

Let's see this applied to a circuit. Say we have an RC circuit with $v_{in} = Au(t)$, where A is constant. We know that

$$RC\frac{d}{dt}v_C(t) + v_C(t) = Au(t).$$

While we could solve this with our ordinary differential methods, we're better than that now. Take the Laplace transform of both sides.

$$\mathcal{L}\left\{RC\frac{d}{dt}v_C(t) + v_C(t)\right\} = \mathcal{L}\{Au(t)\} \tag{147}$$
$$\mathcal{L}\left\{RC\frac{d}{dt}v_C(t)\right\} + \mathcal{L}\{v_C(t)\} = \mathcal{L}\{Au(t)\} \tag{148}$$
$$RC\left(sV_C(s) - v_C(0)\right) + V_C(t) = \frac{A}{s} \tag{149}$$
$$V_C(s) = \frac{A}{RC}\left(\frac{1}{s(s+\frac{1}{RC})}\right) + \frac{v_C(0)}{s+\frac{1}{RC}} \tag{150}$$
$$= \frac{A}{s} - \frac{A}{s+\frac{1}{RC}} + \frac{v_C(0)}{s+\frac{1}{RC}} \tag{151}$$
$$\mathcal{L}\{V_C(s)\} = \mathcal{L}\left\{\frac{A}{s} - \frac{A}{s+\frac{1}{RC}} + \frac{v_C(0)}{s+\frac{1}{RC}}\right\} \tag{152}$$
$$= \mathcal{L}\left\{\frac{A}{s}\right\} - \mathcal{L}\left\{\frac{A}{s+\frac{1}{RC}}\right\} + \mathcal{L}\left\{\frac{v_C(0)}{s+\frac{1}{RC}}\right\} \tag{153}$$
$$= A(1-e^{-\frac{t}{RC}})u(t) + v_C(0)e^{-\frac{t}{RC}}u(t) \tag{154}$$

Isn't that so much *easier*? In all seriousness, computers are much better at algebra than calculus, so it's methods like the Laplace transform that allow computational tools for solving circuits to exist.

Let's tie convolutions and Laplace transforms together now. Say we take the Laplace transform of two functions $f(t)$ and $g(t)$, both of which are 0 for $t < 0$. We can write them as $f(t)u(t)$ and $g(t)u(t)$, and we will. Now, the Laplace transform of their convolution is

$$\mathcal{L}\left\{f(t) * g(t)\right\} = \int_0^\infty \int_{-\infty}^\infty f(\tau)g(t-\tau)d\tau e^{-st}dt \tag{155}$$
$$= \int_0^\infty \int_{-\infty}^\infty f(\tau)u(t)g(t-\tau)d\tau e^{-st}dt \tag{156}$$
$$= \int_0^\infty \int_0^\infty f(\tau)g(t-\tau)d\tau e^{-st}dt \tag{157}$$
$$= \int_0^\infty f(\tau) \int_0^\infty g(t-\tau)e^{-st}dtd\tau \tag{158}$$
$$\lambda = t - \tau \tag{159}$$
$$\mathcal{L}\left\{f(t) * g(t)\right\} = \int_0^\infty f(\tau) \int_0^\infty g(\lambda)e^{-s(\lambda+\tau)}d\lambda d\tau \tag{160}$$
$$= \int_0^\infty f(\tau) \int_0^\infty g(\lambda)e^{-s\lambda}e^{-s\tau}d\lambda d\tau \tag{161}$$
$$= \int_0^\infty f(\tau)e^{-s\tau}d\tau \int_0^\infty g(\lambda)e^{-s\lambda}d\lambda \tag{162}$$
$$= F(s)G(s) \tag{163}$$

So convolution in the time domain corresponds to multiplication in the frequency domain.

Since computing the inverse Laplace is so unattractive, we generally seek a way to break our function into pieces so we can use a table lookup on each piece. A Laplace transform, can always be represented as

$$F(s) = \frac{a_0 + a_1 s + a_2 s^2 + \cdots + a_m s^m}{b_0 + b_1 s + b_2 s^2 + \cdots + b_n s^n},$$

where a_i, b_i are real and rational and $m \leq n$. Think about it, have you ever seen a Laplace transform where the numerator was a higher degree than the denominator? The reason we care about that is because it enables us to write our transform as

$$F(s) = A_0 + \frac{A_1}{s-p_1} + \frac{A_2}{s-p_2} + \cdots + \frac{A_m}{s-p_n}$$

using partial fraction expansion. Via the linearity of the Laplace transform, we can then change each individual addend back into its respective time-domain counterpart. We have three cases to consider.

Case 1: The denominator has real, distinct roots. In this case the transform can be expressed as

$$F(s) = \frac{a_0 + a_1 s + a_2 s^2 + \cdots + a_m s^m}{(s-p_1)(s-p_2)\ldots(s-p_n)} \tag{164}$$
$$= A_0 + \sum_{k=1}^{n} \frac{A_k}{s-p_k}. \tag{165}$$

To find any A_i, simply multiply both sides of eq. 164 by $(s - p_i)$.

You'll obtain

$$\frac{a_0 + a_1 s + a_2 s^2 + \cdots + a_m s^m}{(s-p_1)\ldots(s-p_{i-1})(s-p_{i+1})\ldots(s-p_n)} = (s-p_i)\left(A_0 + \sum_{k\neq i}^{n} \frac{A_k}{s-p_k}\right) + A_i \tag{166}$$

Then set s equal to p_i to obtain

$$\frac{a_0 + a_1 p_i + a_2 p_i^2 + \cdots + a_m p_i^m}{(p_i-p_1)\ldots(p_i-p_{i-1})(p_i-p_{i+1})\ldots(p_i-p_n)} = A_i. \tag{167}$$

Repeat for all p_i to find all A_i.

Case 2: The denominator has real, repeated roots. This would look something like

$$F(s) = \frac{a_0 + a_1 s + a_2 s^2 + \cdots + a_m s^m}{(s-p_1)(s-p_1)\ldots(s-p_n)} \tag{168}$$

$$= \frac{A_1}{s-p_1} + \frac{A_2}{(s-p_1)^2} + \sum_{k=3}^{n} \frac{A_k}{s-p_k}. \tag{169}$$

The same process as in case 1 will take care of this. To find A_2, multiply both sides of eq. 168 by $(s-p_1)^2$ and set $s = p_1$. Proceed as before.

Case 3: The denominator has complex roots. If you're unlucky, you'll have to write your Laplace transform as

$$F(s) = \frac{a_0 + a_1 s + a_2 s^2 + \cdots + a_m s^m}{((s+\sigma)^2 + \omega^2)\ldots(s-p_n)} \tag{170}$$

$$= \frac{a_0 + a_1 s + a_2 s^2 + \cdots + a_m s^m}{(s+\sigma+j\omega)(s+\sigma-j\omega)\ldots(s-p_n)} \tag{171}$$

$$= \frac{A_1 + jA_2}{s+\sigma+j\omega} + \frac{A_1 - jA_2}{s+\sigma-j\omega} + \text{real roots.} \tag{172}$$

In this case, find the real roots with whichever of the two previous cases is applicable and then multiply by $s+\sigma+j\omega$ and $s+\sigma+j\omega$ to solve for the imaginary roots.

Reference

Impedance, Admittance, and Zero-State Response

We're engineers. We're all about making things easier, so even though Laplace transforms have greatly simplified our differential equations, we'd still like to find an easier method to analyze linear circuits. That is precisely what impedance will allow us to do.

Let's think about the current-voltage relationships for our three major components.

Table 1: Laplace transforms

$f(t)$	$\mathcal{L}[f(t)] = F(s)$	
1	$\frac{1}{s}$	(1)
$e^{at}f(t)$	$F(s-a)$	(2)
$u(t-a)$	$\frac{e^{-as}}{s}$	(3)
$f(t-a)$	$e^{-sa}F(s)$	(4)
$\delta(t)$	1	(5)
$\delta(t-t_0)$	e^{-st_0}	(6)
$t^n f(t)$	$(-1)^n \frac{d^n F(s)}{ds^n}$	(7)
$f'(t)$	$sF(s) - f(0)$	(8)
$f^n(t)$	$s^n F(s) - s^{(n-1)} f(0) -$	
	$\cdots - f^{(n-1)}(0)$	(9)
$f(t) * g(t)$	$F(s)G(s)$	(10)
$t^n \ (n = 0, 1, 2, \ldots)$	$\frac{n!}{s^{n+1}}$	(11)
$t^x \ (x \geq -1 \in \mathbb{R})$	$\frac{\Gamma(x+1)}{s^{x+1}}$	(12)
$\sin kt$	$\frac{k}{s^2+k^2}$	(13)
$\cos kt$	$\frac{s}{s^2+k^2}$	(14)
e^{at}	$\frac{1}{s-a}$	(15)
$\sinh kt$	$\frac{k}{s^2-k^2}$	(16)
$\cosh kt$	$\frac{s}{s^2-k^2}$	(17)
$\frac{e^{at}-e^{bt}}{a-b}$	$\frac{1}{(s-a)(s-b)}$	(18)
$\frac{ae^{at}-be^{bt}}{a-b}$	$\frac{s}{(s-a)(s-b)}$	(19)
te^{at}	$\frac{1}{(s-a)^2}$	(20)

Resistors:

$$\mathcal{L}\left\{v_R(t) = Ri_R(t)\right\} = RI_R(s) \tag{173}$$

$$\mathcal{L}\left\{i_R(t) = Gv_R(t)\right\} = GV_R(s) \tag{174}$$

Inductors:

$$\mathcal{L}\left\{v_L(t) = L\frac{di_L(t)}{dt}\right\} = V_L(s) \tag{175}$$

$$= L\left(sI_L(s) - i_L(0)\right) \tag{176}$$

$$\mathcal{L}\left\{i_L(t) = \frac{1}{L}\int_{-\infty}^{t} v_L(\tau)d\tau\right\} = I_L(s) \tag{177}$$

$$= \frac{1}{L}\left(\frac{V_L(s)}{s} + \frac{\int_{-\infty}^{0} v_L(\tau)d\tau}{s}\right) \tag{178}$$

Capacitors:

$$\mathcal{L}\left\{v_c(t) = \frac{1}{C}\int_{-\infty}^{t} i_C(\tau)d\tau\right\} = V_C(s) \tag{179}$$

$$= \frac{1}{C}\left(\frac{I_C(s)}{s} + \frac{\int_{-\infty}^{0} i_C(\tau)d\tau}{s}\right) \tag{180}$$

$$\mathcal{L}\left\{i_c(t) = C\frac{dv_c(t)}{dt}\right\} = I_C(s) \tag{181}$$

$$= C\left(sV_C(s) - v_C(0)\right) \tag{182}$$

The *zero-state response* is the response of the circuit to external sources when its initial conditions are zero. If we have zero-state conditions, then

Resistors: $V_R(s) = RI_R(s)$

Inductors: $V_L(s) = sLI_L(s)$

Capacitors: $V_C(S) = \frac{I_C(s)}{sC}$

We can generalize the concept of resistance to the complex world by defining the impedance Z as

$$Z(s) = \frac{V(s)}{I(s)}.$$

That makes the impedance for each element

Resistors: $Z_R(s) = R$

Inductors: $Z_L(s) = sL$

Capacitors: $Z_C(s) = \frac{1}{sC}$

Under zero-state conditions, the current for each element is given by

Resistors: $I_R(s) = \frac{V_R(s)}{R}$

Inductors: $I_L(s) = \frac{V_L(s)}{sL}$

Capacitors: $I_C(s) = sCV_C(s)$

The admittances for each passive element are

Resistors: $Y_R(s) = \frac{1}{R}$

Inductors: $Y_L(s) = \frac{1}{sL}$

Capacitors: $Y_C(s) = sC$

The concepts of impedance and admittance are extremely attractive because they allow us to sidestep the use of differential equations and solve our circuits linearly. We can basically treat impedance in the frequency realm as we would resistance in the time realm. Here, let's have an example. In the frequency domain, figure 39 becomes 40.

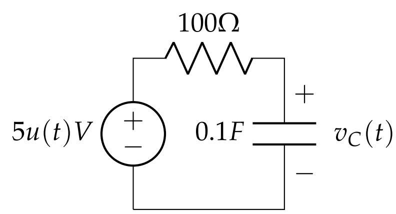

Figure 39: Time domain

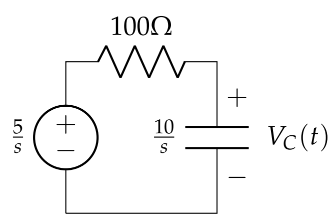

Figure 40: Frequency domain

Since we can treat impedance like resistance, let's do a simple voltage division to solve for $V_C(s)$ (and subsequently, $v_C(t)$).

$$V_C(s) = \frac{Z_C}{Z_C + Z_R} V_{in}(s) \tag{183}$$

$$= \frac{\frac{10}{s}}{\frac{10}{s} + 100} \frac{5}{s} \tag{184}$$

$$= \frac{5}{s(10s+1)} \tag{185}$$

$$= \frac{0.5}{s(s+\frac{1}{10})} \tag{186}$$

$$= \frac{A}{s} + \frac{B}{s+\frac{1}{10}} \tag{187}$$

$$= \frac{5}{s} - \frac{5}{s+\frac{1}{10}}. \tag{188}$$

If we take the inverse Laplace transform of both sides, we find that

$$\mathcal{L}^{-1}\{V_C(s)\} = \mathcal{L}^{-1}\left\{\frac{5}{s}\right\} - \mathcal{L}^{-1}\left\{\frac{5}{s+\frac{1}{10}}\right\} \tag{189}$$

$$= v_C(t) \tag{190}$$

$$= 5u(t) - 5e^{-\frac{t}{10}}u(t) \tag{191}$$

$$= (5 - 5e^{-\frac{t}{10}})u(t) \tag{192}$$

Exactly the result we would achieve using differential equations or Laplace transforms, with arguably much less work. However, we assumed zero-state conditions. Can this method deal with situations where the initial state is not zero? Yes! Consider again figure 40, but this time say $v_C(0) = 2V$. We'll use KVL around the circuit to obtain

$$V_{in}(s) = V_R(s) + V_C(s) \tag{193}$$

$$= RI_C(s) + V_C(s) \tag{194}$$

$$= RC\left(sV_C(s) - v_C(0)\right) + V_C(s) \tag{195}$$

$$\frac{5}{s} = 10\left(sV_C(s) - 2\right) + V_C(s). \tag{196}$$

If we solve for $V_C(s)$, we find that

$$V_C(s) = \frac{5}{s} - \frac{3}{s+0.1}, \tag{197}$$

making our final solution

$$v_C(t) = 5 + (2-5)e^{-\frac{t}{RC}}$$

When a capacitor has non-zero initial conditions the current through it will be of the form

$$i_C(t) = C\frac{dv_C(t)}{dt}$$

which in the frequency domain is

$$I_C(s) = C\left(sV_C(s) - v_C(0)\right).$$

There's two terms here, one corresponding to the current generated by the voltage source and one corresponding to initial conditions. We can think of this physically like figure 41. As can be seen, there's

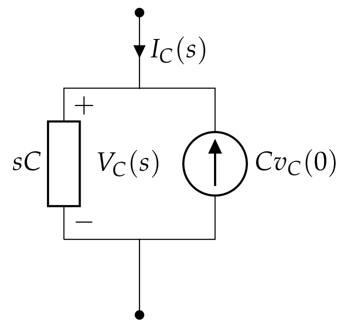

Figure 41: significance of each term

two components to the current. The current due to initial conditions flows opposite $I_C(s)$. That checks out physically. If you start with a bit of charge piled up on your capacitor plates, it's going to want to discharge and that will create a current going from positive to negative. If we find the equivalent Thevenin circuit, we get the circuit in figure 44. We can make similar models for the inductor, as shown

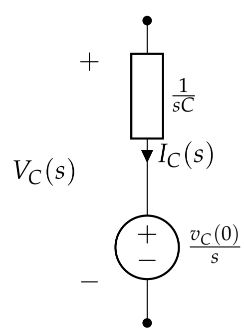

Figure 42: Thevenin equivalent model

in 43 and reffig:inital condition inductor model thev. For the inductor, we have a constant voltage related to the initial conditions and the current is being dissipated by the impedance of the inductor. Which model you use is determined by the circuit you're analyzing. The right choice can make a problem much easier to analyze.

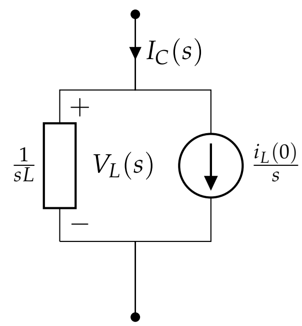

Figure 43: significance of each term

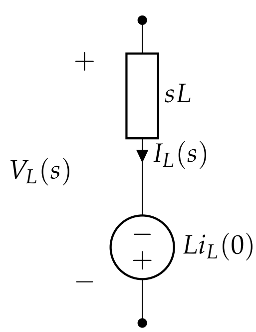

Figure 44: Thevenin equivalent model

We've talked so much about responses, now is a good time to recap all the types of responses we've seen thus far.

- Complete Response. Includes responses from all inputs (independent current and voltage sources) and responses from all initial conditions.
- Zero-Input Response (ZIR). Response to a set of initial conditions when all inputs are deactivated.
- Zero-State Response (ZSR): Response to a specific input signal when all initial conditions are set to zero.
- Forced Response: Response from all components not associated with the complex natural frequencies of the circuit (i.e. the roots of the characteristic equation).
- Natural Response: Response to terms associated with roots of characteristic equation.
- Transient Response: Defined by terms that are neither constant nor sinusoidal. Anything that increases or decays with time.
- Sinusoidal Steady State Response: Response that is sinusoidal with time.

Transfer Functions

Recall that if the output of a circuit is $y(t)$, the input is $x(t)$, and the impulse response is $h(t)$, then

$$y(t) = h(t) * x(t).$$

If we take the Laplace transform of both sides of this equation, we find

$$Y(s) = H(s)X(s)$$

and

$$H(s) = \frac{Y(s)}{X(s)}.$$

$H(s)$ is called the *transfer function*, and the above formula only applies when there are no independent sources within the circuit and all initial conditions are set to zero. If you find the transfer function, you can use it to get either the input (if the output is known) or the output (if the input is known). Once known, responses to any input may be calculated (provided the input variable remains unchanged). The form of the transfer function (or impedance or admittance) reveals information about the circuit or system associated with the transfer function.

The transfer function, along with impedances and admittances, are all rational functions. We can express the transfer function as

$$H(S) = K\frac{(s-z_1)^{q_1}(s-z_2)^{q_2}\dots(s-z_m)^{q_m}}{(s-p_1)^{r_1}(s-p_2)^{r_2}\dots(s-p_n)^{r_n}} \tag{198}$$

where p_n are the *poles* and z_m are the *zeroes*. The constant K is called the *gain constant*. Calling z_m zeroes makes sense, but why poles? To answer that, let's remember that $s = \sigma + j\omega$. Therefore, $H(s)$ is a function on the complex plane. The poles correspond to where we're dividing by zero and the graph of $H(s)$ jumps to infinity. On the complex plane, we often mark them with xs and zeroes with dots. Poles indicate the form of the natural response of a circuit. When you solve the inverse Laplace transform, they're the values that end up as λ in $Ae^{-\lambda t}$. If the order of a pole is greater than one, then some terms will be multiplied by t^n. A circuit is *stable* if conditions remain finite for all t. The transfer function and its poles indicate when the circuit may be unstable. If all poles have $\mathbb{R}\{s\} = \sigma_i < 0$ (that is, if they reside on the left hand side of the complex plane), then it is guaranteed he circuit will be stable. Any pole such that $\mathbb{R}\{s\} = \sigma_i > 0$ indicates system is unstable. Systems with a pole on the $j\omega$ axis of order 1 ($\mathbb{R}\{s\} = \sigma_i = 0$) are marginally stable. Systems with pole(s) on the $j\omega$ axis of order greater than 1 ($\mathbb{R}\{s\} = \sigma_i = 0$) are unstable.