

# *ECE 20002: Electrical Engineering Fundamentals II*

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## *Course Introduction*

Continuation of Electrical Engineering Fundamentals I. The course addresses mathematical and computational foundations of circuit analysis (differential equations, Laplace Transform techniques) with a focus on application to linear circuits having variable behavior as a function of frequency, with emphasis on filtering. Variable frequency behavior is considered for applications of electronic components through single-transistor and operational amplifiers. The course ends

with a consideration of how circuits behave and may be modeled for analysis at high frequencies.

Learning Objectives:

1. Analyze 2nd order linear circuits with sources and/or passive elements
2. Compute responses of linear circuits with and without initial conditions via one-sided Laplace transform techniques
3. Compute responses to linear circuits using transfer function and convolution techniques
4. Analyze and design transistor amplifiers at low, mid and high frequencies

## Field-Effect Transistor Devices

### MOSFETs

Let us begin where ECE 20001 ended, with metal-oxide semiconductor field-effect transistors (MOSFETs). The rectangle below represent a wafer of silicon. The p - Si label indicates that the wafer is primarily doped with boron and the primary carrier type is holes. The two  $n^+$  rectangles designate regions of phosphorus doping. The grey rectangles above the wafer are dielectric layers of silicon dioxide. The black rectangles are ohmic metals that allow for connecting our phosphorus regions to other components. To these metal contacts we attach a source, a gate, and a drain. The source is the source of electron, and the drain is how the electrons exit. The gate will define a pathway between the source and drain. Since the phosphorus re-



Figure 1: nMOSFET diagram

gions are n-type and ergo have free electrons, the primary carrier of this MOSFET are electrons. The way we allow current to flow from source to drain is by increasing the voltage of the gate  $v_{GS}$  to attract an inversion layer underneath the dielectric separating the gate from the silicon wafer. If the voltage of the gate is high enough ( $v_{GS} > V_T$ ) then enough electrons will be attracted to that area for current to flow between source and drain.

We could create a similar MOSFET by inverting the n-type and p-type regions, as in figure 2. In this case the primary current carrier will be holes.

In the case of the nMOSFET in figure 1, a negative gate voltage will attract holes in the semiconductor, forming two oppositely charged areas separated by a distance  $x$ . This establishes an electric field within the oxide layer given by the equation for a parallel plate capacitor

$$\mathcal{E}_x = -\frac{dV}{dx} \quad (1)$$

Likewise, a positive gate voltage *that is less than*  $V_T$  will attract elec-

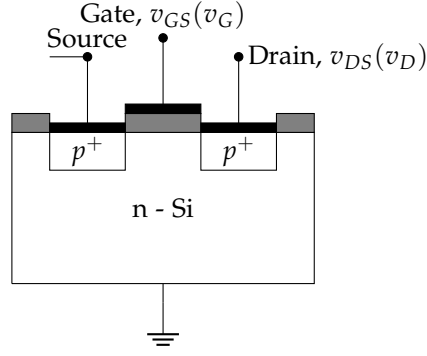


Figure 2: pMOSFET diagram

trons in the semiconductor. This also forms a capacitance of  $C_{ox}$  in the oxide layer, but because the semiconductor is n-type, the electrons will be spread out over a wider area and have their own capacitance  $C_d$ . Thus the total capacitance across the oxide and depletion region  $C$  given by

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_d} \quad (2)$$

If  $0 < V_T < v_{GS}$ , then  $C = f\omega$ , where  $\omega$  is the frequency of our probe.

Figure 3 displays the capacitance-voltage graph of a p-type metal-oxide semiconductor. The capacitance is constant when gate voltage is negative, then falls at the *flat-band voltage*  $V_{GS} = 0V$ , then rapidly rises again after the threshold voltage is reached.



Figure 3: p-type MOS capacitance-voltage characteristic

The resistivity of the inversion channel created by the gate's bias is given by

$$\frac{1}{\rho} = (n\mu_e + p\mu_h)q \quad (3)$$

where  $n$  is the concentration of electrons,  $p$  is the concentration of holes,  $\mu_e$  is the mobility of electrons,  $\mu_h$  is the mobility of holes, and  $q$  is the charge of an electron. The higher the gate voltage, the higher the current between source and drain. Below the threshold voltage there is no current flow because no channel is formed. This relationship is linear provided the drain voltage is less than 150 mV, but above 0.3 V becomes nonlinear. That's because the channel is no longer a regular shape, but narrows in the region of the drain. Below 150 mV, however, this distortion can be assumed negligible. Recall that

$$R = \frac{\rho L}{A} \quad (4)$$

Whereas for small  $v_{DS}$  the area is almost constant, when  $v_{DS} > 0.15V$  the area  $A$  decreases enough that the resistance  $R$  is significantly increased. When the area has decreased to zero at the drain, we reach the *pinch-off* and the drain voltage is at saturation  $v_{DS(sat)}$ . The current still flows constantly for all drain voltage above saturation, however. Before saturation is reached and after the gate voltage is above the threshold, we are in the triode region. In the triode region, the current is given by

$$i_{D(triode)} = \mu C_{ox} \frac{W}{L} \left( (v_{GS} - V_T) v_{DS} - \frac{v_{DS}^2}{2} \right) \quad (5)$$

Sometimes, the constant terms are wrapped up into one constant, like so:

$$i_{D(triode)} = k_n \left( (v_{GS} - V_T) v_{DS} - \frac{v_{DS}^2}{2} \right) \quad (6)$$

In the saturation region,

$$i_{D(sat)} = \mu C_{ox} \frac{W}{L} \frac{(v_{GS} - V_T)^2}{2} \quad (7)$$

$$= k_n \frac{v_{DS(sat)}^2}{2} \quad (8)$$

When we are far away from saturation, the resistance of the channel is given by

$$R_{on} = \frac{\partial v_{DS}}{\partial i_D} \quad (9)$$

$$= \frac{1}{\mu C_{ox} \frac{W}{L} (v_{GS} - V_T)} \quad (10)$$

Figure 4 shows a family of  $i_D$ - $v_{DS}$  curves with differing values of  $v_{GS}$ . Also show as a dashed green line is the saturation current as a function of gate voltage. Let's look at the impact the threshold voltage has by plotting the  $i_D$ - $v_{GS}$  curve for differing values of  $V_T$  in figure 5. Now the green dashed curve corresponds to a threshold voltage of



Figure 4: Transfer characteristics of nMOSFETs

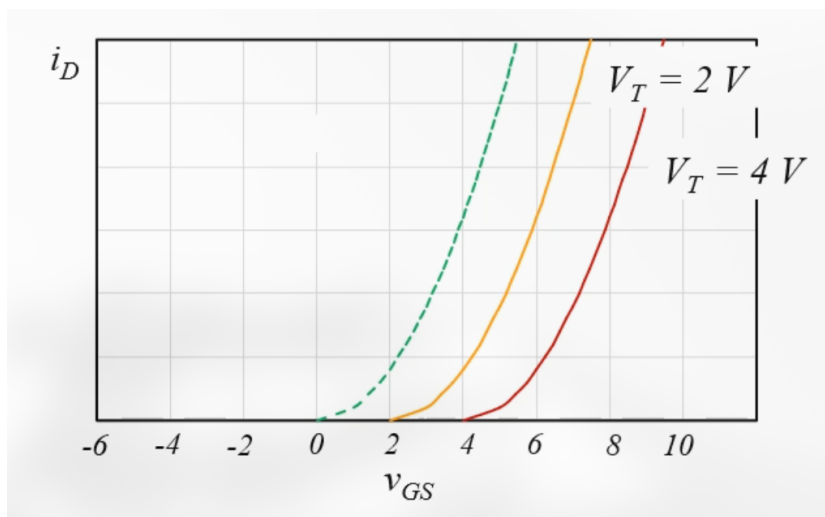


Figure 5:  $i_D$ - $v_{GS}$  curve for select values of  $V_T$

zero. Recall that the threshold voltage is intrinsic to the semiconductor wafer. Doping variations, defect, and shape can all affect the threshold voltage. If we build a depletion-mode nMOSFET, then we allow for negative threshold voltages.

A normally off like in figure 1 has the symbol shown in 6 and is said to be in enhancement mode. If the nMOSFET has an n-channel



Figure 6: nMOSFET schematic

between the source and drain, as shown in figure 7, then it is normally



Figure 7: Normally on nMOSFET diagram

on and its symbol is as seen in figure 8. This kind of nMOSFET is said to be in depletion mode. Note the thicker line between source and

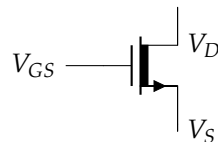


Figure 8: Schematic of normally on nMOSFET

drain representing the n-channel.

Similarly, the pMOSFET shown in figure 2 is a normally off, enhancement mode pMOSFET. A pMOSFET with a p-channel is normally on and in depletion mode.

Let's look at the transfer characteristics of the different types of MOSFETs. figure 4 shows these characteristics for a normally off, enhancement mode nMOSFET. For a normally on, depletion mode nMOSFET the graph is exactly the same, except that the current can flow even when the gate bias is zero since the fabricated channel

allows the flow of electrons from source to drain. The output characteristics for a normally off, enhancement mode pMOSFET are shown in figure 9. A negative bias on the gate will induce a channel of pos-

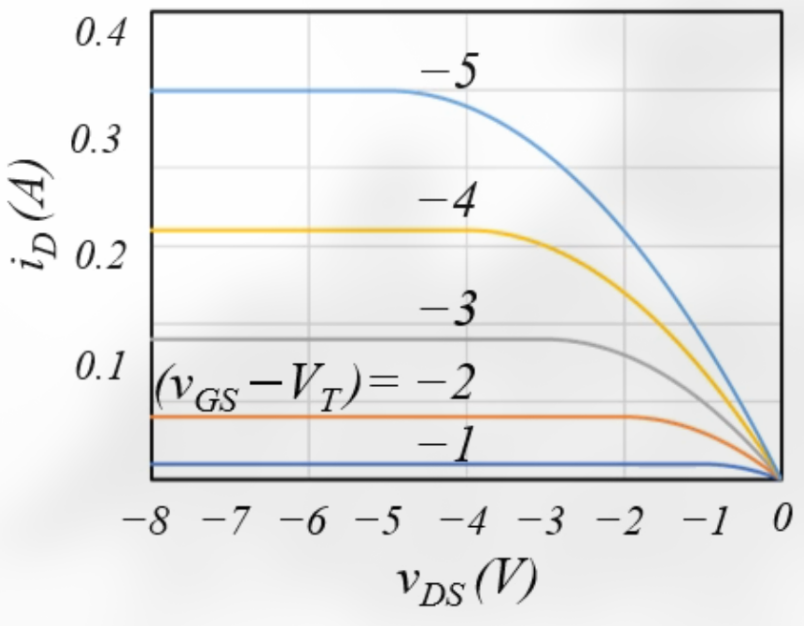


Figure 9:  $i_D$ - $v_{DS}$  curve for select values of  $v_{GS} - V_T$

itive holes in the semiconductor, making the threshold voltage for a pMOSFET negative. Again, the normally on depletion mode pMOSFET graph has the same shape, but since there is an existing channel for current it will flow even for some positive values of  $v_{GS}$ . We need to deplete the channel by pushing away all the holes in it with the bias on the gate in order to turn it off.

To review, there are four kinds of MOSFETs in which we are interested:

- normally off, enhancement mode nMOSFETs
- normally on, depletion mode nMOSFETs
- normally off, enhancement mode pMOSFETs
- normally on, depletion mode pMOSFETs

### Transconductance

Now, let us move on to the topic of transconductance. In the triode region, the transconductance is defined as

$$g_m = \left. \frac{i_D}{v_{GS}} \right|_{Q_{pt}} \quad (11)$$



where

$$Q_{pt} = (I_D, V_{DS}). \quad (12)$$

If we recall equation 5, and substitute for  $i_D$  in equation 11, then we obtain

$$g_m = \mu C_{ox} \frac{W}{L} v_{DS} \quad (13)$$

$$= \frac{i_{D(triode)}}{(v_{GS} - v_T) - \frac{v_{DS}}{2}} \quad (14)$$

In the saturation region,

$$g_m = \frac{di_D}{dv_{GS}}|_{Q_{pt}} \quad (15)$$

and

$$i_{D(sat)} = \mu C_{ox} \frac{W}{L} \frac{(v_{GS} - V_T)^2}{2}. \quad (16)$$

Again combining these two equations,

$$g_m = \mu C_{ox} \frac{W}{L} (v_{GS} - V_T) \quad (17)$$

$$= \frac{2i_{D(sat)}}{(v_{GS} - V_T)} \quad (18)$$

The larger the transconductance, the larger the gain of an amplifier circuit that uses the transistor.

### *Channel length modulation*

By adjusting the voltage of the drain, we can modulate the channel length. Specifically,

$$i_{D(sat)} \propto \frac{1}{L - \Delta L} \quad (19)$$

$$\equiv \frac{1}{L} \left( 1 + \frac{\Delta L}{L} \right). \quad (20)$$

And

$$\Delta L \propto (v_{DS} - v_{DS(sat)}) \quad (21)$$

means that

$$i_{D(sat)} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (v_{GS} - V_T)^2 \left[ 1 + \lambda (v_{DS} - v_{DS(sat)}) \right] \quad (22)$$

where  $\lambda$  is the empirically determined channel length modulation parameter. The output resistance at the drain is given by

$$r_0 = \left[ \frac{\partial i_{D(sat)}}{\partial v_{DS}} \right]^{-1} \quad (23)$$

$$= \left[ \lambda \frac{1}{2} k_n (v_{GS} - V_T)^2 \right]^{-1} \quad (24)$$

$$= \frac{1}{\lambda I_{D(sat)}} \quad (25)$$

$$\approx \frac{V_A}{I_{D(sat)}} \quad (26)$$

Channel length modulation is not important when channel length is relatively large, but it is important on modern transistors where are on the order of nanometers.

### MOSFETs in DC circuits

Consider a circuit with two enhancement mode pMOSFETs. Notice



Figure 10: MOSFET DC circuit

that in figure 10, the drain of  $M_1$  is directly attached to the gate. From this we have

$$v_{DS1} = v_{GS1} \quad (27)$$

$$= v_{GS2} \quad (28)$$

We are told  $M_1$  is in saturation. If these are two identical transistors, then

$$I_{REF} = I_{D(sat)} \quad (29)$$

$$= \frac{1}{2} k_{p1} (v_{GS1} - V_{T1})^2 \quad (30)$$

$$= I_{OUT}. \quad (31)$$

From this, we learn that the reference current is mirrored by the drain current if  $k_{p1} = k_{p2}$  and  $v_{GS1} = v_{GS2}$ .



Figure 11: Inverter

Let us now look at the inverter shown in figure 11. Let's try to find  $V_{out}$  for  $V_{in} = 0V$  and  $V_{in} = 5V$ . We are told that  $V_{T(M1)} = 1V$  and  $V_{T(M2)} = -1V$ , because M1 is an enhancement mode nMOSFET and M2 is an enhancement mode pMOSFET. When  $V_{in} = 0V$ , M1 is off because  $v_{GS1} < V_{T(M1)}$ . Likewise, M2 is on because  $v_{GS2} < V_{T(M2)}$  (recall that M2 is a pMOSFET). Since M1 is off, no current flows and  $V_{out} = 5V$ . For  $V_{in} = 5V$ , M1 flips on while M2 is off. Since M2 is off, no current flows. That means that  $V_{out} = 5V$ .

### Transistors as amplifiers

The circuit shown in figure 12 has both AC and DC voltage sources.



Figure 12: Common-source nMOSFET amplifier circuit

The source labelled by  $V_{GS}$ , all caps, is the DC voltage. The source  $v_{gs}$ , all lowercase, is the AC. This is not to be confused with  $v_{GS}$ , the total

gate bias. The mix of cases indicates we have both AC and DC bias in consideration. The cool thing about this circuit is a small oscillation in the AC input induces a much larger oscillation in the output, hence calling it an amplifier. The output signal is going to be phase shifted by  $180^\circ$ . We can calculate the gain with eq. 32

$$A_v = \frac{v_{ds}}{v_{gs}} \quad (32)$$

In this instance,

$$A_v = \frac{v_{ds}}{v_{gs}} \quad (33)$$

$$= \frac{4.17 \angle 180^\circ}{1 \angle 0^\circ} \quad (34)$$

$$= -4.17 \quad (35)$$

This gain, however, will be somewhat distorted. To reduce distortion we need that  $|v_{gs}| \ll 2(V_{GS} - V_T)$ . The exact value of the "much less" symbol  $\ll$  will depend on the application, but it's common to require  $|v_{gs}| < 0.2(V_{GS} - V_T)$ . If we assume the small signal condition and no channel length modulation, then the transconductance of the amplifier is

$$g_m = \sqrt{2k_n I_{D(sat)}} \quad (36)$$

Figure 13 shows the small signal equivalent circuit of a common source amplifier. Notice the two voltage sources, one AC signal and



Figure 13 Small signal equivalent circuit

one DC bias at the gate. The total input signal is given by

$$v_{GS}(t) = v_{gs}(t) + V_{GS} \quad (37)$$

$$v_{DS}(t) = v_{ds}(t) + V_{DS} \quad (38)$$

The drain current for such a circuit when channel length modulation is accounted for is given by

$$i_{D(clm)} = \frac{1}{2}k_n \left[ v_{gs}^2 + 2(V_{GS} - V_T)v_{gs} + (V_{GS} - V_T)^2 \right] \\ \times \left[ 1 + \lambda(V_{DS} - (V_{GS} - V_T)) + \lambda(v_{ds} - v_{gs}) \right]$$

When channel length modulation can be ignored, the current reduces to

$$i_{D(sat)} = \frac{1}{2}k_n \left[ v_{gs}^2 + 2(V_{GS} - V_T)v_{gs} + (V_{GS} - V_T)^2 \right] \quad (39)$$

For finite output resistance  $r_0$ ,

$$\frac{1}{r_0} = \left[ \frac{\partial i_{D(clm)}}{\partial v_{DS}} \right] \quad (40)$$

$$= \frac{\partial}{\partial v_{DS}} \left\{ \frac{k_n}{2} (v_{GS} - V_T)^2 \left[ 1 + \lambda(v_{DS} - v_{DS(sat)}) \right] \right\} \quad (41)$$

$$= \frac{k_n}{2} (v_{GS} - V_T)^2 \frac{\partial}{\partial v_{DS}} \left[ 1 + \lambda(v_{DS} - v_{DS(sat)}) \right] \quad (42)$$

$$= \lambda \frac{k_n}{2} (v_{GS} - V_T)^2 \quad (43)$$

$$= \lambda I_{D(sat)}. \quad (44)$$

We then define the *intrinsic voltage gain of a MOSFET* as

$$\mu_f = g_m r_0 \quad (45)$$

$$= \sqrt{2k_n I_{D(sat)}} \left( \frac{1}{\lambda I_{D(sat)}} \right) \quad (46)$$

$$= \frac{1}{\lambda} \sqrt{\frac{2k_n}{I_{D(sat)}}} \quad (47)$$

We can greatly simplify circuit analysis by breaking the circuit up into AC and DC. To find the DC equivalent circuit, follow these steps:

1. Replace all capacitors with open circuits
2. Replace all inductors with short circuits
3. Deactivate AC sources
4. Find the Q-point using the DC equivalent circuit

To find the AC equivalent circuit,

1. Replace all capacitors with short circuits at operational frequency
2. Replace all inductors with open circuits at operational frequency
3. Deactivate DC voltages and replace with short circuits
4. Deactivate DC current sources and replace with open circuits
5. Replace the transistor with its small-signal model

### Amplifier topologies

There are three different nMOSFET amplifier topologies we will consider in this class, starting with the common-source amplifier shown in figure 14. The common-source amplifier's input is taken



Figure 14: Common-source amplifier

through the gate, the output is taken through the drain, and the terminal that is common to output and input is the source.

The second topology is the common-gate amplifier shown in figure 15. Here we see that the AC voltage source is applied to the source,



Figure 15: Common-gate amplifier

while the output is taken at the drain and the common terminal is at the gate.

The previous two amplifiers suggest a third, the common-drain amplifier in figure 16. As may be expected, here the common terminal



Figure 16: Common-drain amplifier

is the drain, the input is at the gate, and the output is at the source.

You may be thinking: "what happens if the input and output are swapped? Will the circuit still work as an amplifier?" No.

The voltage gain in a common-drain amplifier is given by

$$A_V = \frac{g_m R'_L}{1 + g_m R'_L} \left( \frac{R_G}{R_I + R_G} \right) \quad (48)$$

where  $R'_L = (r_0 || R_6 || R_3)$ . For a MOSFET where  $r_0 \gg R_L$ ,

$$A_V \approx \frac{R_G}{R_I + R_G} \quad (49)$$

When this is true, the MOSFET is acting as a *voltage follower*.

Figure 17 shows the small-signal model for an nMOSFET called a hybrid-pi model. This model is excellent for common-source and



Figure 17: Hybrid-pi model

common-drain amplifiers. For the common-gate amplifier, the alternative T-model shown in figure 18 is more useful. The voltage gain in a



Figure 18: T-model

common-gate amplifier is given by

$$A_V = \frac{g_m R_L}{1 + g_m (R_I || R_6)} \left( \frac{R_6}{R_I + R_6} \right) \quad (50)$$

Let's recap our three kinds of amplifiers. For the inverting common-source amplifier,

$$A_V = -\frac{g_m R_L}{1 + g_m R_S} \left( \frac{R_G}{R_I + R_G} \right). \quad (51)$$

Additionally,

$$R_{in} = \infty \quad (52)$$

$$R_{out} = R_L \quad (53)$$

For the non-inverting common-gate amplifier,

$$A_V = \frac{g_m R_L}{1 + g_m(R_I || R_6)} \left( \frac{R_6}{R_I + R_6} \right) \quad (54)$$

with

$$R_{in} = \frac{1}{g_m} \quad (55)$$

$$R_{out} = R_L \quad (56)$$

For the follower common-drain amplifier,

$$A_V = \frac{g_m R_L}{1 + g_m R_L} \left( \frac{R_G}{R_I + R_G} \right) \quad (57)$$

$$\approx \left( \frac{R_G}{R_I + R_G} \right). \quad (58)$$

Here,

$$R_{in} = \infty \quad (59)$$

$$R_{out} = \frac{1}{g_m} \quad (60)$$

### Frequency range for FET amplifiers

The *lower-frequency cutoff* for an amplifier circuit is defined as the  $\omega_L$  where the gain  $A_V$  is  $\frac{1}{\sqrt{2}}$  the maximum gain. We are told that

$$\omega_L = \frac{1}{\tau} \quad (61)$$

$$= \frac{1}{r_{eq} C}. \quad (62)$$

If there are multiple capacitors in the circuit, find  $r_{eq}$  for each, calculate all possible values of  $\omega_L$ , and pick the largest. The *higher-frequency cutoff*  $\omega_H$  is also defined as the frequency where the gain  $A_V$  is  $\frac{1}{\sqrt{2}}$  the maximum gain, but the higher of the two values. For a common-source amplifier,

$$\omega_H = \frac{1}{(R_S || R_1 || R_2) C_{gs}} \quad (63)$$

The bandwidth of useable frequencies is  $\omega_H - \omega_L$ .

The higher-cutoff frequency is defined by capacitors within the amplifier circuit,  $C_{gs}$  and  $C_{gd}$ . We do not explore this relation within

$C_{gs}$  is the capacitance between the gate and channel at a point nearer the source, while  $C_{gd}$  is the same but for a point nearer the drain.



this course. However, we are told the following equations are valid in the triode region:

$$C_{gc} = WLC_{ox} \quad (64)$$

$$C_{gd} = \frac{C_{gc}}{2} + C_{gdo}X_{do} \quad (65)$$

$$C_{gs} = \frac{C_{gc}}{2} + C_{gso}X_{so} \quad (66)$$

In the saturation region,

$$C_{gd} = C_{gdo}X_{do} \quad (67)$$

$$C_{gs} = \frac{2}{3}C_{gc} + C_{gso}X_{so} \quad (68)$$

$C_{gso}$  is the capacitance of oxide overlapping source,  $C_{gdo}$  is the capacitance of oxide overlapping drain,  $X_{so}$  is the length of oxide overlap on source, and  $X_{do}$  is the length of oxide overlap on drain.

Typically  $C_{gd}$  is so much smaller than  $C_{gs}$  as to be insignificant.

The maximum useful linear frequency of a transistor is

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{gc}} \quad (69)$$

$$= \frac{1}{2\pi} \frac{\mu}{L^2} (v_{gs} - V_T) \quad (70)$$

In addition to the intrinsic capacitances  $C_{ox}$  and  $C_d$ , there are also parasitic capacitances. The junction capacitance  $C_J$  forms between the source/drain and the semiconductor, while the overlap capacitance  $C_{ov}$  forms between the source/drain and the metal contact on the gate.

### Reference

Region	Conditions
Cut-off	$v_{GS} < V_T$
Triode	$v_{DS} \leq v_{DS(sat)}$
Saturation	$v_{DS} > v_{DS(sat)}$

Figure 19: nMOSFET regions of operation

Region	Conditions
Cut-off	$v_{GS} > V_T$
Triode	$v_{DS} \geq v_{DS(sat)}$
Saturation	$v_{DS} < v_{DS(sat)}$

Figure 20: pMOSFET regions of operation

	nMOSFET	pMOSFET
Cutoff	$v_{GS} < 0$	$v_{GS} > 0$
Triode	$v_{GS} > 0$	$v_{GS} < 0$
Saturation	$v_{GS} > 0$	$v_{GS} < 0$
Enhancement	$V_T > 0$	$V_T < 0$
Depletion	$V_T < 0$	$V_T > 0$

Figure 21: Differences between pMOSFET and nMOSFET

	nMOSFET	pMOSFET
Enhancement		
Depletion		

Figure 22: MOSFET schema

Equation	Condition	Reference
$v_{DS(sat)} = v_{GS} - V_T$	MOSFET	
$i_{D(cutoff)} = 0$	MOSFET	
$i_{D(triode)} = \mu C_{ox} \frac{W}{L} ((v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2})$ $= k_n ((v_{GS} - V_T)v_{DS} - \frac{v_{DS}^2}{2})$ $= \frac{k_n}{2} (2v_{DS(sat)} - v_{DS})v_{DS}$	MOSFET	eq. 5
$i_{D(sat)} = \mu C_{ox} \frac{W}{L} \frac{(v_{GS} - V_T)^2}{2}$ $= k_n \frac{v_{DS(sat)}^2}{2}$	MOSFET	eq. 7
$A_v = \frac{v_{out}}{v_{in}}$	Amplifying transistor	eq. 32
$g_m = \sqrt{2k_n I_{D(sat)}}$	Amplifying transistor	eq. 36
$i_{D(clm)} = \frac{1}{2} k_n \left[ v_{gs}^2 + 2(V_{GS} - V_T)v_{gs} + (V_{GS} - V_T)^2 \right]$ $\times [1 + \lambda(V_{DS} - (V_{GS} - V_T)) + \lambda(v_{ds} - v_{gs})]$	CLM active	eq. 39
$\omega_L = \frac{1}{\tau}$ $= \frac{1}{r_{eq}C}$	Amplifier	eq. 61
$\omega_H = \frac{1}{(R_S    R_1    R_2)C_{gs}}$	Common-source amplifier	eq. 63



Figure 23: Hybrid-pi model



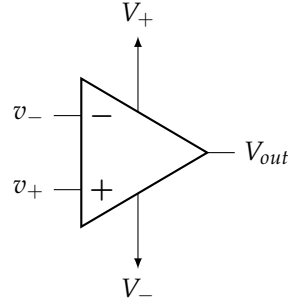
Figure 24: T-model

### Operational Amplifier

The *operational amplifier* (op-amp) is a high voltage gain amplifier with a differential input. It can perform mathematical operations, but it's also commonly used in industrial and consumer products. On any op-amp pinout are eight terminals:

1. offset null
2. inverting input
3. noninverting input
4. negative power supply
5. offset null
6. output
7. positive power supply
8. no connection

The symbol for an op-amp is given in figure 25. We have a potential at the inverting terminal of  $v_-$ , and a potential at the noninverting terminal of  $v_+$ .  $V_-$  and  $V_+$  are the negative and positive power supplies,

Figure 25:  
symbol

amplifier

Figure 26:  
model

amplifier

respectively. We can model the op-amp as in figure 26. The open-loop gain  $A$  is typically  $O(10^4)$ , but can be higher or lower. The input signal is voltage, not current, so we typically make  $R_i$  large to avoid loss of signal. The maximum and minimum possible voltages are clipped to  $V_+$  and  $V_-$ , respectively.

Consider the feedback loop shown in figure 27. Here,  $x_o = Ax_i$

In an ideal op-amp,  $A = \infty$  and  $R_i$  is also  $\infty$ .



Figure 27: Feedback loop

and  $x_f = Bx_o$ . At the summing circle, the feedback  $x_f$  is subtracted from  $x_s$  to yield  $x_i$ :  $x_i = x_s - x_f$ . We define the closed-loop gain as

$$A_f = \frac{x_o}{x_s} \quad (71)$$

$$= \frac{A}{1 + AB} \quad (72)$$

The product  $AB$  is the *loop gain*, and  $1 + AB$  is the *amount of feedback*. When  $AB \gg 1$ ,  $A_f \approx \frac{1}{B}$ . Consider the inverting op-amp shown in figure 28. Because the potential of the noninverting and inverting



Figure 28: Inverting op-amp

terminals of an op-amp are equal, we know that  $V_- = 0$ . Ergo,

$$I_S = \frac{V_S}{R_S} \quad (73)$$

With a little more algebra that makes a useful exercise for the reader, we obtain

$$A_f = -\frac{R_f}{R_S} \quad (74)$$

Hence why this setup is called an inverting op-amp.

### Reference

Ideal op-amp features:

- $v_+ = v_-$
- $A = \infty$
- $R_o = 0$
- $i_- = i_+ = 0$

### Circuit Analysis

#### Differential Equations

An important function in circuit analysis is the exponential function

$$e^x = \sum_{k=0}^{\infty} \frac{x^k}{k!} \quad (75)$$

Any function can be expressed as a linear combination of exponential functions. Recall also that  $\int e^x dx = e^x + C$  and  $\frac{d}{dx} e^x = e^x$ . An *ordinary differential equation* (ODE) is given by

$$y(t) = \sum_{k=0}^n A_k \frac{d^k x(t)}{dt^k} \quad (76)$$

$y(t)$  is the forcing function, our objective is to find  $x(t)$  that matches  $y(t)$ . The process for this is to first solve the specific case when  $y(t) = 0$ , the homogeneous ODE. We then find the particular solution that matches  $y(t)$ . In the case of exponential circuit analysis, the homogeneous case corresponds to analyzing our circuit absent any excitations from forcing functions. To make this clear, we want to solve

$$0 = \sum_{k=0}^n A_k \frac{d^k x(t)}{dt^k}. \quad (77)$$

We assume a solution of the form

$$x_h(t) = Ae^{\lambda t}. \quad (78)$$

Let's consider an example. Say

$$y(t) = 2x(t) + 3\frac{dx(t)}{dt}. \quad (79)$$

We take

$$0 = 2x_h(t) + 3\frac{dx_h(t)}{dt}. \quad (80)$$

If  $x_h(t) = Ae^{\lambda t}$ , then

$$0 = 2Ae^{\lambda t} + 3A\lambda e^{\lambda t}. \quad (81)$$

Cancelling out  $Ae^{\lambda t}$  from both sides, we obtain

$$0 = 2 + 3\lambda. \quad (82)$$

This is the *characteristic equation* of the circuit. Solving this characteristic equation will provide the *natural frequency*  $\lambda$  for the homogeneous ODE solution. Returning to our example, say  $y(t) = 4e^{-t}$ . We can reasonably assume that  $x_p(t) = Be^{-t}$ . Plugging this in, we find that

$$y(t) = 2x(t) + 3\frac{dx(t)}{dt} \quad (83)$$

$$4e^{-t} = 2Be^{-t} + 3(-1)Be^{-t} \quad (84)$$

$$B = -4x_p(t) = -4e^{-t}. \quad (85)$$

$\lambda$  is called the natural frequency because it's what we get without any external excitation.

The complete solution is the superposition of the homogeneous and particular solutions,

$$x(t) = x_h(t) + x_p(t). \quad (86)$$

Recall that although we found  $\lambda$  for the homogenous solution, we have not yet found  $A$ . To do so we require an initial condition. Say in this case the initial condition is given as  $x(0) = 2$ . Then

$$x(0) = 2 \quad (87)$$

$$= -4e^0 + Ae^0 \quad (88)$$

$$A = 6. \quad (89)$$

So the complete solution becomes

$$x(t) = -4e^{-t} + 6e^{-\frac{2}{3}t} \quad (90)$$

### RC and RL Circuits

This isn't a differential equations class, this is a circuits class. The reason we care about ODEs is because they arise in circuits. For example, consider the circuit in figure 29. Remember that

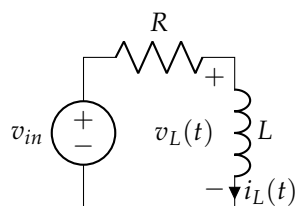


Figure 29: RL circuit

$$v_L = L \frac{di_L(t)}{dt}. \quad (91)$$

Via KVL, we have that

$$v_{in}(t) = v_L(t) + Ri_L(t). \quad (92)$$

Putting the two together,

$$v_{in}(t) = L \frac{di_L(t)}{dt} + Ri_L(t). \quad (93)$$

This is a first-order ODE. Solving it is left as an exercise to the reader. A similar process applies to the RC circuit shown in figure 30. In both

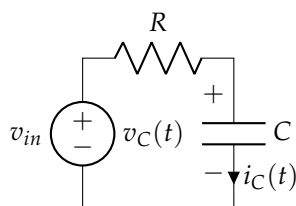


Figure 30: RC circuit

the RC and RL cases, solving the ODE will yield the formulas for  $v_C(t)$  and  $v_L(t)$  with which we are familiar from ECE 20001.

Note that both the inductor and capacitor are non-ideal elements, and if we are to accurately model circuits we must account for this. Specifically, inductors behave non-ideally in the following ways:

- The wire that makes up the coil of the inductor has intrinsic resistance
- The spacing between the wire has intrinsic capacitance
- Hysteresis or eddy currents in the ferrite core have intrinsic resistance

Capacitors have the following non-ideal characteristics:

- The wire connected to the capacitor has intrinsic inductance
- The wire connected to the capacitor has intrinsic resistance
- The insulating dielectric between the plates of the capacitor has a large but finite resistance, and leakage current can therefore flow from one plate to another

The inductor is less ideal than the capacitor, since it necessarily has more non-ideal components than the capacitor. Therefore, for the capacitor, we can comfortably neglect the effects of the non-ideal wire. Figures 31 and 32 show the non-ideal models for inductor and capacitor used in this course.

In real life, the effects of the wire can be minimized by using chip capacitors, which have very short wires.

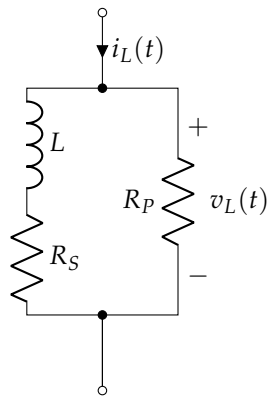


Figure 31: Non-ideal inductor

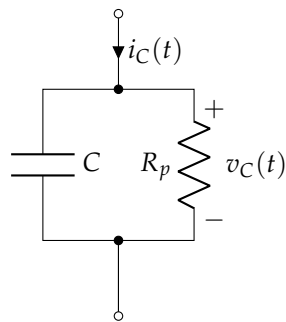


Figure 32: Non-ideal capacitor

### Switched Circuits

The current through an inductor is continuous, even when the voltage across it is not. Likewise, voltage across a capacitor is continuous even if current is not. Recall from ECE 20001 that the time it takes a



variable of interest, inductor current or capacitor voltage, to go from  $x(t_1)$  to  $x(t_2)$  in its respective circuit is given by

$$t_2 - t_1 = \tau \ln \left( \frac{x(t_1) - x(\infty)}{x(t_2) - x(\infty)} \right). \quad (94)$$

If switched events are associated with  $x(t)$ , then eq. 94 can be used to find the time for which a certain circuit configuration is valid.

Consider the circuit in figure 33. We are told that the switch is

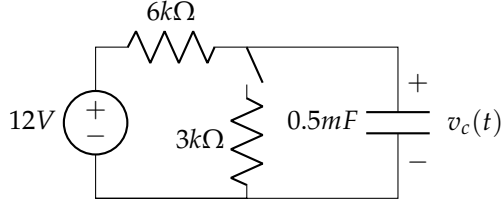


Figure 33: Switched circuit

initially open as shown and closes when  $v_c(t) = 9V$ . The switch opens again when  $v_c(t) = 5V$ .  $v_c(0^+) = 0V$ . We wish to find an expression for  $v_c(t)$  from  $t = 0$  to the third time the switch flips. Let's start by recalling the helpful equation in eq. 95.

$$x(t) = x(\infty) + [x(t_0) - x(\infty)] e^{-\left(\frac{t-t_0}{\tau}\right)} \quad (95)$$

Ergo,

$$v_c(t) = v_c(\infty) + [v_c(t_0) - v_c(\infty)] e^{-\left(\frac{t-t_0}{\tau}\right)} \quad (96)$$

For an RC circuit such as this one,  $\tau = RC$ .

$$v_c(t) = v_c(\infty) + [v_c(t_0) - v_c(\infty)] e^{-\left(\frac{t-t_0}{RC}\right)} \quad (97)$$

We know from our conditions that  $v_c(t_0) = 0$ , so eq. 97 simplifies to

$$v_c(t) = v_c(\infty) - v_c(\infty) e^{-\frac{t}{RC}} \quad (98)$$

In the open configuration,  $v_c(\infty) = 12V$  and  $R = 6k\Omega$ . We know that, but our circuit from  $t = 0$  until  $v_c(t) = 9V$  doesn't. Therefore,

$$t_2 - t_1 = \tau \ln \left( \frac{x(t_1) - x(\infty)}{x(t_2) - x(\infty)} \right) \quad (99)$$

$$= \tau \ln \left( \frac{v_c(t_1) - v_c(\infty)}{v_c(t_2) - v_c(\infty)} \right) \quad (100)$$

$$t_2 = RC \ln \left( \frac{0 - 12}{9 - 12} \right) \quad (101)$$

$$= 3 \ln \left( \frac{-12}{-3} \right) \quad (102)$$

$$\approx 4.16 \quad (103)$$

and

$$v_c(t) = v_c(\infty) - v_c(\infty)e^{-\frac{t}{RC}} \quad (104)$$

$$= 12 - 12e^{-\frac{t}{3}} \quad (105)$$

Now, let's consider what happens after the switch closes. Now  $R = 6k\Omega || 3k\Omega = 2k\Omega$ , and  $v_c(t) = 4V$ . This time around,  $v_c(t_0) = 9V$ . We therefore have

$$t_2 - t_1 = \tau \ln \left( \frac{x(t_1) - x(\infty)}{x(t_2) - x(\infty)} \right) \quad (106)$$

$$t_2 - 4.16 = \ln \left( \frac{9 - 4}{5 - 4} \right) \quad (107)$$

$$t_2 \approx 4.16 + 1.61 \quad (108)$$

$$= 5.77 \quad (109)$$

and

$$v_c(t) = v_c(\infty) + [v_c(t_0) - v_c(\infty)] e^{-\left(\frac{t-t_0}{\tau}\right)} \quad (110)$$

$$= 4 + [9 - 4] e^{-\left(\frac{t-4.16}{1}\right)} \quad (111)$$

$$= 4 + 5e^{-(t-4.16)} \quad (112)$$

Finally, the switch opens again.

$$t_2 = 5.77 + 3 \ln \left( \frac{5 - 12}{9 - 12} \right) \quad (113)$$

$$= 8.31 \quad (114)$$

and

$$v_c(t) = 12 - 7e^{\left(-\frac{t-5.77}{3}\right)} \quad (115)$$

Therefore, our complete function is

$$v_c(t) = \begin{cases} 0 & t \leq 0 \\ 12 - 12e^{-\frac{t}{3}} & 0 \leq t \leq 4.16 \\ 4 + 5e^{-(t-4.16)} & 4.16 \leq t \leq 5.77 \\ 12 - 7e^{\left(-\frac{t-5.77}{3}\right)} & 5.77 \leq t \leq 8.31 \end{cases}$$

### Second-order Differential Equations

Consider the circuit shown in figure 34. By KVL, we see that

$$v_{in}(t) = v_C(t) + v_L(t) \quad (116)$$

and we also know, because  $i$  is the current through a capacitor,

$$i = C \frac{dv_C(t)}{dt} \quad (117)$$

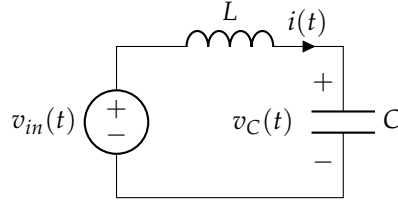


Figure 34: LC circuit

But wait! The voltage through the inductor is

$$v_L(t) = L \frac{di(t)}{dt} \quad (118)$$

$$= L \left( \frac{d}{dt} C \frac{dv_C(t)}{dt} \right) \quad (119)$$

$$= LC \frac{d^2 v_C(t)}{dt^2}. \quad (120)$$

That means

$$v_{in}(t) = LC \frac{d^2 v_C(t)}{dt^2} + v_C(t). \quad (121)$$

Yikes. This is a second order homogeneous equation. We can still solve it by assuming a homogenous solution of the form

$$v_{ch} = Ae^{\lambda t}, \quad (122)$$

But now substitution and cancellation yields

$$0 = LC\lambda^2 + 1 \quad (123)$$

as a characteristic equation, meaning

$$\lambda = \pm j \frac{1}{\sqrt{LC}}. \quad (124)$$

Well, this is no problem for us. To make things a little cleaner let's define  $\omega_o = \frac{1}{\sqrt{LC}}$  as the *natural frequency* of the LC circuit. Now what we have for a homogenous equation is

$$v_{ch} = A_1 e^{j\omega_o t} + A_2 e^{-j\omega_o t} \quad (125)$$

Via Euler's formula

$$e^{j\theta} = \cos(\theta) + j \sin(\theta), \quad (126)$$

we have that

$$v_{ch}(t) = A_1 (\cos(\omega_o t) + j \sin \omega_o t) + A_2 (\cos(-\omega_o t) + j \sin(-\omega_o t)). \quad (127)$$

With a little bit of algebraic manipulation, we find

$$v_{ch}(t) = B_1 \cos(\omega_o t) + B_2 \sin(\omega_o t). \quad (128)$$

What that means for our circuit is that the capacitor's voltage will oscillate back and forth sinusoidally, which is a pretty cool result.

It's incredible how often Euler's formula arises in the natural world, isn't it?

*RLC circuits*

Let's now introduce a resistor to the LC circuit. Consider figure 35, where resistor, inductor, and capacitor are in parallel. We can also

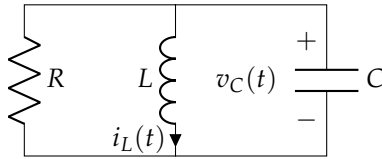


Figure 35: RLC parallel circuit

align the components in parallel, like in figure 36. In either case, the

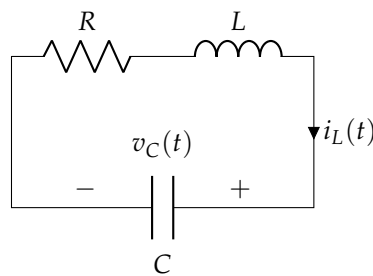


Figure 36: RLC series circuit

resistor dampens the sinusoidal response of the LC circuit. In the case of the parallel circuit of figure 35, as the resistance goes to infinity, the circuit starts to resemble just a plain LC circuit. In the case of the series circuit of 36, as the resistance goes to zero the circuit start to look more like an LC circuit. Deriving an ODE for both of these circuits is a wonderful exercise, give it a try and compare your result to the following expression.

$$F = \frac{d^2x(t)}{dt^2} + \frac{1}{\tau} \frac{dx(t)}{dt} + \frac{x(t)}{LC} \quad (129)$$

where  $\tau = \frac{L}{R}$  for series RLC circuits and  $\tau = RC$  for parallel. Finding the solution to the differential is another great exercise. Here is the characteristic equation:

$$0 = \lambda^2 + \frac{1}{\tau} \lambda + \frac{1}{LC} \quad (130)$$

and here is the general solution to the homogenous equation:

$$x_h(t) = A_1 e^{\lambda_1 t} + A_2 e^{\lambda_2 t} \quad (131)$$

Now the specific values of  $\lambda$  become very relevant, and give us three cases.

Consider how  $R$  affects the differential equation in both the series and parallel cases.

*Case 1:  $\lambda$  real* When  $\lambda$ s are real and distinct, the circuit is *overdamped*. There is no oscillation, and the function simply goes to zero and stops.

*Case 2: both  $\lambda$  identical* When  $\lambda_1 = \lambda_2$ , the circuit is *critically damped*. The signal in the circuit decays exponentially to zero.

*Case 3:  $\lambda$  complex* When  $\lambda$  are complex, they will be conjugates of one another and the circuit is *underdamped*. If  $\lambda$  is imaginary, then the circuit has no dissipation and will oscillate forever. If  $\lambda_1 = -\sigma_p \pm j\omega_d$  and  $\lambda_2 = -\sigma_p \mp j\omega_d$ , then we say  $\sigma_p$  is the attenuation factor and  $\omega_p$  is the damped resonance frequency.

Figure 37 shows each case plotted on the complex plane.

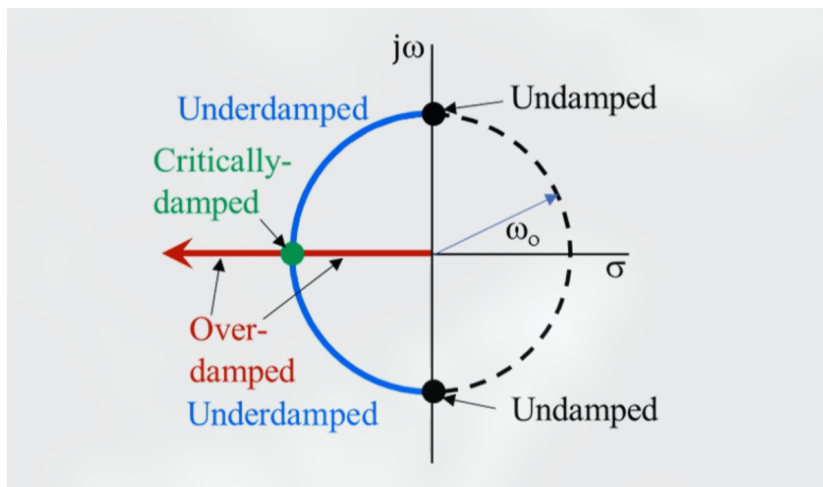


Figure 37: Damping cases on complex plane