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Section: 1

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Bilkent University Electrical and Electronics Engineering

EE202-Circuit Theory

Lab 4:

Voltage Waveform Generator

Introduction:

The purpose of this lab is to design a circuit that transforms square wave input into a desired shape with the help of RC and OPAMP circuits. I implemented two delay circuits. In these circuits, I used RC circuits to set the time delays and op-amps to amplify the voltage. Moving on to the integrator circuits, I used RC components and op-amps to shape the ramp waveforms. Finally, in the subtractor circuit, I combined all these elements to create the desired trapezoidal waveform.

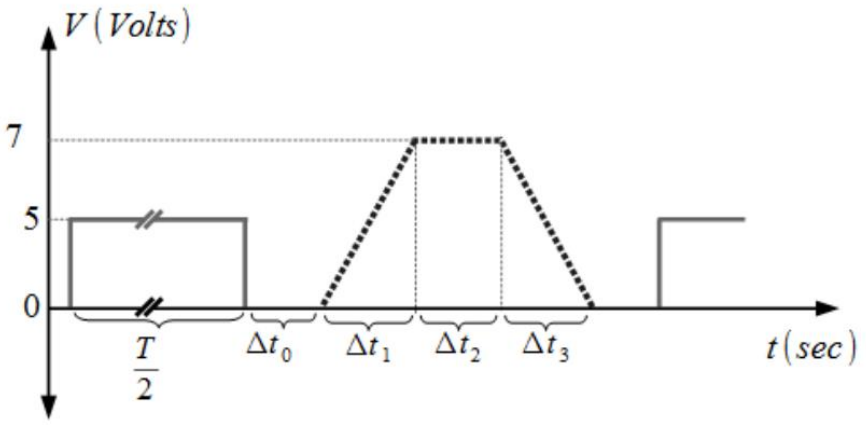

Figure 1: Input (solid gray line) is a square pulse. One period of the output is shown by dashed lines

Specifications are:

$\Delta t0 = 3\ ms, \quad \Delta t1 = 3\ ms, \quad \Delta t2 = 2\ ms, \quad \Delta t3 = 2\ ms$

Input peak voltage = 5 V

Output peak voltage = 7 V

Input frequency: $f < 50\ Hz, \quad T = \frac{1}{f}$

Part 1: Software Implementation

Analysis:

I took 20Hz for this lab in order to calculate the period easily and my input square wave is picked 5V amplitude. We need to create 3 ms (for $\Delta t0$) and 10 ms in total (3 + 3 + 2 + 2) delays to shift the wave. LM324 OpAmp will be used in this lab. Also, Vcc inputs for the OpAmp are as follows: Vcc+ = 8.5 V, Vcc- = 0 V, Vcomp = 2.5 V.

Part 1: Delay Circuits

For the delay, comparator OPAMP circuits are used. Also, note that, all of the OPAMP calculations will be done assuming that the OPAMPs are in the linear region. The delays are calculated as follows (can be checked whether the equations are correct from Figure 2):

By KCL,

$$C_1 . d\frac{V_{C1}}{d_t} + \frac{V_{C1} - V_{in}}{R_1} = 0 \quad \text{(eq. 1.1)}$$

$$d\frac{V_{C1}}{d_t} + \frac{V_{C1}}{R_1 C_1} = \frac{V_{in}}{R_1 C_1} \quad \text{(eq. 1.2)}$$

From eq. 1.2 if we consider the homogeneous part (for the natural response) of the differential eqution we have now eq. 1.3 and solving V_{C1} with respect to *t*, we end up with eq. 1.4 :

$$d\frac{V_{C1}}{d_t} + \frac{V_{C1}}{R_1 C_1} = 0 \quad \text{(eq. 1.3)}$$

$$V_{C1(homogenous)} = c_1 . e^{-\frac{t}{R_1 C_1}} \quad \text{(eq. 1.4)}$$

As for the particular solution (forced response), if we assume V_{in} as 5V,

$$d\frac{V_{C1}}{d_t} + \frac{V_{C1}}{R_1 C_1} = \frac{5}{R_1 C_1} \quad \text{(eq. 1.5)}$$

Therefore, the general solution is:

$$c_1 . e^{-\frac{t}{R_1 C_1}} + 5 = 0 \quad \text{(eq. 1.6)}$$

Considering with the inital conditions, since we know that at t = 0, Vc = 0:

$$V_{C1}(0) = c_1 . e^{-\frac{0}{R_1 C_1}} + 5 = 0 \quad \text{(eq. 1.7)}$$

$$c_1 = -5 \text{ found}$$

$$V_{C1}(t) = -5e^{-\frac{t}{R_1 C_1}} + 5 = 0 \quad \text{(eq. 1.8)}$$

(after inserting initial condition, $V_{C1}(t)$ is found)

There are two circuits creating 3 ms and 10 ms delay. V_{C1} must be equal to Vcomp at t = 3 ms and t = 10 ms to create delays. Inserting these values we get, for the first circuit with 3ms delay,

$$5 - 5e^{-\frac{3ms}{R_1 C_1}} = 2.5$$

(Note: During the calculations for second delay circuit take C_1 as C_2 and R_1 as R_2)

Time constant will be the value, $R_1 C_1 \cong 0.0043$

So, $R_1 = 100k\Omega$, $C_1 = 43nF$ picked

For the second circuit with 10ms delay,

$$5 - 5e^{-\frac{10ms}{R_2 C_2}} = 2.5$$

Time constant will be the value, $R_2 C_2 \cong 0.0144$

So, $R_2 = 43k\Omega$, $C_2 = 330nF$ picked

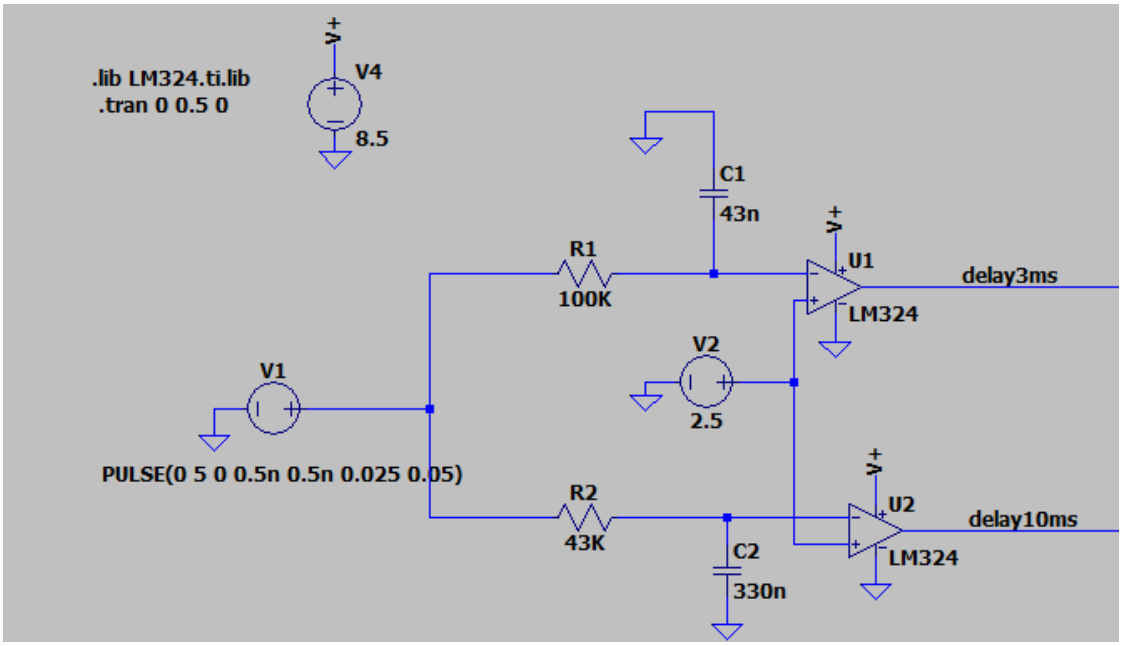

Figure 2: Delay circuits, top is 3ms delay circuit and bottom one is 10ms delay circuit

Part 2: Integrator Circuits

Following that, it was necessary to integrate the square waveforms to achieve a skew line in the provided graph. Using KCL again in the intagrator OPAMP circuit we obtain, (see Figure 3 for the calculations of the equations)

$$C_3 \,.\, d\frac{V_{C_3}}{d_t} + \frac{V_{\_} - V_{delay}}{R_3} = 0 \quad \text{(eq. 2.1)}$$

(both C_3 and C_4 can be used considering two integrator circuits for rest of the calculations also for R_3 and R_4 respectively)

(Vdelay is now the output of the delay circuits)

$$d\frac{V_{C_3}}{d_t} = \frac{V_{delay} - V_{\_}}{R_3 C_3} \quad \text{(eq. 2.2)}$$

$$V_{C_3}(t) = \frac{1}{R_3 C_3} \int (V_{delay} - V_{\_})dt \quad \text{(eq. 2.3)}$$

$$V_{C_3}(t) = \frac{t}{R_3 C_3} (V_{delay} - V_{\_}) + C \quad \text{(eq. 2.4)}$$

Now, isterting the initial condition, we can find constant values:

$$V_{C_3}(0) = 0 \text{ means } C = 0$$

The skew-lines are identical as the shape and delay, therefore component values will be same . When t = 3 ms ($\Delta t1$) Vmax=7 V. Therefore,

$$\frac{3ms}{R_3 C_3}(4.5) = 7 \text{ V}$$

So that, $R_3 C_3 = 0.5185 \times 10^{-3}$ and also,

$R_4 C_4 = 0.5185 \times 10^{-3}$ for the second integrator circuit

$$R_3 = 2.59k\Omega, \quad C_3 = 200nF$$

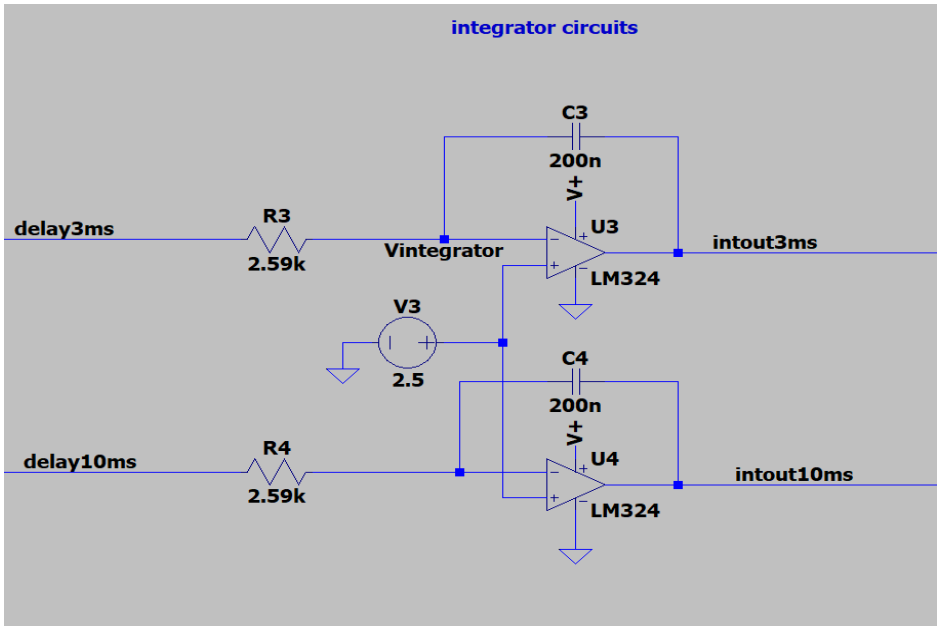

Figure 3: Integrator circuits

Part 3: Subtractor Circuit

For the final shape subtractor circuit is used, calculations based on my circuit is below (check Figure 4 for subtractor circuit calculations):

From KCL at V_ ,

$$\frac{V_- - V_{intout3ms}}{R_5} + \frac{V_- - V_{out}}{R_8} = 0 \quad \text{(eq. 3.1)}$$

$$V_- = \left(\frac{V_{intout3ms}}{R_5} + \frac{V_{out}}{R_8}\right)\left(\frac{1}{\frac{1}{R_5}+\frac{1}{R_8}}\right) \quad \text{(eq. 3.2)}$$

From KCL at V+ ,

$$\frac{V_+ - V_{intout10ms}}{R_6} + \frac{V_+}{R_7} = 0 \quad \text{(eq. 3.3)}$$

$$V_+ = \left(\frac{V_{intout10ms}}{R_6}\right)\left(\frac{1}{\frac{1}{R_6}+\frac{1}{R_7}}\right) \quad \text{(eq. 3.4)}$$

Since OPAMP is in the linear region, V+ = V- . Therefore,

$$\left(\frac{V_{intout3ms}}{R_5} + \frac{V_{out}}{R_8}\right)\left(\frac{1}{\frac{1}{R_5}+\frac{1}{R_8}}\right) = \left(\frac{V_{intout10ms}}{R_6}\right)\left(\frac{1}{\frac{1}{R_6}+\frac{1}{R_7}}\right) \quad \text{(eq. 3.5)}$$

Resistances are chosen as $R5 = R6 = R7 = R8$, then, equation becomes:

$$Vout = Vintout10ms - Vintout3ms$$

Resistances are chosen as $R5 = R6 = R7 = R8$ = 100Ω fort he circuit.

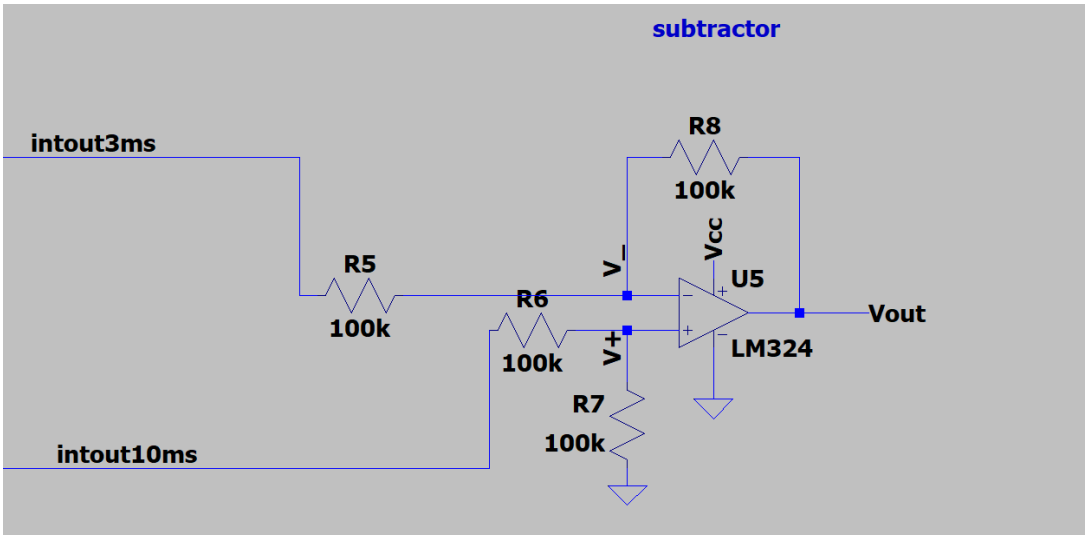

Figure 4:Subtractor Circuit

Simulations:

Initially I created the circuit with the values I derived from the equations (Figure 5). However, simulation results didn't match with the desired time delay range. In order to lower the simulation error, I had to make changes on the capacitance or resistance values on my final circuit by trial and error (in Figure 6 revised circuit is given).

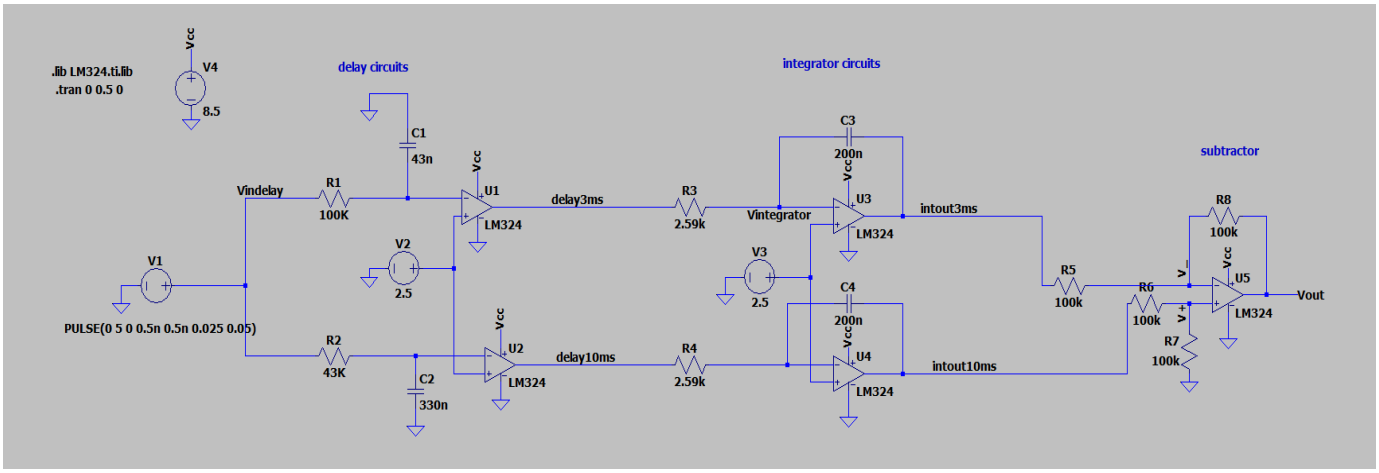

Figure 5: Whole Circuit Before the Revisions

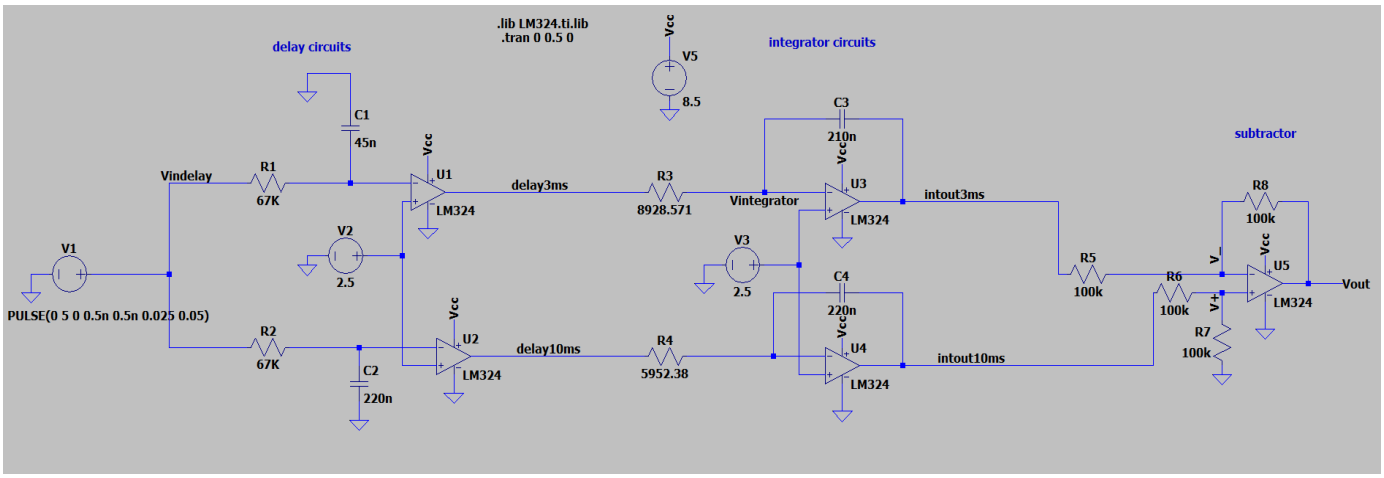

Figure 6: Whole Circuit After the Revisions, Lowering the Error

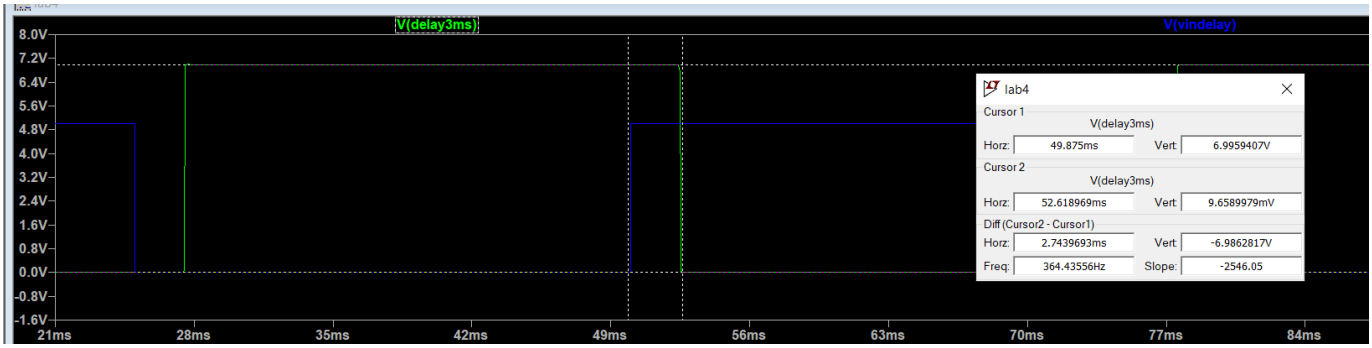

Figure 7: Simulation of the Output of 3ms delay circuit, t = 2.74ms measured

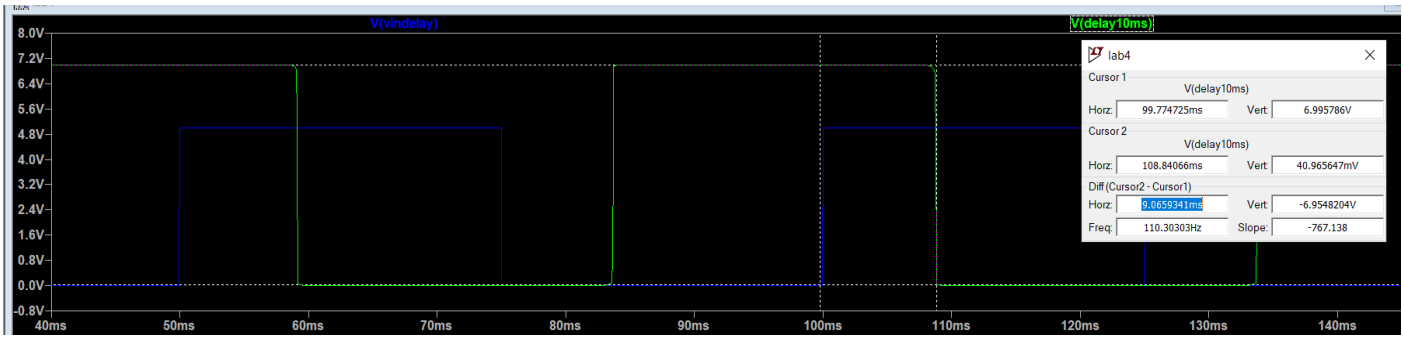

Figure 8: Simulation of 10ms delay circuit, t = 9.066ms measured as an output

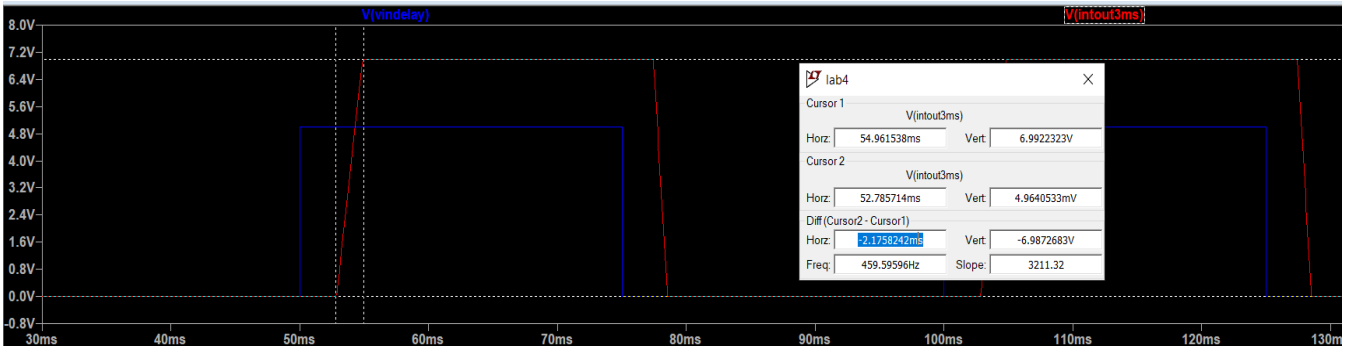

Figure 9: Simulation of the output of first integrator circuit, t = 2.16ms measured

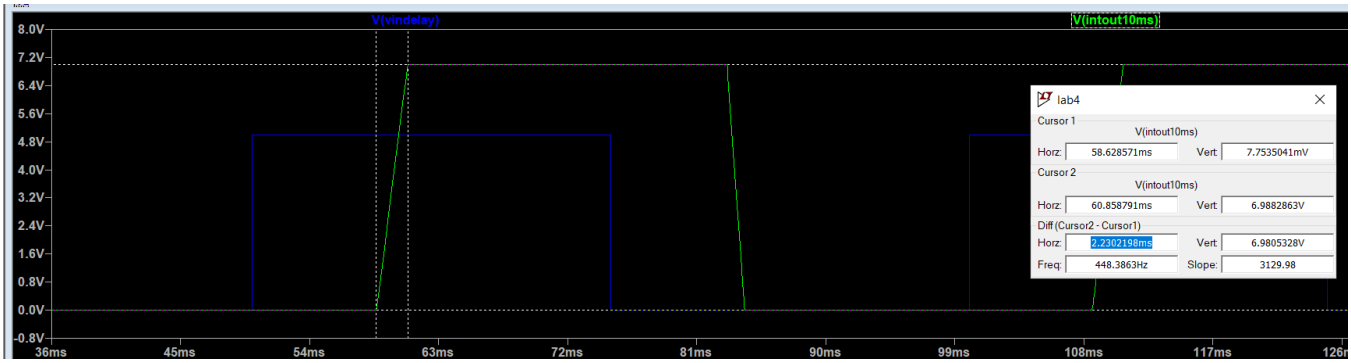

Figure 10: Simulation of the output of second integrator circuit, t = 2.23ms measured

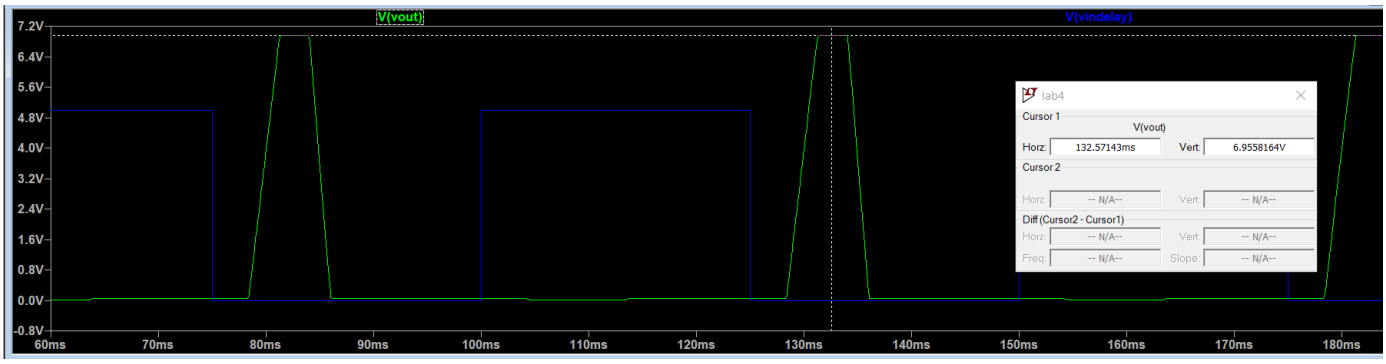

Figure 11: Input and output voltages shown, Vout = 6.96V

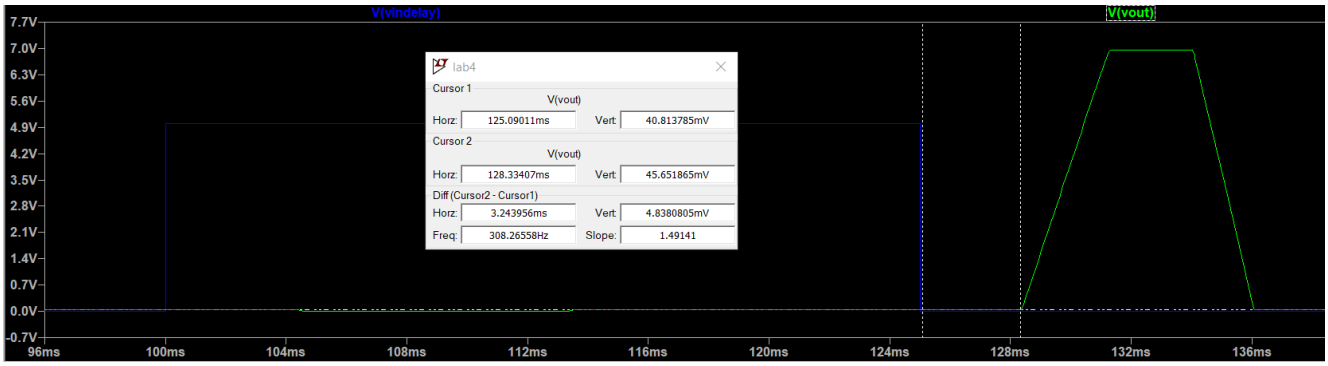

Figure 12: $\Delta t_0 = 3.24$ ms

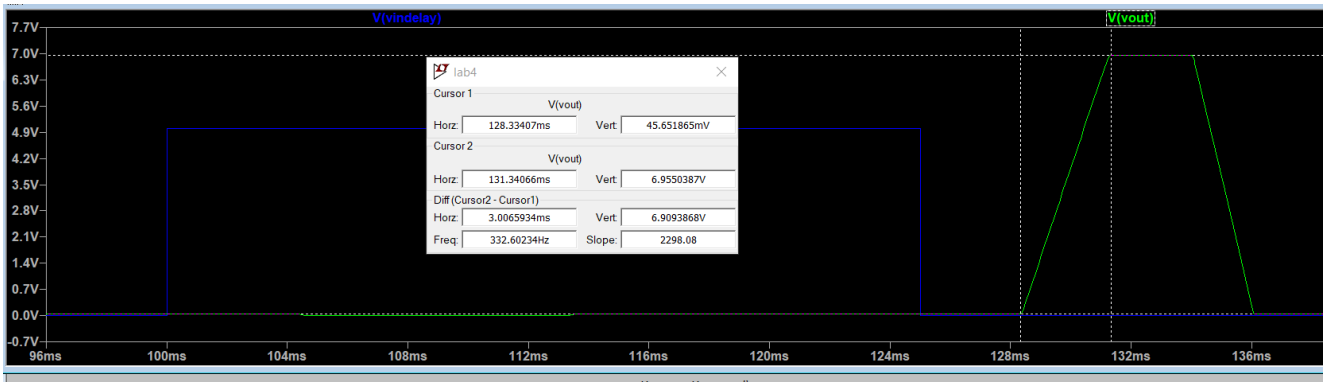

Figure 13: $\Delta t_1 = 3.01$ ms

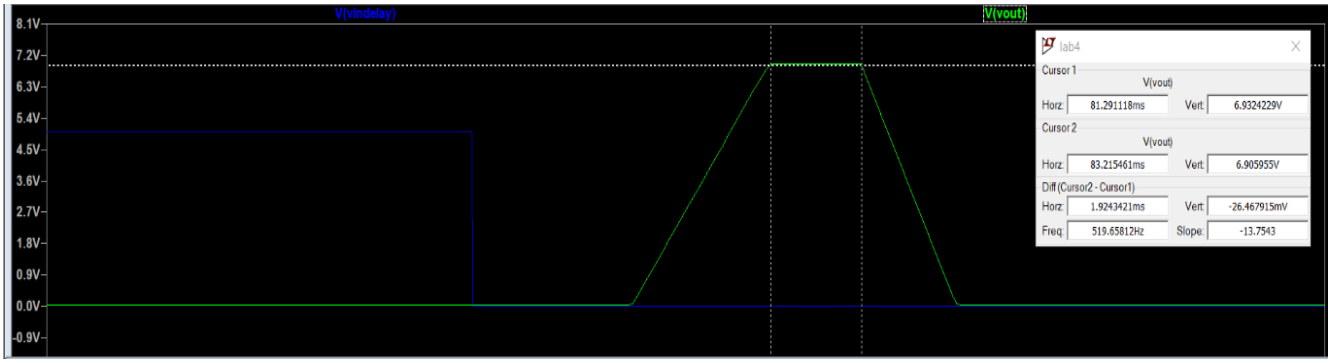

Figure 14: $\Delta t_2 = 1.92$ ms

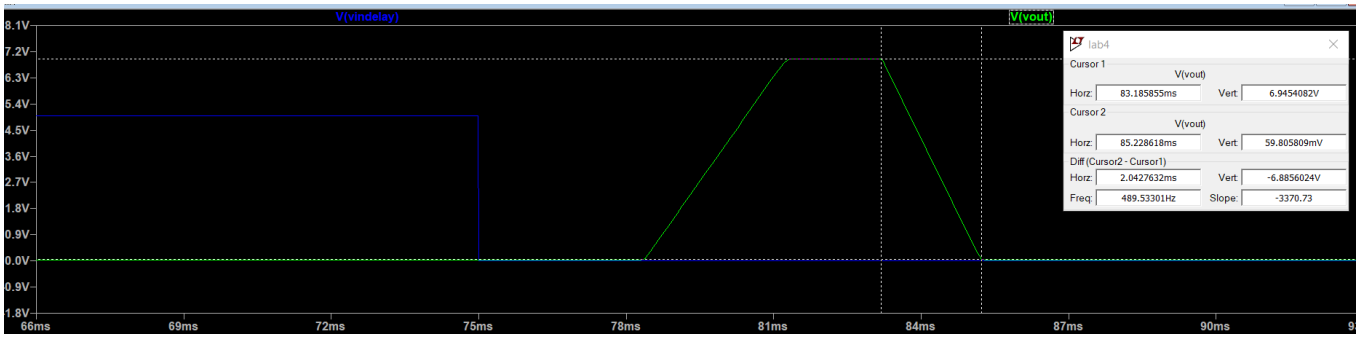

Figure 15: $\Delta t_3 = 2.04$ ms

	Theoretical Value (ms)	**Simulation Result (ms)**	**Error Percentage (%)**
Δt_0	*3*	*3.24*	*8*
Δt_1	*3*	*3.01*	*0.33*
Δt_2	*2*	*1.92*	*4*
Δt_3	*2*	*2.04*	*2*
$\Delta t_0+\Delta t_1+\Delta t_2+\Delta t_3$	*10*	*10.21*	*2.1*

Table 1: Error percentage for the simulation results

Error percentages are below the limit of 10%, therefore, expects the lab requirements.

Part 2: Hardware Implementation

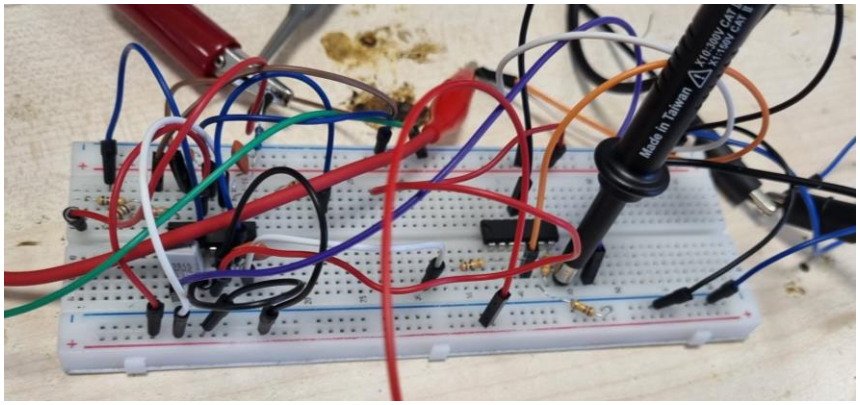

Figure 16: Hardware Implementation

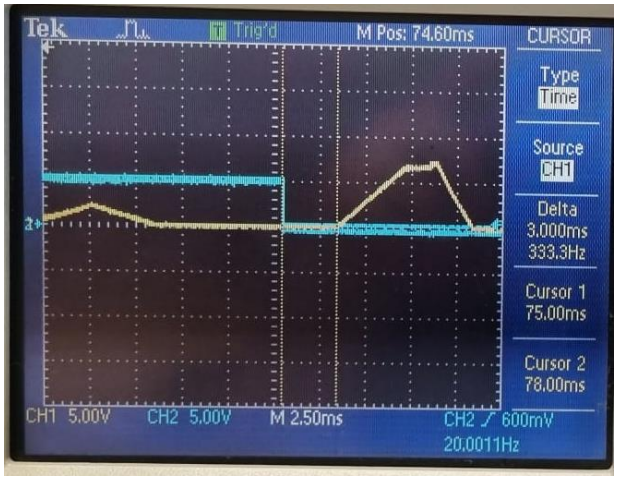

Figure 17: Δt_0 in hardware result, Δt_0 = 3ms

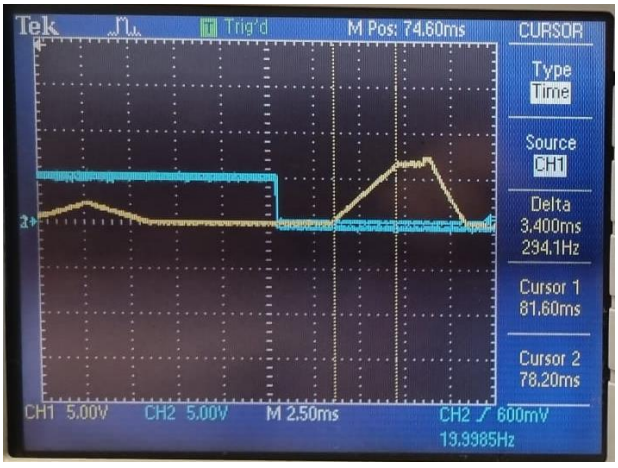

Figure 18: Δt_1 in hardware result, Δt_1 = 3.40 ms

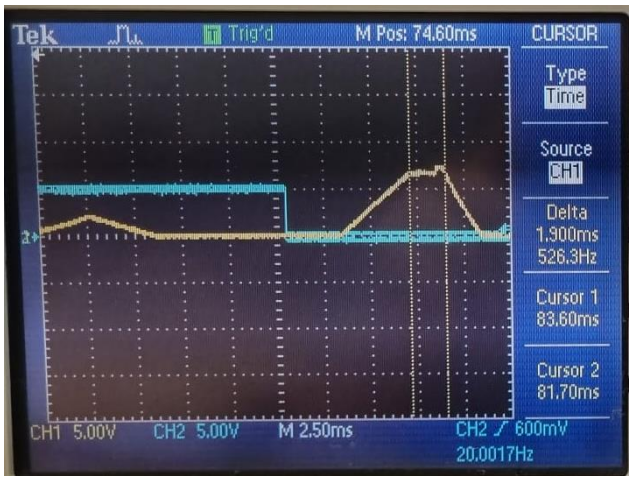

Figure 19: Δt_2 in hardware result, Δt_2 = 1.90 ms

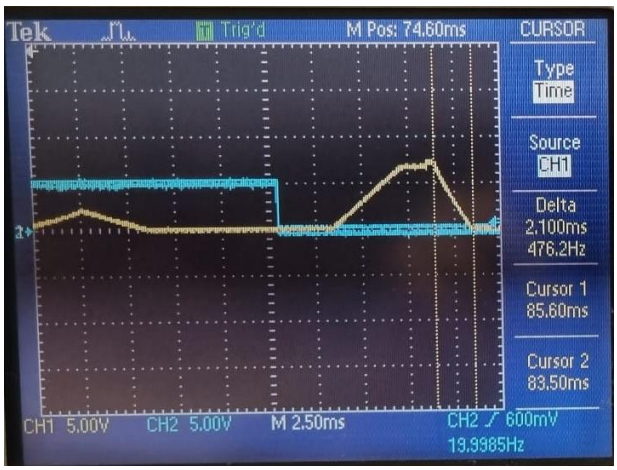

Figure 20: Δt_3 in hardware result, Δt_3 = 2.10 ms

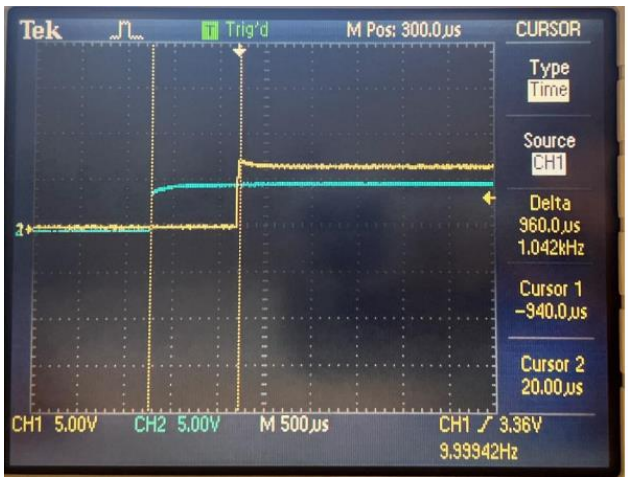

Figure 21: Hardware Output of the first delay circuit

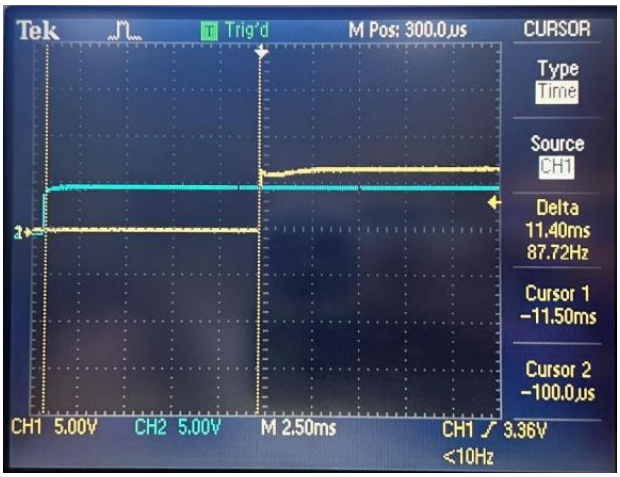

Figure 22: Hardware Output of the second delay circuit

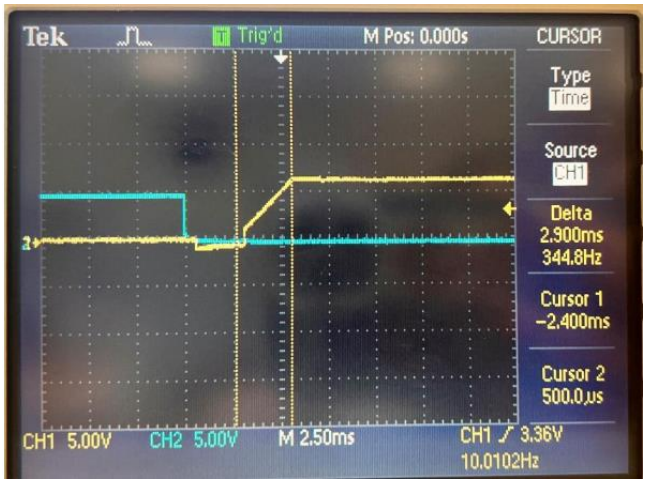

Figure 23: Hardware output of the first integrator circuit

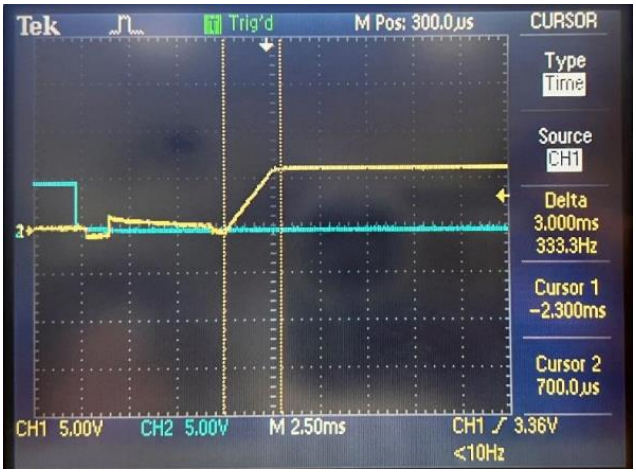

Figure 24: Hardware output of the second integrator circuit

All parts are implemented on a breadboard. Signal generator used with 2.5Vpp pulse input and 1.25 Vpp Dc offset to delete the negative part of the output. DC supply used for Opamps with 8.5 and 0 Volts.

	Theoretical Value (ms)	Hardware Result (ms)	Error (%)
Δt_0	3	3	0
Δt_1	3	3.4	13.3
Δt_2	2	1.9	5
Δt_3	2	2.1	5
$\Delta t_{0+}\Delta t_1+\Delta t_2+\Delta t_3$	10	10.4	4

Table 2: Error percentage for the hardware results

Error percentages are below the desired maximum percenatge so, it is satisfies the requirements.

Conclusion:

All of the results in hardware part meets the expectations (errors vary between 0-13.3 %) of both simulations (simulation errors vary between 0.33-8 %) and calculations made in the analysis part. However, erros could be due to our LM324 OPAMP is not ideal, our signal generator was slighty changing its voltage that it applied. Also, we were using 2 LM324 ICs in order to use 5 different Opamps so that we needed lots of jumpers and cables that are known to cause errro in real life experiments. Furthermore, in the hardware part, I didnt't use the exact same resistance and capacitance values because in lab, there are only standard values. This could be the reason of errors also. This lab taught us how to use Opamps in both saturation mode and linear region. Also, I learned how to create desired outputs manipulating the input wave with the help of different kind of Opamps circuits. In the hardware part, connecting lots of pins and jumpers and feeding all opamps with crocodiles was way hard because when I got a big error, chechking where this error could be stem from and changing the circuits was challenging. Also, in both simulation and hardware parts manipulating the total output and delays were again really challenging the reason why there are many circuits connected to ecah other and therir outputs affect ecah otheras an input. So the relatively small errors in the intermediate steps affect way more in the overall output.

References

https://github.com/MelihKutayYagdereli/EEE-202-Circuit-Theory/blob/main/LAB%204.pdf

Book-Electric-Circuits-9th-ed-J.-Nilsson-S.-Riedel-Prentice-Hall-2011.pdf