Name: Ezgi

Surname: Demir

ID: 22103304

Date: 26.03.2024

EE313-Electronic Circuit Design
Lab3 Preliminary
Push-pull Class-B Power Amplifier

Preliminary Work

In this lab, the design and implementation of a complementary push-pull Class-B power amplifier have been undertaken. This amplifier aims to deliver a minimum of 2.25W to an 8.2Ω resistive load while operating within specified voltage and frequency ranges. Through careful consideration of component selection, circuit configuration, and performance criteria, the objective is to achieve not only the desired power output but also to ensure harmonic distortion remains well below acceptable thresholds, power consumption is minimized under quiescent conditions, and overall efficiency is optimized across the operational range.

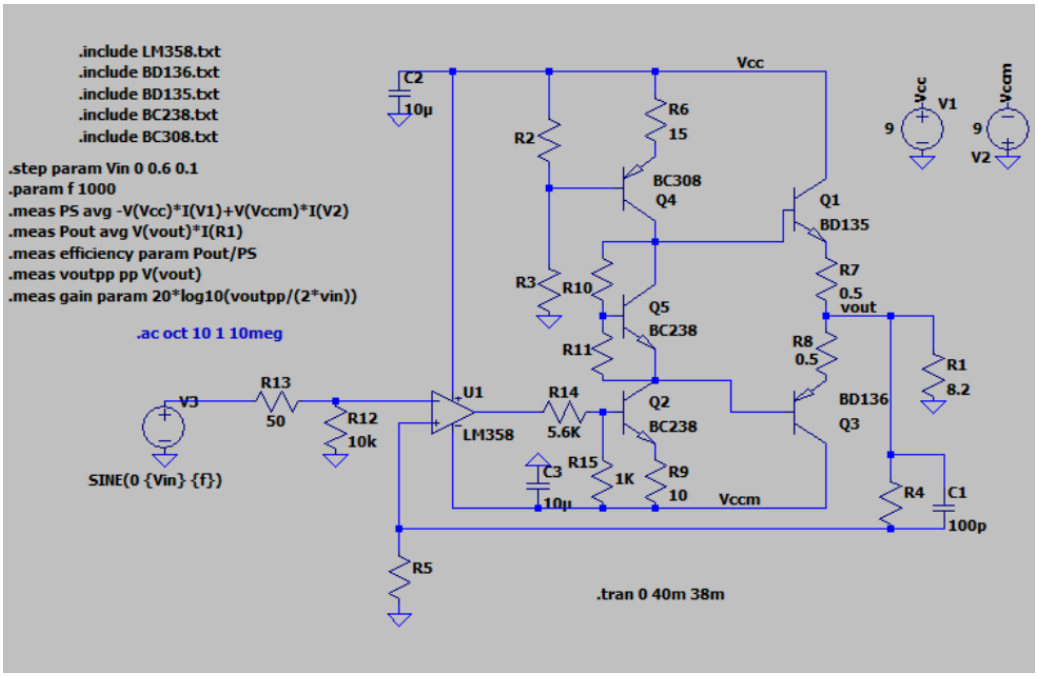

Figure 1: The main circuit where we need to find the appropriate values

First I checked whether I had an stability problem in my circuit, I removed the feedback loop and the OPAMP.

The DC offset voltage of the input voltage should be carefully adjusted (by trial and error) to keep the quiescent output voltage at zero.The input voltage source is now substituting the output of the opamp and now, we are acting like feedback. We are given a a circuit below:

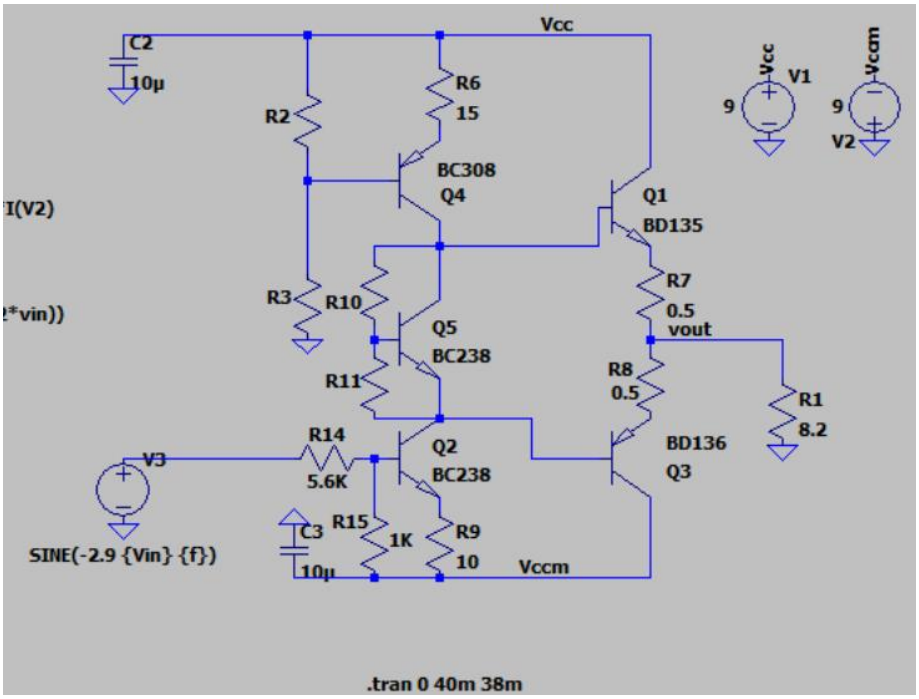

Figure 2: Circuit for solving crossover distortion

Checking the output behavior of this circuit we decided the R10 and R11 values. If we choose R10 too low,we get a croosover distortion. But with the proper value of R10 the voltage transition should be softer. And also from the lab manual we know, R10 and R11 needs to have the relation:

$$V_{CE} \approx \left(1 + \frac{R10}{R11}\right) V_{BE} \quad \text{(eqn. 1)}$$

Also ,the VCE of Q5 should be about twice that of VBE, so that we conclude R10 and R11 has to be very close to each other! I start with taking them both 4.7k and 4.7k. However, when we take them equal I got my Ps very high, not satisifying the 3rd specification (quiescent condition power consumtion). But when I lower R10 little bit but while staying in the not distortion region, I got lower Ps value only in the quiescent condition an at the same time I got more accurate emitter current (Figure 3 and 4) for Q1 and Q3 (which are BD135 npn and BD136 pnp power transistors). (Q4 acts like a curent source).

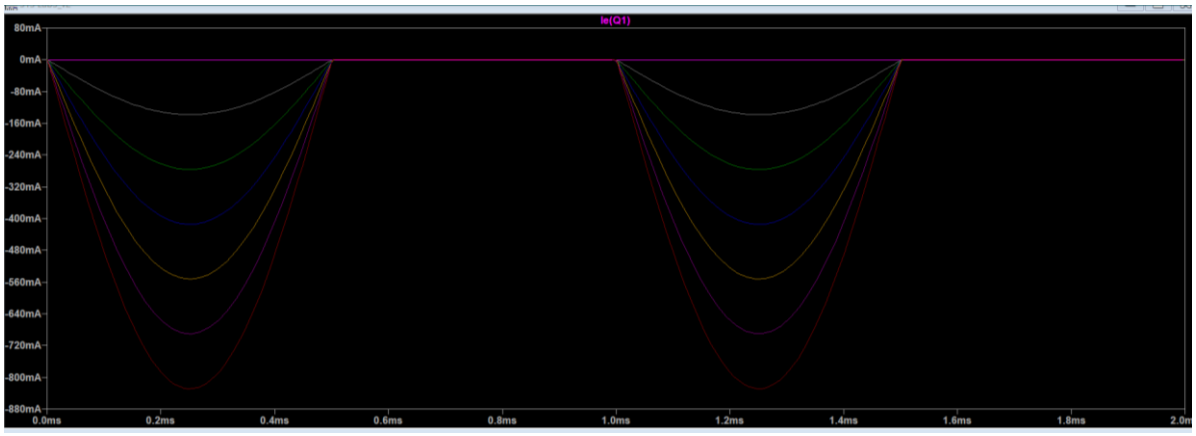

Figure 3: Emitter current of Q1

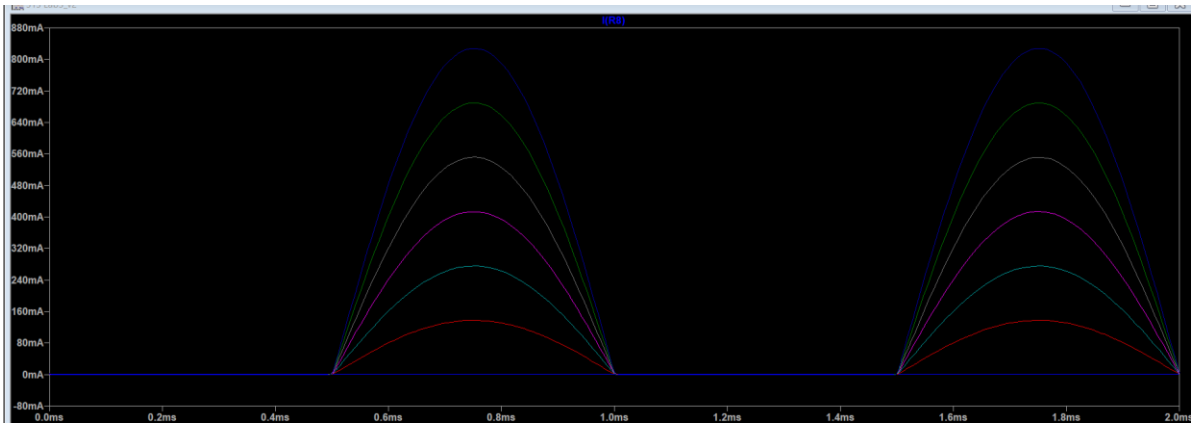

Figure 4: Emitter current of Q3

The current is zero for half the period as expected.

After distortion is solved, I started to give some arbitrary values for the resistors R2, R3, R4 and R5, which I observe they are affecting the efficiency of the circuit, Pout (power dissipation), Ps (input power) and the regions bjt's are working so that the shape of the sine wave we are given as input. I arranged the supply voltage to be at most ±9V. I expected the sinusoidal voltages operate between 10Hz and 20KHz with a gain between 15 dB and 25 dB. With some trail and error I concluded with the below circuit:

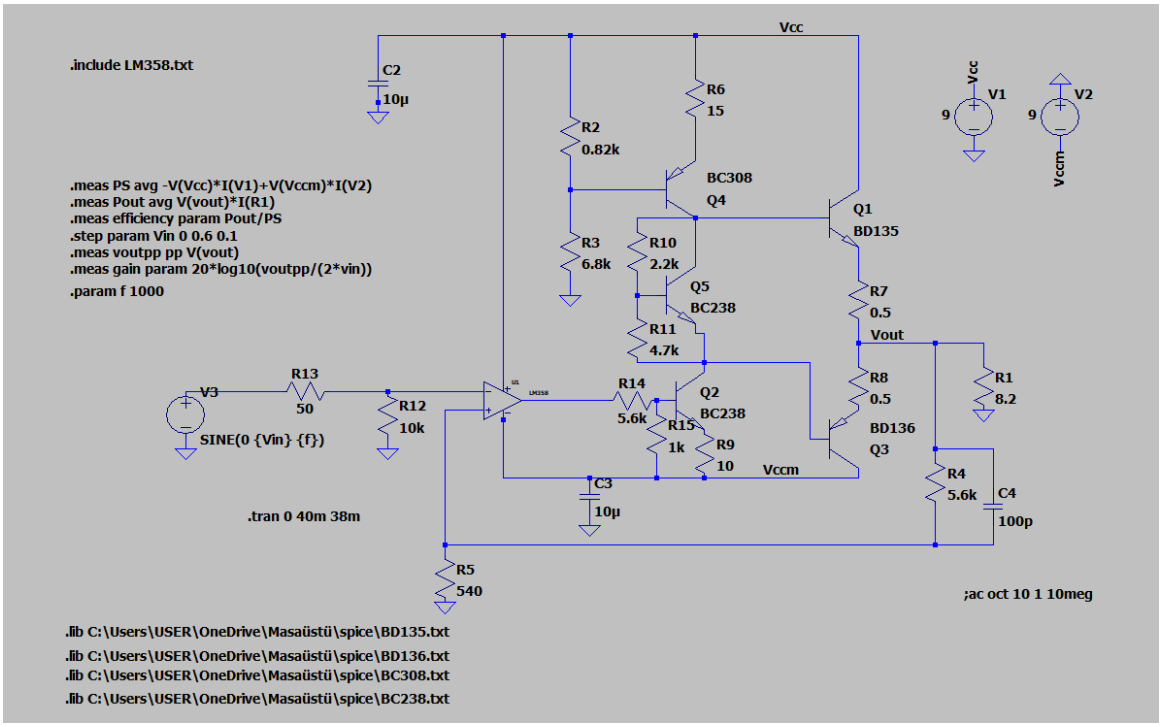

Figure 5: Overall Circuit Design

Now, Let's check whether our circuits obeys the specifications we are given.

Specifiaction 1

The amplifier should deliver at least a 2.19W power to an 8.2Ω resistance (12Vpp to an 8.2Ω power resistor) starting from 10Hz to 40KHz at the chosen gain value.

We take Vin starting from 0 to 0.6 with the steps of 0.1 with the command .step param Vin 0 0.6 0.1. But we are checking the 0.6V input, so we will check the last term of the table. As seen below table, we fist made sure that our circuit delivers approximately 2.25W at 1kHz frequency (because initially we are starting from this frequency) then we continue checking specific frequency values whether our power is lower than 2.19W or not.

.param f 1000

Measurement: pout

step	AVG(v(vout)*i(r1))
1	1.29946e-006
2	0.0779027
3	0.311304
4	0.700383
5	1.24523
6	1.94586
7	2.80325

.param f 10

Measurement: pout

step	AVG(v(vout)*i(r1))
1	1.29946e-006
2	0.0640243
3	0.25457
4	0.571441
5	1.01513
6	1.58581
7	2.28235

.param f 2000

Measurement: pout

step	AVG(v(vout)*i(r1))
1	1.29946e-006
2	0.0775223
3	0.310075
4	0.697673
5	1.24041
6	1.93791
7	2.79051

.param f 5000

Measurement: pout

step	AVG(v(vout)*i(r1))
1	1.29946e-006
2	0.0759973
3	0.303457
4	0.682658
5	1.21377
6	1.90114
7	2.75035

.param f 10000

Measurement: pout

step	AVG(v(vout)*i(r1))
1	1.29946e-006
2	0.0750492
3	0.300337
4	0.677499
5	1.21147
6	1.9022
7	2.74978

.param f 20000

Measurement: pout

step	AVG(v(vout)*i(r1))
1	1.29946e-006
2	0.0747432
3	0.298748
4	0.672155
5	1.20526
6	1.89028
7	2.73313

.param f 40000

Measurement: pout

step	AVG(v(vout)*i(r1))
1	1.29946e-006
2	0.0734149
3	0.291117
4	0.6578
5	1.17406
6	1.83678
7	2.65532

So, specification 1 satisfied.

Specifiaction 2

The harmonics (the highest is possibly the third harmonic) at the 2.25W output power level should be at least 40 dB lower than the fundamental signal at 1 KHz.

To check this we need to simulate with 20 cycles visible on the plot window. Then, right-click on the plot window, View → FFT, to see the amplitude of different harmonics.We can find the dB difference between the fundamental (at 1 KHz) and the third harmonic (at 3 kHz).

Here is my plot look like:

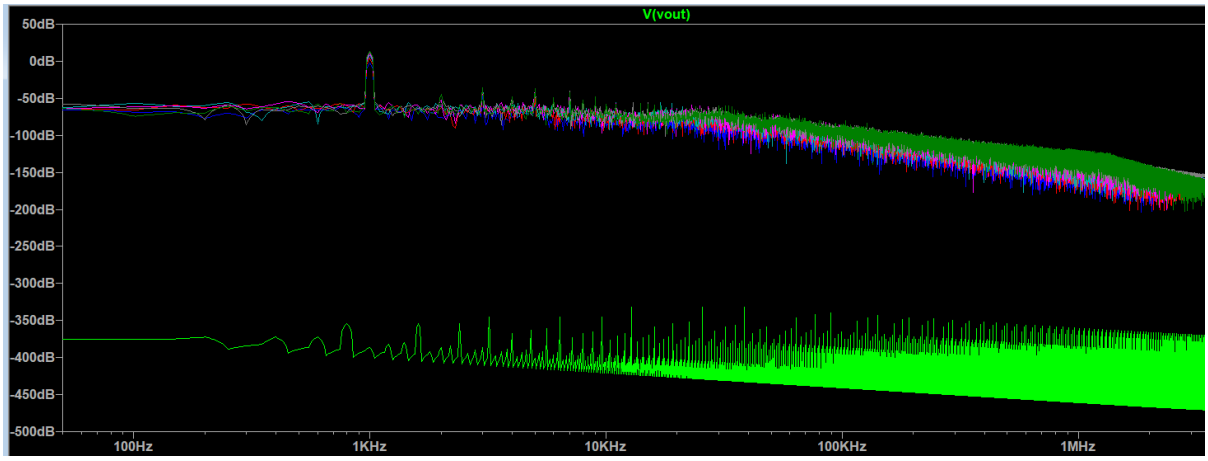

Figure 6: dB Difference

Specifiaction 3

The power consumption at quiescent conditons should be less than 500mW.

In an amplifier circuit, the quiescent condition is the state when there is no input signal applied, and the amplifier is simply maintaining its operating point or biasing conditions. During quiescence, the amplifier consumes power , but it does not produce any significant output signal. The input power that we needed to check with zero input with the command .meas PS avg -V(Vcc)*I(V1)+V(Vccm)*I(V2). (At 1kHz)

```
Measurement: ps
  step            AVG(-v(vcc)*i(v1)+v(vccm)*i(v2))
     1            0.326134          0
     2            1.09904           0
     3            1.8815            0
     4            2.66337           0
     5            3.44445           0
     6            4.22479           0
     7            5.00449           0
```

Figure 7: Ps = 326mW when Vin=0V

Specifiaction 4

The amplifier's overall efficiency (output power/total supply power) should be at least 45% at max power output at 1KHz.

Efficiency is calculated with the ratio of output power and total supply power which is:

$$\eta = \frac{P_{out}}{P_s} \quad \text{(eqn. 2)}$$

Measurement: efficiency	
step	pout/ps
1	3.98444e-006
2	0.0708822
3	0.165455
4	0.262969
5	0.361517
6	0.460582
7	0.560146

Figure 8: Efficiency is calculated about 56%

Efficiency is calculated about 56% which is higher than 45% and meeting the expectations.

Lastly, here is my Vout plot and Vout values with respect to given Vin:

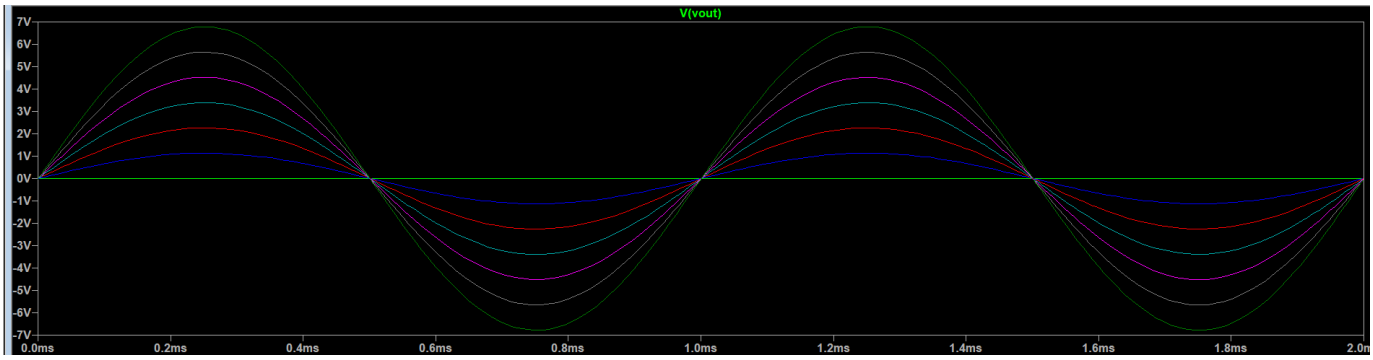

Figure 9: Vout Plot

Measurement: voutpp	
step	PP(v(vout))
1	0
2	2.26105
3	4.51995
4	6.78057
5	9.04478
6	11.3059
7	13.5663

Figure 10: Vout peak to peak values, Vout= 13.566V

At the max level of Vout has be around 12Vpp as we are expected. In my observations I see a little higher than that will higher the efficiency and Pout so that they satisfy the expectations.

My gain was always between 15 and 25dB as required and never changed that much while I am doing trial and error.

Measurement: gain

step	20*log10(voutpp/(2*vin))
1	-1.#IND
2	21.0656
3	21.0615
4	21.0623
5	21.0662
6	21.0661
7	21.0656

Figure 11: Gain values, 21dB

Conclusion

The design and testing process of a complementary push-pull Class-B power amplifier was required to deliver a minimum of 2.25W to an 8.2Ω resistive load over a frequency range of 10Hz to 40KHz, with specific criteria for harmonic distortion, quiescent power consumption, and overall efficiency. Through careful component selection and circuit configuration, the amplifier successfully met all specified requirements.The report discusses the iterative process of circuit design, including stability checks and adjustments to component values to optimize performance. Simulation results and measurements were used to verify the amplifier's compliance with specifications, including power output, harmonic distortion levels, quiescent power consumption, and efficiency. By engaging in this lab, I not only deepen their understanding of amplifier design principles but also develop the practical skills and problem-solving abilities necessary.

#	Name	RefDes	Value
1	CAP100RP	C2, C3	10u
2	CAP100	C4	100p
3	BD135	Q1	
4	BC238	Q2, Q5	
5	BD136	Q3	
6	BC308	Q4	
7	CFR25SJR-52-100K	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15	
8	LM358N	U1	

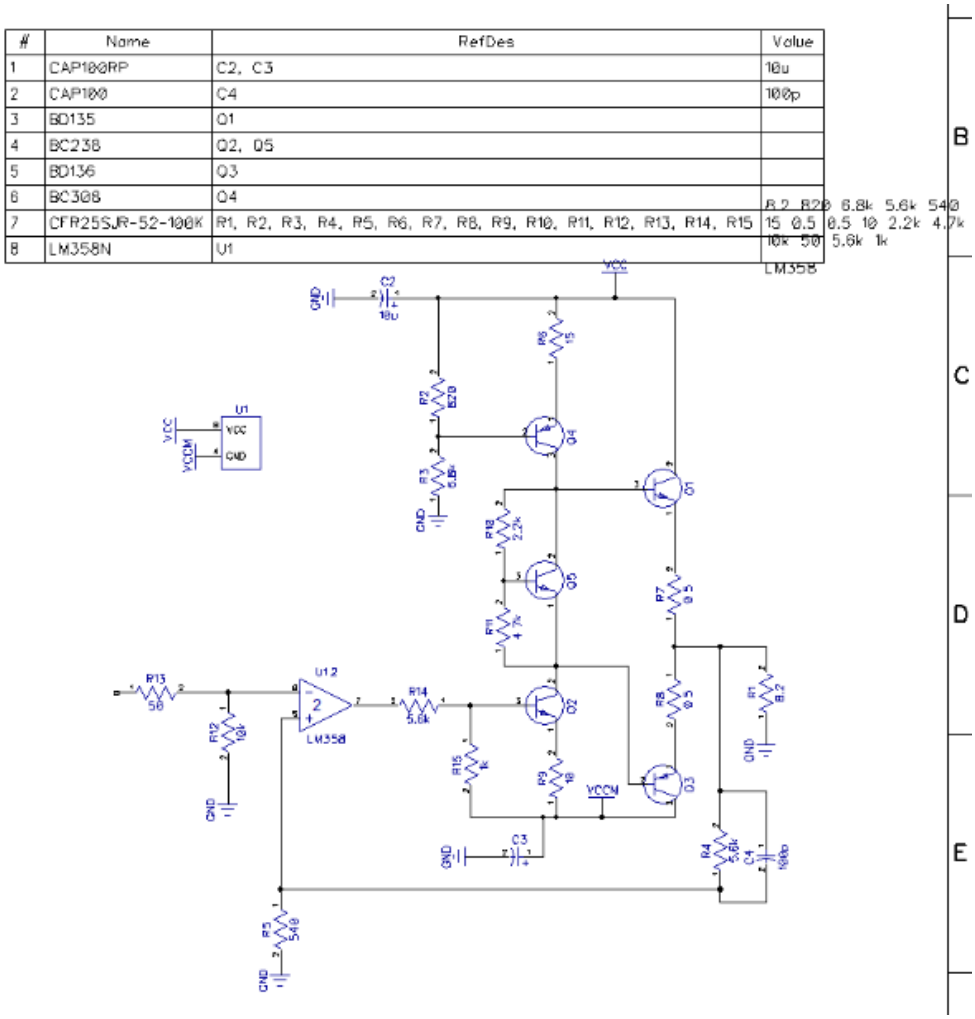

Figure 12: DipTrace Schematic of my Circuit

References

https://moodle.bilkent.edu.tr/2023-2024-spring/pluginfile.php/78197/mod_resource/content/1/BD136.txt

https://moodle.bilkent.edu.tr/2023-2024-spring/pluginfile.php/97549/mod_resource/content/1/Lab3Hints.pdf

https://moodle.bilkent.edu.tr/2023-2024-spring/pluginfile.php/93138/mod_resource/content/3/Lab3.pdf

https://www.electronicdesign.com/technologies/power/whitepaper/21215797/electronic-design-what-is-the-essence-of-quiescent-current

Lecture notes from İnstructor Abdullah Atalar, Spring 2024