**Title:** Lab 1 – Introduction to Xilinx Webpack

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**Date:** 11/7/13

**Class:** ECE 2029 B03

**Introduction:**

The goal of this lab was to become familiar with the Xilinx Webpack design solution by implementing a simple circuit using a schematic and then repeating the process with Verilog code.

We designed and implemented AND, OR and XOR gates connected to the same inputs (switches) and different outputs (LEDs). We also used an inverter controlling a fourth LED attached to one of the common inputs. We implemented this first using a schematic, and then with Verilog code.

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Objectives of the lab & overview of accomplishments

**Discussion and Results:**

Creating the Schematic implementation of a simple circuit:

We set up a new project in the Xilinx Webpack to be designed for the Nexys 3 (Xilinx Spartan6 architecture) and used the ISim simulator. We also set the top-level source to be “Schematic”.

We created a new source file (type Schematic).

In this file we added an AND2 gate, an OR2 gate, an XOR2 gate, and an inverter.

We added short wires to the ends of each of the gates’ inputs and outputs.

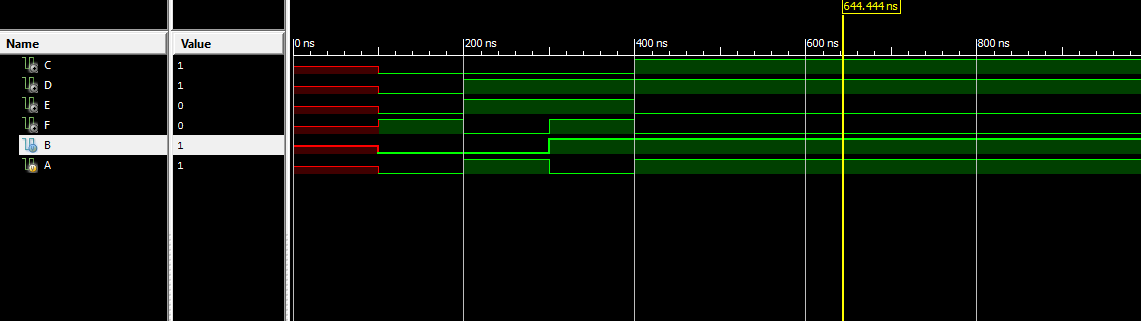
For each gate, we made one of the input wires “A”, and the other “B”, except for the inverter, which we only connected to “A”.

We then made an IO marker on the AND2 gate’s inputs. We also created and named the outputs of the gates “C”, “D”, “E”, and “F” for the AND2, OR2, XOR2, and INVerter respectively.

#Picture# (small) – of schematic

We than created a Verilog Test Fixture and added the code from the lab description (which runs an exhaustive test on the two inputs and pausing 100 ns between changes).

We than ran an ISim Behavioral model simulation with the following result:



The simulator matched the expected results.

##What more can I say??

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Thorough walkthrough of procedure, approach to problem, results discussed.

\*Include new code\* (& screenshots of test benches)

**Summary and Conclusion:**

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Wrap up & summarize work

Describe how conclusions follow from data presented

**Appendices:**

Include all new Verilog code in Monospace font (Courier 9-10 pt)

Both Prelabs