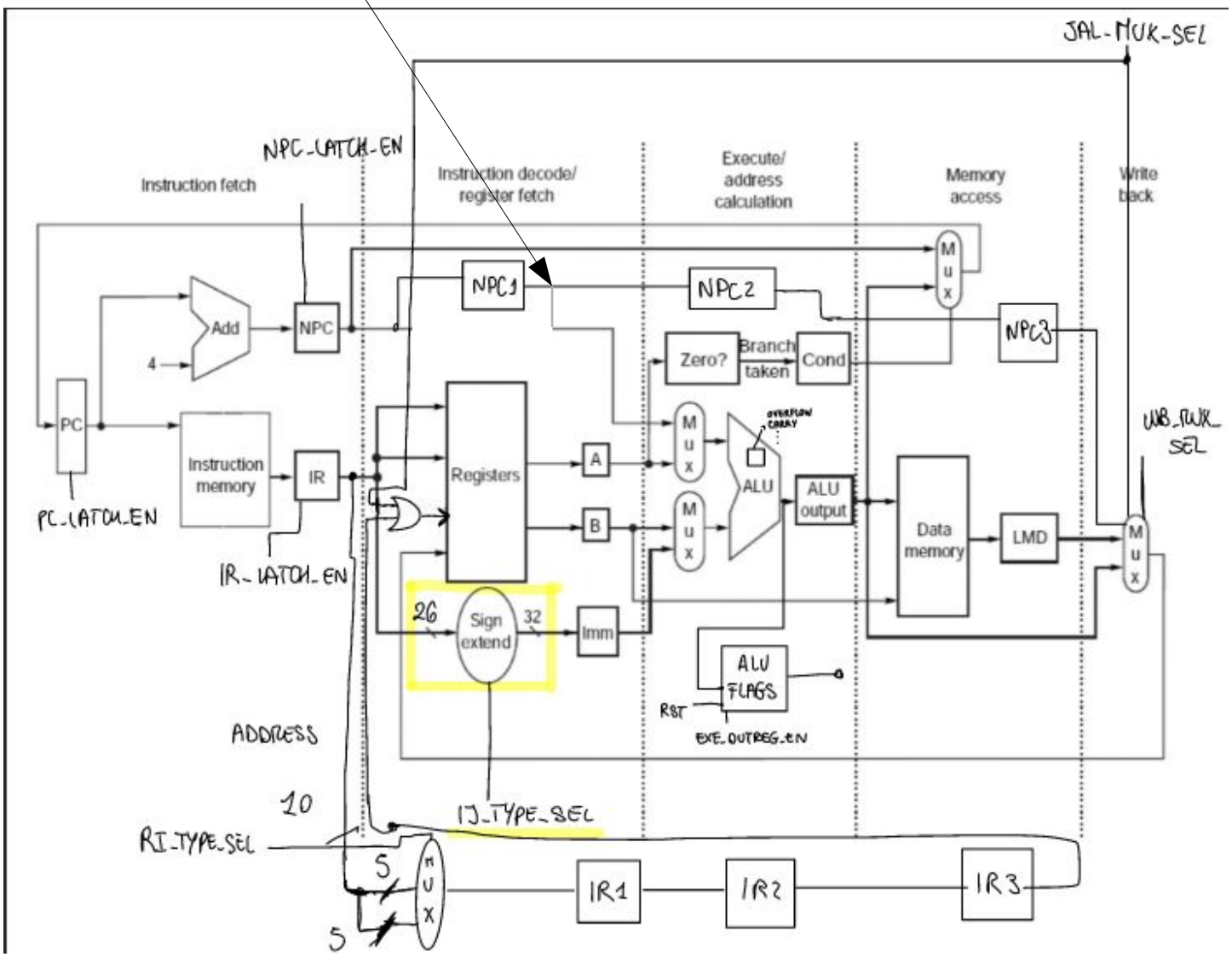
Q1: Should we do this instead of the given data path?



Q2: We already have two registers in the Register File, do they replace registers A and B? In case no, they should be deleted because it would take two clock cycles to have the data at the output of A and B registers

Q3: RF should be change in the case enable = 0. It should keep the output at the output registers as the others registers in the pipeline

Q4: should we put a control when trying to write the reg 0? I've already done it