Faculty of Engineering
MODULE DESCRIPTION FORM

EO303 Digital electronics and embedded systems

Module Registrar: Paul Murray		**Taught To (Course):** 3rd year Graduate Apprentice	
Other Staff Involved: Paul Murray, Andrew Campbell, Fraser MacFarlane, Stuart Bennet		**Credit Weighting:** 20 (ECTS 10)	**Semester:** Term 3
Assumed Prerequisites: EO204 Electronic and Electrical Engineering Systems 1		**Compulsory:** Optional	**Academic Level:** 3

Module Format and Delivery (Hours i.e. 1 credit = 10hrs of study):

Online	Online Tutorial	On-Campus Tutorial	Laboratory/ Studio /Workshop	Group Work	Assignments/ Assessment	Private Study	**Total**
30	28	2	20	0	40	80	200

Educational Aim

To introduce students to the fundamental concepts of digital electronics, and digital circuit design & analysis, and to learn practical skills in designing and testing digital circuits.

Learning Outcomes

LO 1: Become familiar with the different types of digital devices available (e.g. Field Programmable Gate Arrays (FPGAs), Application Specific Integrated Circuits (ASICs), processors, Application Specific Standard Parts (ASSPs)).

LO 2: Understand concepts of basic sequential circuits, including clock, enable and reset signals; types of flip-flops (and their functionality); and setup and hold times.

LO 3: Know how to design circuits based upon flip-flops, such as shift registers, counters, and Finite State Machines (FSMs), and understand the concept of holding state.

LO 4: Be familiar with the architecture and functionality of FPGAs and System-on-Chip (SoCs), and know how embedded systems can be implemented based on these devices.

LO 5: Gain familiarity with the use of software tools to design and test digital circuits (this will include graphical and code-based design entry), and the concept of the 'design flow'.

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Syllabus

Technology Context

Types of digital devices, their attributes, and how designs are created for them – including FPGAs, ASICs, ASSPs, and different types of processors. Consideration of the most suitable device type(s) for certain applications.

Sequential Circuit Elements

Latches, flip-flops and their operation. Expressing behaviour using next state equations, and state tables. Clock concepts and issues, including edge-triggering, and set-up and hold times. Functionality of enable, reset, and preset control signals.

Sequential Circuits

Registers, shift registers and counters. Working with circuit diagrams and timing diagrams.

Finite State Machines (FSMs)

Describing FSMS using state diagrams and state tables; Mealy and Moore FSM types; analysis of FSMs. Design and implementation of FSMs from a given specification. FSM optimisation.

FPGAs and SoCs

Introduction to the architecture and functionality of FPGAs and FPGA-based System-on-Chip (SoC) devices. Concepts of embedded systems.

Design Tools and Flows (focusing on FPGAs)

The role of Electronic Design Automation (EDA) tools. Examples of design entry methods, including Hardware Description Languages (HDLs). The concept of the 'design flow', and its constituent steps (simulation, synthesis, etc.).

Introduction to VHDL

Introductory concepts of the VHDL language for circuit design and writing testbenches.

Practical Design Case Studies

Designing and testing basic sequential circuits and FSMs using graphical tools. Writing VHDL code for digital circuits and testbenches. Specifying inputs and outputs. Following the steps of the design flow to achieve a design working on an FPGA development board.

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Assessment of Learning Outcomes

Criteria:
For each of the Module Learning Outcomes the following criteria will be used to make judgements on student learning:

LO1 *Become familiar with the different types of digital devices available (e.g. Field Programmable Gate Arrays (FPGAs), Application Specific Integrated Circuits (ASICs), processors, Application Specific Standard Parts (ASSPs)).*

C 1: The student should be able to describe the differences between common types of digital electronic devices.

C 2: The student should understand the suitability of different devices for given example applications, given factors such as power consumption, reprogrammability, parallelism, and economies of scale.

C 3: The student should appreciate that different methods of design entry are required, depending on the device type.

LO2 *Understand concepts of basic sequential circuits, including clock, enable and reset signals; types of flip-flops (and their functionality); and setup and hold times.*

C 1: The student should understand the operaton of different types of latches and flip-flops.

C 2: The student should be able to express the operation of latches and flip-flops using next state equations, transition tables, and waveforms.

C 3: The student should be familiar with clock and timing issues.

C 4: The student should know the functionality of control signals such as reset, clock enable, and preset.

LO3 *Know how to design circuits based upon flip-flops, such as shift registers, counters, and Finite State Machines (FSMs), and understand the concept of holding state.*

C 1: The student should understand the operation of shift registers and be able to design a shift register circuit.

C 2: The student should understand the operation of counters, and be able to design counter circuits.

C 3: The student should understand the operation of FSMs, and be able to express and analyse FSMs.

C 4: The student should understand how to develop a functional FSM based on an initial specification.

LO4 *Be familiar with the architecture and functionality of FPGAs and System-on-Chip (SoCs), and know how embedded systems can be implemented based on these devices.*

C 1: The student should have a basic awareness of the architectures of FPGAs and SoCs.

C 2: The student should understand the types of functionality offered by FPGAs and SoCs.

C 3: The student should be able to describe the basic building blocks of an embedded system based on one of these devices.

LO5 *Gain familiarity with the use of software tools to design and test digital circuits (this will include graphical and code-based design entry), and the concept of the 'design flow'.*

C 1: The student should be able to create designs for simple sequential circuits, and FSMs, using graphical tools for design entry.

C 2: The student should be capable of designing basic digital circuits using the VHDL language, creating appropriate testbenches for design verification, and running and interpreting simulations.

C 3: The student should know how to associate the inputs and outputs of a design with physical Input Output Blocks (IOBs) on the FPGA, using a constraints file.

C 4: The student should understand the concept of the 'design flow' and its constituent steps, and be able to complete all the steps to the point of programming the FPGA on a development board.

The standards set for each criterion per Module Learning Outcome to achieve a pass grade are indicated on the assessment sheet for all assessment.

12 Principles of Assessment and Feedback

A detailed explanation of the learning outcomes and their assessment is provided at the outset, reinforced by tailored feedback on performance in tutorials, online quizzes and laboratory sessions.

The individual topics and assessment structure are provided at the beginning of the course to encourage time management.

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Feedback is given regularly during staff-student interactions in on-campus days and through the online learning portal, providing opportunities for self-correction consistently throughout the module.

Peer interactions and staff-student interactions are integral components of tutorials and on-campus days, where group working and technical debate are encouraged.

Assessment Method(s) Including Percentage Breakdown and Duration of Exams

	Examinations			**Courseworks / Labs**		**Projects**	
	Number	Duration	***Max Marks***	Number	***Max Marks***	Number	***Max Marks***
	1	2	60%	9	10%	2	30%
L/Outcomes	LO1-5			LO1-LO5		LO1-LO5	

Coursework / Submissions deadlines: Advised on a regular basis through *Myplace.*

Resit Assessment Procedures:
Resubmission of assignment/coursework sections. Resit exam available in August (tbc). An absence during on campus days will be classed as an exam absence.

Recommended Reading

Additional Student Feedback

Date	**Time**	**Room No**
On-campus days	TBC	TBC

Session: 2019/20

APPROVED

Date of Last Modifications: 16 Jan 2018

Director of Teaching and Learning:

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MODULE TIMETABLE

Module Code:	EO303	**Module Title:**	Digital electronics and embedded systems

Brief Description of Assessment:

Assessment is carried out through a class test during the term and one written exam at the end of the term. Laboratory work is assessed based on worksheets which will each require logbook/mini lab reports and project work submission.

Assessment Timing

Term Three	WK1	WK2	WK3	WK4	WK5	WK6	WK7	WK8	WK9	WK10	WK11	Exam Period
				Lab	**Project 1**	Lab	Lab	Lab	Lab	Lab	Lab Project 2	Final Assessment

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