BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE PILANI, K.K. BIRLA GOA CAMPUS

II SEMESTER 2011-2012

Advanced Computer Organization (CS C342)

Lab 2 Question : Register File

Design and implement the following Register File using verilog HDL with the following specifications. Each Register is made of 32 D-flip flops, i.e. each Register is of size 32 bits. RegFile has 32 such 32-bit Registers.

Use the following modules to implement the same:

1. D_FF(in, out, Clk,WE);
2. Mux32to1(in0, in1, … , in31, out_Mux, select);
3. Decoder5to32(in_Dec, out_Dec);
4. Register(in_Reg, out_Reg, Reg_Write, Clk);
5. RegFile(Rs, Rt, Rd, Data_In, Reg_Write, Bus_A, Bus_B, Clk);
6. Testbench;

Register File