BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI – K. K. BIRLA GOA CAMPUS

Second Semester 2011-2012

CS C342 Advanced Computer Organization

Lab #1: On 21st January 2012

Lab Question

Design and simulate a 3 bit DOWN COUNTER using 8-bit RING COUNTER and 8:3 PRIORITY ENCODER. The RING COUNTER should be made of J-K flip flops. Design all modules using RTL [behavioral and data flow models] logic.

The modules are as follows:

1. module JK_FF (Clock, Reset, J, K, JKOut)
2. module RingCounter (Clock, Reset, RingOut)
3. module Encoder (Input, Output)
4. module DownCounter(Clock, Reset, Out)
5. module testbench

Refer Morris Mano for the diagram of a 4-bit ring counter.

(Hint: The output of the Ring counter should be given as input to the encoder.)