BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE PILANI, K.K. BIRLA GOA CAMPUS

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Advanced Computer Organization (CS C342)

Lab 4: Memory

Design the following layout of memory with address space 4 and addressability 3 using the following modules :

1. D_FF(d_1b, q_1b, Write_1b, clk);
2. Mux4to1(Din0_1b,D in1_1b, Din2_1b, Din3_1b, Dout_1b,Addr_2b);
3. Mux2to1(Dout_3b, Zero_3b,Qout_3b,Read_1b);
4. Decoder2to4(Addr_2b,Loc_4b);
5. Memory(Din_3b,Addr_2b,WE_1b,Read_1b,Qout_3b,clk);