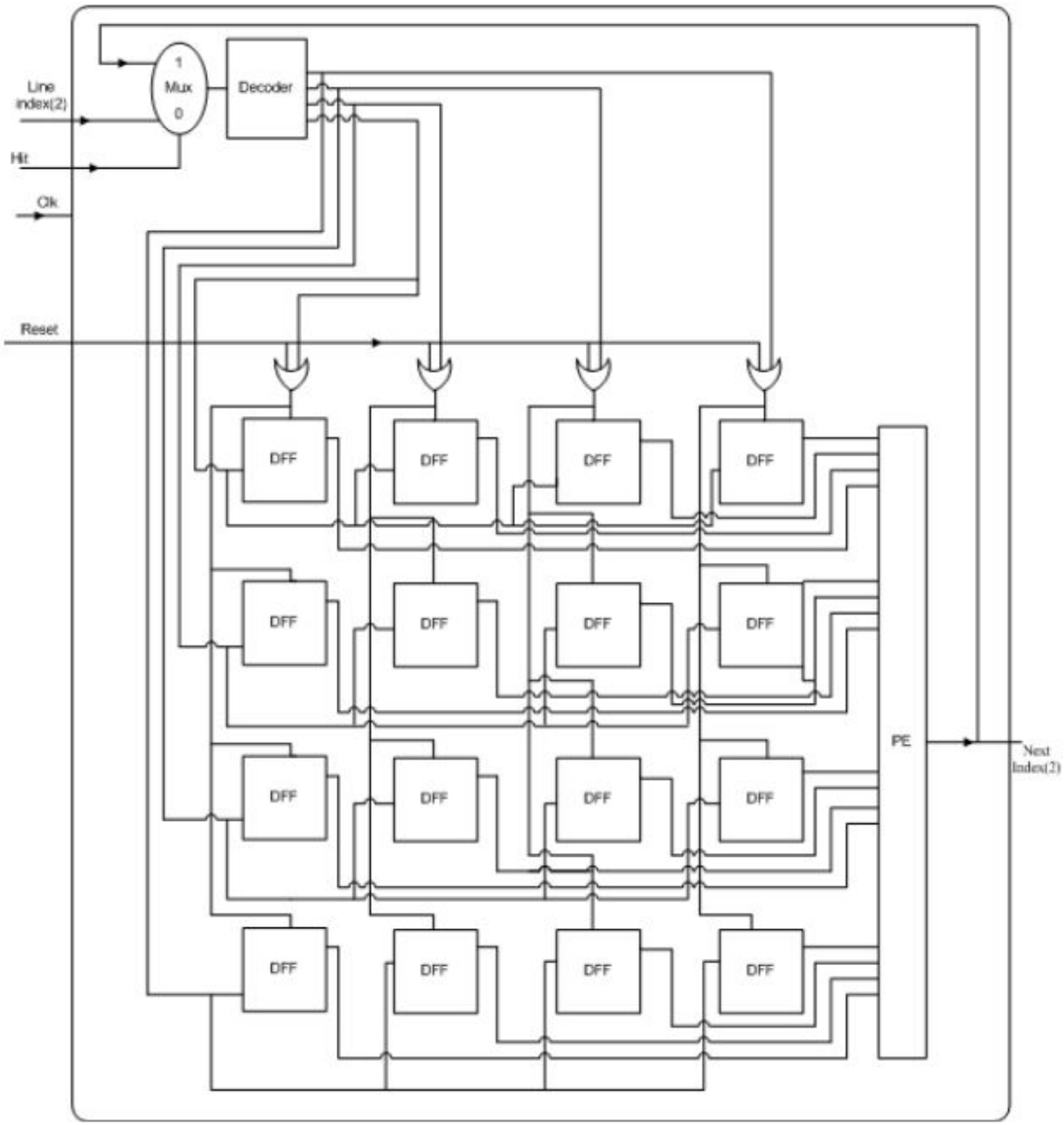
BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE PILANI, K.K. BIRLA GOA CAMPUS

II SEMESTER 2011-2012

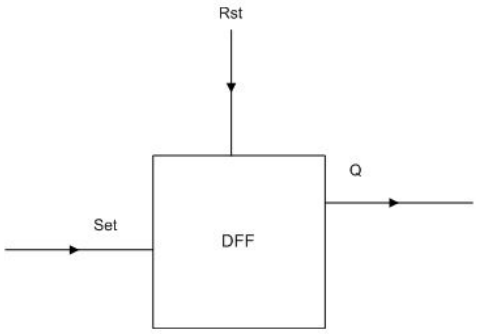
Advanced Computer Organization (CS C342)

Lab 5:Cache Memory

Implement LRU Square Matrix algorithm for a 4 – way set associative cache as shown below:



The connections for DFF in the above diagram are as below:



Use the following modules for implementing LRU Square Matrix replacement circuit :

1. D_FF(Rst_1b, Set_1b, Q_1b, Clk);
2. Mux2to1(Muxin0_2b, Muxin1_2b,Muxout_2b,Hit_1b);
3. Decoder2to4(DecIn_2b,DecOut_4b);
4. CacheMemory (Reset_1b,Memin_4b, Memout0_4b, Memout1_4b , Memout2_4b , Memout3_4b ,Clk);
5. PrioEnco(Ein0_4b, Ein1_4b, Ein2_4b, Ein3_4b, Eout_2b);
6. LRU(Reset_1b,Hit_1b,Lineindex_2b,Nextindex_2b,Clk);