**Analog Reinvented**

**ES9821**

**32-bit High Performance 2 Channel ADC**

**Product Datasheet**

The Sabre ES9821 is a 32-bit analog-to-digital (A/D) converter targeted for professional audio applications such as recording systems, mixer consoles and digital audio workstations (DAW), test equipment, instruments, audio processors, digital turntables, and consumer applications.

The ES9821 has 2 integrated ADCs which use ESS’ patented Hyperstream® II ADC Architecture, which delivers unprecedented audio sound quality and specifications, including a DNR of +120dB & THD+N of -112dB in 2 channel mode.

The SABRE® ADC supports S/PDIF, I2S master/slave, and TDM outputs, and Hardware mode for quick configurations.

The ES9821 has built-in preprogramed filter coefficients to match perfectly with the SABRE PRO Series of DACs including the ES9038PRO. These complimentary filters allow for analog-digital-analog processing with the upmost audio fidelity and minimized time-domain smearing.

The ES9821 has an Ultra-Low Noise Floor Bandwidth of 200kHz. This bandwidth is up to 10 times wider than the competition, enabling higher resolution at higher sample rates.

**DESCRIPTION**

|  |  |
| --- | --- |
| +120dB DNR per channel w/o PLL  -112dB THD+N per channel w/o PLL | Unprecedented dynamic range and ultra-low distortion |
| High Sample Rates | Up to PCM 768kHz |
| Customizable filter characteristics | 1. presets of digital optimal filters |
| Multiple Output formats available | PCM, TDM, and S/PDIF outputs are available |
| I2C, SPI, and Hardware interface control | Configured by microcontroller or other I2C/SPI master, or pins through Hardware Mode |
| Ultra-Low Noise Floor Bandwidth | 200kHz bandwidth enabling higher resolution at higher sample rates |
| Integrated low noise ADC reference regulators | Reduced BOM cost, PCB area and improved DNR if required |
| Low Power Consumption | Simplifies power supply design |
| Low Pin Count Standardized Packaging | 5mm x 5mm, 28 pin QFN |

**Applications**

* Professional digital audio workstations Audio Recording
* Very high-quality microphones
* High quality record turntable to USB conversion

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**Functional Block Diagram**

DVDD AVDD

ACLK1

ACLK2

PLL\_HVREG CHIP\_EN

SS/ADDR1/HW2 MISO/ADDR0/   
MUTE\_MCLK\_CTRL   
SCLK/SCL/HW1 MOSI/SDA/HW0

GPIO4/HW3 GPIO5/HW4

DATA\_CLK/GPIO1 DATA1/GPIO2 DATA2/GPIO3

RT1

DGND

Figure 1 – ES9821 Block Diagram

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**ES9821Q Package**

**28 QFN Pinout**

(Pin 29 is QFN package pad, see package dimensions)

Figure 2 – ES9821Q 28 pin QFN pinout

*Note: Pin 29 is a package pad, used for heat dissipation and is not electrically connected*

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**28 QFN Pin List**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Pin** | **Name** | **Pin Type** | **Reset**  **State** | **Pin Description** |
| 1 | MISO/ADDR0/MUTE\_MCLK\_CTRL | I/O | HiZ | Serial communication for SPI/I2C & HW interface pin, controlled by MODE pin |
| 2 | SCLK/SCL/HW1 | I/O | HiZ | Serial Clock for SCLK (SPI), SCL (I2C), also HW1 controlled by MODE pin |
| 3 | MOSI/SDA/HW0 | I/O | HiZ | Serial communication for SPI/I2C & HW0 interface pin, controlled by MODE |
| 4 | AVCC | Power | Power | 3.3V Supply |
| 5 | AGND | Ground | Ground | Analog Ground |
| 6 | VREF | Power | Power | Low Noise reference (internal) for bandgap circuitry |
| 7 | VREF\_BUF | Power | Power | Low Noise regulator output |
| 8 | AGND | Ground | Ground | Analog Ground |
| 9 | IN\_P1 | AI | HiZ | ADC Channel 1 differential positive (+) input |
| 10 | IN\_M1 | AI | HiZ | ADC Channel 1 differential negative (-) input |
| 11 | IN\_M2 | AI | HiZ | ADC Channel 2 differential negative (-) input |
| 12 | IN\_P2 | AI | HiZ | ADC Channel 2 differential positive (+) input |
| 13 | AVCC\_ADC | Power | Power | ADC reference voltage 3.3V Supply |
| 14 | CHIP\_EN | I/O | HiZ | Active-high chip enable. |
| 15 | ACLK2 | AI | HiZ | Auxiliary Clock Input 2 |
| 16 | RT1 | I | HiZ | Reserved. Must be connected to DGND for normal operation. |
| 17 | ACLK1 | AI | HiZ | Auxiliary Clock Input 1 |
| 18 | MODE | I/O | HiZ | I2C/SPI Control selection or HW mode |
| 19 | PLL\_HVREG | Power | Power | Low Noise reference for PLL regulator |
| 20 | DGND | Ground | Ground | Digital Core Ground |
| 21 | AVDD | Power | Power | 3.3V, I/O Supply |
| 22 | DVDD | Power | Power | Digital Core Supply. Internally Supplied |
| 23 | GPIO5/HW4 | I/O | HiZ | General I/O w/extended functions, HW4 mode control pin controlled by MODE |
| 24 | GPIO4/HW3 | I/O | HiZ | General I/O w/extended functions, HW3 mode control pin controlled by MODE |
| 25 | DATA2/GPIO3 | I/O | HiZ | Serial Data pin, also general I/O w/extended functions |
| 26 | DATA1/GPIO2 | I/O | HiZ | Serial Data pin, also general I/O w/extended functions |

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|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 27 | DATA\_CLK/GPIO1 | I/O | HiZ | Serial Clock pin, also general I/O w/extended functions |
| 28 | SS/ADDR1/HW2 | I/O | HiZ | Serial communication for SPI/I2C & HW2 interface pin, controlled by MODE pin |
| 29\* | Package PAD | - | - | Not electrically connected, used for heat dissipation |

Table 1 - 28 QFN pin list

*Note: Pin 29 is the package pad. See 28 QFN package dimensions for sizing. Connect to DGND if desired.*

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**Configuration Modes**

The ES9821 supports hardware and software configuration modes. Hardware mode allows for simplicity, and software mode allows for more configuration flexibility and customization.

**Software Mode**

The registers for the ES9821 can be accessed either using an I2C or SPI interface.

The MODE pin (pin 18) determines which interface will be used.

**I2C**

Table 2 - Available I2C addresses

* MODE (Pin 18) – ***GND***
* Connect per I2C standard
  + SDA (Pin 3)
  + SCL (Pin 2)
  + ADDR0 (Pin 1)
  + ADDR1 (Pin 28)
* ADDR0 & ADDR1 determine the I2C address

**SPI**

Table 3- Available SPI commands

The SPI slave interface is used when the MODE pin (pin 18) is high.   
   
o Mode (Pin 18) – **AVDD**   
o Connect per SPI standard using pins 1-3, and 28

▪ SCLK (Pin 2)

▪ SS (Pin 28)

▪ MOSI (Pin 3)

▪ MISO (Pin 1)

|  |  |
| --- | --- |
| **SPI command** | **First byte** |
| Write to PLL registers | ***7*** |
| Write to standard registers | ***3*** |
| Read | ***1*** |

The 4-wire SPI data format is: Command (1 byte) + Address (1 byte) + Data

**Required Software Mode Startup Sequence**

ES9821 starts up in master mode, if a clock is on ACLK1, DATA\_CLK (bit clock) and DATA1 (frame clock) will drive out PCM clocks. If using the device in slave mode, the following registers need to be set immediately after CHIP\_EN is asserted to avoid two masters driving clocks into the same digital serial audio bus:

1. Register 29[1:0] = 2'b00, tri-states GPIO1 and GPIO2 outputs.
2. Register 26[7:0] = 8'h11, changes GPIO1 and GPIO2 config, from 'Aux outputs' to 'Aux inputs'
3. Register 4[7:0] = 8'h00, Sets the ES9821 from master mode to slave mode.

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**Hardware Mode**

The ES9821 has pre-configured modes that can be set with external pin configuration. These modes configure the ADC for different serial data rates and set the ADC muting.

**All Hardware modes use ACLK1** and use the default Minimum phase digital filter. These modes are set with pins:

* MODE (pin 18)
* HW0 (pin 3)
* HW1 (pin 2)
* HW2 (pin 28)
* HW3 (pin 24)
* HW4 (pin 23)

Each hardware mode pin has 4 states:

* 0 – Pin directly connected to GND
* 1 – Pin directly connected to AVDD
* Pull 0 – Pin pulled to GND through 47kΩ resistor
* Pull 1 – Pin pulled to AVDD through 47kΩ resistor

**Design Information**

Each hardware mode pin can be configured either with a pull-up or pull-down resistor. For the pull states a 47kΩ resistor is recommended.

* The HW0 and HW1 pins never require a pull up or pull-down resistor.

Pull-down

AVDD or GPIO

HW2/

MODE

HW2/

MODE

47k

GND or GPIO

Figure 3 – Hardware mode pin configurations

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**Muting**

MUTE\_MCLK\_CTRL (Pin 1) is used to control the muting of the output and MCLK rate while in Hardware Mode:

* 0 – Mute, 24.576MHz / 22.579MHz
* 1 – Unmuted, 24.576MHz / 22.579MHz
* Pull 0 – Mute, 49.152MHz / 45.158MHz
* Pull 1 – Unmuted, 49.152MHz / 45.158MHz

**DC Blocking**

GPIO4/HW3 (Pin 24) is used to control the ADC’s DC Blocking feature while in Hardware Mode:

* 0 – DC blocking disabled
* 1 – DC blocking enabled

**S/PDIF**

In hardware modes #4-7, S/PDIF is encoded and output from GPIO5/HW4 in addition to the Left Justified data on the digital serial port (DCLK, DATA1, DATA2)

**TDM Channel Mapping**

In TDM hardware modes, ES9821 supports 4 channels, 8 channels, 16 channels and up to 32 channels per data line through autodetection. For 32 channels, GPIO5/HW4 is used to add 16 to the channel mapped. For example, Hardware modes 16 and 32 are the same hardware configuration except for GPIO5/HW4; HW mode 16 maps the outputs to slots 1 and 2, while HW mode 32 maps the outputs to slots 16 and 17.

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**Hardware Mode Pin Configurations**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **HW**  **Mode** | **FS (kHz)** | **BCK (MHz)** | **MCLK (MHz)** | **BCK/Channel** | **Channel**  **Slots** | **MODE** | **HW2** | **HW1** | **HW0** |
| **I2S Master Mode, Ext MCLK** | | | | | | | | |
| 0 | MCLK / 128 | MCLK / 2 | 24.576/49.152 | 32 | 1,2 | Pull 0 | 0 | 0 | 0 |
| 1 | MCLK / 256 | MCLK / 4 | 24.576/49.152 | 32 | 1,2 | Pull 0 | 0 | 0 | 1 |
| 2 | MCLK / 512 | MCLK / 8 | 24.576/49.152 | 32 | 1,2 | Pull 0 | 0 | 1 | 0 |
| 3 | MCLK / 1024 | MCLK / 16 | 24.576/49.152 | 32 | 1,2 | Pull 0 | 0 | 1 | 1 |
|  | **LJ Master, EXT MCLK (with S/PDIF enabled on GPIO5/HW4)** | | | | | | | | |
| 4 | MCLK / 128 | MCLK / 2 | 24.576/49.152 | 32 | 1,2 | Pull 0 | Pull 0 | 0 | 0 |
| 5 | MCLK / 256 | MCLK / 4 | 24.576/49.152 | 32 | 1,2 | Pull 0 | Pull 0 | 0 | 1 |
| 6 | MCLK / 512 | MCLK / 8 | 24.576/49.152 | 32 | 1,2 | Pull 0 | Pull 0 | 1 | 0 |
| 7 | MCLK / 1024 | MCLK / 16 | 24.576/49.152 | 32 | 1,2 | Pull 0 | Pull 0 | 1 | 1 |
|  | **I2S Slave, Ext MCLK, AutoDetect FS and BCK** | | | | | | | | |
| 8 | 8 < FS ≤ 384 | 64FS | 24.576/49.152 | 32 | 1,2 | Pull 0 | Pull 1 | 0 | 0 |
|  | **LJ Slave, AutoDetect FS and BCK** | | | | | | | | |
| 12 | 8 < FS ≤ 384 | 64FS | 24.576/49.152 | 32 | 1,2 | Pull 0 | 1 | 0 | 0 |
|  | **TDM Left Justified Slave, Autodetect FS and BCK, GPIO5/HW4 =0** | | | | | | | | |
| 16 | 8 < FS ≤ 384 | Auto (64FS,  128FS, 256FS, 512FS, 1024FS) | 24.576/49.152 | 32 | 1,2 | Pull 1 | 0 | 0 | 0 |
| 17 | 8 < FS ≤ 384 | Auto (128FS,  256FS, 512FS, 1024FS) | 24.576/49.152 | 32 | 3,4 | Pull 1 | 0 | 0 | 1 |
| 18 | 8 < FS ≤ 384 | Auto (256FS, 512FS, 1024FS) | 24.576/49.152 | 32 | 5,6 | Pull 1 | 0 | 1 | 0 |
| 19 | 8 < FS ≤ 384 | Auto (256FS, 512FS, 1024FS) | 24.576/49.152 | 32 | 7,8 | Pull 1 | 0 | 1 | 1 |
| 20 | 8 < FS ≤ 384 | Auto (512FS, 1024FS) | 24.576/49.152 | 32 | 9,10 | Pull 1 | Pull 0 | 0 | 0 |
| 21 | 8 < FS ≤ 384 | Auto (512FS, 1024FS) | 24.576/49.152 | 32 | 11,12 | Pull 1 | Pull 0 | 0 | 1 |
| 22 | 8 < FS ≤ 384 | Auto (512FS, 1024FS) | 24.576/49.152 | 32 | 13,14 | Pull 1 | Pull 0 | 1 | 0 |
| 23 | 8 < FS ≤ 384 | Auto (512FS, 1024FS) | 24.576/49.152 | 32 | 15,16 | Pull 1 | Pull 0 | 1 | 1 |
|  | **TDM Left Justified Slave, Autodetect FS and BCK, GPIO5/HW4 =0** | | | | | | | | |
| 24 | 8 < FS ≤ 384 | Auto (32FS, 64FS, 128FS, 256FS, 512FS) | 24.576/49.152 | 16 | 1,2 | Pull 1 | Pull 1 | 0 | 0 |

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|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 25 | 8 < FS ≤ 384 | Auto (64FS,  128FS, 256FS) | 24.576/49.152 | 16 | 3,4 | Pull 1 | Pull 1 | 0 | 1 |
| 26 | 8 < FS ≤ 384 | Auto (128FS, 256FS, 512FS) | 24.576/49.152 | 16 | 5,6 | Pull 1 | Pull 1 | 1 | 0 |
| 27 | 8 < FS ≤ 384 | Auto (128FS, 256FS, 512FS) | 24.576/49.152 | 16 | 7,8 | Pull 1 | Pull 1 | 1 | 1 |
| 28 | 8 < FS ≤ 384 | Auto (256FS, 512FS) | 24.576/49.152 | 16 | 9,10 | Pull 1 | 1 | 0 | 0 |
| 29 | 8 < FS ≤ 384 | Auto (256FS, 512FS) | 24.576/49.152 | 16 | 11,12 | Pull 1 | 1 | 0 | 1 |
| 30 | 8 < FS ≤ 384 | Auto (256FS,  512FS, 1024FS) | 24.576/49.152 | 16 | 13,14 | Pull 1 | 1 | 1 | 0 |
| 31 | 8 < FS ≤ 384 | Auto (256FS, 512FS) | 24.576/49.152 | 16 | 15,16 | Pull 1 | 1 | 1 | 1 |
|  | **TDM Left Justified Slave, Autodetect FS and BCK, GPIO5/HW4 = 1** | | | | | | | | |
| 32 | 8 < FS ≤ 384 | Auto (1024FS) | 24.576/49.152 | 32 | 17,18 | Pull 1 | 0 | 0 | 0 |
| 33 | 8 < FS ≤ 384 | Auto (1024FS) | 24.576/49.152 | 32 | 19,20 | Pull 1 | 0 | 0 | 1 |
| 34 | 8 < FS ≤ 384 | Auto (1024FS) | 24.576/49.152 | 32 | 21,22 | Pull 1 | 0 | 1 | 0 |
| 35 | 8 < FS ≤ 384 | Auto (1024FS) | 24.576/49.152 | 32 | 23,24 | Pull 1 | 0 | 1 | 1 |
| 36 | 8 < FS ≤ 384 | Auto (1024FS) | 24.576/49.152 | 32 | 25,26 | Pull 1 | Pull 0 | 0 | 0 |
| 37 | 8 < FS ≤ 384 | Auto (1024FS) | 24.576/49.152 | 32 | 27,28 | Pull 1 | Pull 0 | 0 | 1 |
| 38 | 8 < FS ≤ 384 | Auto (1024FS) | 24.576/49.152 | 32 | 29,30 | Pull 1 | Pull 0 | 1 | 0 |
| 39 | 8 < FS ≤ 384 | Auto (1024FS) | 24.576/49.152 | 32 | 31,32 | Pull 1 | Pull 0 | 1 | 1 |
|  | **TDM Left Justified Slave, Autodetect FS and BCK, GPIO5/HW4 = 1** | | | | | | | | |
| 40 | 8 < FS ≤ 384 | Auto (512FS) | 24.576/49.152 | 16 | 17,18 | Pull 1 | Pull 1 | 0 | 0 |
| 41 | 8 < FS ≤ 384 | Auto (512FS) | 24.576/49.152 | 16 | 19,20 | Pull 1 | Pull 1 | 0 | 1 |
| 42 | 8 < FS ≤ 384 | Auto (512FS) | 24.576/49.152 | 16 | 21,22 | Pull 1 | Pull 1 | 1 | 0 |
| 43 | 8 < FS ≤ 384 | Auto (512FS) | 24.576/49.152 | 16 | 23,24 | Pull 1 | Pull 1 | 1 | 1 |
| 44 | 8 < FS ≤ 384 | Auto (512FS) | 24.576/49.152 | 16 | 25,26 | Pull 1 | 1 | 0 | 0 |
| 45 | 8 < FS ≤ 384 | Auto (512FS) | 24.576/49.152 | 16 | 27,28 | Pull 1 | 1 | 0 | 1 |
| 46 | 8 < FS ≤ 384 | Auto (512FS) | 24.576/49.152 | 16 | 29,30 | Pull 1 | 1 | 1 | 0 |
| 47 | 8 < FS ≤ 384 | Auto (512FS) | 24.576/49.152 | 16 | 31,32 | Pull 1 | 1 | 1 | 1 |

Table 4 - Hardware mode configurations

**Note 1: In 352.8kHz/384kHz sampling, modes 8,12,16-47 will require a 45.1584Mhz (44.1kHz sampling multiple) or 49.152MHz (48kHz) clock for a 128FS ratio (MCLK/FS ratio).**

**Note 2: MCLK is shown with a 48kHz multiple clock. If 44.1kHz ratios are required, a clock of 22.5792Mhz/45.1584Mhz should be used.**

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**Required Hardware Mode Startup Sequence**

The hardware mode setup sequence is shown below with all hardware pins being defined after CHIP\_EN is asserted.

Note: It is recommended that MUTE\_CTRL is set low until the HW mode is finalized, then asserted last.

CHIP\_EN

HW0

HW1

HW2

MUTE\_CTRL

OUT

Figure 4 – Hardware mode startup sequence for modes

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**Digital Features**

**Digital Signal Path**

**SABRE ADC DIGITAL PATH (2 CHANNEL)**

8x Decimating Filter

DC

Offset

1. THD   
    Compenstation
2. x1, x2, 32

GAIN

Bypass Bypass

Figure 5 – Digital signal path

**Audio Output Formats**

**PCM**

PCM modes include the subset of I2S and Left-Justified (LJ) modes. These modes are set to carry 2 channels of converted data per digital data line, along with 2 lines of audio clocks, the bit clock, and frame clock.

Figure 6 – Left Justified (LJ) subset of PCM mode.

Figure 7 – I2S subset of PCM mode.

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**TDM**

In TDM modes, several ES9821 are used in parallel to increase the number of channels. Examples of TDM128 and   
TDM256 are shown below with a single 4 channel and 8 channel data line, respectively. Each ES9821 can be configured in HW or SW mode to output its data to different slots on the TDM DATA line.

Note: In hardware modes, only Left Justified TDM formats are supported. In software mode, the user can configure it to be I2S TDM format.

Figure 8 – TDM connection of several ES9821 devices in parallel

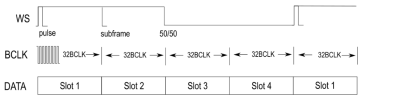


Figure 9 – TDM128 mode

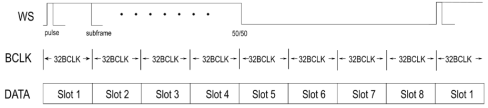


Figure 10 – TDM256 mode

**S/PDIF**

S/PDIF is transmitted over a single signal line using dual phase encoded data, which allows for clock extraction from the data signal line.

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GPIO Configuration

|  |  |  |
| --- | --- | --- |
| **GPIO#\_CFG** | **Function** | **I/O Direction** |
| 0 | analog shutdown | Shutdown (default) |
| 1 | Aux Inputs | Inputs |
| 2 | Aux Outputs | Output |
| 3 | PLL\_CLK\_AVALID | Output |
| 4 | PLL\_LOCKED | Output |
| 5 | Ch1\_CLIP\_INTERRUPT | - |
| 6 | Ch2\_CLIP\_INTERRUPT | - |
| 7 | INTERRUPT (OR of all interrupts) | - |
| 8 | S/PDIF data output | Output |
| 9 | PWM1 | Output |
| 10 | PWM2 | Output |
| 11 | PWM3 | Output |
| 12 | RESERVED | Output |
| 13 | CLK ADC | Output |
| 14 | 1’b0 | Output |
| 15 | 1’b1 | Output |

Table 5 – Standard GPIO Functions

Note: GPIOs can be configured using registers 26-31. For configuring pins as inputs, outputs, or Input/Outputs:

* Input pin
  + GPIOxx IE = 1’b1 (Input Enable), Registers 31-29
  + GPIOxx\_OE = 1’b0 (Output Enable), Registers 31-29

• Output pin   
o GPIOxx\_IE = 1’b0 o GPIOxx\_OE = 1’b1

• In/Out pin (Master Mode) o GPIOxx\_IE = 1’b1 o GPIOxx\_OE = 1’b1

In Master mode GPIO1 & GPIO 2 should be configured as In/Out pins

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**Interrupts**

Interrupts are enabled using individual configuration registers specific to the interrupt function. For example, the Peak Detection interrupt is enabled via Register 43 *ADC\_PEAK\_DETECTOR\_CONFIG*.

Once set, interrupts must be manually cleared via Register 12 *INTERRUPT*.

Register 12 *INTERRUPT* also allows for masking of the interrupt flag bits in Register 224 *READ*  *SYSTEM*  *REGISTER*  *0*.

Interrupts can be mapped to GPIO pins using Registers 26-28 *GPIO\_x/x\_CONFIG*.

**THD Compensation**

THD Compensation minimizes the non-linearities of the ADCs and the input stage overall by adding second order and third order terms:

The ES9821 can help compensate for system second and third harmonic distortion. In hardware mode, the coefficients CH1\_C2 = CH2\_C2 = 6 and CH1\_C3=CH2\_C3=-13 are used, as they were best to minimize any distortion at large amplitudes.

THD compensation is always enabled but if register values are zero, it will be bypassed.

* *Register 56-55, THD COMP C2 CH1*
* *Register 58-57, THD COMP C3 CH1*
* *Register 60-59, THD COMP C2 CH2*
* *Register 62-61, THD COMP C3 CH2*

For best results, compensation coefficients should be tuned for each device in-situ.

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**Digital Filters**

The ES9821 has 8 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates.   
(See Register 64[4:2])

* Minimum phase (default)
* Linear phase fast roll-off apodizing
* Linear phase fast roll-off
* Linear phase fast roll-off low ripple
* Linear phase slow roll-off
* Minimum phase fast roll-off
* Minimum phase slow roll-off
* Minimum phase slow roll-off low dispersion

Note on Minimum phase filters:

Minimum phase filters are asymmetric filters that work to minimize the pre-echo of the filter, while still maintaining an excellent frequency response and they peak earlier than linear phase filters, resulting in a lower group delay. Minimum phase filters usually feature zero cycles of pre-echo, which can result in improved audio quality.

**PCM Filter Properties**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Minimum phase** | | | | | |
| **Parameter** | **Conditions** | **MIN** | **TYP** | **MAX** | **UNIT** |
| Pass band |  |  |  | 0.46 x fs | Hz |
| Stop band | -79 dB | 0.55 x fs |  |  | Hz |
| Group Delay |  | 2.89/fs |  | 9.23/fs | s |
| Flatness (ripple) | 0.0031 |  |  |  | dB |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Linear phase fast roll-off apodizing** | | | | | |
| **Parameter** | **Conditions** | **MIN** | **TYP** | **MAX** | **UNIT** |
| Pass band |  |  |  | 0.41 x fs | Hz |
| Stop band | -83 dB | 0.50 x fs |  |  | Hz |
| Group Delay |  |  | 33.25/fs |  | s |
| Flatness (ripple) | 0.0032 |  |  |  | dB |

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|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Conditions** | **MIN** | **TYP** | **MAX** | **UNIT** |
| Pass band |  |  |  | 0.46 x fs | Hz |
| Stop band | -88 dB | 0.54 x fs |  |  | Hz |
| Group Delay |  |  | 32.88/fs |  | s |
| Flatness (ripple) | 0.0038 |  |  |  | dB |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Linear phase fast roll-off low ripple** | | | | | |
| **Parameter** | **Conditions** | **MIN** | **TYP** | **MAX** | **UNIT** |
| Pass band |  |  |  | 0.46 x fs | Hz |
| Stop band | -78 dB | 0.55 x fs |  |  | Hz |
| Group Delay |  |  | 33.00/fs |  | s |
| Flatness (ripple) | 0.0024 |  |  |  | dB |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Linear phase slow roll-off** | | | | | |
| **Parameter** | **Conditions** | **MIN** | **TYP** | **MAX** | **UNIT** |
| Pass band | -3 dB |  |  | 0.50 x fs | Hz |
| Stop band | -84 dB | 0.81 x fs |  |  | Hz |
| Group Delay |  |  | 5.87/fs |  | s |
| Flatness (ripple) | - |  | - |  | dB |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Minimum phase fast roll-off** | | | | | |
| **Parameter** | **Conditions** | **MIN** | **TYP** | **MAX** | **UNIT** |
| Pass band |  |  |  | 0.46 x fs | Hz |
| Stop band | -86 dB | 0.55 x fs |  |  | Hz |
| Group Delay |  | 2.90/fs |  | 9.23/fs | s |
| Flatness (ripple) | 0.0042 |  |  |  | dB |

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| --- | --- | --- | --- | --- | --- |
| **Minimum phase slow roll-off** | | | | | |
| **Parameter** | **Conditions** | **MIN** | **TYP** | **MAX** | **UNIT** |
| Pass band | -3 dB |  |  | 0.43 x fs | Hz |
| Stop band | -90 dB | 0.80 x fs |  |  | Hz |
| Group Delay |  | 2.03/fs |  | 2.53/fs | s |
| Flatness (ripple) | - |  | - |  | dB |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Minimum phase slow roll-off low dispersion** | | | | | |
| **Parameter** | **Conditions** | **MIN** | **TYP** | **MAX** | **UNIT** |
| Pass band | -3 dB |  |  | 0.43 x fs | Hz |
| Stop band | -89 dB | 0.80 x fs |  |  | Hz |
| Group Delay |  | 12.13/fs |  | 12.20/fs | s |
| Flatness (ripple) | - |  | - |  | dB |

Table 6 – PCM Filter Properties

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**PCM Filter Latency**

The following table shows the simulated latency of each filter at 44.1kHz sampling rate. The latency was measured at the peak amplitude of the impulse response prior to being down-sampled to 1FS. Latency delay will reduce (scale) with sampling rate.

|  |  |
| --- | --- |
| **Digital Filter** | **Delay(us) @ fs=44.1kHz** |
| Minimum phase (default) | 1. us |
| Linear phase fast roll-off apodizing | 1. us |
| Linear phase fast roll-off | 1. us |
| Linear phase fast roll-off low ripple | 1. us |
| Linear phase slow roll-off | 1. us |
| Minimum phase fast roll-off | 1. us |
| Minimum phase slow roll-off | 1. us |
| Minimum phase slow roll-off low dispersion | 1. us |

Table 7 - Latency of Pre-Programmed Digital Filters

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**PCM Filter Frequency Response**

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

|  |  |
| --- | --- |
| **Filter** | **Frequency Response** |
| Minimum phase |  |
| Linear phase fast roll-off apodizing |  |

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|  |  |
| --- | --- |
| Linear phase fast roll-off |  |
| Linear phase fast roll-off low ripple |  |

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|  |  |
| --- | --- |
| Linear phase slow roll-off |  |
| Minimum phase fast roll-off |  |

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|  |  |
| --- | --- |
| Minimum phase slow roll-off |  |
| Minimum phase slow roll-off low dispersion |  |

Table 8 - PCM Filter Frequency Response

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**PCM Filter Impulse Response**

The following impulse responses were obtained from software simulations of these filters. The impulse responses reported below show the decimation path prior to down-sampling to 1FS and are scaled accordingly.

Table 9 - PCM Filter Impulse Response

|  |  |
| --- | --- |
| **Filter** | **Impulse Response** |
| Minimum phase |  |
| Linear phase fast roll-off apodizing |  |

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|  |  |
| --- | --- |
| Linear phase fast roll-off |  |
| Linear phase fast roll-off low ripple |  |
| Linear phase slow roll-off |  |

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|  |  |
| --- | --- |
| Minimum phase fast roll-off |  |
| Minimum phase slow roll-off |  |
| Minimum phase slow roll-off low dispersion |  |

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**64FS Mode**

When 64FS (MCLK/FS ratio) is required, it is necessary for the ES9821 to be running in 64FS Mode. If using automatic sample rate detection with Register 0[5] AUTO\_FS\_DETECT, 64FS Mode cannot be automatically accessed, unless Register 0[6] AUTO\_FS\_DETECT\_BLOCK\_64FS is set to 1’b0. 64FS Mode can be manually entered by setting Register 0[4] ENABLE\_64FS\_MODE to 1’b1, overriding the AUTO\_FS\_DETECT logic.

* Register 0[6] AUTO\_FS\_DETECT\_BLOCK\_64FS
* 1’b0: Allows AUTO\_FS\_DETECT to enter 64FS Mode
* 1’b1: Blocks AUTO\_FS\_DETECT from entering 64FS mode (default)
* Register 0[5] AUTO\_FS\_DETECT
* 1’b0: Manually set sample rate with Register 1[6:0]
* 1’b1: Automatically determine the sample rate (default)
* Register 0[4] ENABLE\_64FS\_MODE

o Use for 64FS ratios, including 705.6/768kHz sample rates This mode enables the Minimum phase 64FS filter. See filter properties. Note: 64FS mode is not supported in Hardware mode (HW).

**Minimum phase 64FS Mode Latency**

The following table shows the simulated latency at 705.6kHz sampling rate. The latency was measured at the peak amplitude of the impulse response prior to being down-sampled to 1FS. Latency delay will reduce (scale) with sampling rate.

|  |  |
| --- | --- |
| **Digital Filter** | **Delay(us) @ fs= 705.6 kHz** |
| Minimum phase 64FS | 9us |

Table 10 - Latency of Minimum phase 64FS filter

**Minimum Phase 64FS Filter Properties**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Minimum Phase 64FS** | | | | | |
| **Parameter** | **Conditions** | **MIN** | **TYP** | **MAX** | **UNIT** |
| Pass band | -3 dB |  |  | 0.57 x fs | Hz |
| Stop band | -94 dB | 0.91 x fs |  |  | Hz |
| Group Delay |  | 1.23/fs |  | 2.68/fs | s |
| Flatness (ripple) |  |  |  |  | dB |

Table 11 – Minimum Phase 64FS Filter Properties

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**Minimum Phase 64FS Filter Frequency Response**

Figure 11 – Minimum Phase 64FS filter response

**Minimum Phase 64FS Impulse Response**

The following impulse responses were obtained from software simulations of these filters. The impulse responses reported below show the decimation path prior to down-sampling to 1FS and are scaled accordingly.

Figure 12 – Minimum Phase 64FS Impulse response

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**Clock Distribution**

The ES9821 includes features for selecting and manipulating the input clock source.

The minimum supported external MCLK is 24.576/22.5792MHz. Below this frequency, it is required to use the APLL.

**Analog ADC**

Reg 2[2:0]

ACLK1

ACLK2

-End Decimation Path Clock   
(CLK\_ADC) 128fs clock

Reg 0[1]

Reg 1[5:0] Reg 0[4]

 Master BCK

Reg 3[6:0]

Reg 4 Reg 6[7:5]

GPIO1

GPIO2

|  |
| --- |
|  |
|  |

BCK

WS

Reg 0[2]

**Digital ADC**

Figure 13 – ES9821 Clock Distribution

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The following list shows the various clocks of the ES9821 and the associated registers for configuration.

**Analog ADC Clock (ADC\_CLK)**

ADC\_CLK must be maintained to be between 22.5792MHz & 24.576MHz

* Reg 2[7] ADC\_CLK\_DIV2

**ADC Back-end Decimation Path Clock (CLK\_IADC)**

CLK\_IADC must be maintained to be between 22.5792MHz & 24.576MHz

* Reg 2[2:0] SELECT\_IADC\_NUM

**ADC Front-end Decimation Path Clock (CLK\_ADC)**

* Reg 0[6] AUTO\_FS\_DETECT\_BLOCK\_64FS
* Reg 0[5] AUTO\_FS\_DETECT
* Reg 0[4] ENABLE\_64FS\_MODE
* Reg 1[6] SELECT\_ADC\_HALF
* Reg 1[5:0] SELECT\_ADC\_NUM

**Master BCK & WS**

* Reg 1[7] AUTO\_CH\_DETECT
* Reg 3[7] SELECT\_I2S\_TDM\_HALF
* Reg 3[6:0] SELECT\_I2S\_TDM\_NUM
* Reg 4[7] MASTER\_BCK\_DIV1
* Reg 4[5:4] MASTER\_FRAME\_LENGTH
* Reg 4[3] MASTER\_WS\_PULSE\_MODE
* Reg 4[2] MASTER\_BCK\_INVERT
* Reg 4[1] MASTER\_WS\_INVERT
* Reg 4[0] MASTER\_MODE\_ENABLE
* Reg 6[7:5] MASTER\_WS\_SCALE
* Reg 6[4:0] TDM\_CH\_NUM

**TDM Clock (CLK\_TDM\_ENC)**

* Reg 0[2] ENABLE\_TDM\_ENCODE

**S/PDIF Clock (CLK\_SPDIF)**

* Reg 0[3] ENABLE\_SPDIF\_ENCODE

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**I2S Master Clock Rate Configurations**

WS can be scaled down further than shown via Register 6 [7:5] *MASTER\_WS\_SCALE*. When enabling 16-bit mode, the following registers must be modified:

* Register 63 [0:1] – enable 16-bit mode on channels 1 and 2
* Register 5 [0] – set TDM length to 16-bits
* Register 4 [5:4] – set master frame length to 16-bits

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **MCLK**  **Frequency** | **WS**  **[kHz]** | **BCK**  **[MHz]** | **Bits** | **Ch** | **Register 1**  **[5:0] SELECT\_ADC\_ NUM** | | **Register 3**  **[6:0]**  **SELECT\_I2S\_TDM\_N UM** | |
| Value | Divider | Value | Divider |
| 22.579  MHz | 44.1 | 2.822 | 32 | 2 | 5’d3 | 4 | 7’d3 | 4 |
| 88.2 | 5.645 | 2 | 5’d1 | 2 | 7’d1 | 2 |
| 176.4 | 11.29  0 | 2 | 5’d0 | 1 | 7’d0 | 1 |
| 44.1 | 1.411 | 16 | 2 | 5’d3 | 4 | 7’d3 | 4 |
| 88.2 | 2.822 | 2 | 5’d1 | 2 | 7’d1 | 2 |
| 176.4 | 5.645 | 2 | 5’d0 | 1 | 7’d0 | 1 |
| 24.576  MHz | 48 | 3.072 | 32 | 2 | 5’d3 | 4 | 7’d3 | 4 |
| 96 | 6.144 | 2 | 5’d1 | 2 | 7’d1 | 2 |
| 192 | 12.28  8 | 2 | 5’d0 | 1 | 7’d0 | 1 |
| 48 | 1.536 | 16 | 2 | 5’d3 | 4 | 7’d3 | 4 |
| 96 | 3.072 | 2 | 5’d1 | 2 | 7’d1 | 2 |
| 192 | 6.144 | 2 | 5’d0 | 1 | 7’d0 | 1 |
| 45.158 | 44.1 | 2.822 | 32 | 2 | 5’d7 | 8 | 7’d7 | 8 |
| 88.2 | 5.645 | 2 | 5’d3 | 4 | 7’d3 | 4 |
| 176.4 | 11.29  0 | 2 | 5’d1 | 2 | 7’d1 | 2 |
| 352.8 | 22.57  9 | 2 | 5’d0 | 1 | 7’d0 | 1 |
| 44.1 | 1.411 | 16 | 2 | 5’d7 | 8 | 7’d7 | 8 |
| 88.2 | 2.822 | 2 | 5’d3 | 4 | 7’d3 | 4 |
| 176.4 | 5.645 | 2 | 5’d1 | 2 | 7’d1 | 2 |
| 352.8 | 11.29  0 | 2 | 5’d0 | 1 | 7’d0 | 1 |
| 49.152  MHz | 48 | 3.072 | 32 | 2 | 5’d7 | 8 | 7’d7 | 8 |
| 96 | 6.144 | 2 | 5’d3 | 4 | 7’d3 | 4 |

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|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | 192 | 12.28  8 |  | 2 | 5’d1 | 2 | 7’d1 | 2 |
| 384 | 24.57  6 | 2 | 5’d0 | 1 | 7’d0 | 1 |
| 48 | 1.536 | 16 | 2 | 5’d7 | 8 | 7’d7 | 8 |
| 96 | 3.072 | 2 | 5’d3 | 4 | 7’d3 | 4 |
| 192 | 6.144 | 2 | 5’d1 | 2 | 7’d1 | 2 |
| 384 | 12.28  8 | 2 | 5’d0 | 1 | 7’d0 | 1 |

Table 12 - I2S Master Clock Rate Configurations

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**I2S Slave Clock Rate Configurations**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **MCLK**  **Frequency** | **WS**  **[kHz]** | **BCK** | **Ch.** | **Register 1**  **[5:0] SELECT\_ADC\_NUM** | | **Register 0**  **[4]**  **ENABLE\_2X\_MODE** | |
| Value | Divider | Value | Multiplier |
| 22.579 MHz | 44.1 | 512FS | 2 | 7’d3 | 4 | 1’b0 | 1x |
| 88.2 | 256FS | 2 | 7’d1 | 2 | 1’b0 | 1x |
| 176.4 | 128FS | 2 | 7’d0 | 1 | 1’b0 | 1x |
| 352.8 | 64FS | 2 | 7’d0 | 1 | 1’b1 | 2x |
| 24.576 MHz | 48 | 512FS | 2 | 7’d3 | 4 | 1’b0 | 1x |
| 96 | 256FS | 2 | 7’d1 | 2 | 1’b0 | 1x |
| 192 | 128FS | 2 | 7’d0 | 1 | 1’b0 | 1x |
| 384 | 64FS | 2 | 7’d0 | 1 | 1’b1 | 2x |
| 45.158 MHz | 44.1 | 1024FS | 2 | 7’d7 | 8 | 1’b0 | 1x |
| 88.2 | 512FS | 2 | 7’d3 | 4 | 1’b0 | 1x |
| 176.4 | 256FS | 2 | 7’d1 | 2 | 1’b0 | 1x |
| 352.8 | 128FS | 2 | 7’d0 | 1 | 1’b0 | 1x |
| 49.152 MHz | 48 | 1024FS | 2 | 7’d7 | 8 | 1’b0 | 1x |
| 96 | 512FS | 2 | 7’d3 | 4 | 1’b0 | 1x |
| 192 | 256FS | 2 | 7’d1 | 2 | 1’b0 | 1x |
| 384 | 128FS | 2 | 7’d0 | 1 | 1’b0 | 1x |

Table 13 - I2S Slave Clock Rate Configurations

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**Digital Audio Output Port**

Pins are configured in Master (AUX Output) or Slave (Aux Input) modes through GPIO Configurations.

**PCM Pin Connections**

See Audio Interface Timing (I2S) for timing criteria. Can select GPIO 4-6 for the datapath.

|  |  |  |
| --- | --- | --- |
| **Pin Name** | **Function** | **Description** |
| GPIO1/DATA\_CLK | I2S BCLK | I2S clock (Master or Slave) |
| GPIO2/DATA1 | I2S WS | I2S WS (Master or Slave) |
| GPIO3/DATA2 | I2S DATA | I2S DATA out (selectable for 2 channels) |

Table 14 - PCM pin connections

**TDM Pin Connections**

See Registers 7-15 for configuration, Can select GPIO 4-6 for the datapath.

|  |  |  |
| --- | --- | --- |
| **Pin Name** | **Function** | **Description** |
| GPIO1/DATA\_CLK | TDM BCK | TDM clock (Master or Slave) |
| GPIO2/DATA1 | TDM WS | TDM WS (Master or Slave) |
| GPIO3/DATA2 | TDM DATA | TDM DATA out (default) |

Table 15 - TDM pin connections

**S/PDIF Pin Connections**

S/PDIF Output is provided on GPIOs. Use GPIOx\_CFG for S/PDIF output.

Table 16 - S/PDIF pin connections

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**Analog Features**

**APLL**

ACLK1

ACLK2 DATA\_CLK

Figure 14 – Functional Block Diagram of ES9821 APLL

The ES9821 has a built in Analog PLL (APLL) for generating frequencies that are unavailable externally. For the application note on the APLL, please ask your FAE or distributor.

For calculation of the PLL frequency output, use the following formulas:

𝐹𝑟𝑒𝑓 = (𝐹𝑖𝑛)

𝐹𝑣𝑐𝑜 = ()∗𝐹𝐵𝐷𝐼𝑉

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𝐹𝑜𝑢𝑡 = ( )∗

Where:

1. FBDIV is a 24-bit number
2. PLL frequency range requirements:
   1. *Fref* requirement: 700kHz < *Fref* < 12 MHz
   2. *Fvco* requirement: 90MHz < *Fvco* < 110MHz
   3. *Fout* requirement: 22.5792/24.576MHz
3. Ni = input divider
   * Accessible from Reg 202-200[9:1], **PLL\_CLK\_IN\_DIV**
4. No = output divider
   * Accessible from Reg 202-200[18:10], **PLL\_CLK\_OUT\_DIV**
5. Nfb = feedback divider
   * Accessible from Reg 199-197[23:0], **PLL\_CLK\_FB\_DIV**

**PLL Registers**

* NI – Register 200-202[9:1] PLL\_CLK\_IN\_DIV
* NO – Register 200-202[18:10] PLL\_CLK\_OUT\_DIV
* FBDIV – Register 197-199[23:0] PLL\_CLK\_FB\_DIV

Clock Selection

* SEL\_PLL\_IN – Register 193[5:4]
  + Selection of PLL clock source (ACLK1/ACLK2/BCK or DATA\_CLK)
* SEL\_PLL\_CLKIN – Register 193[3]
  + Enables SEL\_PLL\_IN source input
* SEL\_SYSCLK\_IN – Register 193[2:1]
  + Selection of the ADC & digital core clock (ACLK1/ACLK2/PLL)

**Note: Only set PLL to output 22-24MHz system clock. 45-49MHz system clock is not supported when using the PLL.**

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**Absolute Maximum Ratings**

|  |  |
| --- | --- |
| **PARAMETER** | **RATING** |
| Positive Supply Voltage   * AVCC\_R/AVCC\_L * AVCC * AVDD * DVDD | * +3.6V with respect to Ground * +3.6V with respect to Ground * +3.6V with respect to Ground * +1.4V with respect to Ground |
| Storage temperature | –65°C to +150°C |
| Operating Junction Temperature | +125°C |
| Voltage range for digital input pins | –0.3V to AVDD (nom) + 0.3V |
| ESD Protection  Human Body Model (HBM) Charge Device Model (CDM) | 2kV  500V |

Table 17 - Absolute maximum ratings

**WARNING:** Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

**WARNING:** Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

**IO Electrical Characteristics**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **PARAMETER** | **SYMBOL** | **MINIMUM** | **MAXIMUM** | **UNIT** | **COMMENTS** |
| High-level input voltage | VIH | (AVDD / 2) + 0.4 |  | V |  |
| Low-level input voltage | VIL |  | 0.4 | V |  |
| High-level output voltage | VOH | AVDD – 0.2 |  | V | IOH = ((AVDD / 2) +1.4) mA |
| Low-level output voltage | VOL |  | 0.2 | V | IOL = ((AVDD / 2) + 1.7) mA |

Table 18 - IO electrical characteristics

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**Recommended Operating Conditions**

These are the recommended operating conditions for the ES9821.

|  |  |  |
| --- | --- | --- |
| **PARAMETER** | **SYMBOL** | **CONDITIONS** |
| Operating temperature | TA | –20°C to +85°C |
| AVCC |  | 3.3V |
| AVCC\_ADC |  | 3.3V |
| AVDD |  | 3.3V |
| VREF |  | Internal |
| VREF\_BUF |  | Internal |
| DVDD |  | Internal |
| Input DC offset |  | AVCC/2 |

***Note: The minimum supported external MCLK is 24.576/22.5792MHz. Below this frequency, it is required to use the APLL.***

Table 19 - Recommended operating conditions

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**Power Consumption**

Test Conditions (unless otherwise noted)

TA = 25oC, AVCC = AVCC\_ADC = AVDD = +3.3V, fs = 48kHz, **MCLK = 49.152MHz**, I2S output, with -1dBFS output signal

**MCLK of 49.152Mhz will work for all sample rates**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | | **Min** | **Typ** | **Max** | **Unit** |
|  | | | | | |
| **Standby** | CHIP\_EN = 0 |  |  |  |  |
| AVCC |  |  | 7.1 |  | uA |
| AVCC\_ADC |  |  | 2.2 |  | uA |
| AVDD |  |  |  |  | uA |
| **48kHz, 49.152MHz, HW#3** | Master Mode |  |  |  |  |
| AVCC |  |  | 6.5 |  | mA |
| AVCC\_ADC |  |  | 6.7 |  | mA |
| AVDD |  |  | 12.1 |  | mA |
|  | | | | | |
| **48kHz, 24.576MHz, HW#3** | Slave Mode |  |  |  |  |
| AVCC |  |  | 6.5 |  | mA |
| AVCC\_ADC |  |  | 6.7 |  | mA |
| AVDD |  |  | 7.3 |  | mA |

Table 20 – 49.152MHz MCLK power consumption

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**Performance**

Test Conditions (unless otherwise noted)

TA = 25oC, AVCC = AVCC\_ADC = AVDD = +3.3V, fs = 48kHz, MCLK = 49.152MHz, I2S output, 1kHz

Measurements were done using ESS Evaluation Board (EVB)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | | | **Min** | **Typ** | **Max** | **Unit** |
| Resolution |  |  |  | 32 |  | Bit |
|  | | | | | | |
| 0dBFS Input Voltage (differential) |  |  |  | 2 |  | Vrms |
|  | | | | | | |
| THD+N Ratio (w/o PLL)  @ fs=48kHz, BW=20Hz-20kHz | 2 ch mode | -1dBFS |  | -112 | -109 | dB |
| THD+N Ratio (w/ PLL)  @ fs=48kHz, BW=20Hz-20kHz |  | -106 | -102 |
|  | | | | | | |
| DNR A-weighted (w/o PLL) | 2ch mode | - 60dBFS | 117 | 120 |  | dB |
| DNR A-weighted (w/ PLL) | 106 | 110 |  |
|  | | | | | | |
| Interchannel Gain Mismatch |  |  |  | ±0.05 | ±0.1 | dB |

Table 21 – Performance test results

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**Timing Requirements**

**I2C Slave Interface**

Stop Start

Figure 15 – I2C Slave Control Interface Timing

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **CLK**  **Constraint** | **Standard-Mode** | | **Fast-Mode** | | **Unit** |
| **MIN** | **MAX** | **MIN** | **MAX** |
| SCL Clock Frequency | fSCL | < CLK/20 | 0 | 100 | 0 | 400 | kHz |
| START condition hold time | tHD;STA |  | 4.0 | - | 0.6 | - | μs |
| LOW period of SCL | tLOW | >10/CLK | 4.7 | - | 1.3 | - | μs |
| HIGH period of SCL (>10/CLK) | tHIGH | >10/CLK | 4.0 | - | 0.6 | - | μs |
| START condition setup time (repeat) | tSU;STA |  | 4.7 | - | 0.6 | - | μs |
| SDA hold time from SCL falling   * All except NACK read * NACK read only | tHD;DAT |  | 0  2/CLK | - | 0  2/CLK | - | μs s |
| SDA setup time from SCL rising | tSU;DAT |  | 250 | - | 100 | - | ns |
| Rise time of SDA and SCL | tr |  | - | 1000 |  | 300 | ns |
| Fall time of SDA and SCL | tf |  | - | 300 |  | 300 | ns |
|  | tSU;STO |  | 4 | - | 0.6 | - | μs |
| Bus free time between transmissions | tBUF |  | 4.7 | - | 1.3 | - | μs |
| Capacitive load for each bus line | Cb |  | - | 400 | - | 400 | pF |

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Table 22 - I2C Slave Control Interface Timing definitions

Figure 16 – I2C single byte examples of read and write instructions

**SPI Slave Interface**

**SPI Commands**

o 0x01: Read

o 0x03: Write

o 0x07: Write-only Registers 192-203 (0xC0 – 0xCB)

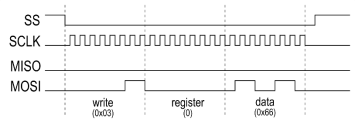


Figure 17 – SPI single byte write

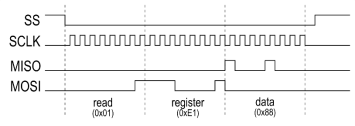


Figure 18 – SPI single byte Read

Figure 19 – SPI multi-byte read

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**PCM/TDM Timing Requirements**

**MCLK edge to BCK edge**

The ES9821 has a phase relationship requirement between MCLK (System Clock) and BCK (Bit Clock).

Figure 20 – 45/49MHz MCLK with BCK phase relationship

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **MCLK [MHz]** | **Minimum** | **Maximum** | **Unit** |
| BCK “↓” to MCLK “↓” | t*BFMF* | 49.152 / 45.1584 | - | 11 | ns |
| MCLK “↓” to BCK “↓” | t*MFBF* | 1.5 | - | ns |

Table 23 – Timing relationship for 45/49MHz MCLK & BCK

Figure 21 – 22/25MHz MCLK with BCK phase relationship

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **Symbol** | **MCLK [MHz]** | **Minimum** | **Maximum** | **Unit** |
| BCK “↓” to MCLK “↓” | t*BFMF* | 24.576 / 22.5792 | - | 1 | ns |
| MCLK “↓” to BCK “↓” | t*MFBF* | 24.576 / 22.5792 | - | 13 | ns |

Table 24 – Timing relationship for 22/24MHz MCLK & BCK

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**Register Overview**

ES9821 features two different register interfaces. There is a standard I2C slave interface, and a synchronous I2C slave interface. The standard I2C slave interface requires a system clock present through ACLK or from the PLL to write and read registers. The synchronous I2C slave interface does not require a system clock, and allows for write- only configuration of the PLL registers to create a system clock from some reference clock (th rough DATA\_CLK, or ACLK pins).

**Standard I2C Slave Interface (Device Address 0x40,0x42,0x44,0x46) Read/Write Registers**

Registers 0–65 (0x00 – 0x41) are read/write registers

**Read-only Registers**

Registers 224 – 240 (0xE0 – 0xF0) are read only registers.

**Synchronous I2C Slave Interface (Device Address 0x48,0x4A,0x4C,0x4E)**

This interface contains Write-only registers. These registers can be written even when there is no system clock present. When the device is inactive (CHIP\_EN = 0), all peripherals are automatically disabled and all clocks are stopped.

**Write-only Registers**

Registers 192 – 204 (0xC0 – 0xCC) are write only registers.

**Multi-Byte Registers**

Multi-byte registers must be written from LSB to MSB. Data is latched when MSB is written. Multi-byte registers must be read from LSB to MSB. Data is latched when LSB is read. MSB is always stored in the highest register address.

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**Register Map**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **Register** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| 0x00 | 0 | SYS CONFIG | SOFT\_RESET | AUTO\_ FS\_DETECT\_ BLOCK\_64FS | AUTO\_ FS\_DETECT | ENABLE\_ 64FS\_MODE | ENABLE\_SPDIF \_ENCODE | ENABLE\_TDM\_ ENCODE | ENABLE\_ ADC | RESERVED |
| 0x01 | 1 | ADC CLOCK CONFIG1 | AUTO\_CH\_ DETECT | SELECT\_ ADC\_HALF | SELECT\_ADC\_NUM | | | | | |
| 0x02 | 2 | ADC CLOCK CONFIG2 | ADC\_CLK\_DIV2 | RESERVED | | | | SELECT\_IADC\_NUM | | |
| 0x03 | 3 | I2S/TDM MASTER CLK CONFIG | SELECT\_I2S\_ TDM\_HALF | SELECT\_I2S\_TDM\_NUM | | | | | | |
| 0x04 | 4 | I2S/TDM MASTER MODE CONFIG | MASTER\_ BCK\_DIV1 | MASTER\_ WS\_IDLE | MASTER\_FRAME\_LENGTH | | MASTER\_WS\_ PULSE\_MODE | MASTER\_BCK\_ INVERT | MASTER\_WS\_ INVERT | MASTER\_ MODE\_ENABLE |
| 0x05 | 5 | TDM CONFIG1 | RESERVED | | | | | TDM\_VALID\_ EDGE | TDM\_LJ | TDM\_LENGTH |
| 0x06 | 6 | TDM CONFIG2 | MASTER\_WS\_SCALE | | | TDM\_CH\_NUM | | | | |
| 0x07 | 7 | TDM SLOT CONFIG CH1 | RESERVED | | SLAVE\_BCK\_ INVERT | TDM\_SLOT\_SEL\_CH1 | | | | |
| 0x08 | 8 | TDM SLOT CONFIG CH2 | RESERVED | | | TDM\_SLOT\_SEL\_CH2 | | | | |
| 0x09 - 0x0B | 9 -  11 | RESERVED | RESERVED | | | | | | | |
| 0x0C | 12 | INTERRUPT | RESERVED | | INTERRUPT\_ CLEAR\_CH2\_ CLIP\_DETECT | INTERRUPT\_ CLEAR\_CH1\_ CLIP\_DETECT | RESERVED | | INTERRUPT\_ MASK\_CH2\_ CLIP\_DETECT | INTERRUPT\_ MASK\_CH1\_ CLIP\_DETECT |
| 0x0D | 13 | SPDIF CONFIG | SPDIF\_CS | | | | | | | |
| 0x0E | 14 | SPDIF\_CS | | | | | | | |
| 0x0F | 15 | SPDIF\_CS | | | | | | | |
| 0x10 | 16 | SPDIF\_CS | | | | | | | |
| 0x11 | 17 | SPDIF\_CS | | | | | | | |
| 0x12 | 18 | SYNC CONTROL 1 | FORCE\_ PLL\_LOCKED | SYNC\_ POSEDGE\_ FRAME | RESERVED | | | | | |
| 0x13 - 0x19 | 19 -  25 | RESERVED | RESERVED | | | | | | | |
| 0x1A | 26 | GPIO1/2 CONFIG | GPIO2\_CFG | | | | GPIO1\_CFG | | | |
| 0x1B | 27 | GPIO3/4 CONFIG | GPIO4\_CFG | | | | GPIO3\_CFG | | | |
| 0x1C | 28 | GPIO5 CONFIG | GPIO5\_READ | RESERVED | | | GPIO5\_CFG | | | |
| 0x1D | 29 | GPIO SETTINGS 1 | GPIO3\_SDB | GPIO2\_SDB | GPIO1\_SDB | GPIO5\_OE | GPIO4\_OE | GPIO3\_OE | GPIO2\_OE | GPIO1\_OE |
| 0x1E | 30 | GPIO SETTINGS 2 | INVERT\_GPIO1 | GPIO5\_WK\_EN | GPIO4\_WK\_EN | GPIO3\_WK\_EN | GPIO2\_WK\_EN | GPIO1\_WK\_EN | GPIO5\_SDB | GPIO4\_SDB |
| 0x1F | 31 | GPIO SETTINGS 3 | GPIO4\_READ | GPIO3\_READ | GPIO2\_READ | GPIO1\_READ | INVERT\_GPIO5 | INVERT\_GPIO4 | INVERT\_GPIO3 | INVERT\_GPIO2 |
| 0x20 | 32 | PWM1 COUNT | PWM1\_COUNT | | | | | | | |
| 0x21 | 33 | PWM1 FREQUENCY | PWM1\_FREQ | | | | | | | |
| 0x22 | 34 | PWM1\_FREQ | | | | | | | |
| 0x23 | 35 | PWM2 COUNT | PWM2\_COUNT | | | | | | | |
| 0x24 | 36 | PWM2 FREQUENCY | PWM2\_FREQ | | | | | | | |
| 0x25 | 37 | PWM2\_FREQ | | | | | | | |
| 0x26 | 38 | PWM3 COUNT | PWM3\_COUNT | | | | | | | |
| 0x27 | 39 | PWM3 FREQUENCY | PWM3\_FREQ | | | | | | | |
| 0x28 | 40 | PWM3\_FREQ | | | | | | | |
| 0x29 | 41 | ADC DATAPATH CONTROL | RESERVED | ADC\_BYPASS\_ FIR2X | ADC\_BYPASS\_ FIR4X | RESERVED | | | CH1\_AVR | MONO\_MODE |
| 0x2A | 42 | ADC DC BLOCKING & SCALE CONFIG | ADC\_DATA\_SCALE\_CH2 | | ADC\_DATA\_SCALE\_CH1 | | ADC\_ SELECT\_DC\_ BLOCK\_CH2 | ADC\_ SELECT\_DC\_ BLOCK\_CH1 | ADC\_ ENABLE\_DC\_ BLOCK\_CH2 | ADC\_ ENABLE\_DC\_ BLOCK\_CH1 |
| 0x2B | 43 | ADC PEAK DETECTOR CONFIG | ADC\_LOCK\_ PEAK | ADC\_DECAY\_RATE | | | | | ADC\_ ENABLE\_PEAK \_DETECT\_CH2 | ADC\_ ENABLE\_PEAK \_DETECT\_CH1 |
| 0x2C | 44 | ADC CH1 PEAK DETECTOR LEVEL | ADC\_CLIP\_LEVEL\_CH1 | | | | | | | |
| 0x2D | 45 | ADC CH2 PEAK DETECTOR LEVEL | ADC\_CLIP\_LEVEL\_CH2 | | | | | | | |
| 0x2E | 46 | ADC CH1 DC OFFSET | ADC\_CH1\_DC\_OFFSET | | | | | | | |
| 0x2F | 47 | ADC\_CH1\_DC\_OFFSET | | | | | | | |
| 0x30 | 48 | ADC CH2 DC OFFSET | ADC\_CH2\_DC\_OFFSET | | | | | | | |
| 0x31 | 49 | ADC\_CH2\_DC\_OFFSET | | | | | | | |
| 0x32 | 50 | ADC CH1 VOLUME | ADC\_CH1\_VOLUME | | | | | | | |
| 0x33 | 51 | ADC\_CH1\_VOLUME | | | | | | | |
| 0x34 | 52 | ADC CH2 VOLUME | ADC\_CH2\_VOLUME | | | | | | | |
| 0x35 | 53 | ADC\_CH2\_VOLUME | | | | | | | |
| 0x36 | 54 | ADC VOLUME RATE | ADC\_VOLUME\_RATE | | | | | | | |
| 0x37 | 55 | THD COMP C2 CH1 | THD\_C2\_CH1 | | | | | | | |
| 0x38 | 56 | THD\_C2\_CH1 | | | | | | | |
| 0x39 | 57 | THD COMP C3 CH1 | THD\_C3\_CH1 | | | | | | | |
| 0x3A | 58 | THD\_C3\_CH1 | | | | | | | |
| 0x3B | 59 | THD COMP C2 CH2 | THD\_C2\_CH2 | | | | | | | |
| 0x3C | 60 | THD\_C2\_CH2 | | | | | | | |
| 0x3D | 61 | THD COMP C3 CH2 | THD\_C3\_CH2 | | | | | | | |
| 0x3E | 62 | THD\_C3\_CH2 | | | | | | | |
| 0x3F | 63 | RESERVED | RESERVED | | | | | | | |
| 0x40 | 64 | ADC FIR FILTER | RESERVED | | | ADC\_FILTER\_SHAPE | | | RESERVED | |
| 0x41 | 65 | RESERVED | RESERVED | | | | | | | |
| 0xC0 | 192 | PLL SOFT RESET | AO\_SOFT\_ RESET | PLL\_SOFT\_ RESET | RESERVED | | | | | PLL\_CLK\_ PHASE |
| 0xC1 | 193 | PLL CLOCK SELECT | RESERVED | EN\_ADC\_CLK | SEL\_PLL\_IN | | EN\_PLL\_CLKIN | SEL\_SYSCLK\_IN | | RESERVED |
| 0xC2 | 194 | RESERVED | RESERVED | | | | | | | |
| 0xC3 | 195 | PLL VCO & CP CONFIG | PLL\_CP\_BIAS\_SEL | | | RESERVED | | | PLL\_VCO\_PDB | PLL\_CP\_PDB |
| 0xC4 | 196 | PLL VCO CONTROL | PLL\_VCO\_BAND\_CTRL | | | RESERVED | | | | |
| 0xC5 | 197 | PLL FEEDBACK DIV | PLL\_CLK\_FB\_DIV | | | | | | | |
| 0xC6 | 198 | PLL\_CLK\_FB\_DIV | | | | | | | |
| 0xC7 | 199 | PLL\_CLK\_FB\_DIV | | | | | | | |
| 0xC8 | 200 | PLL IN & OUT DIV | PLL\_CLK\_IN\_DIV | | | | | | | PLL\_FB\_ DIV\_LOAD |

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|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0xC9 | 201 |  | RESERVED | | PLL\_CLK\_OUT\_DIV | | | | PLL\_CLK\_IN\_DIV | |
| 0xCA | 202 | PLL\_REG\_PDB | | PLL\_REG\_BYP | | RESERVED | PLL\_CLK\_ OUT\_DIV\_ PHASE\_ENB | RESERVED | |
| 0xCB | 203 | PLL VREF SELECT | RESERVED | | PLL\_DIG\_RSTB | RESERVED | | | PLL\_HVREG\_VREF\_SEL | |
| 0xCC | 204 | RESERVED | RESERVED | | | | | | | |
| 0xE0 | 224 | READ SYSTEM REGISTER 0 | CLIP\_FLAG\_ CH2 | CLIP\_FLAG\_ CH1 | RESERVED | | | | | |
| 0xE1 | 225 | CHIP ID | CHIP\_ID | | | | | | | |
| 0xE2 - 0xE6 | 226 -  230 | RESERVED | RESERVED | | | | | | | |
| 0xE7 | 231 | TDM VALID READ | RESERVED | | TDM\_VALID | RESERVED | | | | |
| 0xE8 | 232 | GPIO INPUT READ | RESERVED | | | GPIO5\_I\_R | GPIO4\_I\_R | GPIO3\_I\_R | GPIO2\_I\_R | GPIO1\_I\_R |
| 0xE9 - 0xEC | 233 -  236 | RESERVED | RESERVED | | | | | | | |
| 0xED | 237 | ADC PEAK CH1 | ADC1\_PEAK | | | | | | | |
| 0xEE | 238 | ADC1\_PEAK | | | | | | | |
| 0xEF | 239 | ADC PEAK CH2 | ADC2\_PEAK | | | | | | | |
| 0xF0 | 240 | ADC2\_PEAK | | | | | | | |

Table 25 – ES9821 Register Map

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**Register Listing**

Some RESERVED registers do not default to 0x00 and should not be modified for normal operation. If the value of the reserved registers is changed from the default state, it will be noted. Register defaults are set after CHIP\_EN is asserted.

**System Registers**

**Register 0: SYS CONFIG**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bits** | **[7]** | **[6]** | **[5]** | **[4]** | **[3]** | **[2]** | **[1]** | **[0]** |
| **Default** | 1'b0 | 1'b1 | 1'b1 | 1'b0 | 1'b0 | 1'b1 | 1'b0 | 1'b0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7]** | SOFT\_RESET | Performs soft reset to digital core except for the PLL REGISTERS.   * 1'b0: Disabled (default) * 1'b1: Enabled |
| **[6]** | AUTO\_FS\_DETECT\_BLOCK\_64FS | Disables AUTO\_FS\_DETECT from using 64FS mode.   * 1'b0: AUTO\_FS\_DETECT can use 64FS mode * 1'b1: AUTO\_FS\_DETECT is unable to use 64FS mode  (default) |
| **[5]** | AUTO\_FS\_DETECT | * 1'b0: Auto FS detect is disabled * 1'b1: Auto tune SELECT\_ADC\_NUM (SYS\_CLK/CLK\_ADC ratio) according to detected FS (default) |
| **[4]** | ENABLE\_64FS\_MODE | Enables 64FS mode to run the ADC decimation path at 64FS.   * 1'b0: 64FS mode disabled (default) * 1'b1: 64FS mode enabled   Note: This mode should be used for high sample rate (i.e., 705.6/768kHz) |
| **[3]** | ENABLE\_SPDIF\_ENCODE | Enables S/PDIF encoding clock.   * 1'b0: S/PDIF clock disabled (default) * 1'b1: S/PDIF clock enabled |
| **[2]** | ENABLE\_TDM\_ENCODE | Enables I2S/TDM encoding clock.   * 1'b0: I2S/TDM clock disabled * 1'b1: I2S/TDM clock enabled (default) |
| **[1]** | ENABLE\_ADC | Enables ADC decimation path clocks.  • 1'b0: Clocks disabled (default)  • 1'b1: Clocks enabled |
| **[0]** | RESERVED | NA |

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**Register 1: ADC CLOCK CONFIG1**

|  |  |  |  |
| --- | --- | --- | --- |
| **Bits** | **[7]** | **[6]** | **[5:0]** |
| **Default** | 1'b0 | 1'b0 | 6'd3 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7]** | AUTO\_CH\_DETECT | Enables BCK/FRAME ratio auto detect to determine TDM channels.   * 1'b0: Disabled (default) * 1'b1: Auto detect BCK/FRAME ratio to determine the number of TDM channels |
| **[6]** | SELECT\_ADC\_HALF | Specifies whether to half SELECT\_ADC\_NUM divider.  • 1'b0: Divide by SELECT\_ADC\_NUM + 1 (default)  • 1'b1: Divide by half of SELECT\_ADC\_NUM + 1  Note: Can only produce half of an odd number divide |
| **[5:0]** | SELECT\_ADC\_NUM | Whole number divide value + 1 for CLK\_ADC  (SYS\_CLK/divide\_value).   * 6'd0: Whole number divide value + 1 = 1 * 6'd3: Whole number divide value + 1 = 4 (default) * 6'd31: Whole number divide value + 1 = 32 |

**Register 2: ADC CLOCK CONFIG2**

|  |  |  |  |
| --- | --- | --- | --- |
| **Bits** | **[7]** | **[6:3]** | **[2:0]** |
| **Default** | 1'b0 | 4'b0000 | 3'd0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7]** | ADC\_CLK\_DIV2 | Sets ADC clock rate   * 1'b0: full rate (default) * 1'b1: 1/2 rate |
| **[6:3]** | RESERVED | NA |
| **[2:0]** | SELECT\_IADC\_NUM | Whole number divide value + 1 for CLK\_IADC  (SYS\_CLK/divide\_value).   * 3'd0: Whole number divide value + 1 = 1 (default) * 3'd1: Whole number divide value + 1 = 2 * 3'd7: Whole number divide value + 1 = 8 |

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**Register 3: I2S/TDM MASTER CLK CONFIG**

|  |  |  |
| --- | --- | --- |
| **Bits** | **[7]** | **[6:0]** |
| **Default** | 1'b0 | 7'd3 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7]** | SELECT\_I2S\_TDM\_HALF | Specifies whether to half SELECT\_I2S\_TDM\_NUM divider.  • 1'b0: Divide by SELECT\_I2S\_TDM\_NUM + 1 (default)  • 1'b1: Divide by half of SELECT\_I2S\_TDM\_NUM + 1  Note: Can only produce half of an odd number divide |
| **[6:0]** | SELECT\_I2S\_TDM\_NUM | Whole number divide value + 1 for I2S/TDM master encoding clock  (SYS\_CLK/divide\_value).   * 7'd0: Whole number divide value + 1 = 1 (default) * 7'd1: Whole number divide value + 1 = 2 * 7'd127: Whole number divide value + 1 = 128 |

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**Register 4: I2S/TDM MASTER MODE CONFIG**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Bits** | **[7]** | **[6]** | **[5:4]** | **[3]** | **[2]** | **[1]** | **[0]** |
| **Default** | 1'b0 | 1'b0 | 2'd0 | 1'b0 | 1'b1 | 1'b1 | 1'b1 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7]** | MASTER\_BCK\_DIV1 | When enabled, master BCK is I2S/TDM master encoding clock. Otherwise, BCK is less than or equal to (I2S/TDM master encoding clock)/2 (unless when ENABLE\_64FS\_MODE is set).   * 1'b0: BCK is not I2S/TDM master encoding clock (default) * 1'b1: BCK is I2S/TDM master encoding clock |
| **[6]** | MASTER\_WS\_IDLE | Sets the value of master WS when WS is idle.   * 1'b0: WS is 0 when idle (default) * 1'b1: WS is 1 when idle |
| **[5:4]** | MASTER\_FRAME\_LENGTH | Selects the bit length in each I2S/TDM channel in master mode.   * 2'd0: 32-bit (default) * 2'd2: 16-bit * Others: Reserved |
| **[3]** | MASTER\_WS\_PULSE\_MODE | When enabled, master WS is a pulse signal instead of a 50% duty cycle signal. The pulse width is 1 BCK cycle.   * 1'b0: 50% duty cycle WS signal (default) * 1'b1: Pulse WS signal |
| **[2]** | MASTER\_BCK\_INVERT | Inverts master BCK.   * 1'b0: Non-inverted * 1'b1: Inverted (default) |
| **[1]** | MASTER\_WS\_INVERT | Inverts master WS.   * 1'b0: Non-inverted * 1'b1: Inverted (default) |
| **[0]** | MASTER\_MODE\_ENABLE | Enables I2S/TDM master mode and generates master BCK and master WS.   * 1'b0: Disabled * 1'b1: Enabled (default) |

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**Register 5: TDM CONFIG1**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bits** | **[7:3]** | **[2]** | **[1]** | **[0]** |
| **Default** | 5'd0 | 1'b1 | 1'b0 | 1'b0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:3]** | RESERVED | NA |
| **[2]** | TDM\_VALID\_EDGE | Sets on which WS edge the frame starts.   * 1'b0: Frame starts on posedge of WS * 1'b1: Frame starts on negedge of WS (default) |
| **[1]** | TDM\_LJ | Sets left-justified mode.   * 1'b0: Not left-justified (default) * 1'b1: Left-justified |
| **[0]** | TDM\_LENGTH | Sets data length in each channel.   * 1'b0: 32-bit (default) * 1'b1: 16-bit |

**Register 6: TDM CONFIG2**

|  |  |  |
| --- | --- | --- |
| **Bits** | **[7:5]** | **[4:0]** |
| **Default** | 3'd0 | 5'd1 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:5]** | MASTER\_WS\_SCALE | In I2S/TDM master mode, tunes master BCK/WS ratio by scaling master WS. It allows more TDM slots in a fixed frame.   * 3'd0: No scale (default) * 3'd1: Scale down WS by 2 * 3'd2: Scale down WS by 4 * 3'd3: Scale down WS by 8 * 3'd4: Scale down WS by 16 * Others: Reserved |
| **[4:0]** | TDM\_CH\_NUM | Sets number of channels in each frame.   * 5'd0: 1 channel * 5'd1: 2 channels (default) * 5'd31: 32 channels |

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**Register 7: TDM SLOT CONFIG CH1**

|  |  |  |  |
| --- | --- | --- | --- |
| **Bits** | **[7:6]** | **[5]** | **[4:0]** |
| **Default** | 2'b00 | 1'b0 | 5'd0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:6]** | RESERVED | NA |
| **[5]** | SLAVE\_BCK\_INVERT | Slave BCK invert enable.   * 1'b0: Non-inverted (default) * 1'b1: Invert BCK input |
| **[4:0]** | TDM\_SLOT\_SEL\_CH1 | Selects which TDM channel slot is filled by ADC Ch1 data.  • 5'd0: Slot 1 (default)  • 5'd1: Slot 2  • 5'd31: Slot 32 |

**Register 8: TDM SLOT CONFIG CH2**

|  |  |  |
| --- | --- | --- |
| **Bits** | **[7:5]** | **[4:0]** |
| **Default** | 3'b000 | 5'd1 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:5]** | RESERVED | NA |
| **[4:0]** | TDM\_SLOT\_SEL\_CH2 | Selects which TDM channel slot is filled by ADC Ch2 data.  • 5'd0: Slot 1  • 5'd1: Slot 2 (default)  • 5'd31: Slot 32 |

**Register 11-9: RESERVED**

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**Register 12: INTERRUPT**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Bits** | **[7:6]** | **[5]** | **[4]** | **[3:2]** | **[1]** | **[0]** |
| **Default** | 2'b00 | 1'b0 | 1'b0 | 2'b00 | 1'b0 | 1'b0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:6]** | RESERVED | NA |
| **[5]** | INTERRUPT\_CLEAR\_CH2\_CLIP\_ DETECT | Clears the clip detection interrupt of ADC Ch2   * 1'b0: Interrupt held if asserted and not masked (default) * 1'b1: Interrupt cleared |
| **[4]** | INTERRUPT\_CLEAR\_CH1\_CLIP\_ DETECT | Clears the clip detection interrupt of ADC Ch1   * 1'b0: Interrupt held if asserted and not masked (default) * 1'b1: Interrupt cleared |
| **[3:2]** | RESERVED | NA |
| **[1]** | INTERRUPT\_MASK\_CH2\_CLIP\_ DETECT | Masks the clip detection interrupt of ADC Ch2  • 1'b0: Interrupt masked (default)   * 1'b1: Interrupt held if asserted |
| **[0]** | INTERRUPT\_MASK\_CH1\_CLIP\_ DETECT | Masks the clip detection interrupt of ADC Ch1  • 1'b0: Interrupt masked (default)   * 1'b1: Interrupt held if asserted |

**Register 17-13: SPDIF CONFIG**

|  |  |
| --- | --- |
| **Bits** | **[39:0]** |
| **Default** | 40'd0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[39:0]** | SPDIF\_CS | Configures SPDIF sub-code bits. |

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**Register 18: SYNC CONTROL 1**

|  |  |  |  |
| --- | --- | --- | --- |
| **Bits** | **[7]** | **[6]** | **[5:0]** |
| **Default** | 1'b1 | 1'b0 | 6'd0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7]** | FORCE\_PLL\_LOCKED | Clock locking status control with PLL\_LOCKED.   * 1'b0: clock locking status is determined by PLL\_LOCKED * 1'b1: ignores PLL\_LOCKED signal from PLL and sets clock locking status to 1 (default) |
| **[6]** | SYNC\_POSEDGE\_FRAME | Selects which edge of the sync reference signal is used.   * 1'b0: Sync to negative edge of the sync reference (default) * 1'b1: Sync to positive edge of the sync reference |
| **[5:0]** | RESERVED | NA |

**Register 25-19: RESERVED**

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**GPIO Registers**

**Register 26: GPIO1/2 CONFIG**

|  |  |  |
| --- | --- | --- |
| **Bits** | **[7:4]** | **[3:0]** |
| **Default** | 4'd2 | 4'd2 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:4]** | GPIO2\_CFG | Configure GPIO2  GPIO Function Selection   * 4'd0: Analog outputs off - shutdown * 4'd1: Aux inputs - input * 4'd2: Aux outputs - output (default) * 4'd3: Clock valid flag - output * 4'd4: PLL locked flag - output * 4'd5: Ch1 clip interrupt - output * 4'd6: Ch2 clip interrupt - output * 4'd7: OR of all interrupts -output * 4'd8: S/PDIF data output - output * 4'd9: Output PWM1 - output * 4'd10: Output PWM2 - output * 4'd11: Output PWM3 - output * 4'd12: Reserved * 4'd13: CLK\_ADC - output * 4'd14: Output 0 - output * 4'd15: Output 1 - output |
| **[3:0]** | GPIO1\_CFG | Configure GPIO1  GPIO Function Selection |

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|  |  |  |
| --- | --- | --- |
|  |  | * 4'd0: Analog outputs off - shutdown * 4'd1: Aux inputs - input * 4'd2: Aux outputs - output (default) * 4'd3: Clock valid flag - output * 4'd4: PLL locked flag - output * 4'd5: Ch1 clip interrupt - output * 4'd6: Ch2 clip interrupt - output * 4'd7: OR of all interrupts -output * 4'd8: S/PDIF data output - output * 4'd9: Output PWM1 - output * 4'd10: Output PWM2 - output * 4'd11: Output PWM3 - output * 4'd12: Reserved * 4'd13: CLK\_ADC - output * 4'd14: Output 0 - output * 4'd15: Output 1 - output |

**Register 27: GPIO3/4 CONFIG**

|  |  |  |
| --- | --- | --- |
| **Bits** | **[7:4]** | **[3:0]** |
| **Default** | 4'd0 | 4'd2 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:4]** | GPIO4\_CFG | Configure GPIO4  GPIO Function Selection   * 4'd0: Analog outputs off - shutdown * 4'd1: Aux inputs - input * 4'd2: Aux outputs - output * 4'd3: Clock valid flag - output * 4'd4: PLL locked flag - output * 4'd5: Ch1 clip interrupt - output * 4'd6: Ch2 clip interrupt - output * 4'd7: OR of all interrupts -output * 4'd8: S/PDIF data output - output * 4'd9: Output PWM1 - output * 4'd10: Output PWM2 - output * 4'd11: Output PWM3 - output * 4'd12: Reserved * 4'd13: CLK\_ADC - output * 4'd14: Output 0 - output * 4'd15: Output 1 - output |
| **[3:0]** | GPIO3\_CFG | Configure GPIO3 |

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|  |  |  |
| --- | --- | --- |
|  |  | GPIO Function Selection   * 4'd0: Analog outputs off - shutdown * 4'd1: Aux inputs - input * 4'd2: Aux outputs - output (default) * 4'd3: Clock valid flag - output * 4'd4: PLL locked flag - output * 4'd5: Ch1 clip interrupt - output * 4'd6: Ch2 clip interrupt - output * 4'd7: OR of all interrupts -output * 4'd8: S/PDIF data output - output * 4'd9: Output PWM1 - output * 4'd10: Output PWM2 - output * 4'd11: Output PWM3 - output * 4'd12: Reserved * 4'd13: CLK\_ADC - output * 4'd14: Output 0 - output * 4'd15: Output 1 - output |

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**Register 28: GPIO5 CONFIG**

|  |  |  |  |
| --- | --- | --- | --- |
| **Bits** | **[7]** | **[6:4]** | **[3:0]** |
| **Default** | 1'b0 | 3'd0 | 4'd0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7]** | GPIO5\_READ | GPIO5 readback enable.   * 1'b0: GPIO5 readback disabled (default) * 1'b1: Allows readback of GPIO5 input |
| **6:4]** | RESERVED | NA |
| **[3:0]** | GPIO5\_CFG | Configure GPIO5  GPIO Function Selection   * 4'd0: Analog outputs off - shutdown * 4'd1: Aux inputs - input * 4'd2: Aux outputs - output * 4'd3: Clock valid flag - output * 4'd4: PLL locked flag - output * 4'd5: Ch1 clip interrupt - output * 4'd6: Ch2 clip interrupt - output * 4'd7: OR of all interrupts -output * 4'd8: S/PDIF data output - output * 4'd9: Output PWM1 - output * 4'd10: Output PWM2 - output * 4'd11: Output PWM3 - output * 4'd12: Reserved * 4'd13: CLK\_ADC - output * 4'd14: Output 0 - output * 4'd15: Output 1 - output |

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**Register 29: GPIO SETTINGS 1**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bits** | **[7]** | **[6]** | **[5]** | **[4]** | **[3]** | **[2]** | **[1]** | **[0]** |
| **Default** | 1'b0 | 1'b1 | 1'b1 | 1'b0 | 1'b0 | 1'b1 | 1'b1 | 1'b1 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7]** | GPIO3\_SDB | GPIO3 input enable.   * 1'b0: GPIO3 input disabled (default) * 1'b1: GPIO3 input enabled |
| **[6]** | GPIO2\_SDB | GPIO2 input enable.   * 1'b0: GPIO2 input disabled * 1'b1: GPIO2 input enabled (default) |
| **[5]** | GPIO1\_SDB | GPIO1 input enable.   * 1'b0: GPIO1 input disabled * 1'b1: GPIO1 input enabled (default) |
| **[4]** | GPIO5\_OE | GPIO5 output enable.   * 1'b0: Tristate GPIO5 output (default) * 1'b1: GPIO5 output enabled |
| **[3]** | GPIO4\_OE | GPIO4 output enable.   * 1'b0: Tristate GPIO4 output (default) * 1'b1: GPIO4 output enabled |
| **[2]** | GPIO3\_OE | GPIO3 output enable.   * 1'b0: Tristate GPIO3 output * 1'b1: GPIO3 output enabled (default) |
| **[1]** | GPIO2\_OE | GPIO2 output enable.   * 1'b0: Tristate GPIO2 output * 1'b1: GPIO2 output enabled (default) |
| **[0]** | GPIO1\_OE | GPIO1 output enable.   * 1'b0: Tristate GPIO1 output * 1'b1: GPIO1 output enabled(default) |

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**Register 30: GPIO SETTINGS 2**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bits** | **[7]** | **[6]** | **[5]** | **[4]** | **[3]** | **[2]** | **[1]** | **[0]** |
| **Default** | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7]** | INVERT\_GPIO1 | GPIO1 invert enable.   * 1'b0: Non-invert (default) * 1'b1: Invert GPIO1 output |
| **[6]** | GPIO5\_WK\_EN | GPIO5 weak keeper enable.   * 1'b0: GPIO5 weak keeper disabled (default) * 1'b1: GPIO5 weak keeper enabled |
| **[5]** | GPIO4\_WK\_EN | GPIO4 weak keeper enable.   * 1'b0: GPIO4 weak keeper disabled (default) * 1'b1: GPIO4 weak keeper enabled |
| **[4]** | GPIO3\_WK\_EN | GPIO3 weak keeper enable.   * 1'b0: GPIO3 weak keeper disabled (default) * 1'b1: GPIO3 weak keeper enabled |
| **[3]** | GPIO2\_WK\_EN | GPIO2 weak keeper enable.   * 1'b0: GPIO2 weak keeper disabled (default) * 1'b1: GPIO2 weak keeper enabled |
| **[2]** | GPIO1\_WK\_EN | GPIO1 weak keeper enable.   * 1'b0: GPIO1 weak keeper disabled (default) * 1'b1: GPIO1 weak keeper enabled |
| **[1]** | GPIO5\_SDB | GPIO5 input enable.   * 1'b0: GPIO5 input disabled (default) * 1'b1: GPIO5 input enabled |
| **[0]** | GPIO4\_SDB | GPIO4 input enable.   * 1'b0: GPIO4 input disabled (default) * 1'b1: GPIO4 input enabled |

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**Register 31: GPIO SETTINGS 3**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bits** | **[7]** | **[6]** | **[5]** | **[4]** | **[3]** | **[2]** | **[1]** | **[0]** |
| **Default** | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7]** | GPIO4\_READ | GPIO 4 readback enable.   * 1'b0: GPIO4 readback disabled (default) * 1'b1: Allows readback of GPIO4 input |
| **[6]** | GPIO3\_READ | GPIO 3 readback enable.   * 1'b0: GPIO3 readback disabled (default) * 1'b1: Allows readback of GPIO3 input |
| **[5]** | GPIO2\_READ | GPIO 2 readback enable.   * 1'b0: GPIO2 readback disabled (default) * 1'b1: Allows readback of GPIO2 input |
| **[4]** | GPIO1\_READ | GPIO 1 readback enable.   * 1'b0: GPIO1 readback disabled (default) * 1'b1: Allows readback of GPIO1 input |
| **[3]** | INVERT\_GPIO5 | GPIO5 invert enable.   * 1'b0: Non-invert (default) * 1'b1: Invert GPIO5 output |
| **[2]** | INVERT\_GPIO4 | GPIO4 invert enable.   * 1'b0: Non-invert (default) * 1'b1: Invert GPIO4 output |
| **[1]** | INVERT\_GPIO3 | GPIO3 invert enable.   * 1'b0: Non-invert (default) * 1'b1: Invert GPIO3 output |
| **[0]** | INVERT\_GPIO2 | GPIO2 invert enable.   * 1'b0: Non-invert (default) * 1'b1: Invert GPIO2 output |

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**Register 32: PWM1 COUNT**

|  |  |
| --- | --- |
| **Bits** | **[7:0]** |
| **Default** | 8'h00 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:0]** | PWM1\_COUNT | 8-bit value to set the number of SYS\_CLK periods the PWM signal is high for.   * 8'h00: Disabled (default) * 8'h01: Minimum * 8'hFF: Maximum |

**Register 34-33: PWM1 FREQUENCY**

|  |  |
| --- | --- |
| **Bits** | **[15:0]** |
| **Default** | 16'h0000 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[15:0]** | PWM1\_FREQ | 16-bit value to set the frequency of the PWM signal in terms of SYS\_CLK divisions.   * 16'h0000: Disabled (default) * 16'h0001: Minimum * 16'hFFFF: Maximum   𝑆𝑌𝑆 𝐶𝐿𝐾  𝑓𝑟𝑒𝑞𝑢𝑒𝑛𝑐𝑦 [𝐻𝑧] =  𝑃𝑊𝑀1 𝐹𝑅𝐸𝑄 + 1  𝑃𝑊𝑀1 𝐶𝑂𝑈𝑁𝑇  𝐷𝑢𝑡𝑦 𝐶𝑦𝑐𝑙𝑒 [%] = ( ) × 100  𝑃𝑊𝑀1 𝐹𝑅𝐸𝑄 + 1 |

**Register 35: PWM2 COUNT**

|  |  |
| --- | --- |
| **Bits** | **[7:0]** |
| **Default** | 8'h00 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:0]** | PWM2\_COUNT | 8-bit value to set the number of SYS\_CLK periods the PWM signal is high for.   * 8'h00: Disabled (default) * 8'h01: Minimum * 8'hFF: Maximum |

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**Register 37-36: PWM2 FREQUENCY**

|  |  |
| --- | --- |
| **Bits** | **[15:0]** |
| **Default** | 16'h0000 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[15:0]** | PWM2\_FREQ | 16-bit value to set the frequency of the PWM signal in terms of SYS\_CLK divisions.   * 16'h0000: Disabled (default) * 16'h0001: Minimum * 16'hFFFF: Maximum   𝑆𝑌𝑆 𝐶𝐿𝐾  𝑓𝑟𝑒𝑞𝑢𝑒𝑛𝑐𝑦 [𝐻𝑧] =  𝑃𝑊𝑀2 𝐹𝑅𝐸𝑄 + 1  𝑃𝑊𝑀2 𝐶𝑂𝑈𝑁𝑇  𝐷𝑢𝑡𝑦 𝐶𝑦𝑐𝑙𝑒 [%] = ( ) × 100  𝑃𝑊𝑀2 𝐹𝑅𝐸𝑄 + 1 |

**Register 38: PWM3 COUNT**

|  |  |
| --- | --- |
| **Bits** | **[7:0]** |
| **Default** | 8'h00 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:0]** | PWM3\_COUNT | 8-bit value to set the number of SYS\_CLK periods the PWM signal is high for.   * 8'h00: Disabled (default) * 8'h01: Minimum * 8'hFF: Maximum |

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**Register 40-39: PWM3 FREQUENCY**

|  |  |
| --- | --- |
| **Bits** | **[15:0]** |
| **Default** | 16'h0000 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[15:0]** | PWM3\_FREQ | 16-bit value to set the frequency of the PWM signal in terms of SYS\_CLK divisions.   * 16'h0000: Disabled (default) * 16'h0001: Minimum * 16'hFFFF: Maximum   𝑆𝑌𝑆 𝐶𝐿𝐾  𝑓𝑟𝑒𝑞𝑢𝑒𝑛𝑐𝑦 [𝐻𝑧] =  𝑃𝑊𝑀3 𝐹𝑅𝐸𝑄 + 1  𝑃𝑊𝑀3 𝐶𝑂𝑈𝑁𝑇  𝐷𝑢𝑡𝑦 𝐶𝑦𝑐𝑙𝑒 [%] = ( ) × 100  𝑃𝑊𝑀3 𝐹𝑅𝐸𝑄 + 1 |

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**ADC Registers**

**Register 41: ADC DATAPATH CONTROL**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Bits** | **[7]** | **[6]** | **[5]** | **[4:2]** | **[1]** | **[0]** |
| **Default** | 1'b1 | 1'b0 | 1'b0 | 3'b000 | 1'b0 | 1'b0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7]** | RESERVED | NA |
| **[6]** | ADC\_BYPASS\_FIR2X | DFir\_2x bypass control.   * 1'b0: Non-bypass (default) * 1'b1: Bypass DFir\_2x |
| **[5]** | ADC\_BYPASS\_FIR4X | DFir\_4x bypass control.   * 1'b0: Non-bypass (default) * 1'b1: Bypass DFir\_4x |
| **[4:2]** | RESERVED | NA |
| **[1]** | CH1\_AVR | Use (CH1+CH2)/2 as CH1 data.  • 1'b0: Disabled (default)  • 1'b1: Enabled |
| **[0]** | MONO\_MODE | Mute CH2 decimation path.  • 1'b0: Disabled (default)  • 1'b1: Enabled |

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**Register 42: ADC DC BLOCKING & SCALE CONFIG**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Bits** | **[7:6]** | **[5:4]** | **[3]** | **[2]** | **[1]** | **[0]** |
| **Default** | 2'd0 | 2'd0 | 1'b0 | 1'b0 | 1'b0 | 1'b0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:6]** | ADC\_DATA\_SCALE\_CH2 | ADC CH2 data scale.   * 2'd0: +0dB * 2'd1: +6dB * 2'd2: +12dB * 2'd3: +18dB |
| **[5:4]** | ADC\_DATA\_SCALE\_CH1 | ADC CH1 data scale.   * 2'd0: +0dB * 2'd1: +6dB * 2'd2: +12dB * 2'd3: +18dB |
| **[3]** | ADC\_SELECT\_DC\_BLOCK\_CH2 | Controls DC blocking filter output for CH2 decimation path.   * 1'b0: Bypass DC blocking filter output (default) * 1'b1: Use DC blocking filter output |
| **[2]** | ADC\_SELECT\_DC\_BLOCK\_CH1 | Controls DC blocking filter output for CH1 decimation path.   * 1'b0: Bypass DC blocking filter output (default) * 1'b1: Use DC blocking filter output |
| **[1]** | ADC\_ENABLE\_DC\_BLOCK\_CH2 | CH2 DC blocking filter control.   * 1'b0: Disabled (default) * 1'b1: Enable DC blocking filter |
| **[0]** | ADC\_ENABLE\_DC\_BLOCK\_CH1 | CH1 DC blocking filter control.   * 1'b0: Disabled (default) * 1'b1: Enable DC blocking filter |

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**Register 43: ADC PEAK DETECTOR CONFIG**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bits** | **[7]** | **[6:2]** | **[1]** | **[0]** |
| **Default** | 1'b0 | 5'd10 | 1'b0 | 1'b0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7]** | ADC\_LOCK\_PEAK | Locks the stored value of the peak detectors (CH1/2) for reading back.   * 1'b0: Stored value is allowed to update (default) * 1'b1: Stored value is locked |
| **[6:2]** | ADC\_DECAY\_RATE | Sets the speed at which the stored value of the peak detector will decay when the input signal is below the stored value.   * 5'd0: Instant decay * 5'd10: Default * 5'd31: Slowest decay |
| **[1]** | ADC\_ENABLE\_PEAK\_DETECT\_ CH2 | Enables the ADC CH2 signal peak detector.   * 1'b0: Disabled (default) * 1'b1: Enabled |
| **[0]** | ADC\_ENABLE\_PEAK\_DETECT\_ CH1 | Enables the ADC CH1 signal peak detector.   * 1'b0: Disabled (default) * 1'b1: Enabled |

**Register 44: ADC CH1 PEAK DETECTOR LEVEL**

|  |  |
| --- | --- |
| **Bits** | **[7:0]** |
| **Default** | 8'hFF |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:0]** | ADC\_CLIP\_LEVEL\_CH1 | Threshold value of the CH1 clip detector.   * 8'h01: -48dB * 8'hFF: 0dB (default) |

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**Register 45: ADC CH2 PEAK DETECTOR LEVEL**

|  |  |
| --- | --- |
| **Bits** | **[7:0]** |
| **Default** | 8'hFF |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:0]** | ADC\_CLIP\_LEVEL\_CH2 | Threshold value of the CH2 clip detector.   * 8'h01: -48dB * 8'hFF: 0dB (default) |

**Register 47-46: ADC CH1 DC OFFSET**

|  |  |
| --- | --- |
| **Bits** | **[15:0]** |
| **Default** | 16'h0000 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[15:0]** | ADC\_CH1\_DC\_OFFSET | ADC CH1 signed DC offset.   * Negative offset is valid from 16'h8000 (-30dB) to 16'hFFFF (-114dB). * 16'h0000: Zero offset (default) * Positive offset is valid from 16'h7FFF (-30dB) to 16'h0001 (-114dB).   |𝐴𝐷𝐶 𝐶𝐻1 𝐷𝐶 𝑂𝐹𝐹𝑆𝐸𝑇|  𝑑𝑐 𝑜𝑓𝑓𝑠𝑒𝑡 [𝑑𝐵] = 20 ∗ 𝑙𝑜𝑔10 ( ) |

**Register 49-48: ADC CH2 DC OFFSET**

|  |  |
| --- | --- |
| **Bits** | **[15:0]** |
| **Default** | 16'h0000 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[15:0]** | ADC\_CH2\_DC\_OFFSET | ADC CH2 signed DC offset.   * Negative offset is valid from 16'h8000 (-30dB) to 16'hFFFF (-114dB). * 16'h0000: Zero offset (default) * Positive offset is valid from 16'h7FFF (-30dB) to 16'h0001 (-114dB).   |𝐴𝐷𝐶 𝐶𝐻2 𝐷𝐶 𝑂𝐹𝐹𝑆𝐸𝑇|  𝑑𝑐 𝑜𝑓𝑓𝑠𝑒𝑡 [𝑑𝐵] = 20 ∗ 𝑙𝑜𝑔10 ( ) |

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**Register 51-50: ADC CH1 VOLUME**

|  |  |
| --- | --- |
| **Bits** | **[15:0]** |
| **Default** | 16'h7FFF |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[15:0]** | ADC\_CH1\_VOLUME | Next desired ADC CH1 signed volume coefficient.   * 16'h0000: Mute * 16'h0001 (-90dB): Minimum * 16'h7FFF (0dB): Maximum (default)   Note: 16'h8000 to 16'hFFFF is a phase inverted version of the volume.  |𝐴𝐷𝐶 𝐶𝐻1 𝑉𝑂𝐿𝑈𝑀𝐸|  𝑣𝑜𝑙𝑢𝑚𝑒 [𝑑𝐵] = 20 ∗ 𝑙𝑜𝑔10 ( ) |

**Register 53-52: ADC CH2 VOLUME**

|  |  |
| --- | --- |
| **Bits** | **[15:0]** |
| **Default** | 16'h7FFF |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[15:0]** | ADC\_CH2\_VOLUME | Next desired ADC CH2 signed volume coefficient.   * 16'h0000: Mute * 16'h0001 (-90dB): Minimum * 16'h7FFF (0dB): Maximum (default)   Note: 16'h8000 to 16'hFFFF is a phase inverted version of the volume.  |𝐴𝐷𝐶 𝐶𝐻2 𝑉𝑂𝐿𝑈𝑀𝐸|  𝑣𝑜𝑙𝑢𝑚𝑒 [𝑑𝐵] = 20 ∗ 𝑙𝑜𝑔10 ( ) |

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**Register 54: ADC VOLUME RATE**

|  |  |
| --- | --- |
| **Bits** | **[7:0]** |
| **Default** | 8'h00 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:0]** | ADC\_VOLUME\_RATE | Value by which the old coefficient value is incremented/decremented to reach the new coefficient.   * 8'h00: Instant (default) * 8'h01: Slowest ramp rate * 8'hFF: Fastest ramp rate |

**Register 56-55: THD COMP C2 CH1**

|  |  |
| --- | --- |
| **Bits** | **[15:0]** |
| **Default** | 16'h0000 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[15:0]** | THD\_C2\_CH1 | A 16-bit signed coefficient for correcting for the CH1 second harmonic distortion.  𝑜𝑢𝑡𝑝𝑢𝑡 = 𝑥 + 𝑐2 ∗ 𝑥2 + 𝑐3 ∗ 𝑥3 |

**Register 58-57: THD COMP C3 CH1**

|  |  |
| --- | --- |
| **Bits** | **[15:0]** |
| **Default** | 16'h0000 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[15:0]** | THD\_C3\_CH1 | A 16-bit signed coefficient for correcting for the CH1 third harmonic distortion.  𝑜𝑢𝑡𝑝𝑢𝑡 = 𝑥 + 𝑐2 ∗ 𝑥2 + 𝑐3 ∗ 𝑥3 |

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**Register 60-59: THD COMP C2 CH2**

|  |  |
| --- | --- |
| **Bits** | **[15:0]** |
| **Default** | 16'h0000 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[15:0]** | THD\_C2\_CH2 | A 16-bit signed coefficient for correcting for the CH2 second harmonic distortion.  𝑜𝑢𝑡𝑝𝑢𝑡 = 𝑥 + 𝑐2 ∗ 𝑥2 + 𝑐3 ∗ 𝑥3 |

**Register 62-61: THD COMP C3 CH2**

|  |  |
| --- | --- |
| **Bits** | **[15:0]** |
| **Default** | 16'h0000 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[15:0]** | THD\_C3\_CH2 | A 16-bit signed coefficient for correcting for the CH2 third harmonic distortion.  𝑜𝑢𝑡𝑝𝑢𝑡 = 𝑥 + 𝑐2 ∗ 𝑥2 + 𝑐3 ∗ 𝑥3 |

**Register 63: RESERVED Register 64: ADC FIR FILTER**

|  |  |  |  |
| --- | --- | --- | --- |
| **Bits** | **[7:5]** | **[4:2]** | **[1:0]** |
| **Default** | 3'd4 | 3'd0 | 2'b00 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:5]** | RESERVED | NA |
| **[4:2]** | ADC\_FILTER\_SHAPE | Selects the 8x decimation FIR filter shape.   * 3'd0: Minimum phase (default) * 3'd1: Linear phase fast roll-off apodizing * 3'd2: Linear phase fast roll-off * 3'd3: Linear phase fast roll-off low ripple * 3'd4: Linear phase slow roll-off * 3'd5: Minimum phase fast roll-off * 3'd6: Minimum phase slow roll-off * 3'd7: Minimum phase slow roll-off low dispersion |
| **[1:0]** | RESERVED | NA |

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**Register 65: RESERVED**

**PLL Registers**

**Register 192: PLL SOFT RESET**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bits** | **[7]** | **[6]** | **[5:1]** | **[0]** |
| **Default** | 1'b0 | 1'b0 | 5'd0 | 1'b0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7]** | AO\_SOFT\_RESET | Performs soft reset to the digital core and clocked registers (0-64).   * 1'b0: Disabled (default) * 1'b1: Enable |
| **[6]** | PLL\_SOFT\_RESET | Performs soft reset to only the Always-On Registers (192-203).   * 1'b0: Disabled (default) * 1'b1: Enable |
| **[5:1]** | RESERVED | NA |
| **[0]** | PLL\_CLK\_PHASE | Digital/analog ADC clock invert phase enable.   * 1'b0: Digital/analog ADC clocks have inverted phase (default) * 1'b1: Digital/analog ADC clocks have the same phase  (recommended value) |

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**Register 193: PLL CLOCK SELECT**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Bits** | **[7]** | **[6]** | **[5:4]** | **[3]** | **[2:1]** | **[0]** |
| **Default** | 1'b0 | 1'b1 | 2'b10 | 1'b0 | 2'b00 | 1'b1 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7]** | RESERVED | NA |
| **[6]** | EN\_ADC\_CLK | Enables analog ADC clock.   * 1'b0: Disabled * 1'b1: Enabled (default) |
| **[5:4]** | SEL\_PLL\_IN | Selects PLL input clock source when EN\_PLL\_CLKIN is set.   * 2'b00: ACLK1 * 2'b01: ACLK2 * 2'b10: DATA\_CLK (default) * 2'b11: Reserved |
| **[3]** | EN\_PLL\_CLKIN | Allows SEL\_PLL\_IN to select PLL input clocks.   * 1'b0: Disables SEL\_PLL\_IN (default) * 1'b1: Enables SEL\_PLL\_IN |
| **[2:1]** | SEL\_SYSCLK\_IN | Selects digital core and ADC clock source when EN\_ANA\_CLKIN is set.   * 2'b00: ACLK1 (default) * 2'b01: ACLK2 * 2'b10: PLL * 2'b11: Reserved |
| **[0]** | RESERVED | NA |

**Register 194: RESERVED**

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**Register 195: PLL VCO & CP CONFIG**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bits** | **[7:5]** | **[4:2]** | **[1]** | **[0]** |
| **Default** | 3'b111 | 3'b111 | 1'b0 | 1'b0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:5]** | PLL\_CP\_BIAS\_SEL | Sets the Charge Pump current:   * 3'b011: 4uA (recommended value) * 3'b111: 8uA (default) |
| **[4:2]** | RESERVED | NA |
| **[1]** | PLL\_VCO\_PDB | Enables/disables the PLL voltage-controlled oscillator (VCO).   * 1'b0: Disabled (default) * 1'b1: Enabled |
| **[0]** | PLL\_CP\_PDB | Enables/disables the PLL charge pump.   * 1'b0: Disabled (default) * 1'b1: Enabled |

**Register 196: PLL VCO CONTROL**

|  |  |  |
| --- | --- | --- |
| **Bits** | **[7:5]** | **[4:0]** |
| **Default** | 3'b011 | 5'b00011 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:5]** | PLL\_VCO\_BAND\_CTRL | Selects the frequency band of the VCO.  • 3'b010: (recommended value)  • 3'b011: (default) |
| **[4:0]** | RESERVED | NA |

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**Register 199-197: PLL FEEDBACK DIV**

|  |  |
| --- | --- |
| **Bits** | **[23:0]** |
| **Default** | 24'd0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[23:0]** | PLL\_CLK\_FB\_DIV | Sets the PLL clock feedback divider.   * 24'd0: Reserved (default) * 24'dn: Divide by 2^25/n |

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**Register 202-200: PLL IN & OUT DIV**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bits** | **[23:22]** | **[21:20]** | **[19]** | **[18]** | **[17:14]** | **[13:10]** | **[9:1]** | **[0]** |
| **Default** | 2'b00 | 2'b00 | 1'b1 | 1'b0 | 4'd0 | 4'd0 | 9'd0 | 1'b0 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[23:22]** | PLL\_REG\_PDB | Power Down the PLL regulators.   * 2'b00: Disables the PLL regulators * 2'b11: Enables the PLL regulators (Normal Operation) Note: Other options not valid |
| **[21:20]** | PLL\_REG\_BYP | Bypass mode of the PLL regulators.   * 2'b00: Normal Operation * 2'b11: Bypass the PLL regulators Note: Other options not valid |
| **[19]** | RESERVED | NA |
| **[18]** | PLL\_CLK\_OUT\_DIV\_PHASE\_ENB | * 1'b0: Locks the PLL clock output divider phase. (default) * 1'b1: Disabled |
| **[17:14]** | RESERVED | NA |
| **[13:10]** | PLL\_CLK\_OUT\_DIV | Sets the Output Division (No) of the PLL.  • 4'd0: Divide by 1  • 4'd1: Divide by 2 (Normal starting value)  • 4'd3: Divide by 4  • 4'dn: Divide by (n + 1) |
| **[9:1]** | PLL\_CLK\_IN\_DIV | Sets the Input Division (Ni) of the PLL.  • 9'd0: Divide by 1  • 9'd1: Divide by 2 (Normal starting value)  • 9'd3: Divide by 4  • 9'dn: Divide by (n + 1) |
| **[0]** | PLL\_FB\_DIV\_LOAD | Load PLL\_CLK\_FB\_DIV  • Write 1'b1 then 1'b0 to load PLL\_CLK\_FB\_DIV value |

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**Register 203: PLL VREF SELECT**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bits** | **[7:6]** | **[5]** | **[4:2]** | **[1:0]** |
| **Default** | 2'b00 | 1'b0 | 3'b010 | 2'b01 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:6]** | RESERVED | NA |
| **[5]** | PLL\_DIG\_RSTB | Resets the Digital core of the PLL. |
| **[4:2]** | RESERVED | NA |
| **[1:0]** | PLL\_HVREG\_VREF\_SEL | PLL HVREG reference voltage selection  • 2'b00: 1.6V (optimum value)   * 2'b01: 1.7V (default) |

**Register 204: RESERVED**

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**Readback Registers**

**Register 224: READ SYSTEM REGISTER 0**

|  |  |  |  |
| --- | --- | --- | --- |
| **Bits** | **[7]** | **[6]** | **[5:0]** |
| **Default** | - | - | - |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7]** | CLIP\_FLAG\_CH2 | ADC CH2 clip detection interrupt readback.   * 1'b0: Inactive * 1'b1: Active |
| **[6]** | CLIP\_FLAG\_CH1 | ADC CH1 clip detection interrupt readback.   * 1'b0: Inactive * 1'b1: Active |
| **[5:0]** | RESERVED | NA |

**Register 225: CHIP ID**

|  |  |
| --- | --- |
| **Bits** | **[7:0]** |
| **Default** | 8'h88 |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:0]** | CHIP\_ID | Chip ID |

**Register 230-227: RESERVED**

**Register 231: TDM VALID READ**

|  |  |  |  |
| --- | --- | --- | --- |
| **Bits** | **[7:6]** | **[5]** | **[4:0]** |
| **Default** | - | - | - |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:6]** | RESERVED | NA |
| **[5]** | TDM\_VALID | TDM valid flag |
| **[4:0]** | RESERVED | NA |

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**Register 232: GPIO INPUT READ**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Bits** | **[7:5]** | **[4]** | **[3]** | **[2]** | **[1]** | **[0]** |
| **Default** | - | - | - | - | - | - |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[7:5]** | RESERVED | NA |
| **[4]** | GPIO5\_I\_R | GPIO5 input readback. |
| **[3]** | GPIO4\_I\_R | GPIO4 input readback. |
| **[2]** | GPIO3\_I\_R | GPIO3 input readback. |
| **[1]** | GPIO2\_I\_R | GPIO2 input readback. |
| **[0]** | GPIO1\_I\_R | GPIO1 input readback. |

**Register 236-234: RESERVED**

**Register 238-237: ADC PEAK CH1**

|  |  |
| --- | --- |
| **Bits** | **[15:0]** |
| **Default** | - |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[15:0]** | ADC1\_PEAK | Ch1 detected signal peak value readback.  Note: Requires reg43[0] ADC\_ENABLE\_PEAK\_DETECT\_CH1 to enable functionality. |

**Register 240-239: ADC PEAK CH2**

|  |  |
| --- | --- |
| **Bits** | **[15:0]** |
| **Default** | - |

|  |  |  |
| --- | --- | --- |
| **Bits** | **Mnemonic** | **Description** |
| **[15:0]** | ADC2\_PEAK | Ch2 detected signal peak value readback.  Note: Requires reg43[1] ADC\_ENABLE\_PEAK\_DETECT\_CH2 to enable functionality. |

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**ES9821 Reference Schematic (Hardware Mode)**

**See Hardware section for additional details on configuration for Hardware mode**

Figure 22 – ES9821Q Reference schematic for normal operation in Hardware (HW) mode

*Schematic subject to change*

Note 1: Pin 29 QFN Package Pad (EPAD) should be connected to DGND

Note 2: See Hardware mode section for additional details on configuration for Hardware mode

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**ES9821 Reference Schematic (Software Mode)**

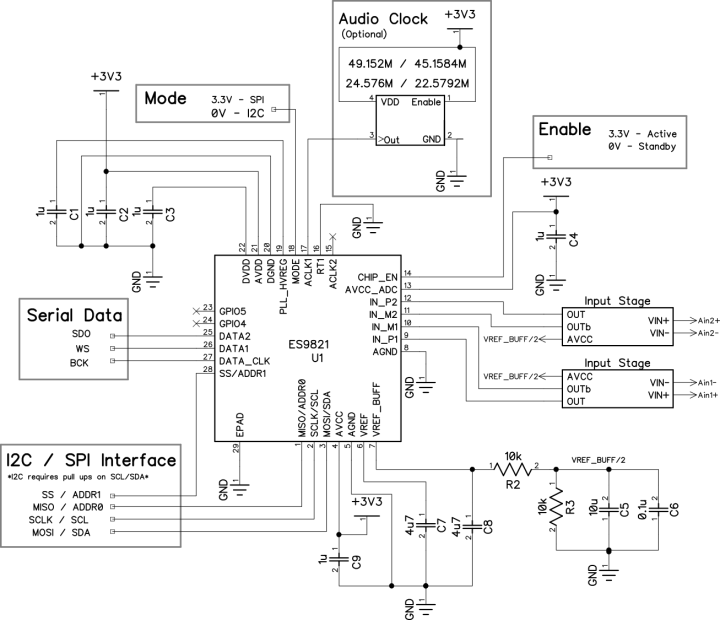


Figure 23 – ES9821Q Reference schematic for normal operation in Software (SW) mode

*Schematic subject to change*

Note 1: Pin 29 QFN Package Pad (EPAD) should be connected to DGND

Note 2: Pullup resistors are required on the SCL/SDA pins if using the I2C interface

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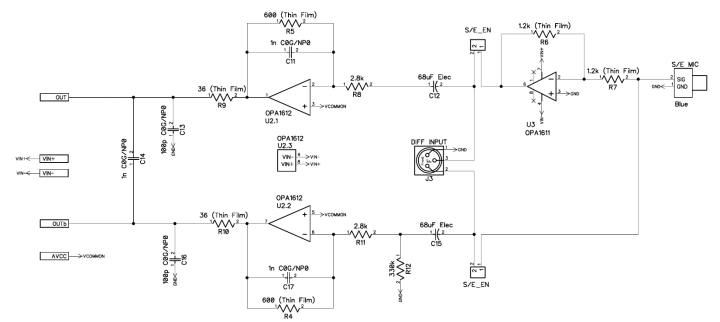


Figure 24 – Reference schematic ADC input stage for Single Ended (S/E) and differential input

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**Internal Pad Circuitry**

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin** | **Type** | **Pin**  **Number** | **Equivalent Circuit** |
| AVCC\_ADC AVDD AVCC | Power | 13  21  4 |  |
| AGND  AGND  DGND | Ground | 5  8  20 |  |
| CHIP\_EN | Reset | 14 |  |
| MISO/ADDR0/MUTE\_MCLK\_CTRL  SCLK/SCL/HW1 MOSI/SDA/HW0 MODE  GPIO5/HW4 GPIO4/HW3 DATA2/GPIO3 DATA1/GPIO2 DATA\_CLK/GPIO1 SS/ADDR1/HW2 | Digital I/O | 1  2  3  18  23  24  25  26  27  28 |  |

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|  |  |  |  |
| --- | --- | --- | --- |
| VREF VREF\_BUF | Analog\_IO\_2 XVDD | 6  7 |  |
| IN\_P1 IN\_P2 IN\_M1 IN\_M2 | Analog IO  ADC | 9  12  10  11 |  |
| DVDD | IO Power | 22 |  |

Table 26 – Internal pad circuitry

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**28 QFN Package Dimensions** 









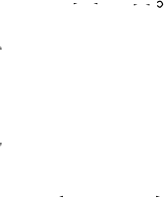


Figure 25 – 28 QFN package dimensions

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**28 QFN Top View Marking**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Package Type | A | B | C | D | E | F | G |
| QFN 5mm x 5mm | 4.0 | 1.6 | 0.2 | 0.4 | 0.2 | 0.1 | 0.3 |

|  |  |
| --- | --- |
| Mnemonic | Description |
| T | Tracking number |
| W | Work week |
| Y | Last digit of year |
| L | Lot number |
| R | Silicon Revision |

*Marking is subject to change. This drawing is not to scale.*

Figure 26 – ES9821Q QFN Marking

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**Reflow Process Considerations**

**Temperature Controlled**

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size   
(RPC-2 Pb-Free Process – Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

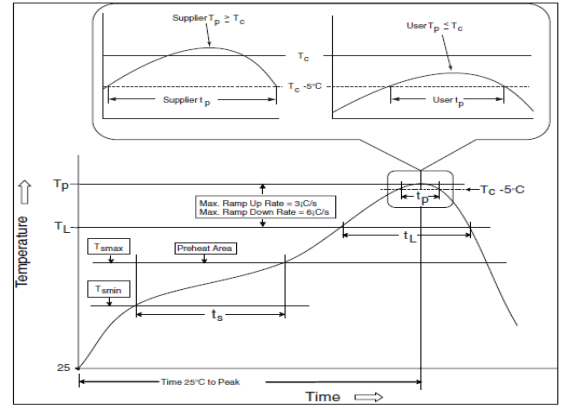


Figure 27 – IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

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Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

**Manual**

Allowed up to 2 times with maximum temperature of 350°C no longer than 3 seconds.

**RPC-1 Classification reflow profile**

|  |  |
| --- | --- |
| **Profile Feature** | **Pb-Free Assembly** |
| **Preheat/Soak**  Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax) | 150°C  200°C  60-120 seconds |
| Ramp-up rate (TL to Tp) | 3°C / second maximum |
| Liquidous temperature (TL) Time (tL) maintained above TL | 217°C  60-150 seconds |
| Peak package body temperature (Tp) | For users Tp must not exceed the classification temp in Table RPC-2.  For suppliers Tp must equal or exceed the Classification temp in Table RPC-2. |
| Time (tp)\* within 5°C of the specified classification temperature (Tc), see **Error! Reference source not found.**9 | 30\* seconds |
| Ramp-down rate (Tp to TL) | 6°C / second maximum |
| Time 25°C to peak temperature | 1. minutes maximum |
| * Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum. | |

Table 27 – RPC-1 Classification reflow profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.

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For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds. For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

**RPC-2 Pb-Free Process – Classification Temperatures (Tc)**

|  |  |  |  |
| --- | --- | --- | --- |
| **Package Thickness** | **Volume mm3, <350** | **Volume mm3, 350 to 2000** | **Volume mm3, >2000** |
| <1.6 mm | 260°C | 260°C | 260°C |
| 1.6 mm – 2.5 mm | 260°C | 250°C | 245°C |
| >2.5 mm | 250°C | 245°C | 245°C |

Table 28 – RPC-2 Pb free classification temperatures

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

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**Ordering Information**

|  |  |  |
| --- | --- | --- |
| **Part Number** | **Description** | **Package** |
| **ES9821Q** | SABRE 32-bit 2 Channel ADC with built in digital filters, and multiple output formats | 5mm x 5mm 28 QFN |
| **ES9821QT\***   * **Inquire for availability** | ES9821Q with extended temperature range (-40 deg C to 105 deg C) | 5mm x 5mm 28 QFN |

Table 29 – Ordering information

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**Revision History**

Current Version 0.4

|  |  |  |
| --- | --- | --- |
| **Rev.** | **Date** | **Notes** |
| 0.1.3 | Nov 5, 2021 | Initial release |
| 0.1.4 | Dec 21, 2021 | * Updated Register 42 descriptions for clarity * Updated HW/SW schematics with correct AVCC voltage |
| 0.2.1 | Sept, 2022 | * Added HW modes 12-15 to Hardware Mode Pin Configurations * Reserved Register 12[6] & [2] * Unreserved Register 193[5:4] * Update Power Consumption numbers * Reserved Register 194 * Updated Register 224,225, 32-40, 4[7] * Added note to add pullup resistors for I2S software mode * Updated Performance Table values * Removed PU from Digital I/O equivalent circuit * Updated Register 202-200: PLL SETTING 3 [18:1] descriptions * Added Analog PLL section |
| 0.3.1 | Feb, 2023 | * Updated Testing Conditions for Analog Performance table * Added image and wording to THD compensation section * Added Audio Output Formats in Digital Features * Added DC Blocking info in Hardware Mode section * Added GPIO5 designation in Hardware Mode tables * Updated APLL section register reference to correct register * Changed “MSB” Justified to “Left” Justified * Updated power consumption table * Added register overview section * Added Timing requirements sections * Updated SPI and I2C sections * Added Configuration Modes section over Hardware and Software Modes * Added design information under Hardware modes * Updated Digital Signal Path diagram * Added PCM/TDM MCLK/BCLK to timing requirements * Unreserved Register 0[6-5], 193[0], updated other registers * Added Software Mode recommended startup * Moved RC information to Hardware Mode * Updated reference schematics * Updated APLL section |
| 0.4 | May, 2023 | * Updated Register 192[0] * Updated formatting |

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|  |  |  |
| --- | --- | --- |
|  |  | * Updated digital filter section * Reserved HW modes 9-11, 13-15 * Updated Registers 53-46 * Updated Clock distribution section * Updated HW mode table, added notes * Updated HW reference schematic |

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