DG0634
Demo Guide
Running CoreTSE_AHB IP based Webserver on SmartFusion2 using lwIP and FreeRTOS - Libero SoC v11.7 SP2

Microsemi
Power Matters.™

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

50200634. 3.0 11/16

Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- Libero SoC, FlashPro, and SoftConsole design requirements were updated. For more information, see Design Requirements, page 4.
- Throughout the document, the names of SoftConsole projects used in the demo design (and the associated figures) were updated.

1.2 Revision 2.0

Updated the document for Libero v11.7 software release (SAR 77067).

1.3 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Running CoreTSE_AHB IP based Webserver on SmartFusion2 Devices

This demo design associated with this document shows the CoreTSE_AHB IP based implementation of the Webserver application on the SmartFusion2 Security Evaluation Kit. SmartFusion2 devices have built-in microcontroller subsystem (MSS) media access controller (MAC) for Ethernet solutions. This demo guide describes how to use the CoreTSE_AHB intellectual property (IP) core and not MSS Ethernet MAC for running the Webserver application. The soft IP CoreTSE_AHB is useful when a solution demands more than one Ethernet interface. Microsemi Core Triple-Speed (CoreTSE) Ethernet IP is a configurable soft IP core that complies with the IEEE 802.3 standard.

The CoreTSE IP core enables system designers to implement a broad range of Ethernet designs, from low cost 10/100 Ethernet to higher performance 1 gigabit ports. The CoreTSE IP core is suited for use in networking equipment such as switches, routers, and data acquisition systems.

The CoreTSE IP has the following major interfaces:

- 10/100/1000 Mbps Ethernet MAC with a gigabit media independent interface (GMII) and ten bit interface (TBI) to support serial gigabit media independent interface (SGMII), 1000BASE-T, and 1000BASE-X.
- GMII or TBI physical layer interface connects to Ethernet PHY
- MAC data path interface

The CoreTSE IP Ethernet MAC can be configured as GMII or TBI for Ethernet network at 10/100/1000 Mbps data transfer rates (line speeds).

The CoreTSE IP core is available in two different versions:

- CoreTSE_AHB: Uses AHB interface for both the transmit and receive paths. This IP works for SmartFusion2 system-on-chip (SoC) field programmable gate array (FPGA).
- CoreTSE (Non-AMBA): Uses direct access to the MAC with a streaming packet interface. This IP works for IGLOO®2 FPGA.

For more information about CoreTSE_AHB IP, see the *CoreTSE_AHB Handbook*.

Note: CoreTSE_AHB IP core requires license for using in Libero® SoC design. For license request, contact soc_marketing@microsemi.com.

This demo demonstrates the following

- Use of CoreTSE_AHB IP-based Ethernet MAC connection to a serial gigabit media independent interface (SGMII) PHY.
- Integration of CoreTSE_AHB driver with the lwIP TCP/IP stack and the FreeRTOS operating system.
- Implementation of Webserver on the SmartFusion2 Security Evaluation Kit board.
- Procedure to run the Webserver design on the SmartFusion2 Security Evaluation Kit board.

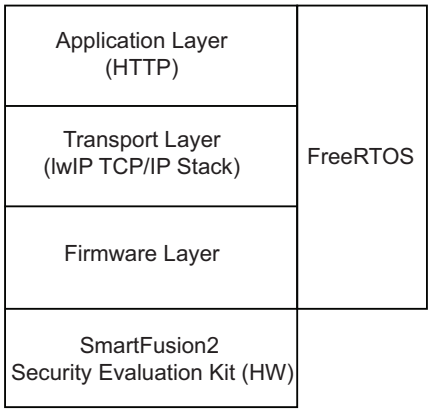
2.1 Webserver Demo Design Layers

The Webserver and TFTP server demo designs have the following layers.

- Application layer
- Transport layer (lwIP TCP/IP stack)
- RTOS and firmware layer

The following figure is a block diagram of three layers in Webserver application on the SmartFusion2 device.

Figure 1 • **Webserver Application on a SmartFusion2 FPGA**



2.1.1 Application Layer

The Webserver handles the HTTP request from the client browser and transfers the static pages to the client in response to their request. These pages run on the client (host PC) browser. When the URL with IP address (for example, http://10.60.3.25) is typed in the browser, the HTTP request is sent to the port on the Webserver. The Webserver interprets the request and responds to the client with the requested page or resource.

2.1.2 Transport Layer (lwIP TCP/IP Stack)

The lwIP TCP/IP stack, developed by Adam Dunkels at the swedish institute of computer science (SICS), is suitable for the embedded systems because of its low system resource usage. The lwIP stack can be used with or without the operating system. It consists of the actual implementations of IP, ICMP, UDP, and TCP protocols, as well as the support functions such as buffer and memory management.

The lwIP is available (under a BSD license) in C source-code format for download at http://download.savannah.gnu.org/releases/lwip/.

2.1.3 RTOS and Firmware Layer

FreeRTOS is an open-source, real-time operating system kernel. In this demo FreeRTOS is used to prioritize and schedule tasks. For more information and the latest source code, see http://www.freertos.org.

The firmware provides the software driver implementation to configure and control the following MSS components:

- Multi-mode universal asynchronous receiver/transmitter (MMUART)
- General purpose input and output (GPIO)
- Real-time clock (RTC)

2.2 Design Requirements

The following table lists the hardware, software, firmware, and IP requirements for this demo design.

Table 1 • **Design Requirements**

Design Requirements	Description
Hardware	
SmartFusion2 Security Evaluation Kit: - 12 V adapter - FlashPro4 - USB A to Mini-B cable	Rev D or later
RJ45 cable	–
Host PC or Laptop	Windows 64-bit Operating System
Software	
Libero System-on-Chip (SoC)	v11.7 SP2
FlashPro Programming Software	v11.7 SP2
SoftConsole	v4.0
Host PC Drivers	*USB to UART drivers*
Browser	Mozilla Firefox or Internet Explorer
CoreTSE Driver	v2.3.100
IP	
CoreTSE_AHB IP	v2.1.105 (license provided on request)

2.3 Demo Design

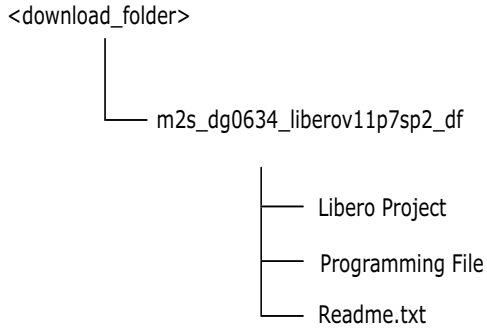
The demo design files are available for download at:
http://soc.microsemi.com/download/rsc/?f=m2s_dg0634_liberov11p7sp2_df

The demo design files include:

- A Libero SoC hardware project with the corresponding SoftConsole firmware project
- Sample files
- Programming files
- A `Readme.txt` file

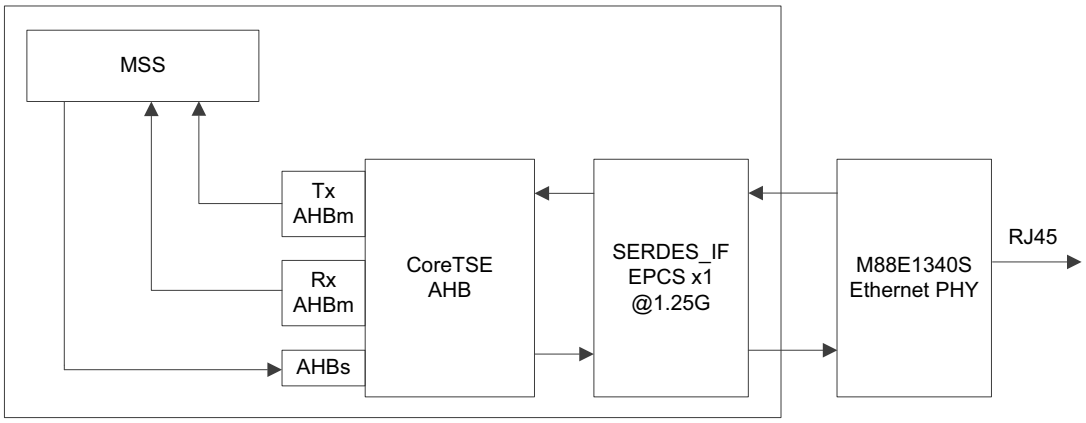
The following figure shows the top-level structure of the demo design files. For more information, see the `Readme.txt` file.

Figure 2 • **Demo Design Files Top-Level Structure**



The following figure shows the demo design block diagram.

Figure 3 • **Block Diagram of CoreTSE_AHB Webserver Demo**



In the Webserver demo design, CoreTSE_AHB IP is instantiated in the FPGA fabric and connected to the on-board Ethernet Marvell PHY using the high-speed serial interface (SERDES_IF).

The following sections explain the initialization and configuration of CoreTSE_AHB, SERDES_IF and the Ethernet packet transmission and reception.

2.3.1 CoreTSE_AHB IP MAC Initialization

The CoreTSE_AHB IP MAC is configured in the TBI mode. The ARM Cortex-M3 (micro controller subsystem) is used to initialize the CoreTSE_AHB IP MAC in 1000 Base-T and the on-board Ethernet PHY.

2.3.2 SERDES_IF Configuration

The high-speed SERDES_IF is configured in the external physical coding sub layer (EPCS) mode lane 3 and is connected between the CoreTSE_AHB IP MAC and the on-board Ethernet PHY.

2.3.3 Ethernet Packet Reception

The CoreTSE_AHB IP MAC receives the Ethernet packet from the on-board Ethernet PHY through high-speed SERDES_IF using the built-in DMA controller.

2.3.4 Ethernet Packet Transmission

CoreTSE_AHB MAC transmits the Ethernet packet from the built-in DMA controller to the on-board Ethernet PHY through high-speed SERDES_IF.

The Security Evaluation Kit acts as a Webserver and the host PC acts as a web client that accesses the Webserver features through the RJ45 interface.

2.4 Demo Design Features

- Webserver: Displays options for the following:
  - RTC and Ethernet interface data display
  - Blinking LEDs
  - HyperTerminal display
  - SmartFusion2 Google search

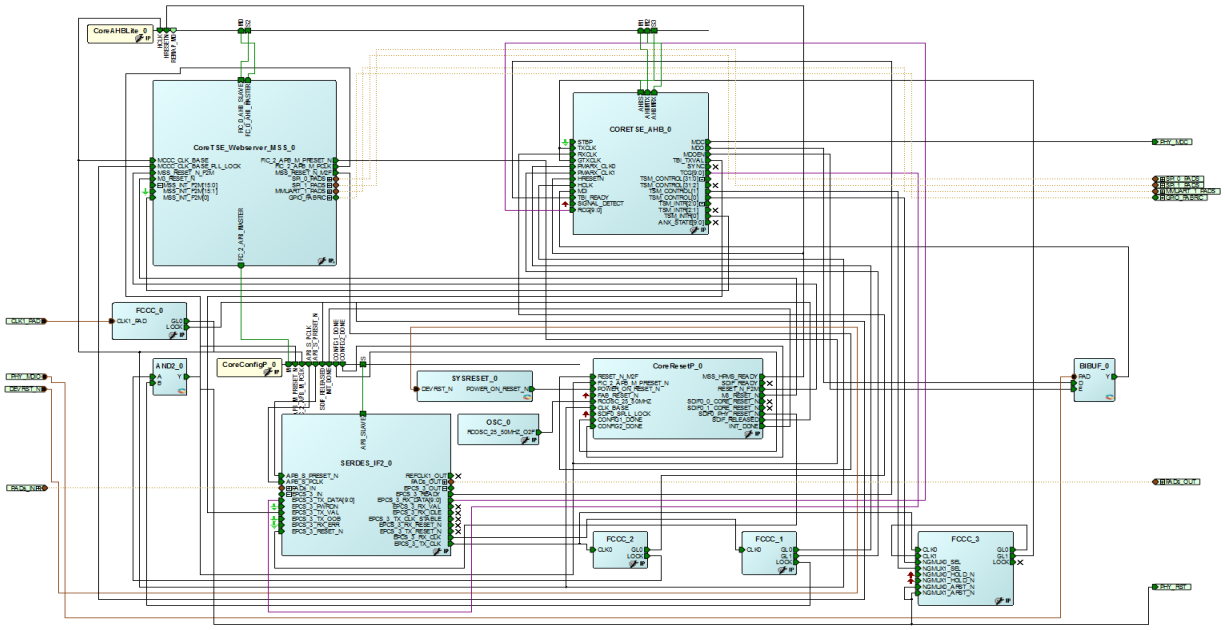
2.5 Demo Design Description

The demo design is implemented using an SGMII PHY interface by configuring the CoreTSE_AHB IP MAC for the ten-bit interface (TBI) operation.

2.5.1 Libero SoC Hardware Project

The following figure shows the Libero SoC hardware design implementation for the demo design.

Figure 4 • **Libero SoC Top-Level Hardware Design**

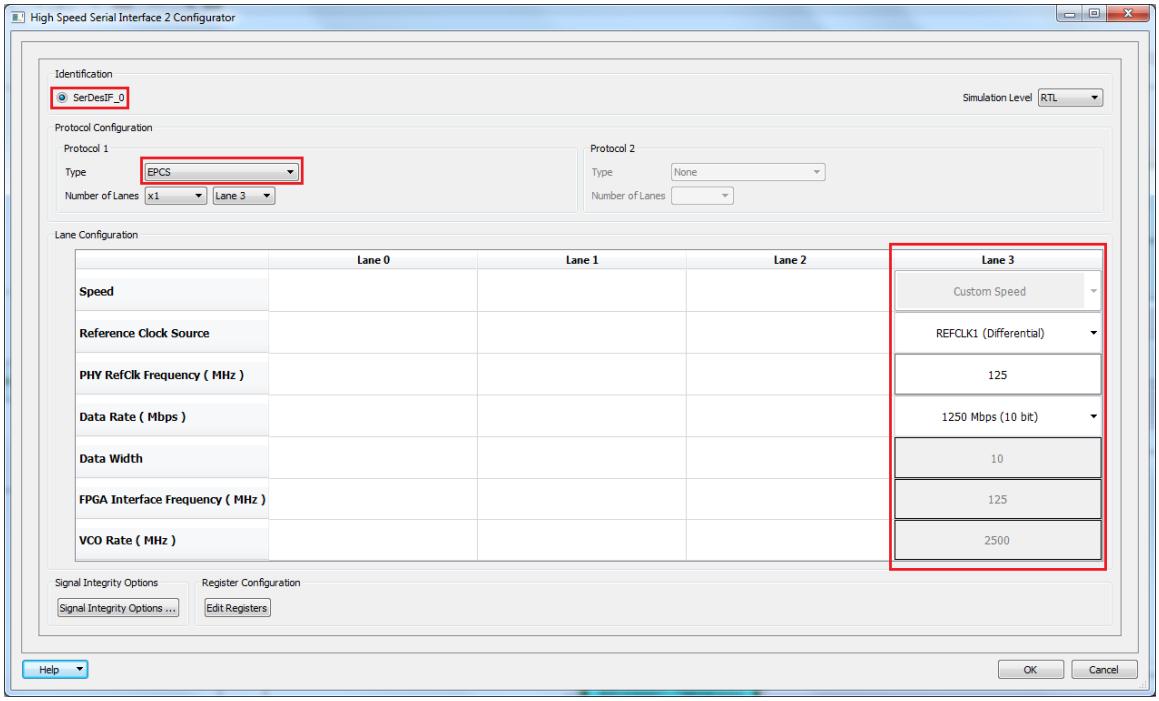


The Libero SoC hardware project uses the following SmartFusion2 MSS resources and IPs:

- **MMUART_1** for RS-232 communications on the Security Evaluation Kit
- **GPIO**: Interfaces the light emitting diodes (LEDs)
- **CoreTSE_AHB IP** core
- SERDES_IF and **SERDES_IF_2** configured for **SERDESIF_0 EPCS Lane 3**, as shown in the following figure.

For more information on SERDES_IF, see the *UG0447: SmartFusion2 and IGLOO2 High Speed Serial Interfaces User Guide.*

Figure 5 • **High-Speed Serial Interface Configurator Window**



2.5.1.1 Package Pin Assignment

Each LED and PHY interface signal on the SmartFusion2 board has a package pin assigned to it.

The following table lists the LED port names and corresponding package pins.

Table 2 • **LED to Package Pin Assignment**

Port Name	Package Pin
LED_1	E1
LED_2	F4
LED_3	F3
LED_4	G7
LED_5	H7
LED_6	J6
LED_7	H6
LED_8	H5

The following table lists the PHY interface signals, signal direction, and corresponding package pins.

Table 3 • **PHY Interface Signals to Package Pins Assignments**

Port Name	Direction	Package Pin
PHY_MDC	Output	J3
PHY_MDIO	Input	J4
PHY_RST	Output	K6

2.5.1.2 SoftConsole Firmware Project

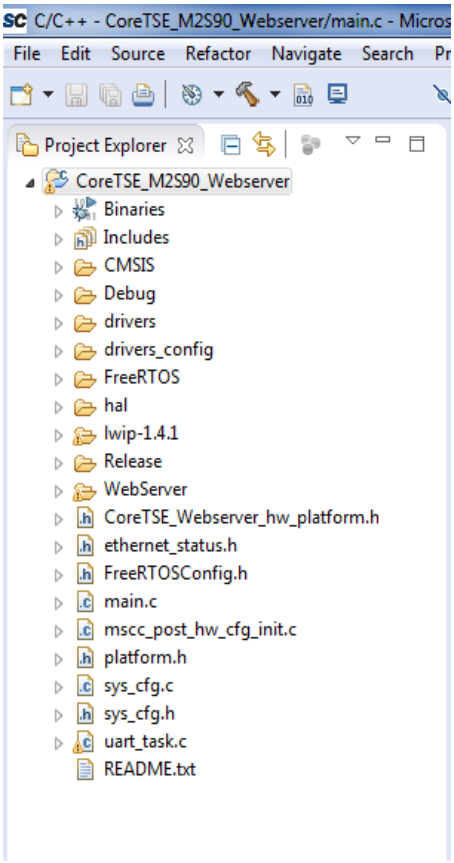
Open the CoreTSE_AHB Webserver SoftConsole project using the standalone SoftConsole IDE.

The following stacks are used for this demo design:

- **lwIP TCP/IP** stack version 1.4.1
- **FreeRTOS** (www.freertos.org)

The following figure shows the SoftConsole software directory structure of the demo design.

Figure 6 • **SoftConsole Project Explorer Window**



The SoftConsole workspace has CoreTSE_M2S90_Webserver, which contains implementation of the Webserver application using lwIP and FreeRTOS.

Note: To run the SoftConsole project in debug mode, see Appendix: Running the SoftConsole Project in Debug Mode, page 23.

The following figure shows the driver versions used for the demo.

Figure 7 • **Demo Design Driver Versions**

	Generate		Instance Name	Core Type	Version	Compatible Hardware Instance
1	☑		CoreTSE_Driver_0	CoreTSE_Driver	2.3.100	CoreTSE_Webserver:CORETSE_AHB_0
2	☑		SmartFusion2_CMSIS_0	SmartFusion2_CMSIS	2.3.105	CoreTSE_Webserver_MSS
3	☑		SmartFusion2_MSS_GPIO_Driver_0	SmartFusion2_MSS_GPIO_Driver	2.1.102	CoreTSE_Webserver_MSS:GPIO
4	☑		SmartFusion2_MSS_HPDMA_Driver_0	SmartFusion2_MSS_HPDMA_Driver	2.2.100	CoreTSE_Webserver_MSS
5	☑		SmartFusion2_MSS_MMUART_Driver_0	SmartFusion2_MSS_MMUART_Driver	2.1.100	CoreTSE_Webserver_MSS:MMUART_1
6	☑		SmartFusion2_MSS_NVM_Driver_0	SmartFusion2_MSS_NVM_Driver	2.4.100	CoreTSE_Webserver_MSS
7	☑		SmartFusion2_MSS_RTC_Driver_0	SmartFusion2_MSS_RTC_Driver	2.2.100	CoreTSE_Webserver_MSS:RTC
8	☑		SmartFusion2_MSS_SPI_Driver_0	SmartFusion2_MSS_SPI_Driver	2.2.101	CoreTSE_Webserver_MSS:SPI_0
9	☑		SmartFusion2_MSS_SPI_Driver_1	SmartFusion2_MSS_SPI_Driver	2.2.101	CoreTSE_Webserver_MSS:SPI_1
10	☑		SmartFusion2_MSS_System_Services_Driver_0	SmartFusion2_MSS_System_Services_Driver	2.7.100	CoreTSE_Webserver_MSS
11	☑		SmartFusion2_MSS_Timer_Driver_0	SmartFusion2_MSS_Timer_Driver	2.2.100	CoreTSE_Webserver_MSS

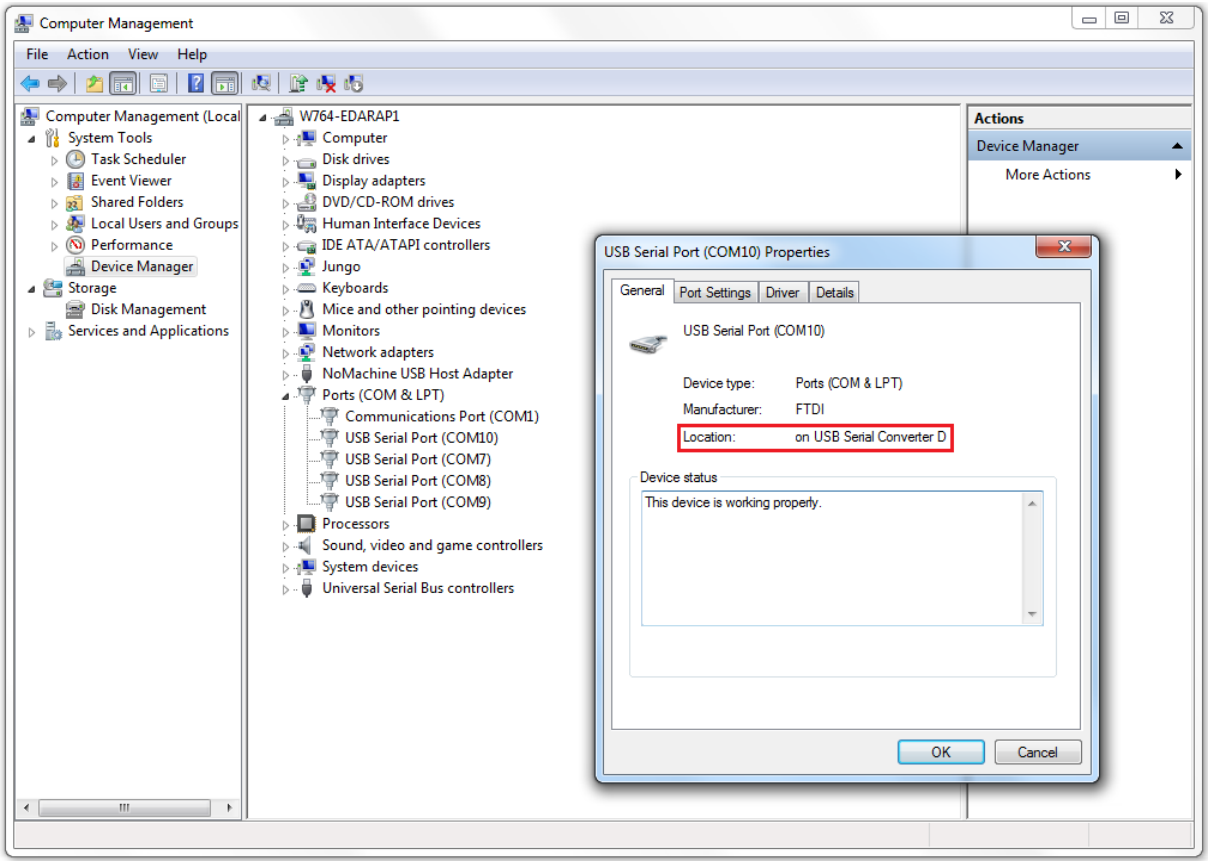
2.6 Setting Up the Demo Design

The following steps describe how to setup the demo for the SmartFusion2 Security Evaluation Kit board:

1. Connect the host PC to the J18 connector using the USB A to Mini-B cable. The USB to UART bridge drivers are automatically detected.
2. From the detected four COM ports, right-click any one of the COM ports and select Properties. The selected COM port properties window is displayed.
3. Ensure to have the **Location** as **on USB Serial Converter D** in the Properties window, as shown in the following figure.

Note: Make a note of the COM port number for serial port configuration and ensure that the COM port location is specified as **on USB Serial Converter D**.

Figure 8 • **Device Manager Window**



4. Install the USB driver, if it is not detected automatically.
5. Install the FTDI D2XX driver for serial terminal communication through the FTDI Mini USB cable.

Download the drivers and installation guide from:
www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip.

6. Connect the jumpers on the SmartFusion2 Security Evaluation Kit board, as shown in the following table. For information on jumper locations, see Appendix: Jumper Locations, page 19.

CAUTION: Switch **OFF** the power supply switch, **SW7**, before making the jumper connections.

Table 4 • **SmartFusion2 FPGA Security Evaluation Kit Jumper Settings**

Jumper	Pin From	Pin To	Comments
J22, J23, J24, J8, J3	1	2	These are the default jumper settings of the SmartFusion2 Security Evaluation Kit board. Ensure that jumpers are set accordingly.

7. Connect the power supply to the J6 connector in the SmartFusion2 Security Evaluation Kit.
8. This design example can run in both static IP and dynamic IP modes. By default, the programming files are provided for dynamic IP mode.
    - For static IP, connect the host PC to the J13 connector on the SmartFusion2 Security Evaluation Kit board using an RJ45 cable.
    - For dynamic IP, connect any one of the open network ports to the J13 connector of the SmartFusion2 Security Evaluation Kit board using an RJ45 cable.

2.6.1 Board Setup

Snapshots of the SmartFusion2 Security Evaluation Kit board with the setup is given in Appendix: Board Setup for Running the Demo, page 18.

2.7 Running the Demo Design

The following steps describe how to run the demo design.

1. Download the demo design from:
http://soc.microsemi.com/download/rsc/?f=m2s_dg0634_liberov11p7sp2_df
2. Switch **ON** the SW7 power supply switch.
3. Start any of the serial terminal emulation programs such as:
    - HyperTerminal
    - PuTTY
    - TeraTerm

Note: In this demo, HyperTerminal is used.

The configuration for the program is:

- Baud Rate: 115200
- Eight data bits
- One stop bit
- No parity
- No flow control

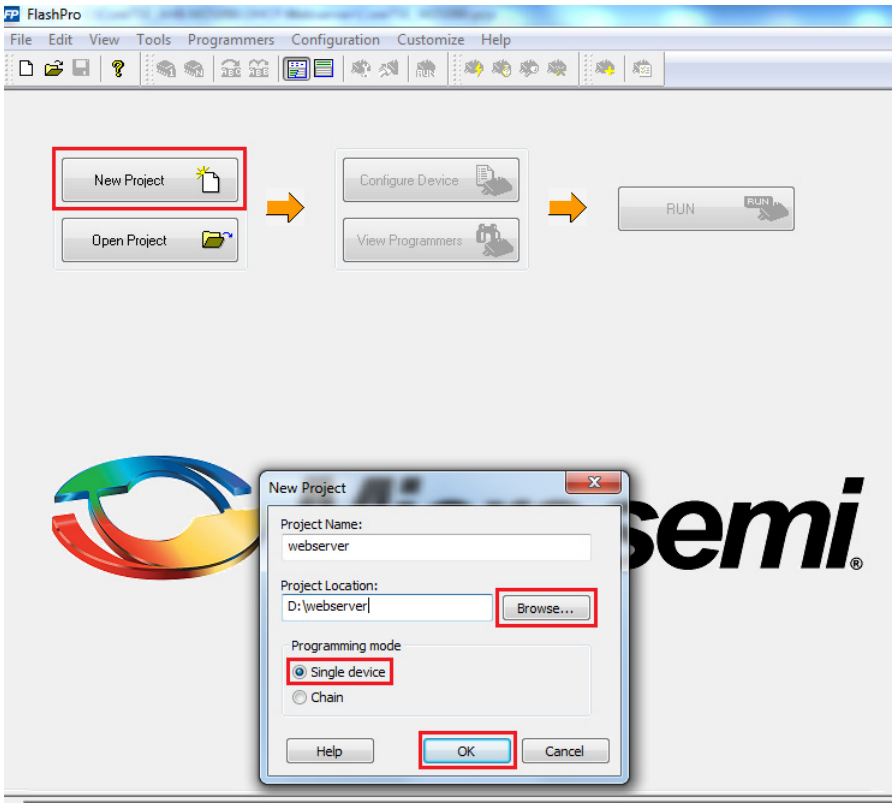
For information on configuring the serial terminal emulation programs, see the *Configuring Serial Terminal Emulation Programs Tutorial*.

2.7.1 Running Webserver Demo

The following steps describe how to run the Webserver demo:

1. Launch the **FlashPro** software.
2. Click **New Project**.
3. In the **New Project** window, enter the project name.

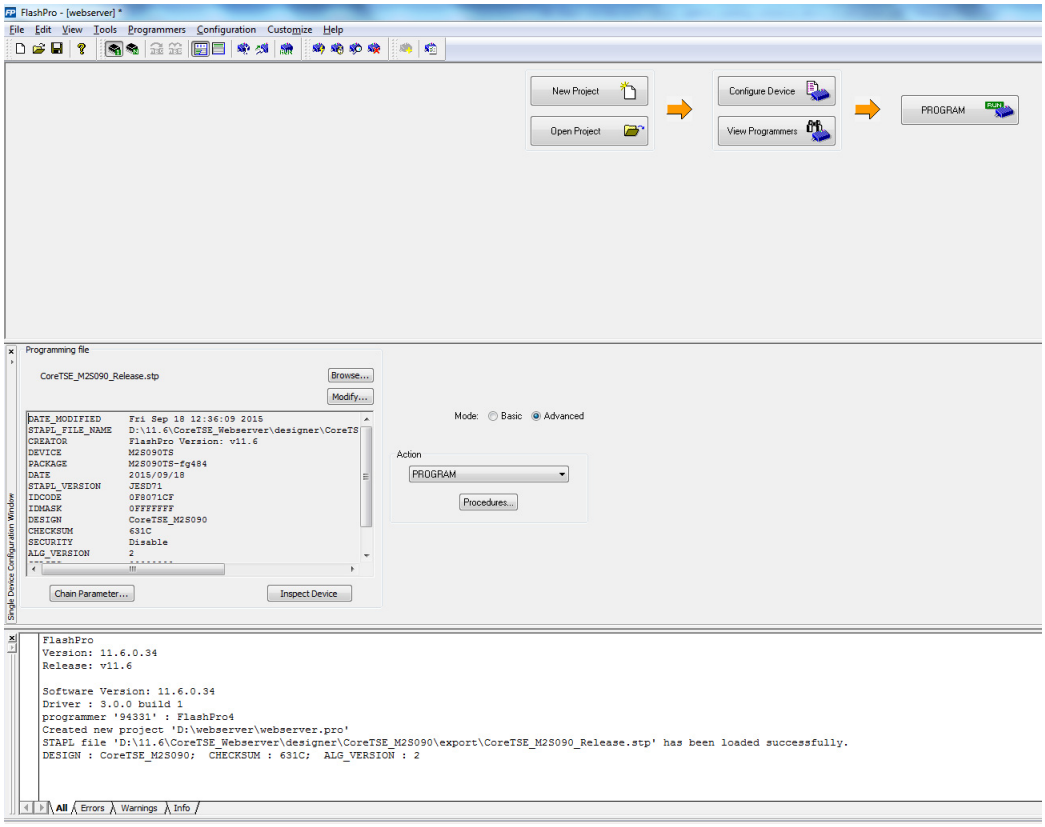
Figure 9 • **FlashPro New Project Window**



4. Click **Browse** and navigate to the location where the project is required to be saved.
5. Select **Single device** as the **Programming mode**.
6. Click **OK** to save the project.
7. Click **Configure Device,** as shown in Figure 10, page 12.

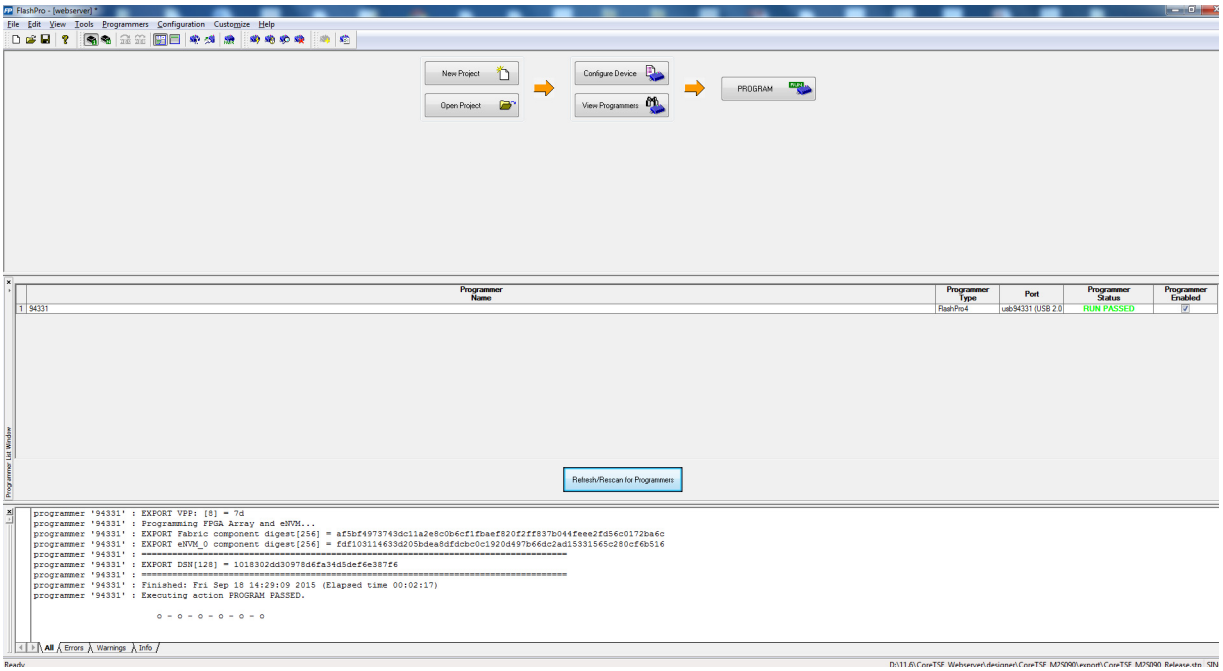
8. Click **Browse**, navigate to the location where the file is located and select the file. The default location is: *<download_folder>\ProgrammingFiles\webserver*. The required programming file is selected and is ready to be programmed in the device.

Figure 10 • **FlashPro Project Configuration Window**



9. Click **PROGRAM** to start programming the device. Wait until a message is displayed indicating that the program has passed.

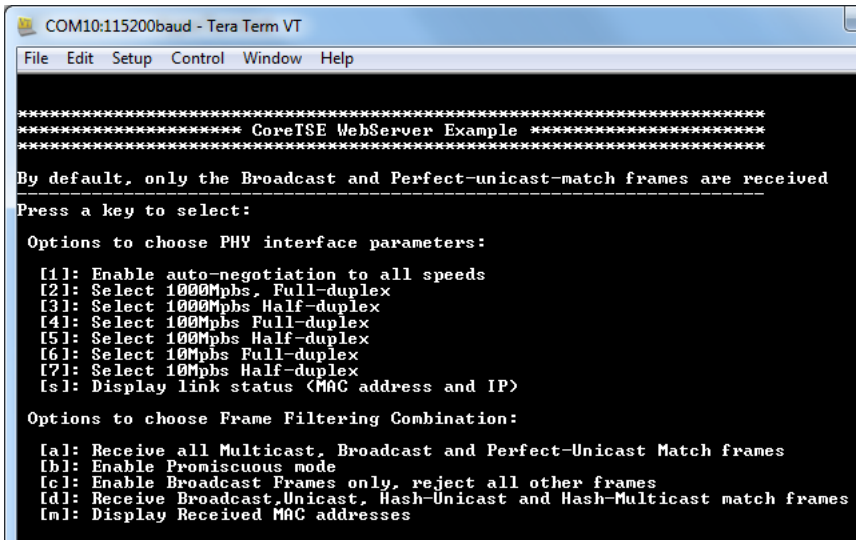
Figure 11 • **FlashPro Program Passed**



Note: The demo can be run in static and dynamic modes. To run the design in static IP mode, follow the steps mentioned in the Appendix: Running the Design in Static IP Mode, page 20.

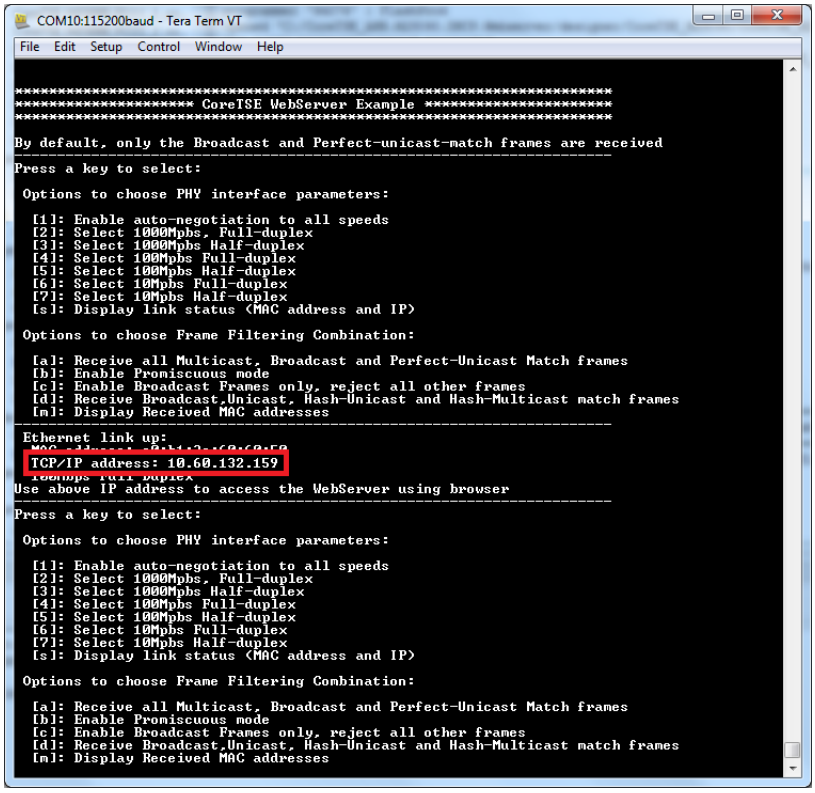
10. Power cycle the SmartFusion2 Security Evaluation Kit board.
    A welcome message is displayed in the HyperTerminal window, as shown in the following figure.

Figure 12 • **HyperTerminal with Welcome Message**



11. Press **S** on the keyboard till the IP address is displayed, as shown in following figure.

Figure 13 • **HyperTerminal with IP Address**

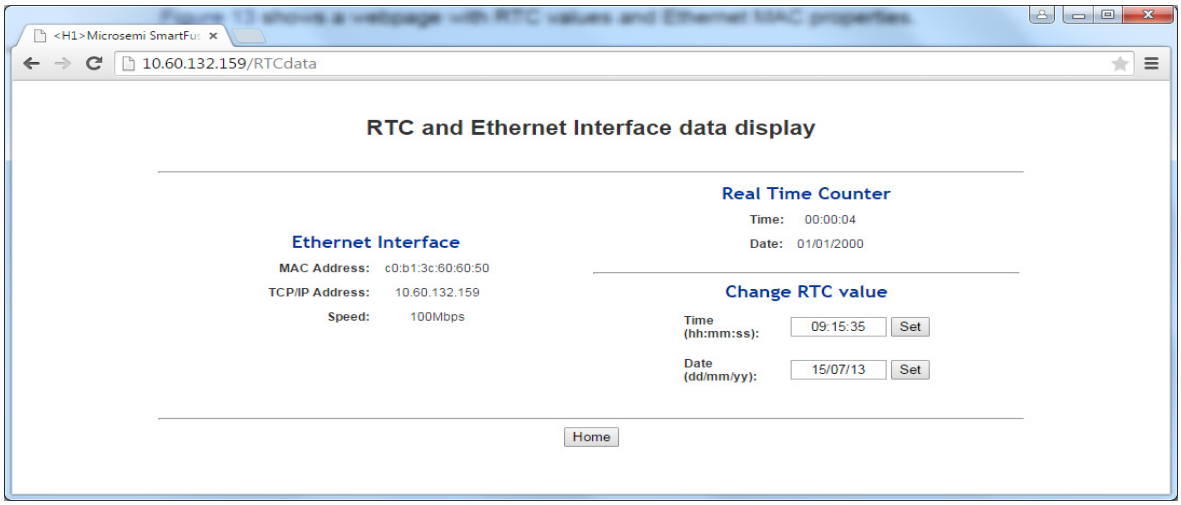


12. Enter the IP address displayed on the HyperTerminal in the address bar of the browser (Mozilla Firefox) to run the Webserver. The main menu of the Webserver is shown in Figure 14, page 14.
13. Click **RTC and Ethernet Interface data display**.

Figure 14 • **Main Menu of Webserver**

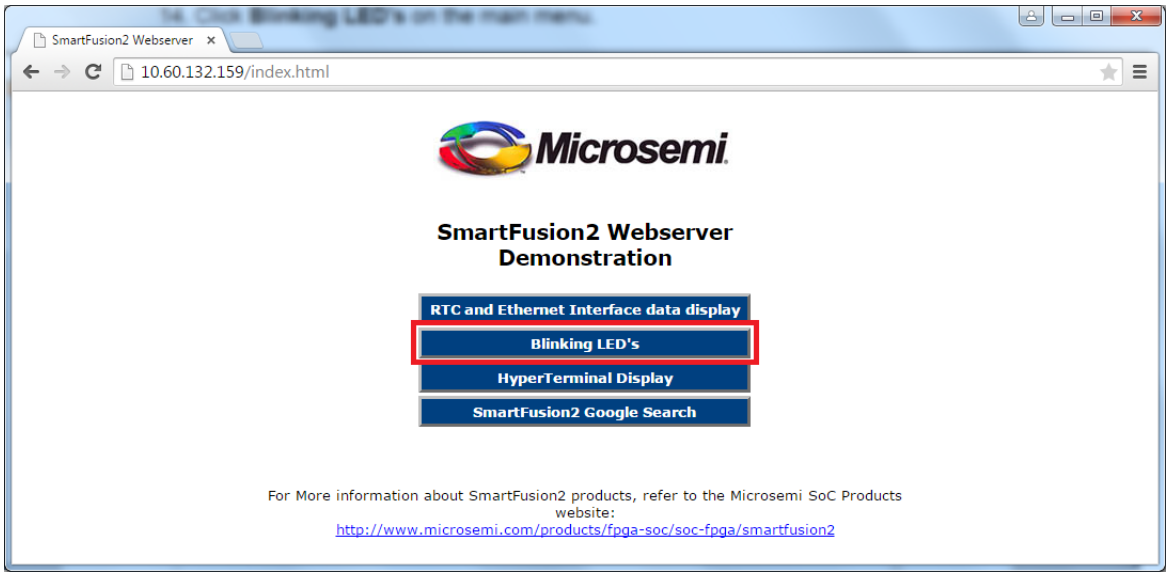
The following web page appears, displaying RTC values and Ethernet MAC properties.

Figure 15 • **Webserver RTC and Ethernet Interface Data Display**



14. Click **Home** to go back to the main menu.
15. Click **Blinking LEDs** on the main menu.

Figure 16 • **Selecting Blinking LEDs**

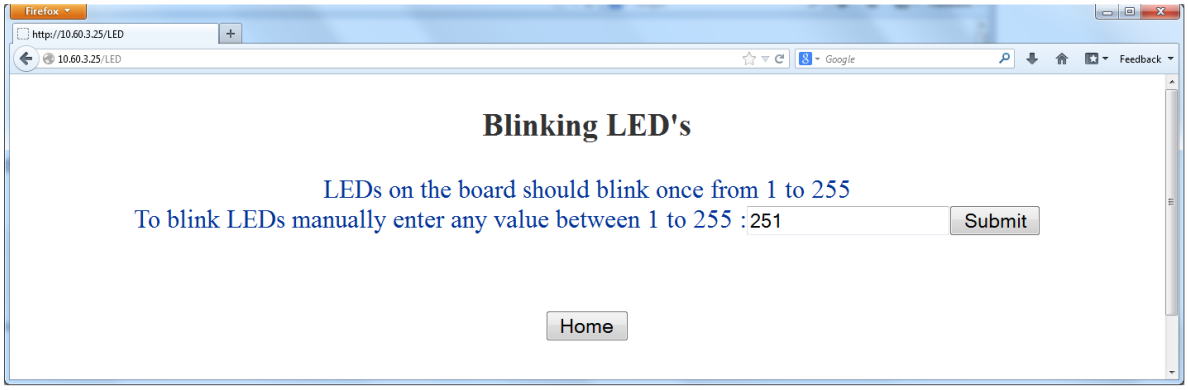


The LEDs on the board start blinking, and a web page appears, with an option to enter a values to toggle LEDs manually.

16. Enter any number between 1 to 255 to toggle the LEDs manually and click **Submit**.
    For example, if 1 is entered, LED1 goes OFF. If 255 is entered, all the eight LEDs go OFF.

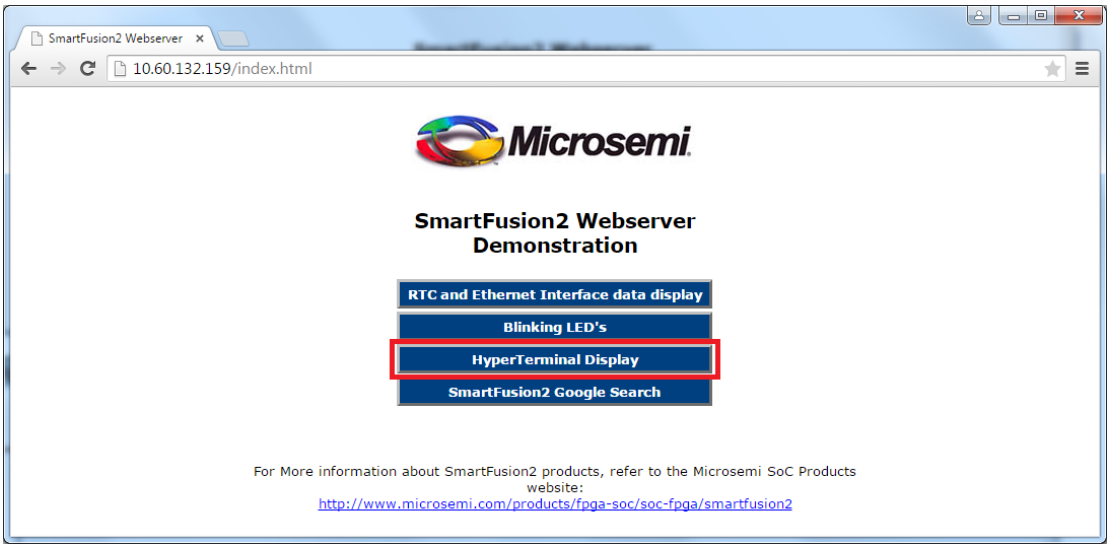
Note: The SmartFusion2 Security Evaluation Kit has Active Low LEDs.

Figure 17 • **Blinking LEDs**



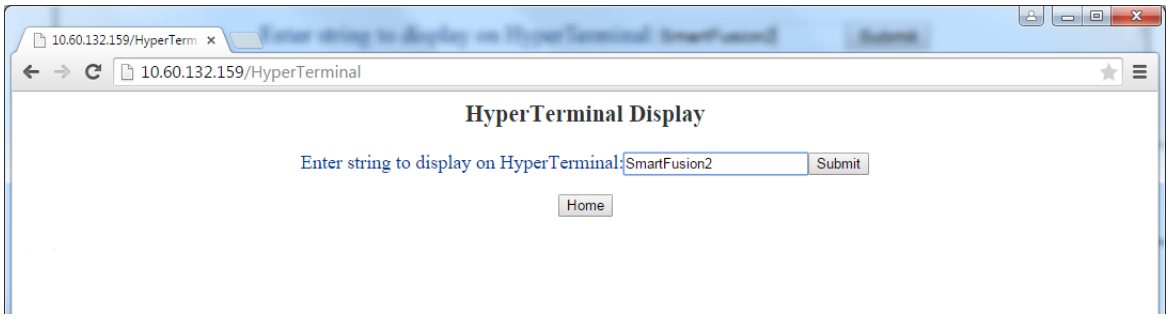
17. Click **Home** to go back to the main menu.
18. Click **HyperTerminal Display** on the main menu.

Figure 18 • **Selecting HyperTerminal Display**



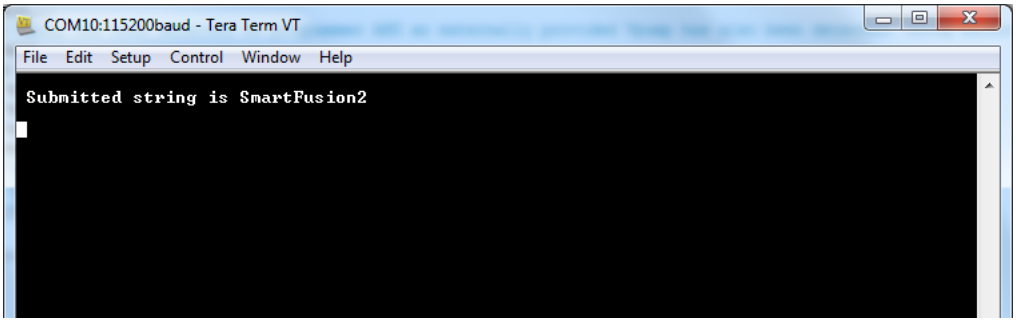
A web page appears with an option to enter a string value to be displayed in HyperTerminal.

Figure 19 • **Webserver HyperTerminal Display**



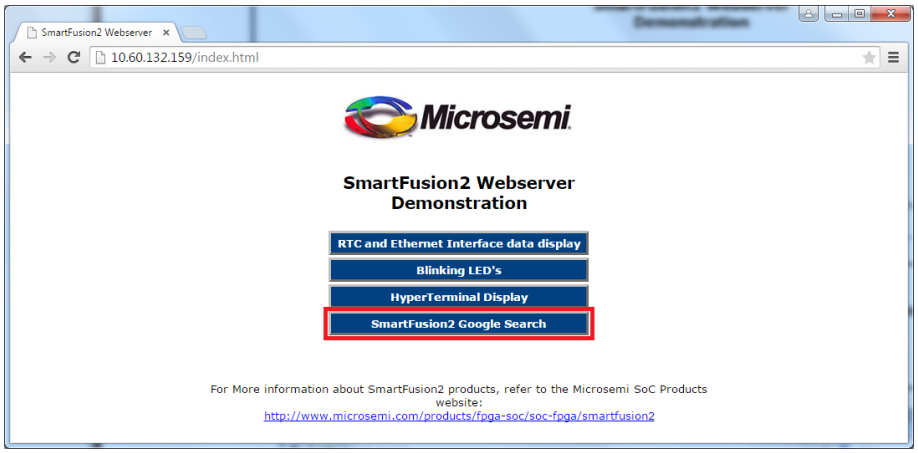
The entered string is displayed on HyperTerminal, as shown in the following figure.

Figure 20 • **String Display on HyperTerminal**



19. Click **Home** to go back to the main menu.
20. Click **SmartFusion2 Google Search**.

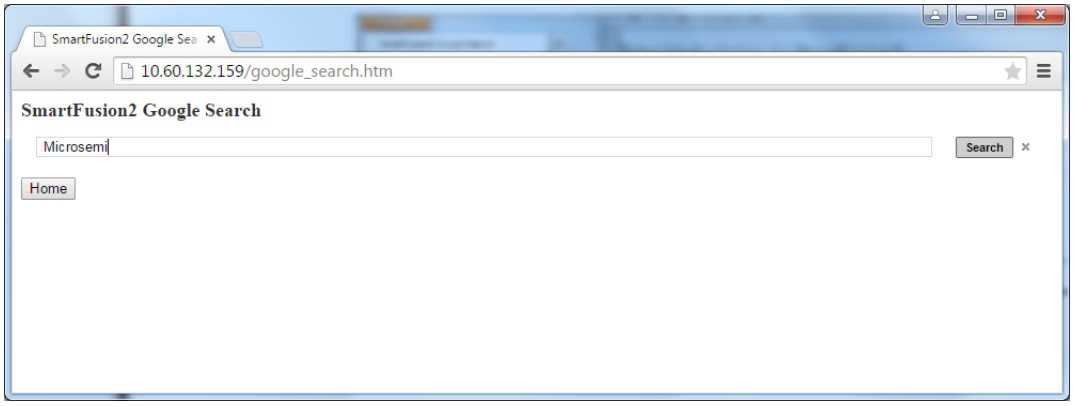
Figure 21 • **Selecting SmartFusion2 Google Search**



Note: An Internet connection is required to access the SmartFusion2 Google search page.

A web page appears, with the **SmartFusion2 Google search** option.

Figure 22 • **Webserver SmartFusion2 Google Search**

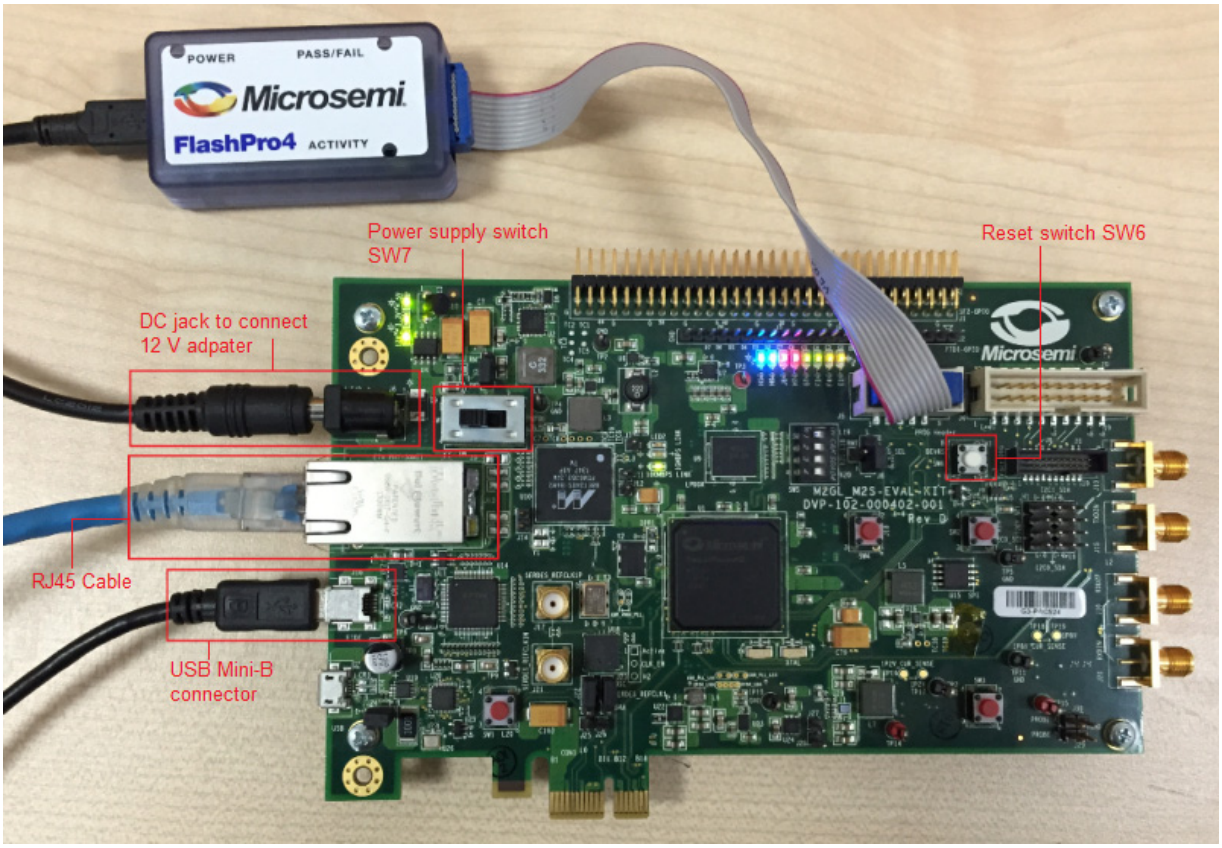


21. Click **Home** to go back to the main menu.

3 Appendix: Board Setup for Running the Demo

The following figure shows the board setup for running the demo on the SmartFusion2 Security Evaluation Kit board.

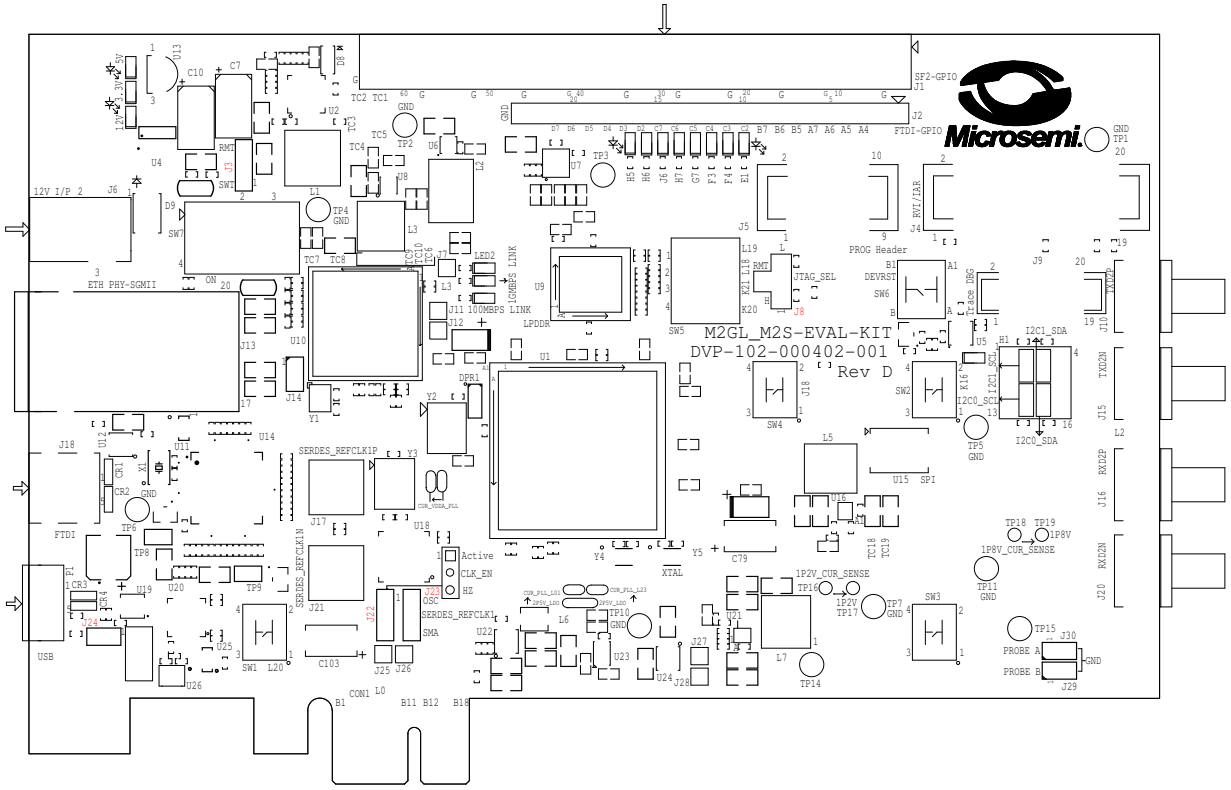
Figure 23 • **SmartFusion2 Security Evaluation Board Setup**



4 Appendix: Jumper Locations

The following figure shows the jumper locations in the SmartFusion2 Security Evaluation Kit board.

Figure 24 • **SmartFusion2 Security Evaluation Kit Silkscreen Top View**



Note: Jumpers highlighted in red are set by default.

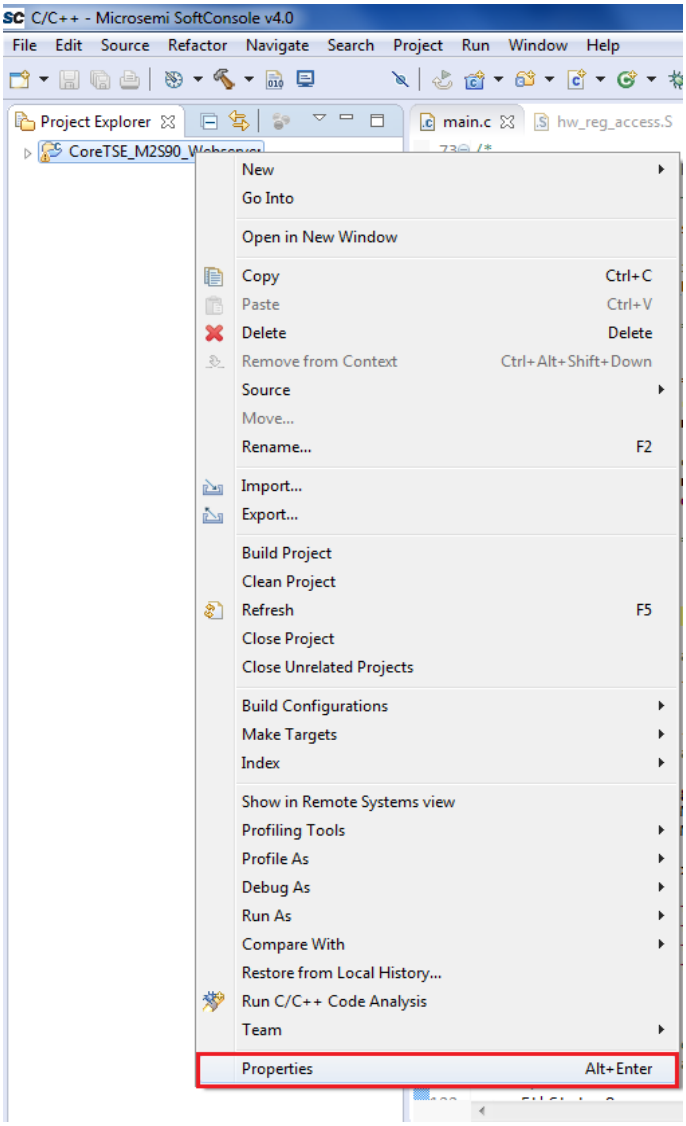
Note: The location of the jumpers in the preceding figure are searchable.

5 Appendix: Running the Design in Static IP Mode

The following steps describe how to run the design in static IP mode:

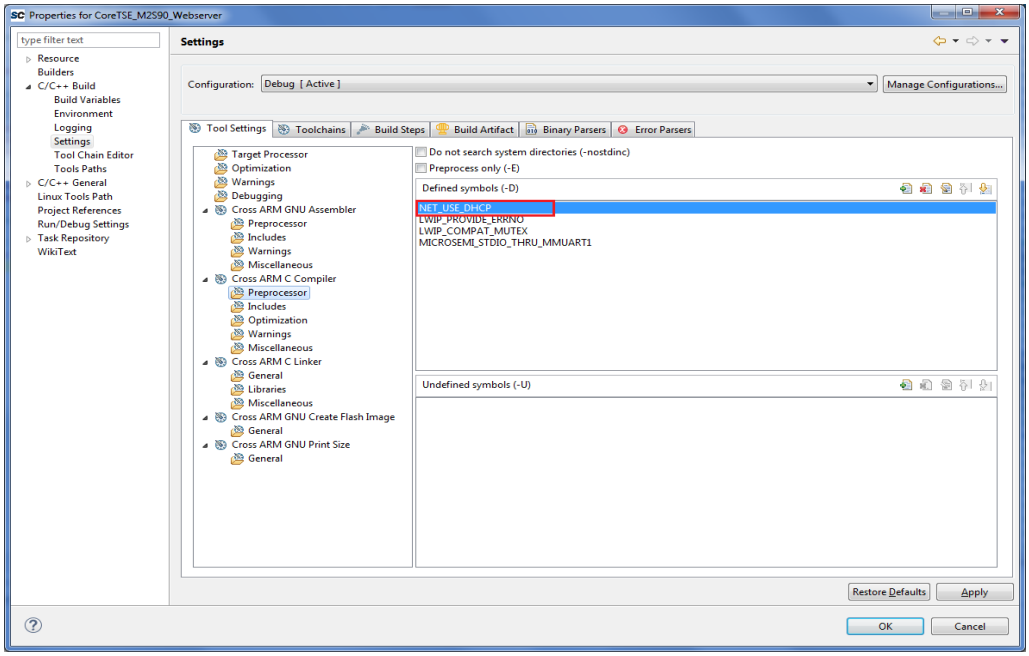
1. To run the webserver design in static IP mode, right-click the **CoreTSE_M2S90_Webserver project** and select **Properties,** as shown in the following figure.

Figure 25 • **Project Explorer Window of SoftConsole Project**



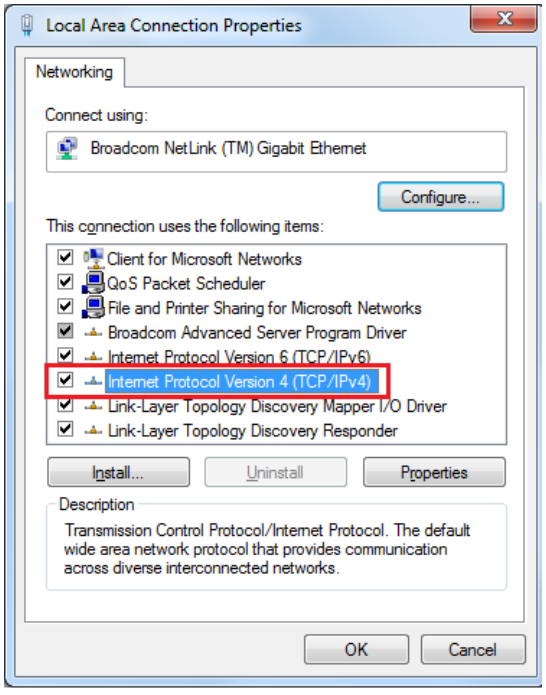
2. Remove the symbol **NET_USE_DHCP** in **Tool Settings** of the **Properties** for **CoreTSE_M2S90_Webserver** window, as shown in the following figure.

Figure 26 • **CoreTSE_M2S90_Webserver Properties Window**



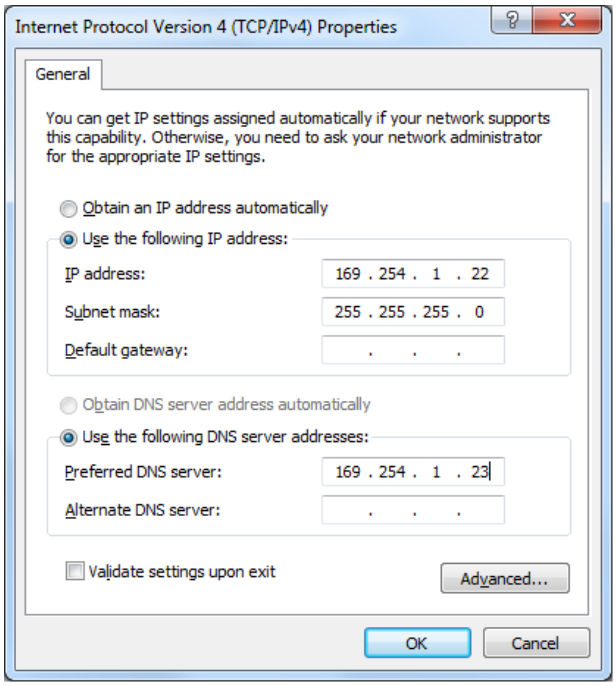
3. If the device is connected in static IP mode and the board static IP address is 169.254.1.23, change the host TCP/IP settings to reflect the IP address. The following figure shows the host PC TCP/IP settings.

Figure 27 • **Host PC TCP/IP Settings**



The following figure shows the static IP address settings.

Figure 28 • **Static IP Address Settings**



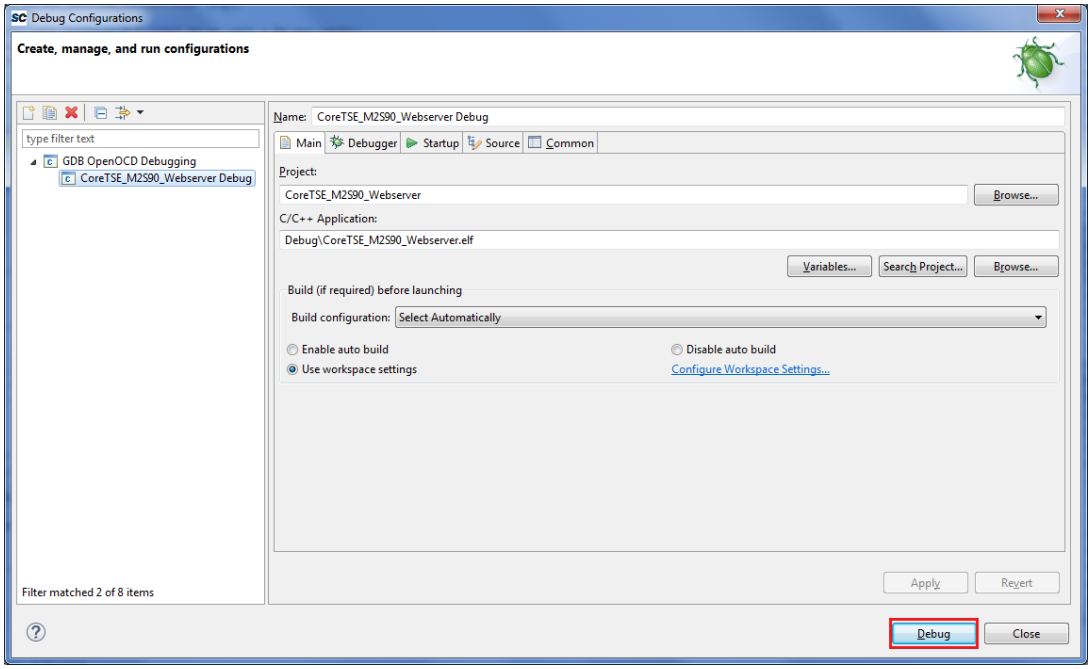
4. After configuring the settings, compile the design, load it into memory, and run it using SoftConsole.

6 Appendix: Running the SoftConsole Project in Debug Mode

The following steps describe how to run the SoftConsole project in Debug mode:

1. Select **Debug Configurations** from the **Run** menu of the SoftConsole. The **Debug Configurations** dialog box is displayed, as shown in the following figure.

Figure 29 • **Debug Configurations**



2. Select the target and click **Debug**.

Note: To run the application in debug mode, FlashPro4 JTAG programmer is required.