DG0441
Demo Guide
SmartFusion2 SoC FPGA Adaptive FIR Filter - Libero SoC v11.8 SP1

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Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 7.0

In revision 7.0, the document is updated for Libero v11.8 SP1 software release.

1.2 Revision 6.0

Updated the document for Libero v11.7 software release.

1.3 Revision 5.0

Updated the document for Libero v11.6 software release.

1.4 Revision 4.0

Updated the document for Libero v11.5 software release.

1.5 Revision 3.0

Updated the document for Libero v11.4 software release.

1.6 Revision 2.0

The following changes are made in revision 2.0 of this document

- Updated the document for Libero v11.3 software release.
- The Theory of Operation section is updated.

1.7 Revision 1.0

Revision 1.0 was the first publication of this document.

2 SmartFusion2 SoC FPGA - Adaptive FIR Filter Demo

2.1 Introduction

The SmartFusion®2 SoC FPGA devices integrate a fourth generation flash-based FPGA fabric and an ARM Cortex-M3 processor. The SmartFusion2 SoC FPGA fabric includes embedded mathblocks, which are optimized specifically for digital signal processing (DSP) applications such as,
finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast fourier transform (FFT) functions.

Adaptive filter automatically adjusts the filter coefficients according to the underlying adaptive algorithm and the input signal characteristics. Due to its self adjustment of transfer function of an unknown system and computational requirements, adaptive filters are widely used in different areas of DSP application such as communication, biomedical instrumentation, audio processing, and video processing.

The least mean square (LMS) is a basic adaptive algorithm used in adaptive filters to update the filter coefficients. The LMS algorithm has advantages over other algorithms because of its simplicity, less computations, and best performance in terms of the number of iterations required for convergence.

In this demo, an Adaptive FIR filter application, the suppression of a narrow band signal interference on a wide band signal is implemented using an SmartFusion2 device. Refer to Figure 1, page 2.

The LMS algorithm is implemented in the FPGA fabric to adjust the filter weights/coefficients based on mean square error (MSE) approach. CoreFIR IP is used to perform the filtering operation and CoreFFT IP is used to generate the output spectrum to observe that the narrow band interfering signal component is suppressed. The host interface is implemented in microcontroller subsystem (MSS) to communicate with the Host PC. A user friendly `SF2_Adaptive_FIR_Filter.exe` generates input signals (narrow band signal and wide band signal), and also plots the input or output waveforms and the required spectrum.

Figure 1 • **Narrowband Interference Cancellation**

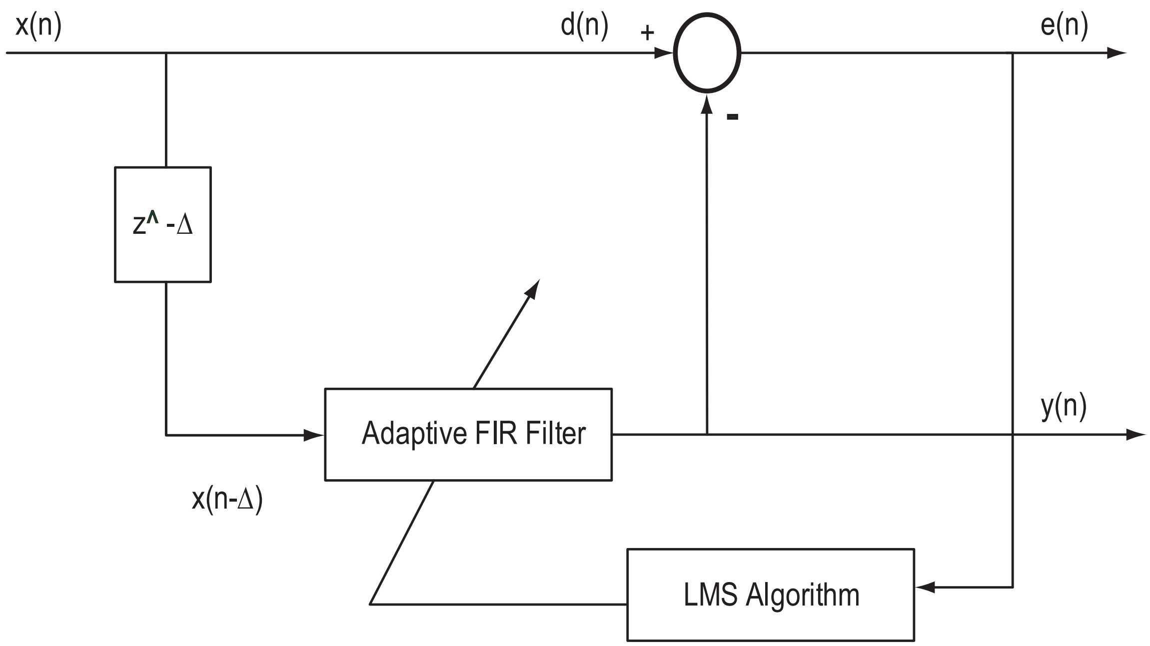
2.2 Theory of Operation

Adaptive filters are mainly categorized into four basic architectures:

- System identification
- Noise cancellation
- Linear prediction
- Inverse modeling

In this demo, linear prediction architecture is used to implement adaptive filter. The LMS algorithm uses a gradient search technique to determine the filter coefficients that minimize the mean square prediction error. The estimate of the gradient is based on the sample values of the tap-input vector and the error signal. The algorithm iterates over each coefficient in the filter, moving it in the direction of the approximated gradient. After reaching the optimal filter coefficients, the error signal e(n) consists of the wideband signal. The following figure shows the linear prediction based adaptive filter architecture.

Figure 2 • **Linear Prediction Adaptive Filter Architecture**



The input signal x(n) consists of a desired wideband signal corrupted by narrow band signals that are not required, refer to Figure 3, page 4. In a linear prediction architecture, the desired signal d(n) is same as the input signal x(n) and delayed input x(n-Δ) is fed to the adaptive filter as shown in Figure 2, page 3. The delay factor Δ (delta) de-correlates the wideband component and correlates the narrow band component of the desired signal d(n) with the delayed input signal x(n-Δ).

The adaptive filter tries to estimate the narrow band component y(n), and forms an equivalent transfer function, which is similar to that of narrow band filters centered at the frequencies of the narrow band components of the input signal. At the summing junction, the filtered input signal subtracted with delayed input signal produces an error signal. The error signal is used by the LMS algorithm to adjust the filter coefficients. After some iterations, the error signal converges to a wide band component.

The following equations describe computing the coefficients using LMS algorithm.

$$y(n) = \sum_{k=0}^{k=l-1} h(n) \times x(n-\Delta-k)$$

EQ 1

where,

According to the above equation, narrowband component y(n), is the adaptive filter output

h(n) indicates the filter weights/coefficients

x(n-Δ) is the input signal to adaptive filter

l is length of the filter (number of taps)

k is the index variable.

The error is computed using the following equation:

$$e(n) = d(n) - y(n)$$

EQ 1

where,

e(n) is the error signal

d(n) is desired signal

The filter weights/coefficients are updated using the following equation:

$$h(n+1) = h(n) + \mu * e(n) * x(n-\Delta)$$

EQ 2

where,

h(n+1) indicates the estimated filter weights

h(n) is present filter weights

μ is the step size factor

Figure 3 • **Input Spectrum of Narrow Band Signal + Wide Band Signal**

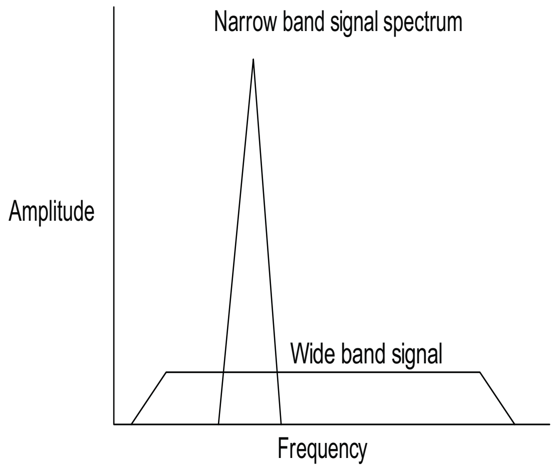
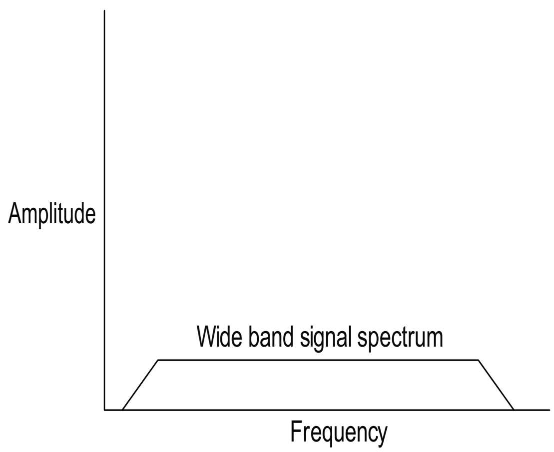


Figure 4 • **Output Spectrum of Wide Band Signal**



2.3 Design Requirements

Table 1 • **Design Requirements**

Design Requirements	Description
Hardware Requirements	
SmartFusion2 Starter Kit • FlashPro4 programmer • USB A to Mini-B cable	SF2-484-STARTER-KIT (M2S010-FGG484)
SmartFusion2 Security Evaluation Kit • FlashPro4 programmer • USB A to Mini-B cable	Rev D or later (M2S090TS-FGG484)
Host PC or Laptop	Windows 7, 64-bit Operating System
Software Requirements	
Libero® System-on-Chip (SoC)	v11.8 SP1
SoftConsole	v 4.0
FlashPro Programming Software	v11.8 SP1
Host PC Drivers	USB to UART drivers
Framework	Microsoft.NET Framework 4 Client for launching demo GUI

2.4 Demo Design

The design files are available for download from the following path in the Microsemi® website:

- SmartFusion2 Starter Kit:
  http://soc.microsemi.com/download/rsc/?f=m2s_dg0441_starter_liberov11p8_sp1_df
- SmartFusion2 Security Evaluation Kit:
  http://soc.microsemi.com/download/rsc/?f=m2s_dg0441_eval_liberov11p8_sp1_df

Design files include:

- Design files
- Programming files
- GUI executable
- Readme file

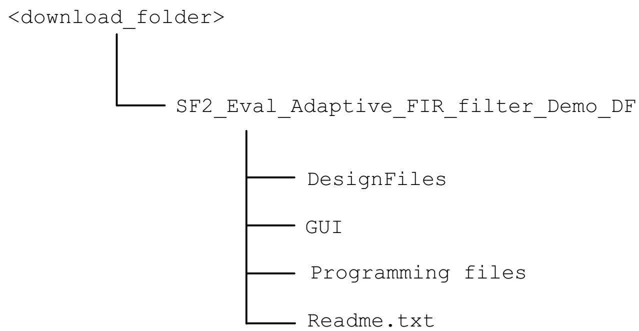
The following figure shows the top-level structure of the SmartFusion2 Starter kit design files. For further details, refer to the `readme.txt` file.

Figure 5 • **SmartFusion2 Starter Kit Demo Design Files Top-Level Structure**

```
<download_folder>
    |
    └── SF2_Starter_Adaptive_FIR_filter_Demo_DF
            |
            ├── DesignFiles
            ├── GUI
            ├── Programming files
            └── Readme.txt
```

The following figure shows the top-level structure of the SmartFusion2 Security Evaluation kit design files. For further details, refer to the `readme.txt` file.

Figure 6 • **SmartFusion2 Security Evaluation Kit Demo Design Files Top-Level Structure**

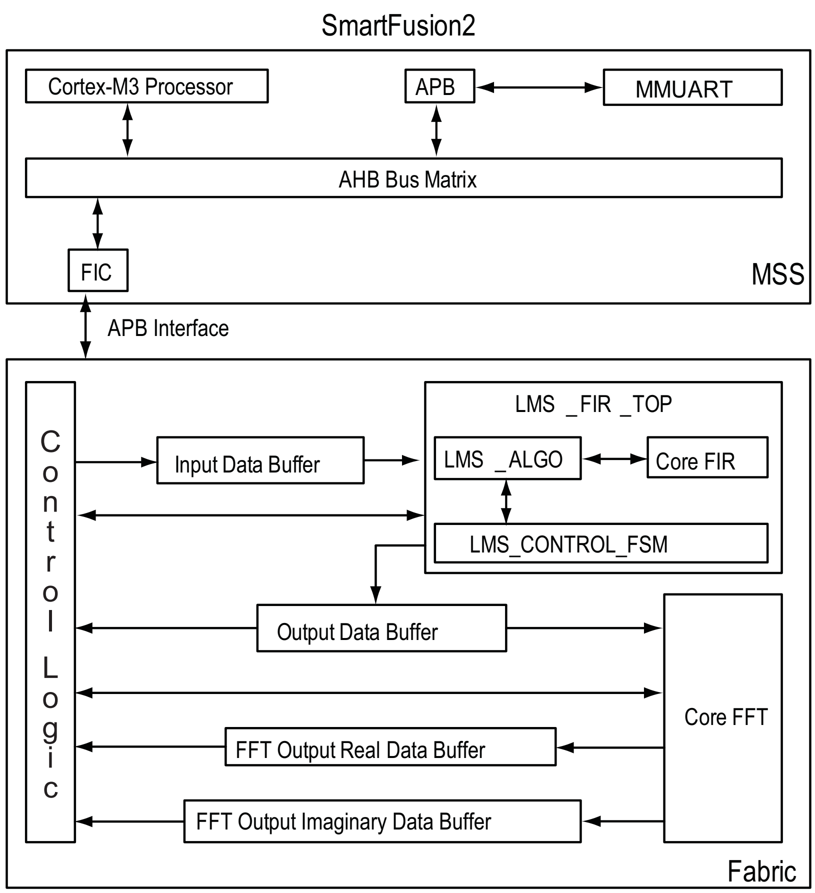


2.4.1 Demo Design Description

This demo design uses the following blocks:

- MSS block
- Control logic (user RTL)
- LMS_FIR_TOP (Smart Design)
- TPSRAM (IPcore)
- CoreFFT (IPcore)

Figure 7 • **Adaptive FIR Filter Demo Block Diagram**



2.4.1.1 MSS Block

The MSS block sends and receives the data between the Host PC (GUI interface) and FPGA fabric logic. The MMUART interface is used to communicate with the Host PC. FIC_0 interface (advanced peripheral bus (APB) master) is used to communicate with the fabric user logic.

2.4.1.2 Control Logic

This is the user logic that is implemented in the fabric and consists of the following two finite-state machines (FSM)s:

- **Data Handling**: Implements and controls operations like loading the filter input data to the corresponding input data buffer, reading of processed data, and FFT data values. An APB bus slave is implemented to communicate with the MSS APB master.
- **Filter Control**: Controls the FIR filter and FFT operations. Loads the filtered data to the corresponding output buffer and moves the FFT output data to the corresponding output data buffer.

2.4.1.3 LMS_FIR_TOP

This is a SmartDesign block implemented in the fabric. It consists of the following blocks:

- **LMS_CONTROL_FSM**: This FSM is implemented in the register-transfer level (RTL) to provide the control signals to the LMS_ALGO block.
- **LMS_ALGO**: This LMS algorithm is implemented in the RTL to compute the error signal, correction factor, filter coefficients, and to send the filter coefficients to the Core FIR filter.
- **CoreFIR**: CoreFIR IP is used in the re-loadable coefficient mode to configure its coefficients on the fly. CoreFIR IP configuration is as follows:
  - Filter Type: Single rate fully enumerated
  - No of taps: 16
  - Coefficients type: Reloadable
  - Coefficients bit width: 16 (signed)
  - Data bit width: 16 (signed)
  - Filter structure: Transposed with no symmetry

2.4.1.4 TPSRAM IP

TPSRAM IP uses the following configurations:

- Input signal data buffer (depth: 1024, width: 16)
- Output signal buffer (depth: 1024, width: 16)
- Output signal FFT real data buffer (depth: 1024, width: 16)
- Output signal FFT imaginary data buffer (depth: 1024, width: 16)

2.4.1.5 CoreFFT

CoreFFT IP is used to generate the frequency spectrum of the filtered data. CoreFFT IP configuration is as follows:

- FFT Architecture: In place
- FFT type: Forward
- FFT Scaling: Conditional
- FFT Transform Size: 256
- Width: 16

For detailed SmartDesign implementation and resource usage summary, refer to Appendix: SmartDesign Implementation, page 25.

2.5 Setting Up the Demo Design for SmartFusion2 Starter Kit

The following steps describe how to setup the hardware demo for SmartFusion2 Starter kit:

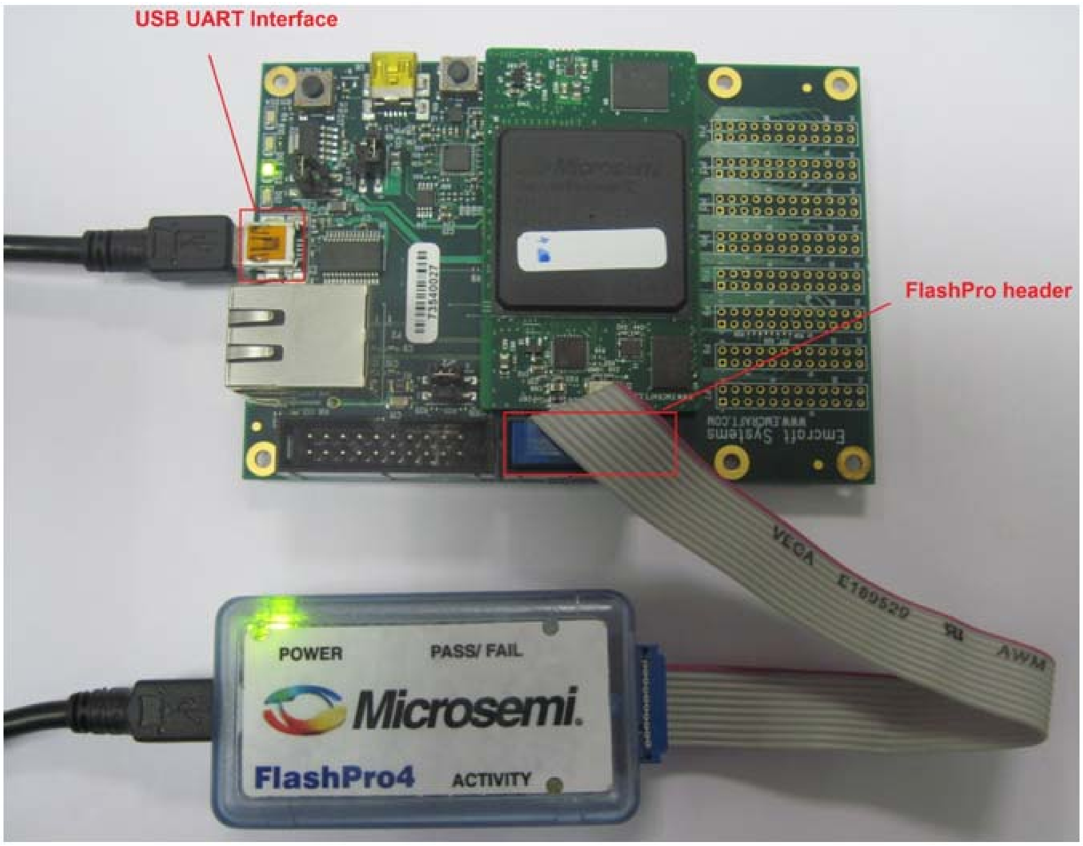
1. Connect the jumpers on the SmartFusion2 Starter kit board as shown in the following table.

Table 2 • **SmartFusion2 Starter Kit Jumper Settings**

Jumper	Configuration	Comments
JP1	1-2 Close, 3-4 Open	Enable power on the M2S-FG484 SOM (VCC3).
JP2	1-2 Open, 3-4 Close	Select appropriate JTAG mode and enable power to the SmartFusion2 JTAG controller.
JP3	1-3 Open, 2-4 Close	Use the mini-USB port as the power source.

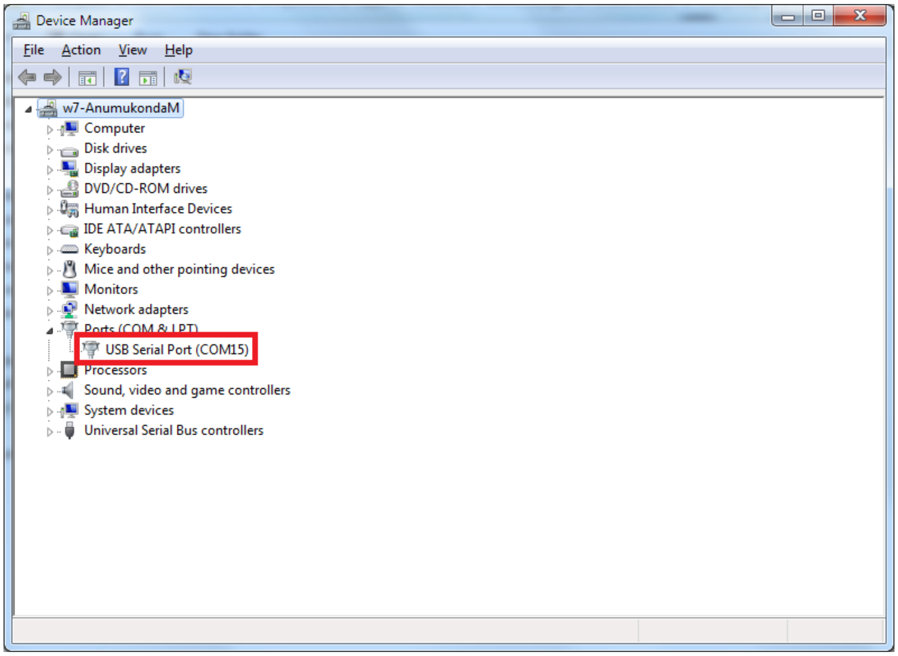
2. Connect the FlashPro4 programmer to the P5 connector of the SmartFusion2 Starter kit board.
3. Connect the Host PC USB port to the P1 Mini USB connector on the SmartFusion2 Starter kit board using the USB Mini-B cable.
   The following figure shows the board setup for running the Adaptive FIR filter demo on the SmartFusion2 Starter kit.

Figure 8 • **SmartFusion2 SoC FPGA Starter Kit Setup**



4. Ensure that the USB to universal asynchronous receiver-transmitter (UART) bridge drivers are automatically detected. This can be verified in the **Device Manager** of the Host PC.
   The following figure shows the USB Serial port.

Figure 9 • USB to UART Bridge Drivers for SmartFusion2 Starter Kit



5. If USB to UART bridge drivers are not installed, download and install the drivers from www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip

2.5.1 Setting Up the Demo Design for SmartFusion2 Security Evaluation Kit

The following steps describe how to setup the hardware demo for Security Evaluation kit:

1. Connect the jumpers on the SmartFusion2 Security Evaluation kit board as shown in the following table.

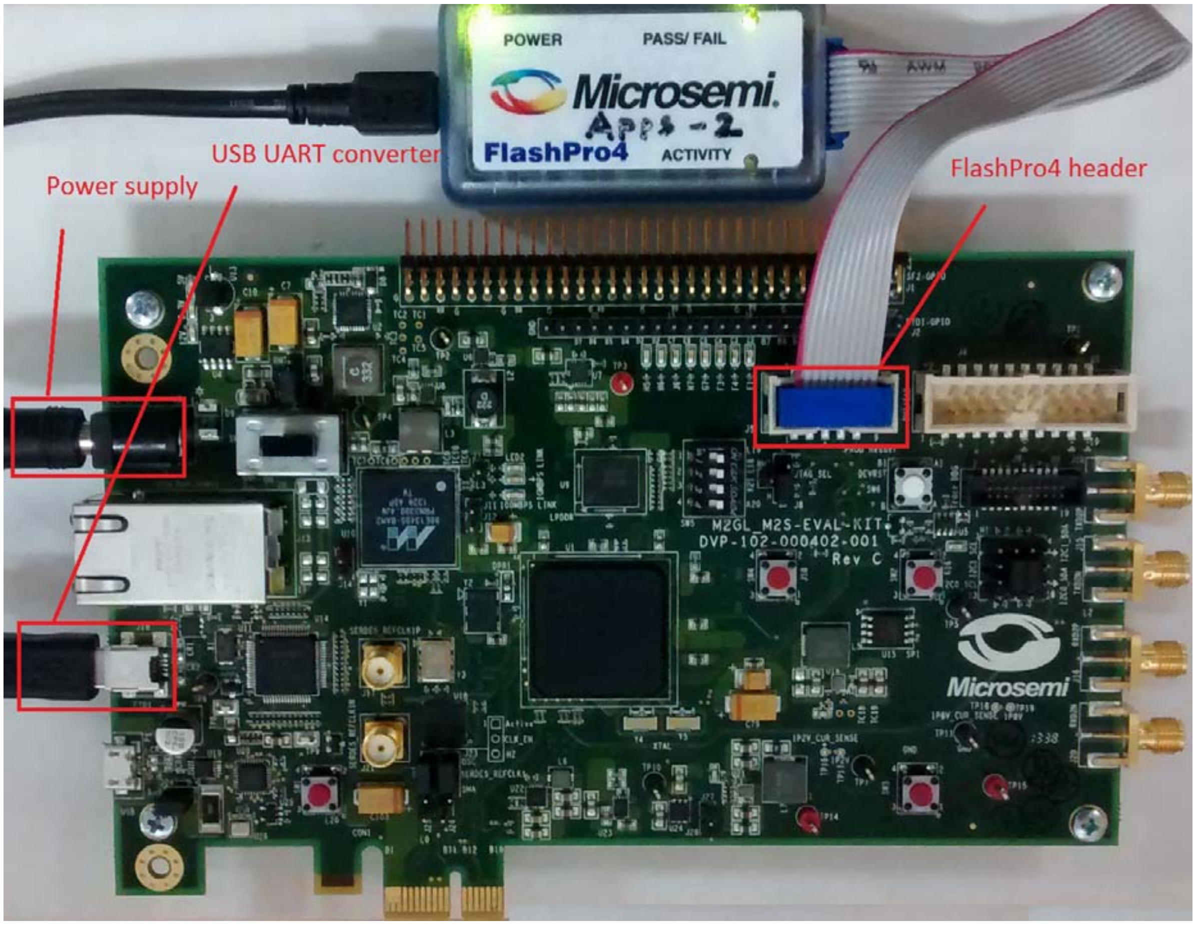
Table 3 • **SmartFusion2 Security Evaluation Kit Jumper Settings**

Jumper	Configuration	Comments
J23	–	Jumper to select switch-side multiplexer (MUX) inputs of A or B to the lineside.
	Close	Pin 1-2 (Input A to the lineside) that is on board 125 MHz differential clock oscillator output will be routed to lineside.
	Open	Pin 2-3 (Input B to the lineside) that is external clock required to source through SMA connectors to the lineside.
J22	–	Jumper to select the output enables control for the lineside outputs.
	Close	Pin 1-2 (Lineside output enabled)
	Open	Pin 2-3 (Lineside output disabled)
J24	Open	Jumper to provide the VBUS supply to USB when using in Host mode.
J8	–	JTAG selection jumper to select between RVI header or FP4 header for application debug.
	Close	Pin 1-2 FP4 for SoftConsole/FlashPro
	Open	Pin 2-3 RVI for Keil™ ULINK™/IAR J-Link®
	Open	Pin 2-4 for Toggling JTAG_SEL signal remotely using GPIO capability of FT4232 chip.
J3	–	Jumpers to select either SW2 input or signal ENABLE_FT4232 from FT4232H chip.

1. Ensure that the power supply switch SW7 is OFF while making the jumper connections.
2. Connect the Power supply to the J6 connector, switch on the power supply switch, SW7.

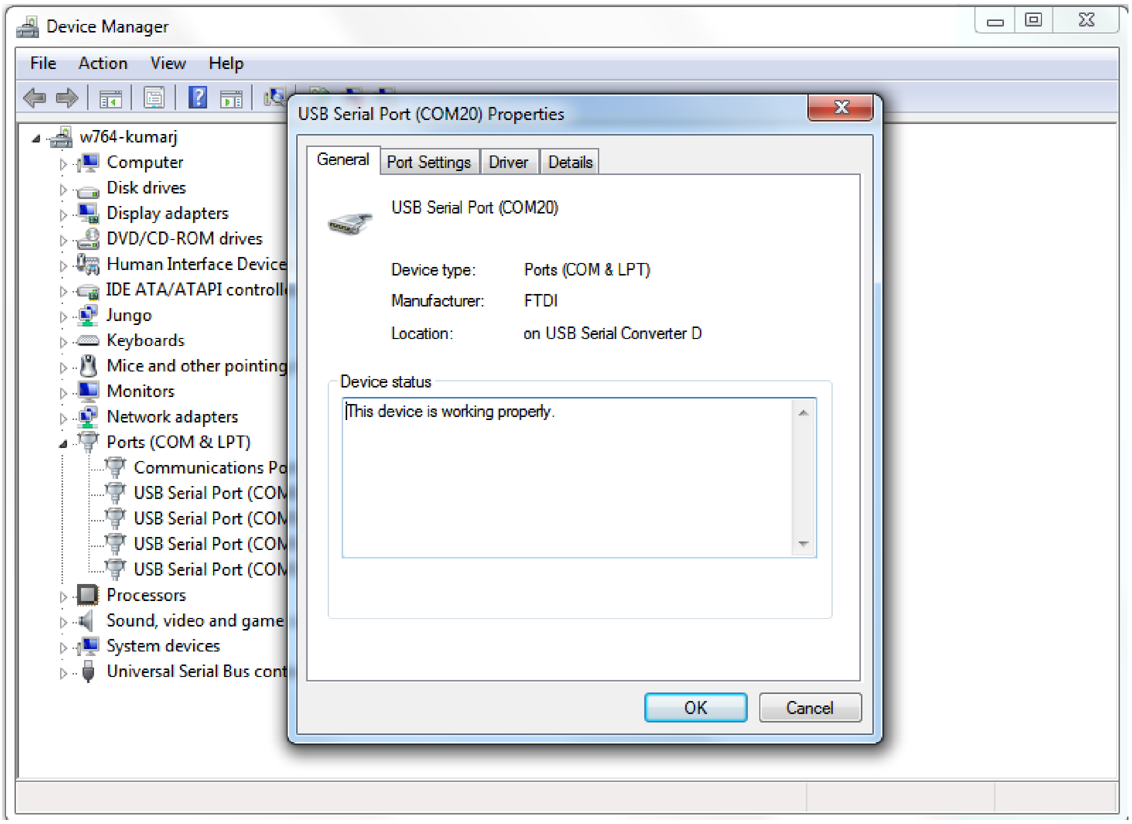
2. Connect the FlashPro4 programmer to the J5 connector of the SmartFusion2 Security Evaluation kit board.
3. Connect the Host PC USB port to the P1 Mini USB connector on the SmartFusion2 Security Evaluation kit board using the USB Mini-B cable.
   The following figure shows the board setup for running the DSP Adaptive FIR filter demo on the SmartFusion2 Security Evaluation kit.

Figure 10 • **SmartFusion2 Security Evaluation Kit Setup**



4. Switch **ON** the SW7 power supply switch.
5. Ensure that the USB to UART bridge drivers are automatically detected. This can be verified in the **Device Manager** of the Host PC. The following figure shows the USB Serial port.

Figure 11 • **USB to UART Bridge Drivers for SmartFusion2 Security Evaluation Kit**



6. If USB to UART bridge drivers are not installed, download and install the drivers from www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip.

2.6 Programming the Demo Design

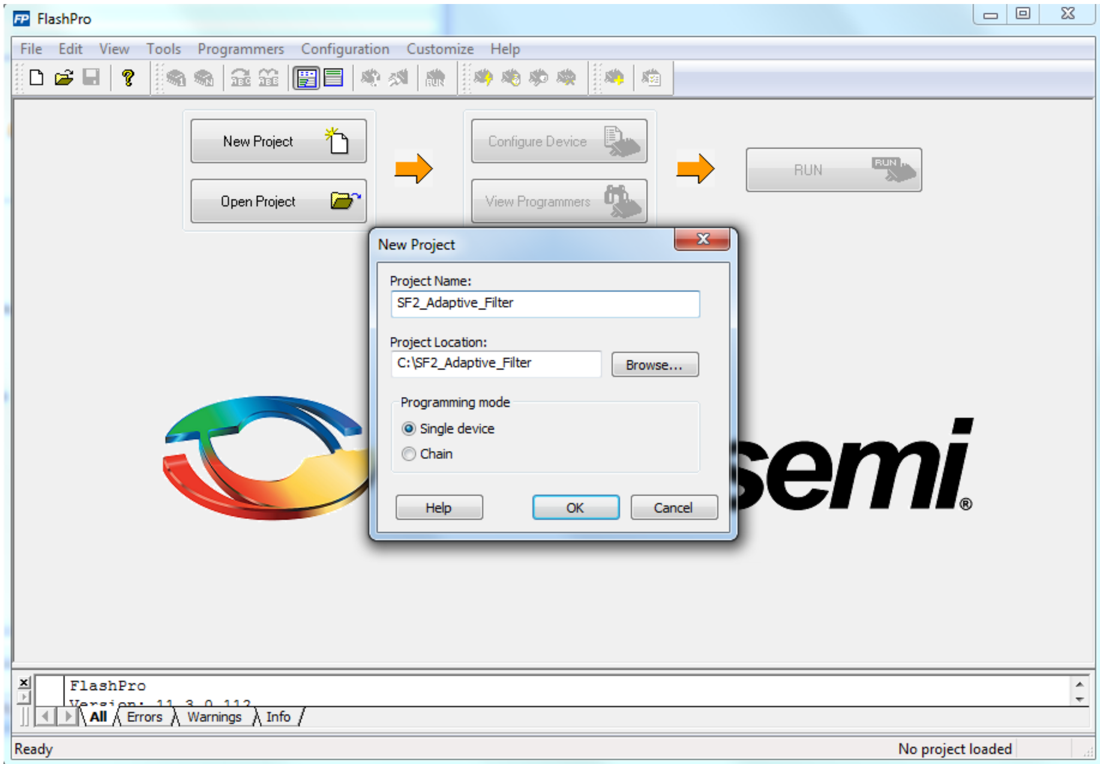
The following steps describe how to program the demo design:

Download the demo design from the following links:

- SmartFusion2 Starter Kit: *http://soc.microsemi.com/download/rsc/?f=m2s_dg0441_starter_liberov11p8_sp1_df*
- SmartFusion2 Security Evaluation Kit: *http://soc.microsemi.com/download/rsc/?f=m2s_dg0441_eval_liberov11p8_sp1_df*

1. Launch the FlashPro software.
2. Click **New Project**.
3. In the **New Project** window, enter the project name as SF2_Adaptive_Filter.

Figure 12 • **FlashPro - New Project**



4. Click **Browse** and navigate to the location where you want to save the project.
5. Select **Single device** as the **Programming mode**.
6. Click **OK** to save the project.

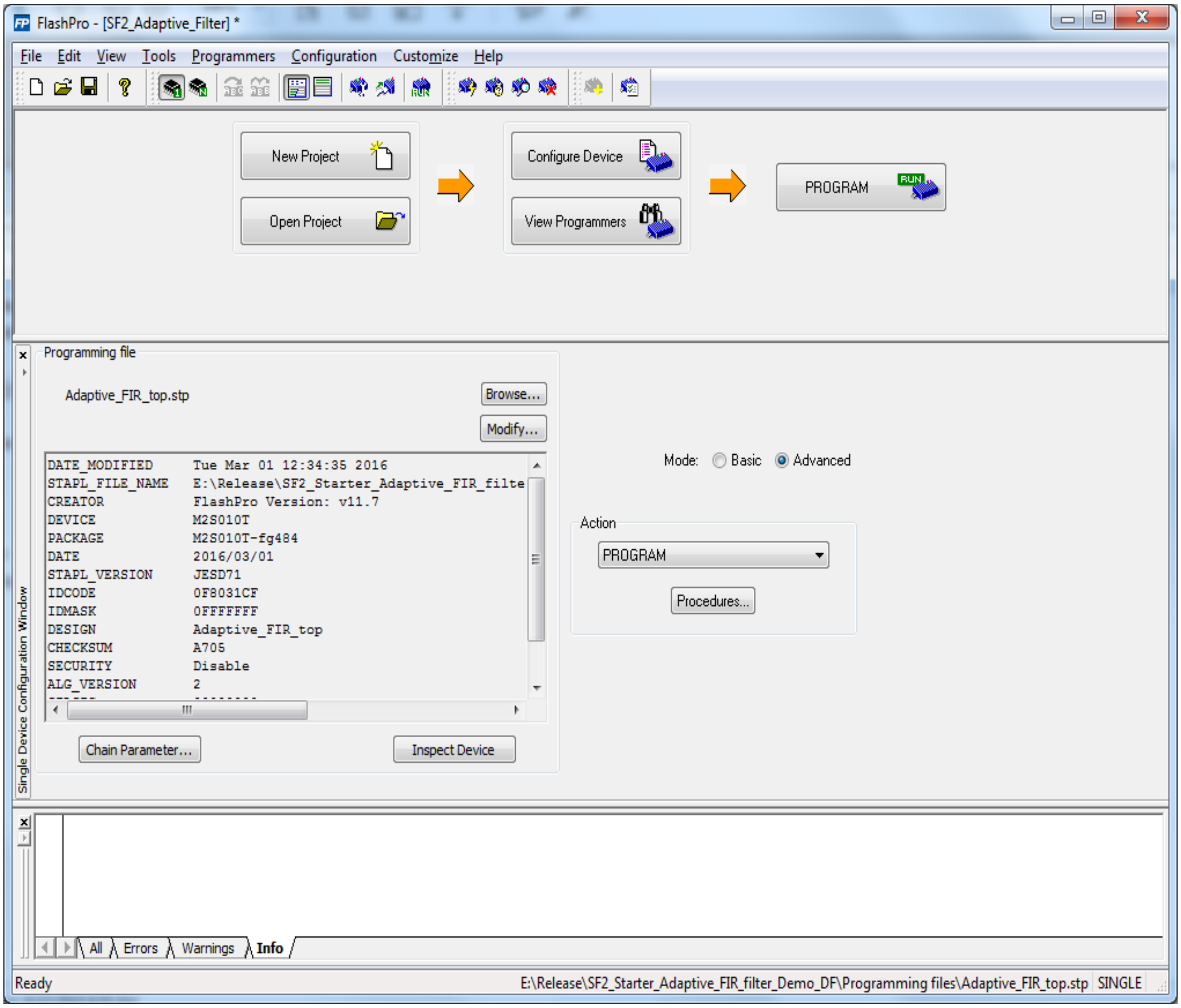
2.6.1 Setting Up the Device

The following steps describe how to configure the device:

1. Click **Configure Device** on the FlashPro GUI.
2. Click **Browse** and navigate to the location where the `Adaptive_FIR_top.stp` file is located and select the file. The default location of the programming file is:
   - SmartFusion2 Starter Kit:
     <download_folder>\SF2_Starter_Adaptive_FIR_filter_Demo_DF\Programming files\Adaptive_FIR_top.stp
   - SmartFusion2 Security Evaluation Kit:
     <download_folder>\SF2_Eval_Adaptive_FIR_filter_Demo_DF\Programming files\Adaptive_FIR_top.stp
3. Click **Open**. The required programming file is selected and is ready to be programmed in the device.
4. Select **Advanced** as Mode and **PROGRAM** as Action.

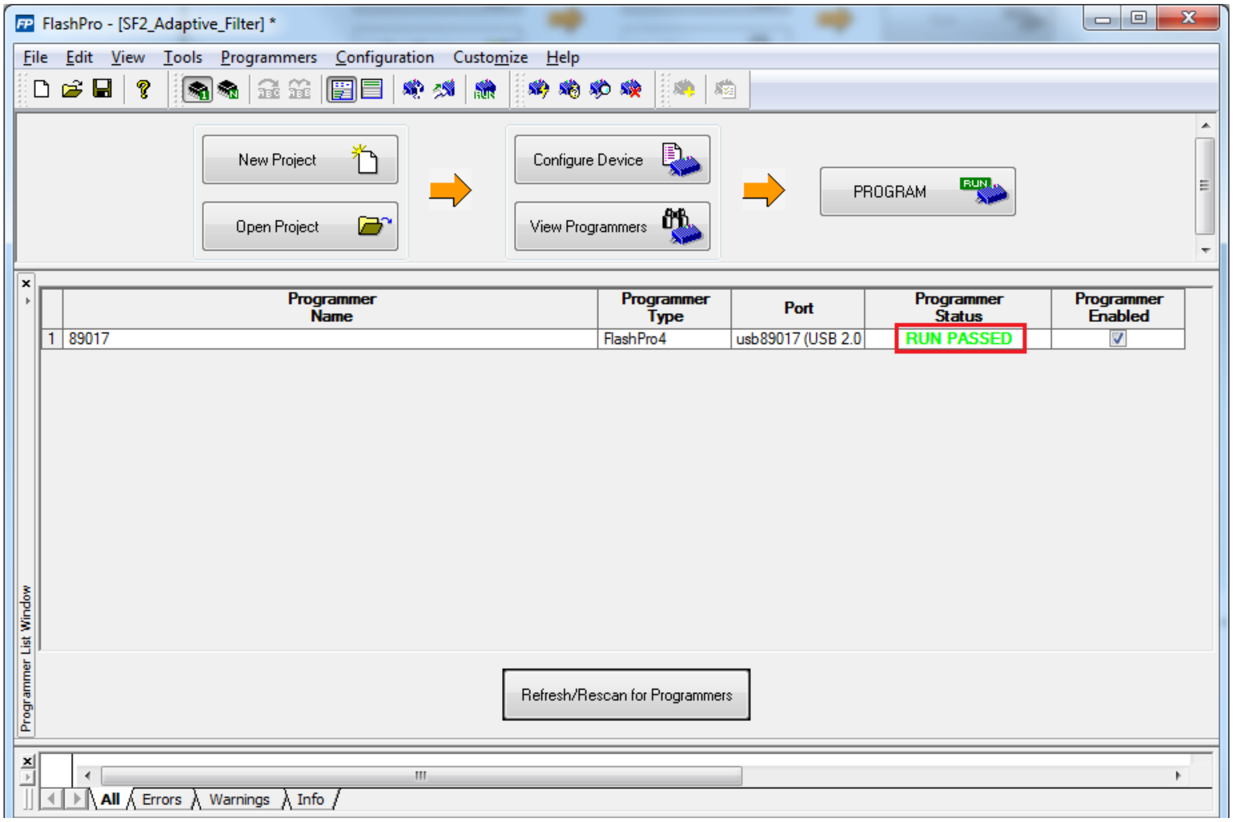
2.6.2 Programming the Device

Figure 13 • **FlashPro Project Configuration**



Click **PROGRAM** to start programming the device. Wait until programmer status is changed to **RUN PASSED** as shown in the following figure.

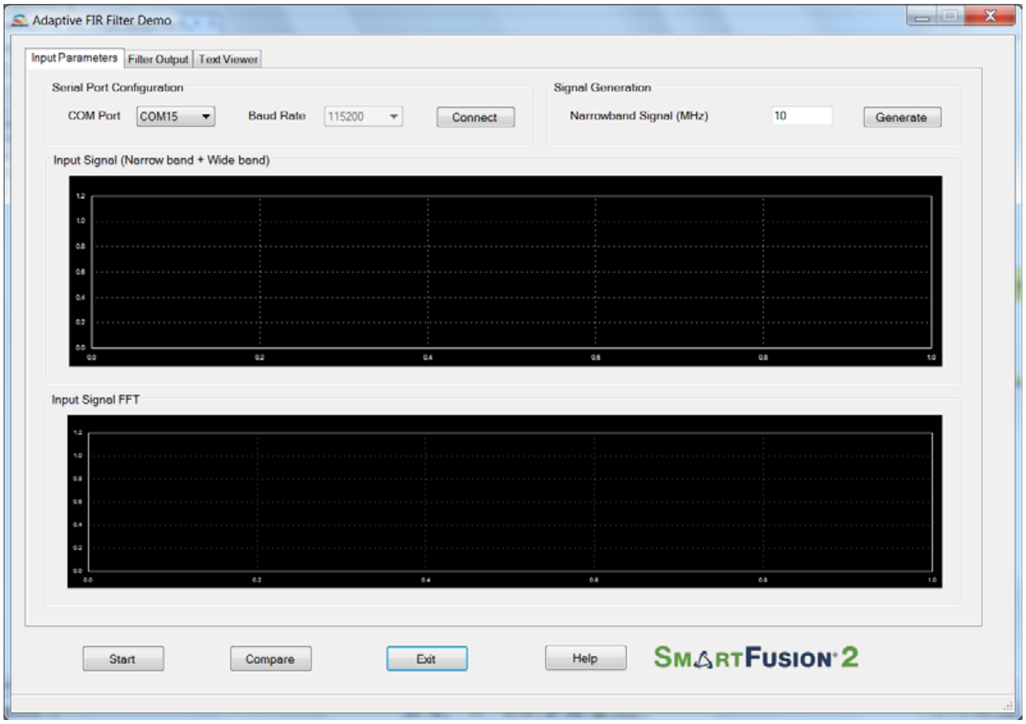
Figure 14 • **FlashPro Project RUN Passed**



2.6.3 Adaptive FIR Filter Demo GUI

The Adaptive FIR filter demo is provided with a user-friendly GUI that runs on the Host PC and communicates with the SmartFusion2 Starter kit. The UART is used as the underlying communication protocol between the Host PC and SmartFusion2 Starter kit or SmartFusion2 Security Evaluation kit. The following figure shows the Adaptive FIR filter demo GUI.

Figure 15 • **Adaptive FIR Filter Demo GUI**



The Adaptive FIR filter demo window consists of the following tabs:

- **Input Parameters**: Configures the serial COM port, filter generation, and signal generation.
- **Filter Output**: Plots error signal and its frequency spectrum
- **Text Viewer**: Shows the coefficients, input signal, output signal, and FFT data values

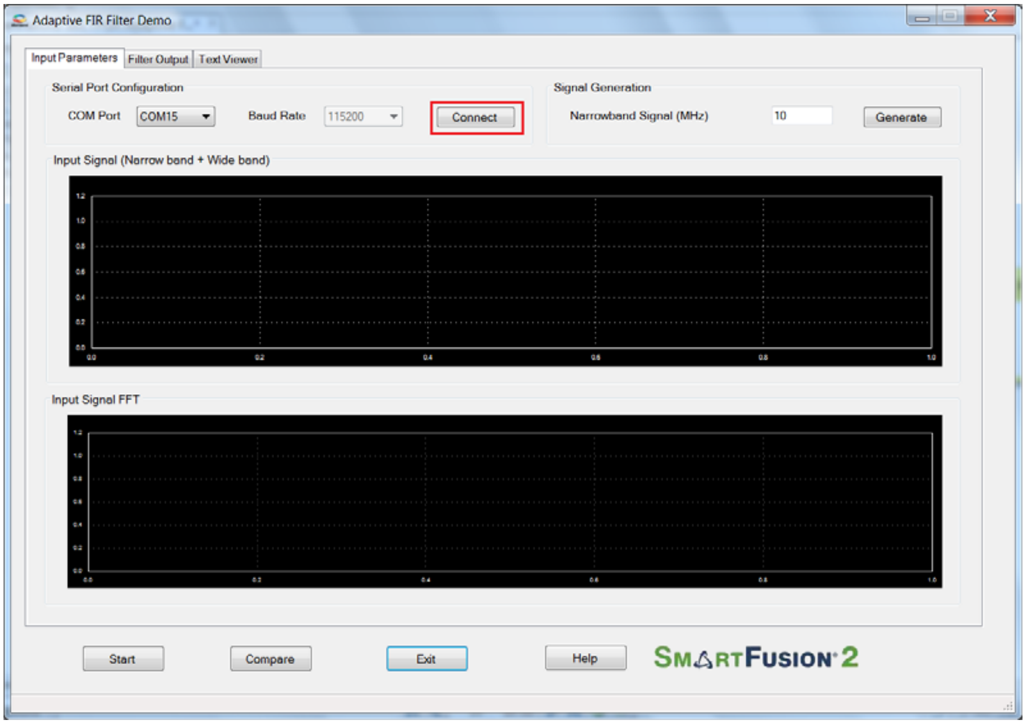
Click **Help** for more information on the GUI.

2.7 Running the Design

1. Launch the Adaptive FIR filter demo GUI, install and invoke the executable file provided with the design files. The default location of the executable files are:
   - SmartFusion2 Starter Kit:
     <download_folder>\SF2_Starter_Adaptive_FIR_filter_Demo_DF\GUI\SF2_Adaptive_FIR_Filter.exe
   - SmartFusion2 Security Evaluation Kit:
     <download_folder>\SF2_Eval_Adaptive_FIR_filter_Demo_DF\GUI\SF2_Adaptive_FIR_Filter.exe

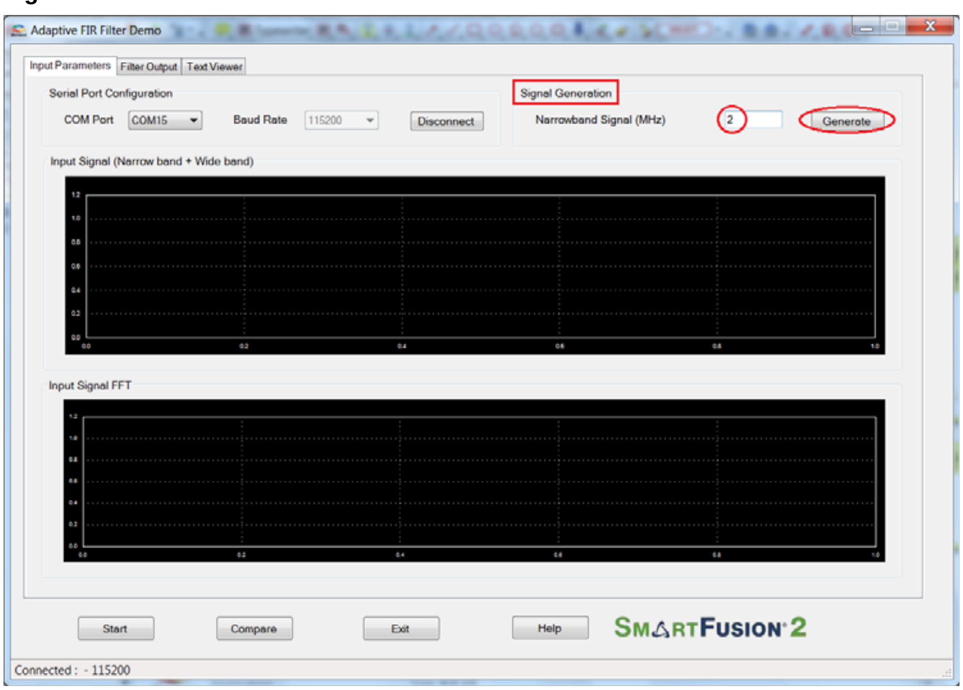
The Adaptive FIR filter Demo window is displayed, refer to the following figure.

Figure 16 • **Serial Port Configuration**



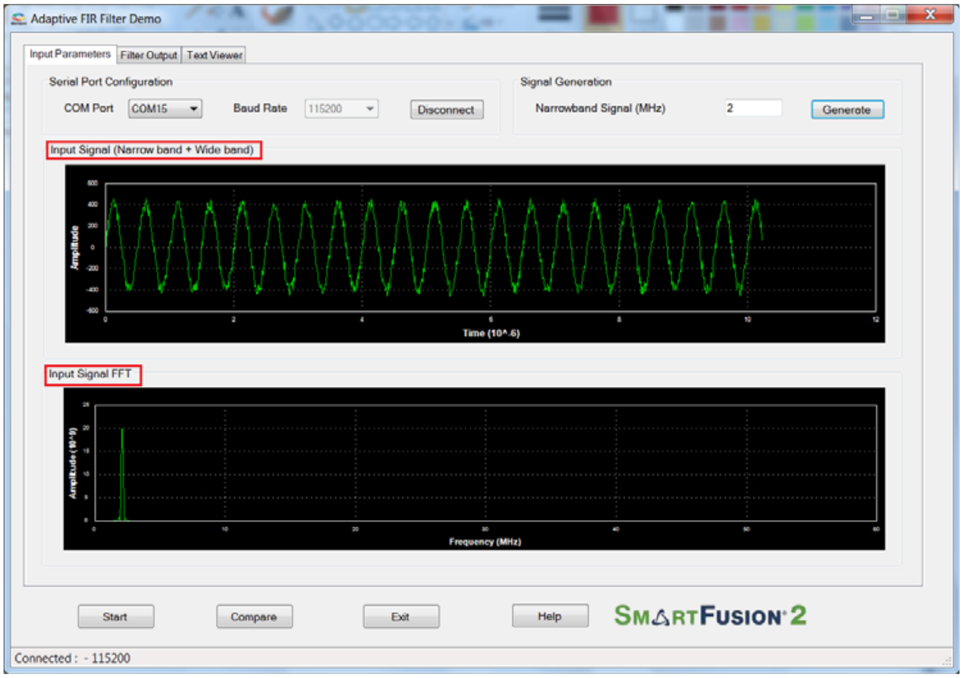
2. **Serial Port Configuration**: The COM port number is automatically detected and baud rate is fixed at 115200. Click **Connect**. Refer to the preceding figure.
3. **Signal Generation**: Enter the narrowband signal frequency as 2 MHz (supported range is 1 MHz to 20 MHz) and click **Generate**. Refer to the following figure.

Figure 17 • **Signal Generation**



Adaptive FIR Filter Demo adds the wide band signal (generated inside the Adaptive FIR filter demo window) to the narrow band signal component and plots the combined signal (Narrowband and Wideband), FFT spectrum. Refer to the following figure.

Figure 18 • **Signal Generation**

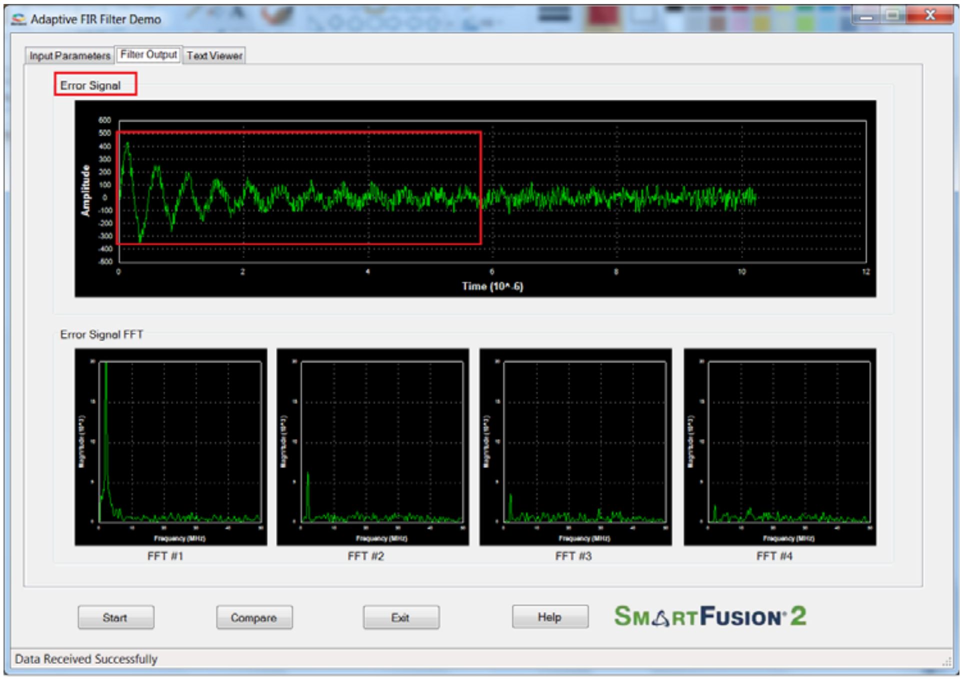


4. Click **Start** to load the input data (1K samples) to the SmartFusion2 device for processing the filtering operation, refer to the following figure.

Figure 19 • **Adaptive FIR Filter Demo - Start**

After completing the filter operation, the GUI receives the error data and its FFT data from the Smart-Fusion2 device and plots as shown in the following figure. The error signal plot shows the suppression of narrowband component from the wideband signal only after the required number of iterations.

Figure 20 • **Error Signal: Time and Frequency Plot**



The narrowband signal component is suppressed gradually in the Error signal frequency spectrum. This can be observed in the Error signal FFT plot as shown in the following figure.

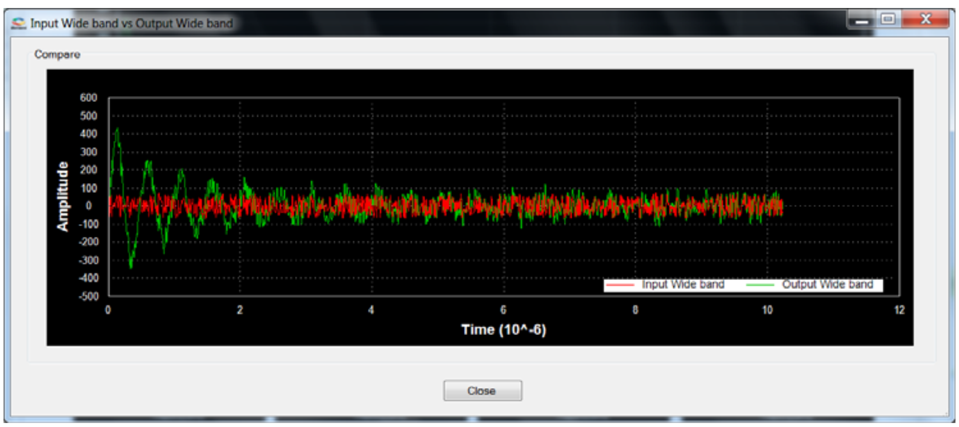
Figure 21 • **Error Signal: Time and Frequency Plot**

5. Click **Compare** to analyze the input wide band data with the output wide band data.

Figure 22 • Compare Error Signal: Time and Frequency Plot

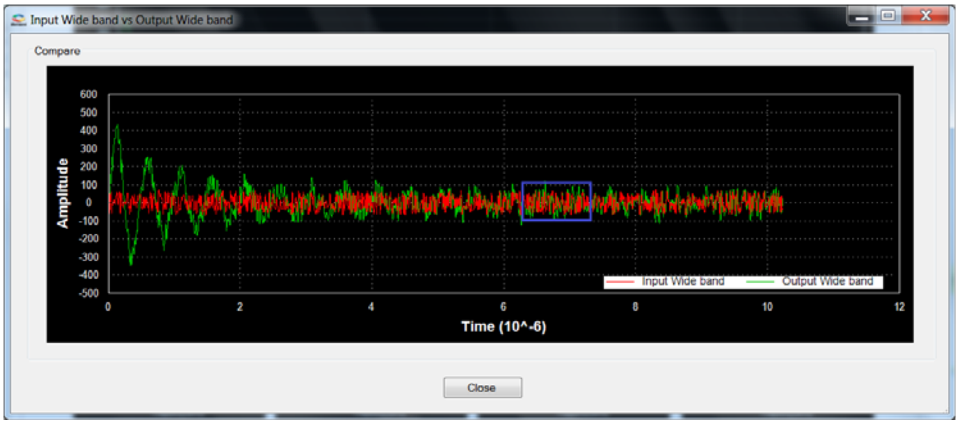
A window displaying the comparison between the input wide band and output wide band is displayed, refer to the following figure.

Figure 23 • Comparison of Input Wide Band and Output Wide Band



The plot can be zoomed in for comparison, refer to the following figure.

Figure 24 • **Input Wide Band vs Output Wide Band**



6. Compare the Error signal (Output wide band signal) with the input wide band signal, refer to the following figure. The narrow band interfering component is eliminated and the wide band signal is preserved in error signal.

Figure 25 • **Comparison of Input Wide Band and Output Wide Band**

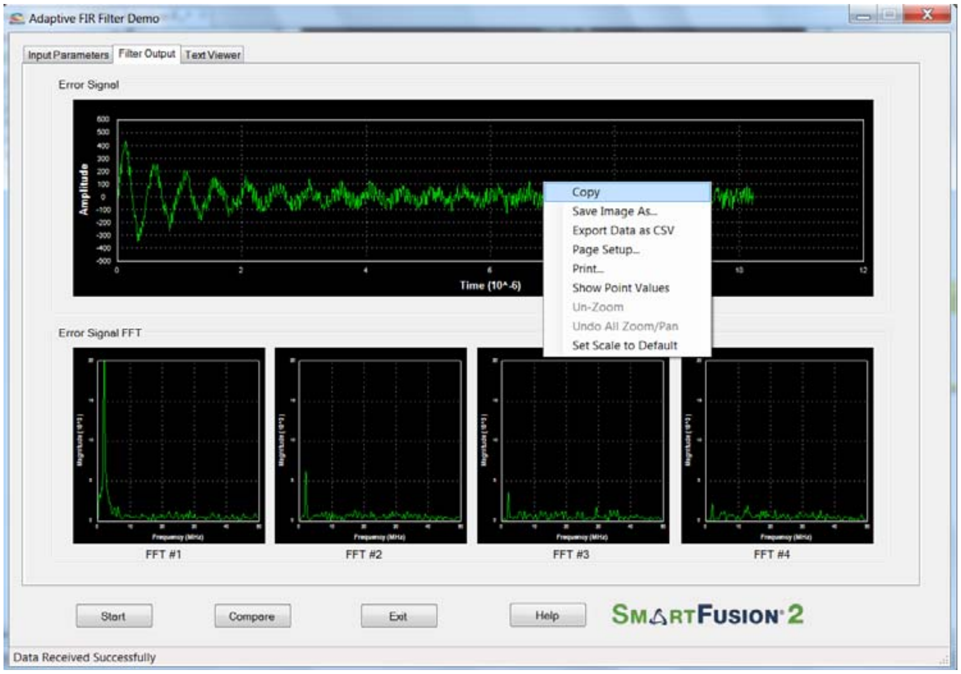
7. Click **Close**, refer to the following figure.

Figure 26 • **Closing Input Wide Band vs Output Wide Band**

8. You can copy, save, export, and customize page and configure print setup for the Error Signal plot. Right-click the **Error Signal** plot.
9. From the context sensitive pop-up, select the required option.
   It shows the different options as shown in the following figure.
   The data can be copied, saved, and exported to CSV plot for analysis purpose.

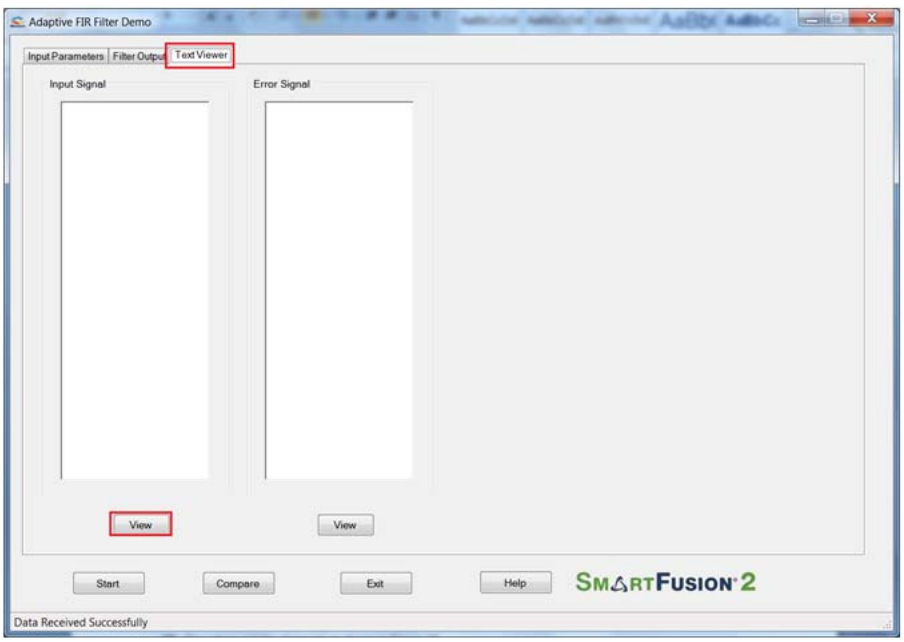
Page setup, print, show point values, Zoom, and set scale to default are other options for signal analysis.

Figure 27 • **Error Signal - GUI Options**



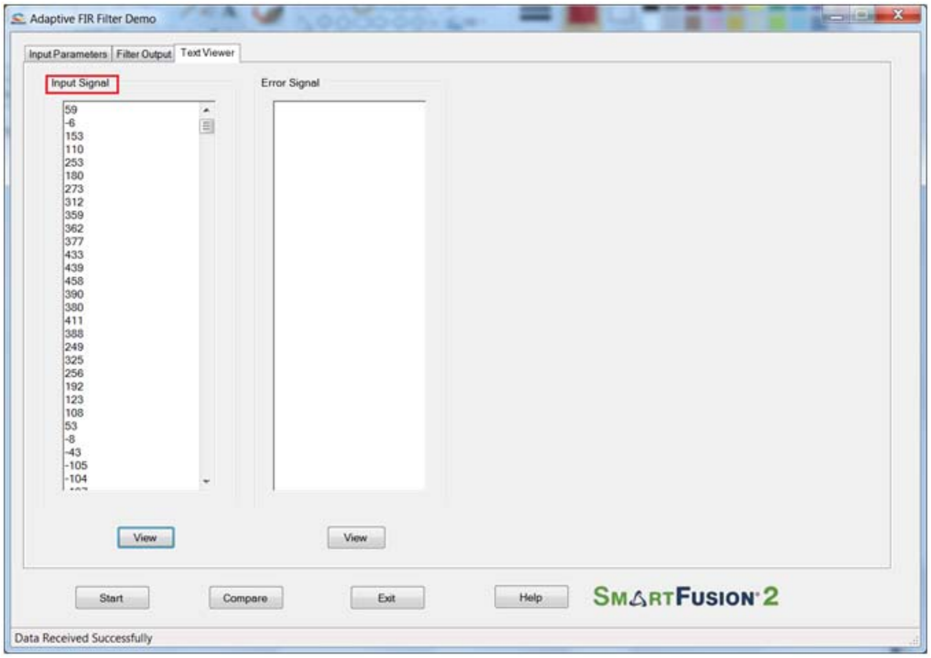
10. The input signal and error signal values can be viewed in the **Text Viewer** tab. Click the **Text Viewer** tab and then click the corresponding **View** shown in the following figure.

Figure 28 • **Text Viewer**



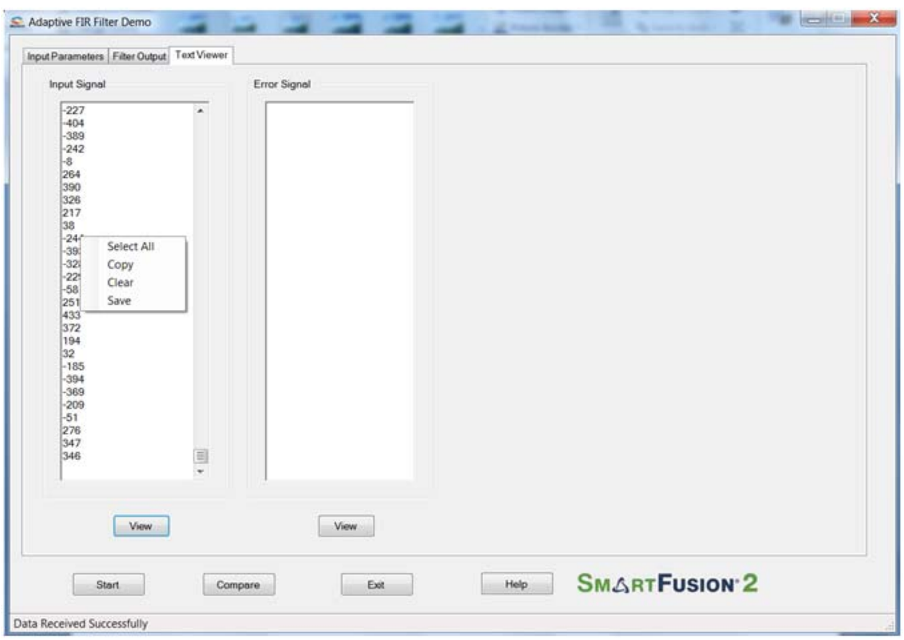
The following figure shows the **Text Viewer** tab showing the **Input Signal** values.

Figure 29 • **Text Viewer: Input Signal Values**



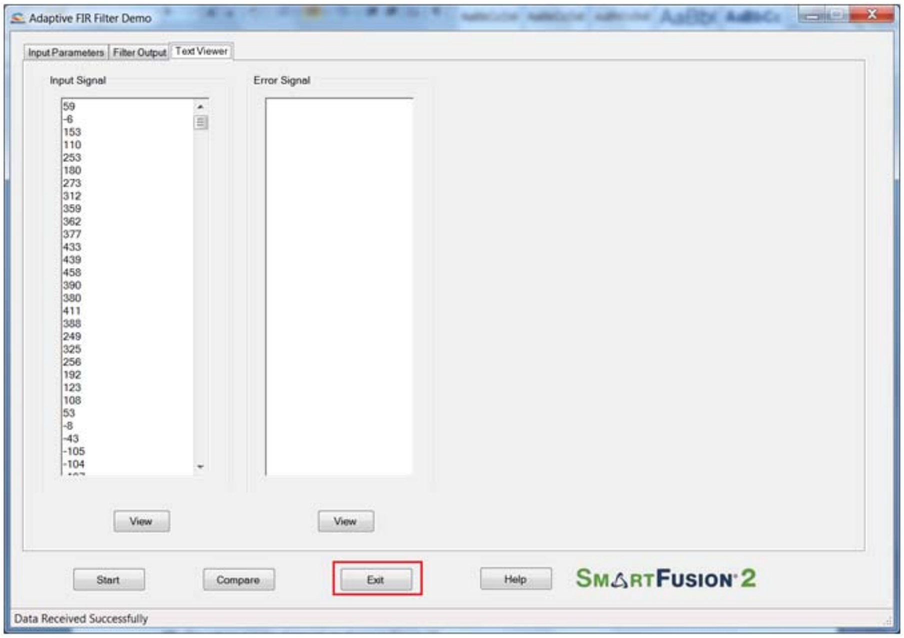
11. To save the Input Signal as a text file, right-click the **Input Signal** window. The Input Signal window displays different options as shown in the following figure.
12. Click **Save**. Select **OK** to save the text file.

Figure 30 • **Text Viewer - Coefficients Save Options**



13. Click **Exit** to stop the demo, see the following figure.

Figure 31 • **Exit Demo**



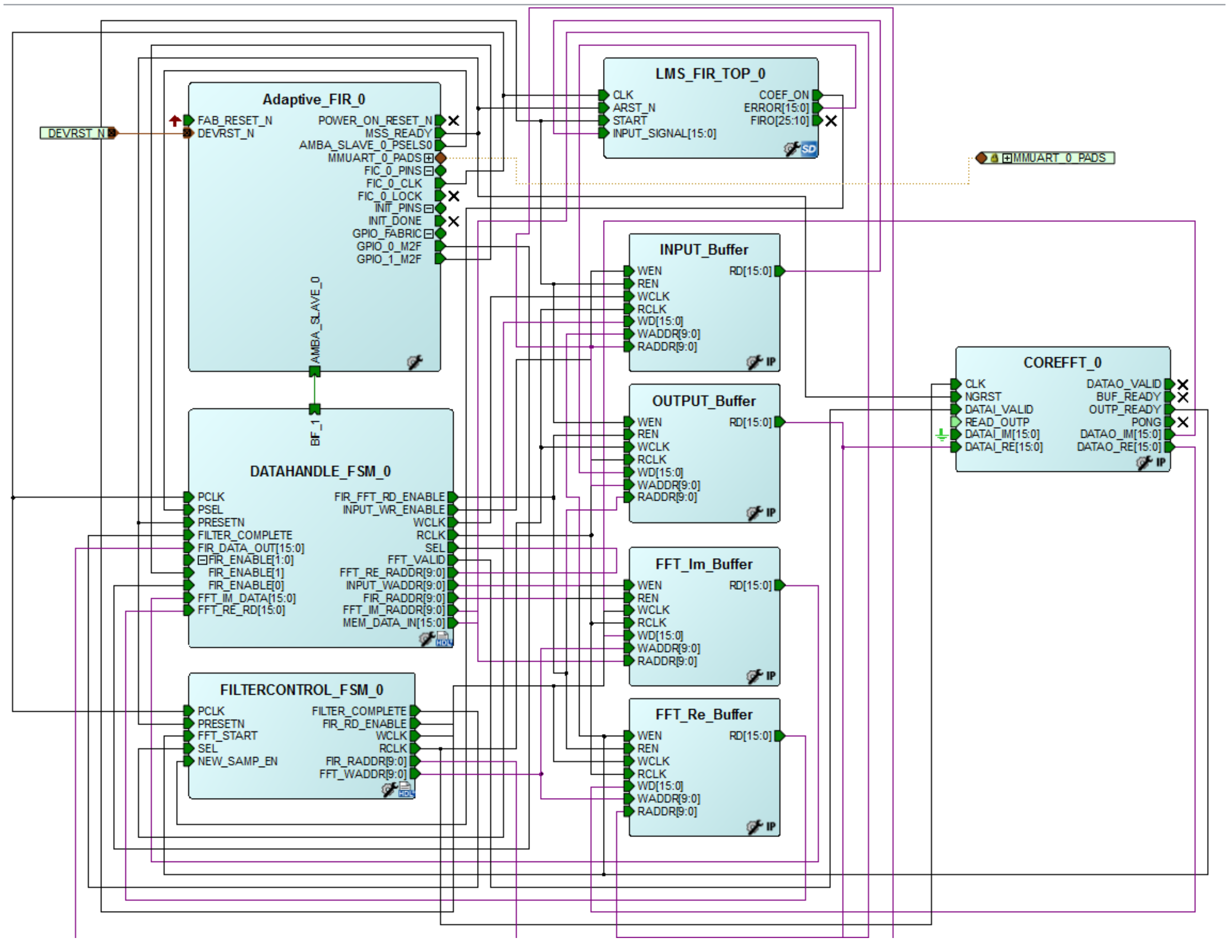
2.8 Conclusion

This demo provides information about the features of the SmartFusion2 device including mathblocks and how to use Microsemi IPs (CoreFIR and CoreFFT) or narrow band interference cancellation application using adaptive filters. This Adaptive FIR filter based-demo is easy to use and provides several options to understand and implement digital signal processing (DSP) filters on the SmartFusion2 device.

3 Appendix: SmartDesign Implementation

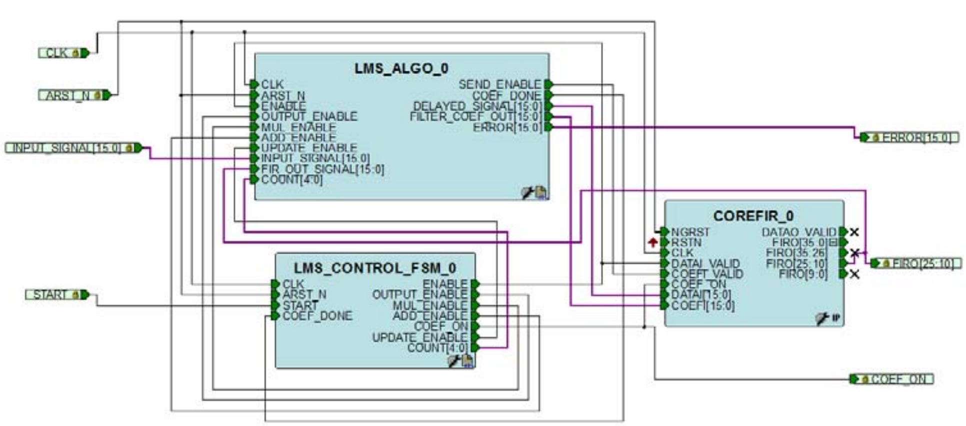
Adaptive FIR filter SmartDesign is shown in the following figure.

Figure 32 • **Adaptive FIR Filter SmartDesign**



SmartDesign LMS_FIR_TOP is shown in the following figure.

Figure 33 • **LMS_FIR_TOP Smart Design**



The following table shows SmartDesign blocks in Adaptive FIR filter.

Table 4 • Adaptive FIR Filter Demo Smart Design Blocks and Description

S.No	Block Name	Description
1	Adaptive_FIR	FIR_FILTER_0 is a System Builder generated component, in which MMUART is configured to handle the communication between the host PC and fabric logic. To generate a System Builder component, refer to the *SmartFusion2 System Builder User Guide*.
2	DATAHANDLE_FSM	Control logic to send/receive the data between MSS and data buffers
3	FILTERCONTROL_FSM	Control logic to generate the control signals for FIR and FFT operations
4	LMS_FIR_TOP	SmartDesign
5	INPUT_Buffer	FIR input signal data buffer
	OUTPUT_Buffer	FIR output signal buffer
	FFT_Im_Buffer	FFT output imaginary data buffer
	FFT_Re_Buffer	FFT output real data buffer
6	COREFFT	COREFFT IP

The following table shows SmartDesign blocks in LMS_FIR_TOP.

Table 5 • LMS_FIR_TOP Smart Design Blocks and Description

S.No	Block Name	Description
1	LMS_ALGO	LMS algorithm implemented in RTL to compute error, correction factor, and filter coefficients.
2	LMS_CONTROL_FSM	FSM implemented in RTL to control LMS_ALGO block
3	COREFIR	COREFIR IP

4 Appendix: Resource Usage Summary

The following table shows Adaptive FIR filter demo resource usage summary.

Device: SmartFusion2 device

Die: M2S010

Package: 484 FBGA

Table 6 • **Adaptive FIR Filter Demo Resource Usage Summary**

Type	Used	Total	Percentage
4LUT	2834	12084	23.45
DFF	2827	12084	23.39
RAM64x18	0	22	0
RAM1Kx18	11	21	52.38
MACC	13	22	59.09

The following table shows Adaptive FIR filter resource usage summary.

Device: SmartFusion2 device

Die: M2S090TS

Package: 484 FBGA

Table 7 • **Adaptive FIR Filter Demo Resource Usage Summary**

Type	Used	Total	Percentage
4LUT	2833	86184	3.29
DFF	2827	86184	3.28
RAM64x18	0	112	0.00
RAM1K18	11	109	10.09
MACC	13	84	15.48

The following table shows MACC blocks usage summary.

Table 8 • **MACC Blocks Usage Summary**

CoreFIR	CoreFFT	LMS_ALGO	Total
8	04	1	13