BME 393L Lab 2: Intro to FPGAs

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January 29th, 2022

Pre-Lab

Question 1

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library ieee;
use ieee.std_logic_1164.all;
entity Lab2Prelab is
port( SW: in std_logic_vector(3 downto 0);
      LEDG: out std_logic_vector(3 downto 0)
      );
end entity Lab2Prelab;
architecture main of Lab2Prelab is
signal a1, a0, b1, b0: std_logic;
begin
a1 <= SW(1);
a0 <= SW(0);
b1 <= SW(3);
b0 <= SW(2);
LEDG(3) <= (a0 AND b0) AND (a1 AND b1);
LEDG(2) <= (a0 NAND b0) AND (a1 AND b1);
LEDG(1) <= ((a0 AND b1) AND (b0 NAND a1)) OR
           ((a0 NAND b1) AND (b0 AND a1));
LEDG(0) <= a0 AND b0;
end architecture main;
```

a) Four inputs (SW 0-3) and four outputs (LEDG 0-3) were defined in VHDL.
b) If each input and output are considered as individual components, then they represent 1 bit each. However, given the behaviour of the circuit, they can also be considered as two 2-bit inputs and one 4-bit output.

Table 1: Truth Table for the circuit in Figure 3.1.

a1	a0	b1	b0	p3	p2	p1	p0
0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	0	0	1	0	0
1	0	0	1	0	0	1	0
1	0	1	1	0	1	1	0
0	1	0	0	0	0	0	0
0	1	1	0	0	0	1	0

0	1	0	1	0	0	0	1
0	1	1	1	0	0	1	1
1	1	0	0	0	0	0	0
1	1	1	0	0	1	1	0
1	1	0	1	0	0	1	1
1	1	1	1	1	0	0	1

Question 2

Table 2: Truth Table for 2-bits Adder

a1	a0	b1	b0	c2	c1	c0	Minterm
0	0	0	0	0	0	0	$a_1'a_0'b_1'b_0'$
0	0	0	1	0	0	1	$a_1'a_0'b_1'b_0$
0	0	1	0	0	1	0	$a_1'a_0'b_1b_0'$
0	0	1	1	0	1	1	$a_1'a_0'b_1b_0$
0	1	0	0	0	0	1	$a_1'a_0b_1'b_0'$
0	1	0	1	0	1	0	$a_1'a_0b_1'b_0$
0	1	1	0	0	1	1	$a_1'a_0b_1b_0'$
0	1	1	1	1	0	0	$a_1'a_0b_1b_0$
1	0	0	0	0	1	0	$a_1a_0'b_1'b_0'$
1	0	0	1	0	1	1	$a_1a_0'b_1'b_0$
1	0	1	0	1	0	0	$a_1a_0'b_1b_0'$
1	0	1	1	1	0	1	$a_1a_0'b_1b_0$
1	1	0	0	0	1	1	$a_1a_0b_1'b_0'$
1	1	0	1	1	0	0	$a_1a_0b_1'b_0$
1	1	1	0	1	0	1	$a_1a_0b_1b_0'$
1	1	1	1	1	1	0	$a_1a_0b_1b_0$

$c2 = a_1'a_0b_1b_0 + a_1a_0'b_1b_0' + a_1a_0'b_1b_0 + a_1a_0b_1'b_0 + a_1a_0b_1b_0' + a_1a_0b_1b_0$

$c1 = a_1'a_0'b_1b_0' + a_1'a_0'b_1b_0 + a_1'a_0b_1'b_0 + a_1'a_0b_1b_0' + a_1a_0'b_1'b_0' + a_1a_0'b_1'b_0 + a_1a_0b_1'b_0' + a_1a_0b_1b_0$

$c0 = a_1'a_0'b_1'b_0 + a_1'a_0'b_1b_0 + a_1'a_0b_1'b_0' + a_1'a_0b_1b_0' + a_1a_0'b_1'b_0 + a_1a_0'b_1b_0 + a_1a_0b_1'b_0' + a_1a_0b_1b_0'$

Thirteen primitive gates are needed for c2, twenty-five gates for c1, and twenty-five gates for c0 if the SOP equations are not reduced.