BME 393L Lab 1: Simple Circuit

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In-Lab

4.1 Simulation of a VHDL code

```
library ieee;
use ieee.std_logic_1164.all;

entity First_circuit is
      port( SW:         in    std_logic_vector(3 downto 0);
            LEDG:       out   std_logic_vector(2 downto 0)
            );
end entity First_circuit;

architecture main of First_circuit is
signal xor1, xor2, xor3:    std_logic;
signal and1, and2, and3:    std_logic;
signal or1:                 std_logic;

begin

xor1 <= sw(0) xor sw(2);
and1 <= sw(0) and sw(2);
xor2 <= sw(1) xor sw(3);
and2 <= sw(1) and sw(3);
xor3 <= and1 xor xor2;
and3 <= and1 and xor2;
or1 <= and2 or and3;
LEDG(0) <= xor1;
LEDG(1) <= xor3;
LEDG(2) <= or1;

end architecture main;
```

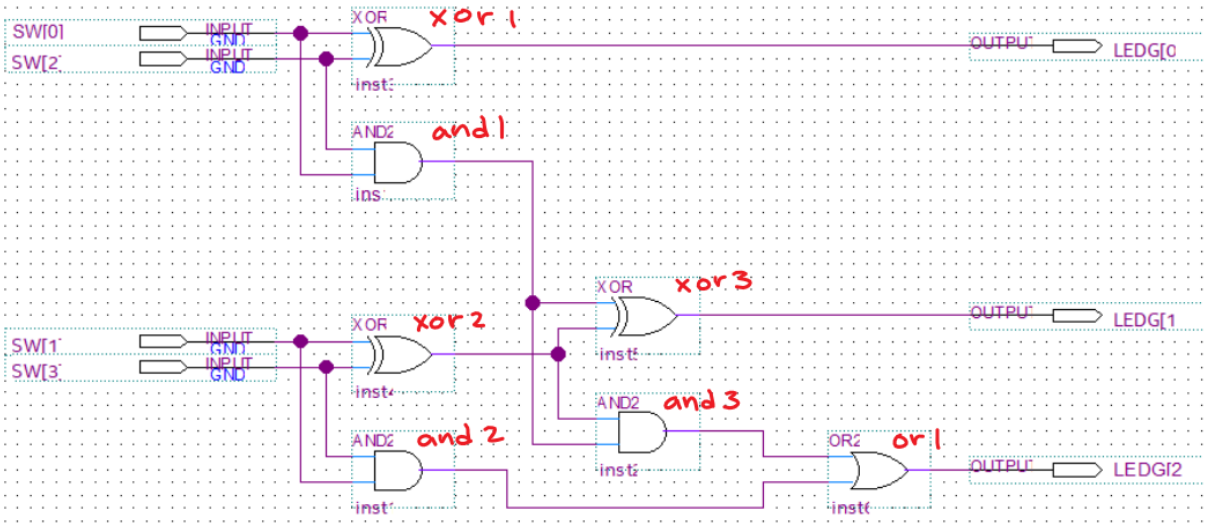

Figure 1: Gates are named and translated into the VHDL code above.

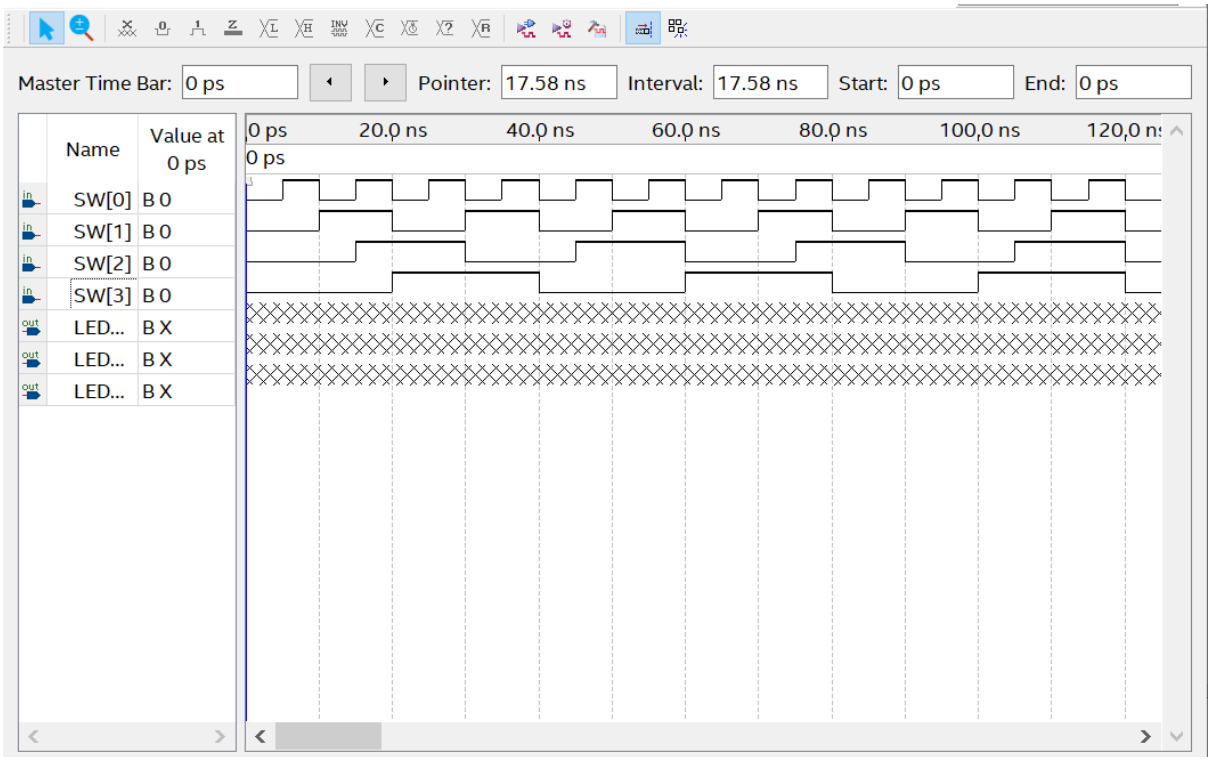

Figure 2: Inputs SW[0] to SW[3] are overwritten with 10-40 nanosecond pulses, respectively.

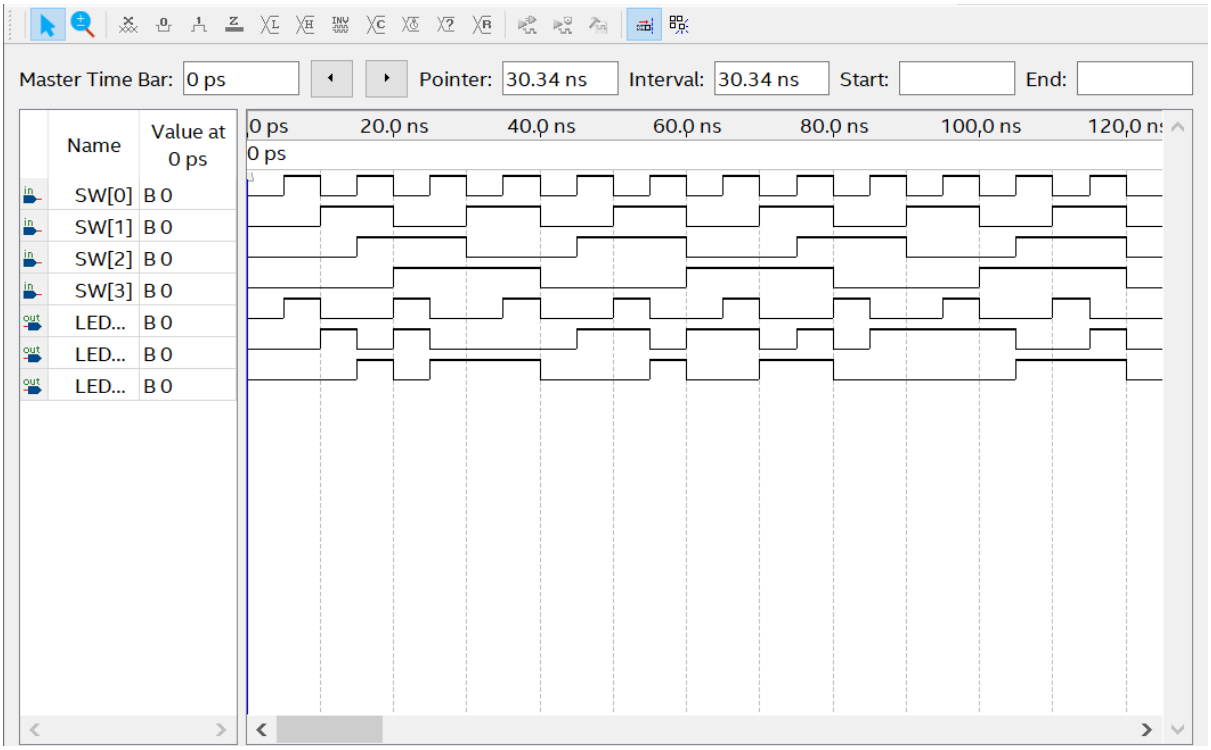

Figure 3: Outputs are generated from LED[0] to LED[2].

Table 1: Truth table for the VHDL circuit.

a(1) SW[3]	a(0) SW[2]	b(1) SW[1]	b(0) SW[0]	c(2) LEDG[2]	c(1) LEDG[1]	c(0) LEDG[0]
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

4.2. Schematic entry in digital circuits

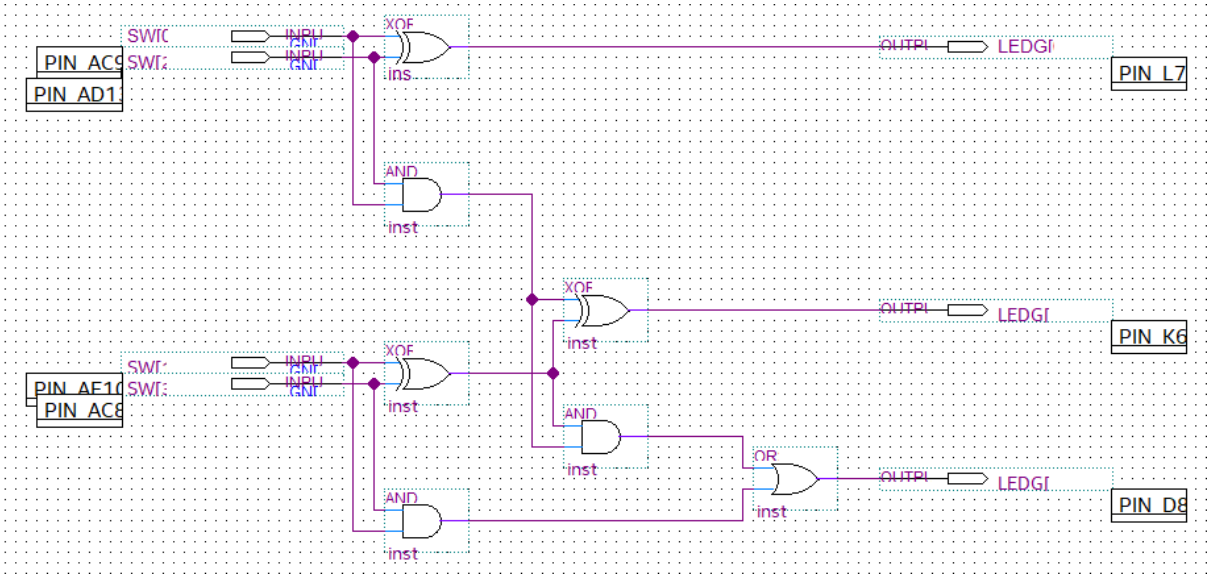

Figure 4. Simple Circuit Schematic Entry.

From top to bottom, the input pins are labeled SW[0], SW[1], SW[2], and SW[3]. In the same order, the output pins are labeled LEDG[0], LEDG[1], LEDG[2].

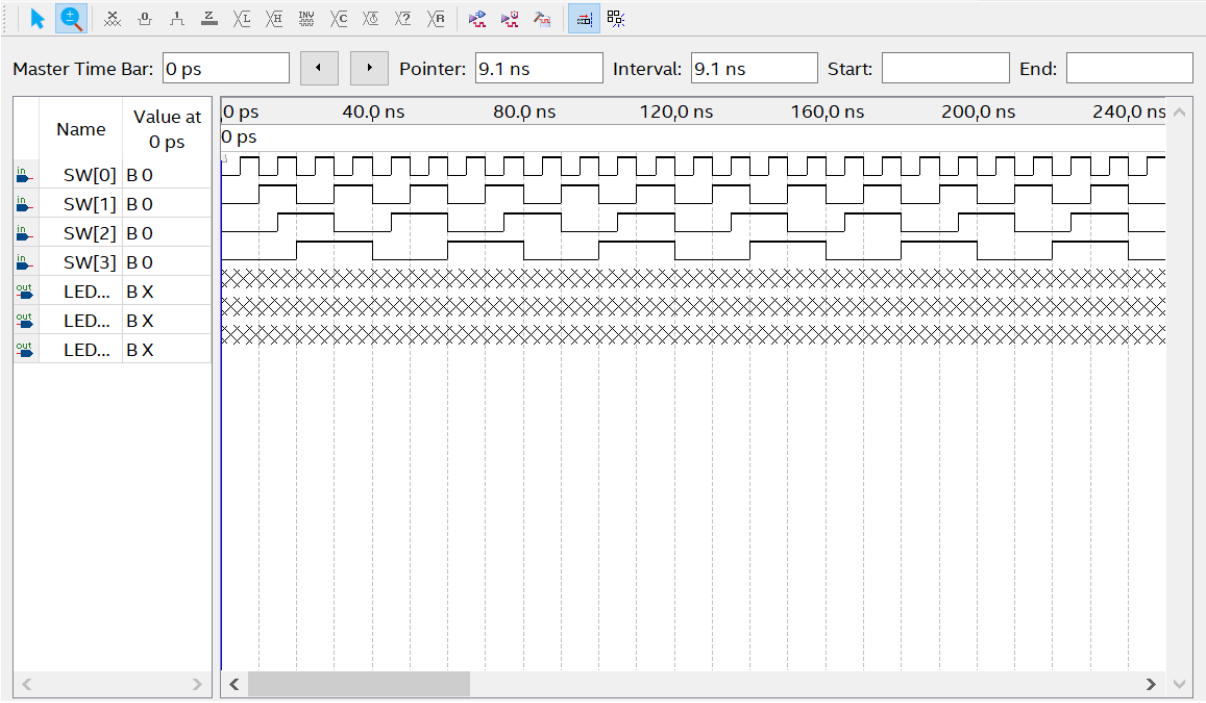

Figure 5. Waveform Input for Simple Circuit Schematic Entry.

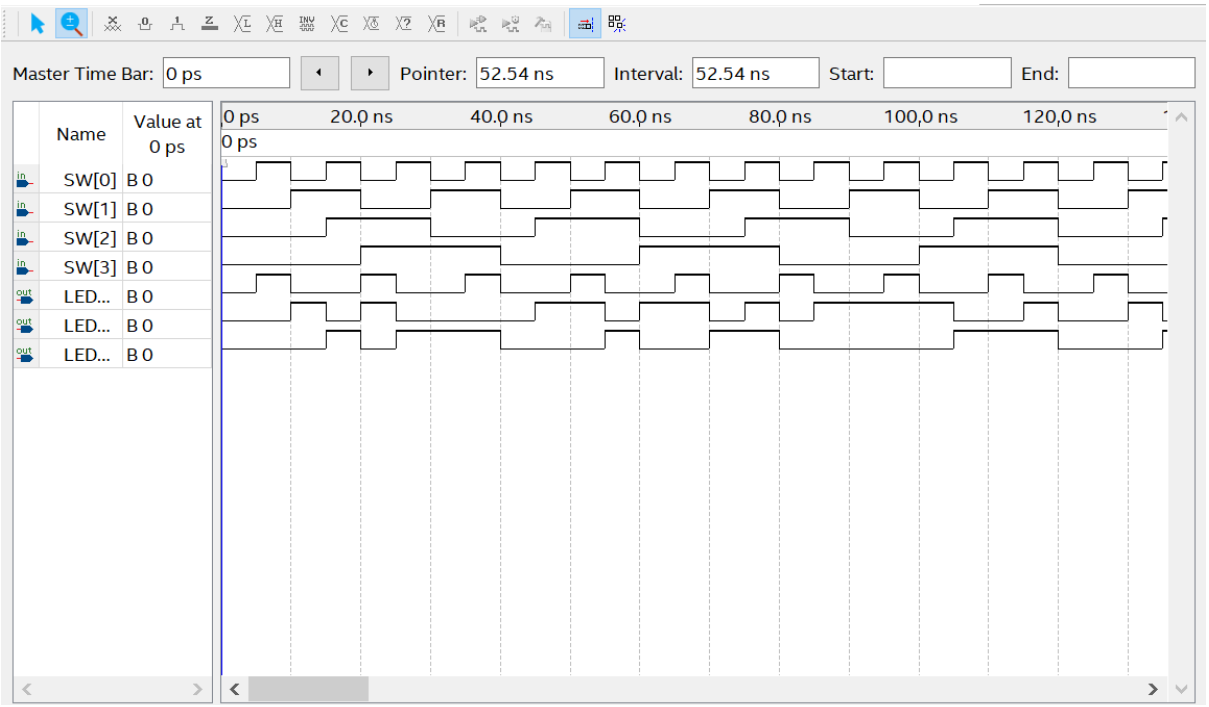

Figure 6. Simulation Results for Simple Circuit Schematic Circuit.

Table 2: Truth table for schematic entry circuit.

a(1) SW[3]	a(0) SW[2]	b(1) SW[1]	b(0) SW[0]	c(2) LEDG[2]	c(1) LEDG[1]	c(0) LEDG[0]
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

5.1. Lab Report

Table 1 from Section 4.1 and Table 2 from Section 4.2 are identical. This is also reflected in Figure 3 and Figure 6 having the same input and output waveforms. The result is expected because the circuit architecture is the same, just represented in two different formats.

Table 3: Inputs SW[0] and SW[1] are represented as Input A, SW[2] and SW[3] are presented as Input B, and the three LEDs are represented as Output C.

Input B (Decimal)	Input A (Decimal)	Output C (Decimal)
0	0	0
0	1	1
0	2	2
0	3	3

1	0	1
1	1	2
1	2	3
1	3	4
2	0	2
2	1	3
2	2	4
2	3	5
3	0	3
3	1	4
3	2	5
3	3	6

According to Table 3, Output C displays the sum of Input A and Input B. Therefore, the circuit is an adder for two two-bit binary numbers.