BME 393L Lab 2: Intro to FPGAs

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In-Lab

4.1.1. Downloading Digital Circuit on FPGA

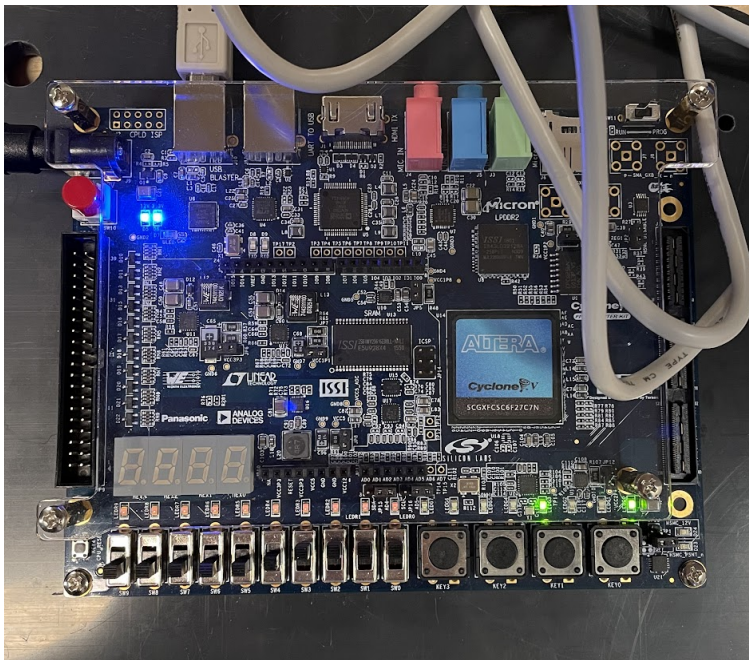

Figure 1: 2-bit multiplier circuit downloaded on FPGA

4.1.2. Primitive gates on breadboard

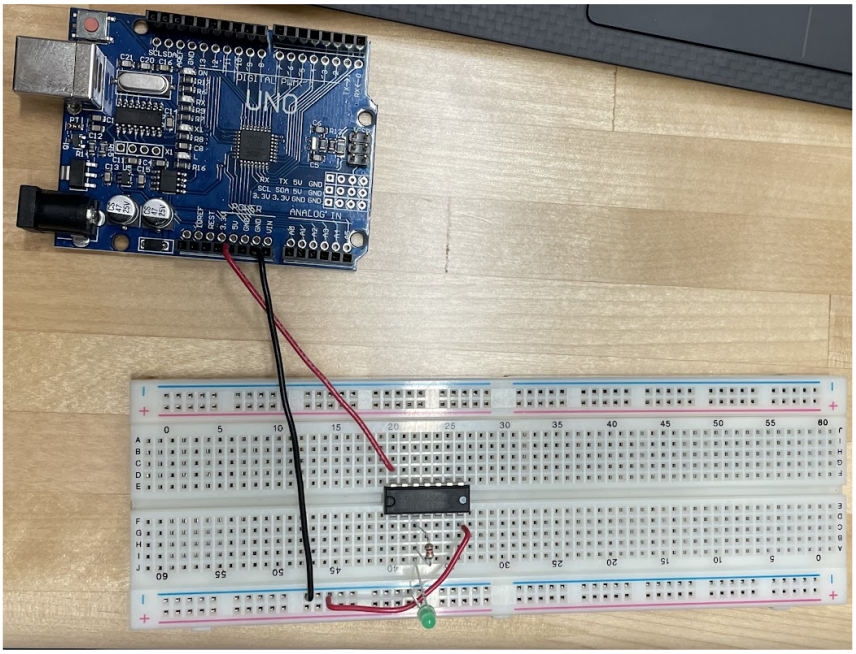

Figure 2: One-resistor circuit

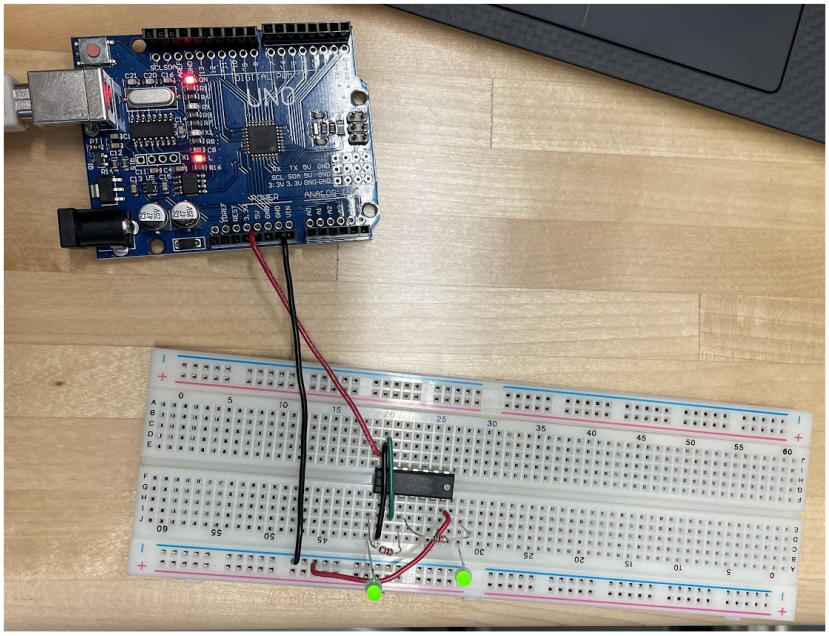

Figure 3: Two-resistor circuit

The voltage measurements are shown in Table 6 and Table 7 in the Lab Report section.

4.1.3. Four-bits adder

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity four_bit is
port( SW:   in std_logic_vector(9 downto 0);
      LEDG: out std_logic_vector(4 downto 0)
      );
end entity four_bit;

architecture main of four_bit is
signal a: std_logic_vector(3 downto 0);
signal b: std_logic_vector(9 downto 6);
signal c: std_logic_vector(4 downto 0);
begin
a <= SW(3 downto 0);
b <= SW(9 downto 6);
c <= ('0' & a) + ('0' & b);
LEDG(4 downto 0) <= std_logic_vector(c);
end architecture main;
```

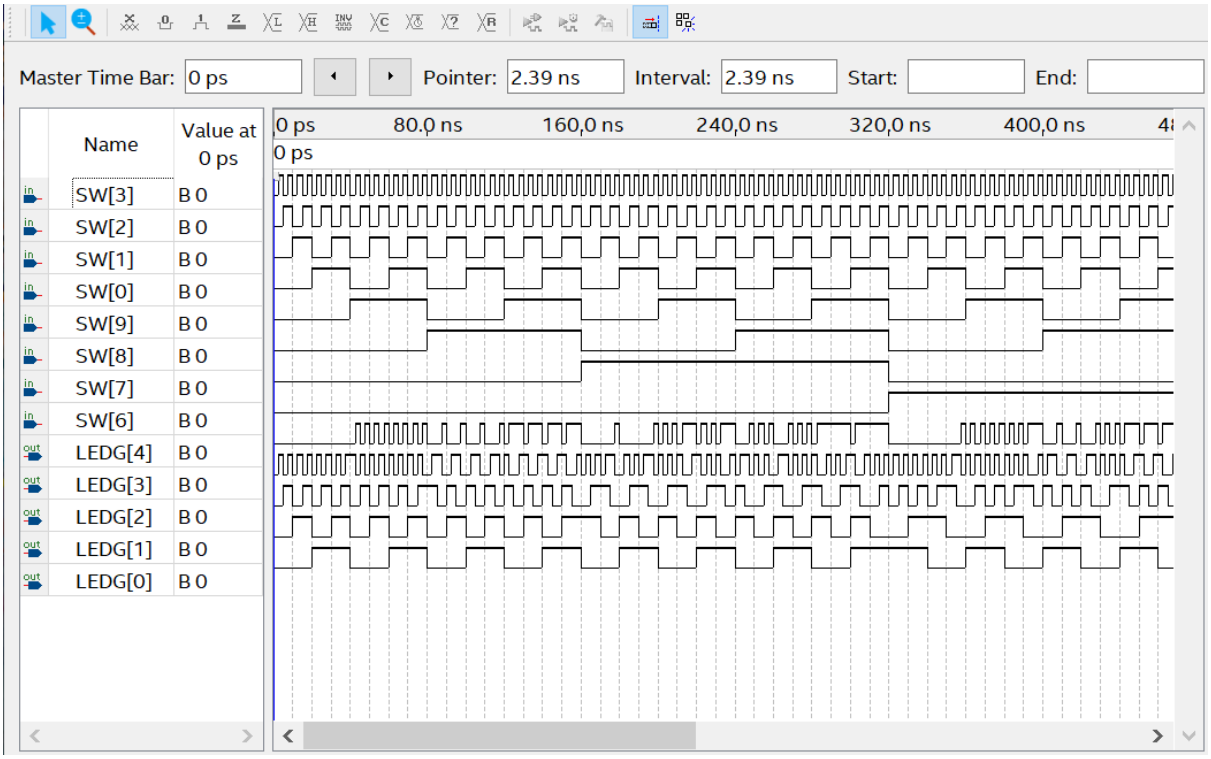

Figure 4: Simulated VHDL outputs for the 4-bit adder

Table 1: Truth Table for 4-bit adder

Input a SW(3 downto 0)	Input b SW(9 downto 6)	Output c (Binary)	Output c (Hexadecimal)
0	0	00000	0
2	5	00111	7
8	3	01011	B
A	5	01111	F
7	9	10000	10
6	D	10011	13
B	7	10010	12
E	C	11010	1A
F	F	11110	1E

Lab Report

1. VHDL Code for Section 4.1.1

```
library ieee;
use ieee.std_logic_1164.all;
```

```
entity Lab2Prelab is
port( SW: in std_logic_vector(3 downto 0);
      LEDG: out std_logic_vector(3 downto 0)
      );
end entity Lab2Prelab;
architecture main of Lab2Prelab is
signal a1, a0, b1, b0: std_logic;
begin
a1 <= SW(1);
a0 <= SW(0);
b1 <= SW(3);
b0 <= SW(2);
LEDG(3) <= (a0 AND b0) AND (a1 AND b1);
LEDG(2) <= (a0 NAND b0) AND (a1 AND b1);
LEDG(1) <= ((a0 AND b1) AND (b0 NAND a1)) OR
           ((a0 NAND b1) AND (b0 AND a1));
LEDG(0) <= a0 AND b0;
end architecture main;
```

Based on Table 1 in the Prelab, the p-vector is the product of a-vector and b-vector. Therefore, the circuit is a multiplier for two 2-bit binary numbers.

2. Reducing the Number of Gates for the 2-Bit Multiplier

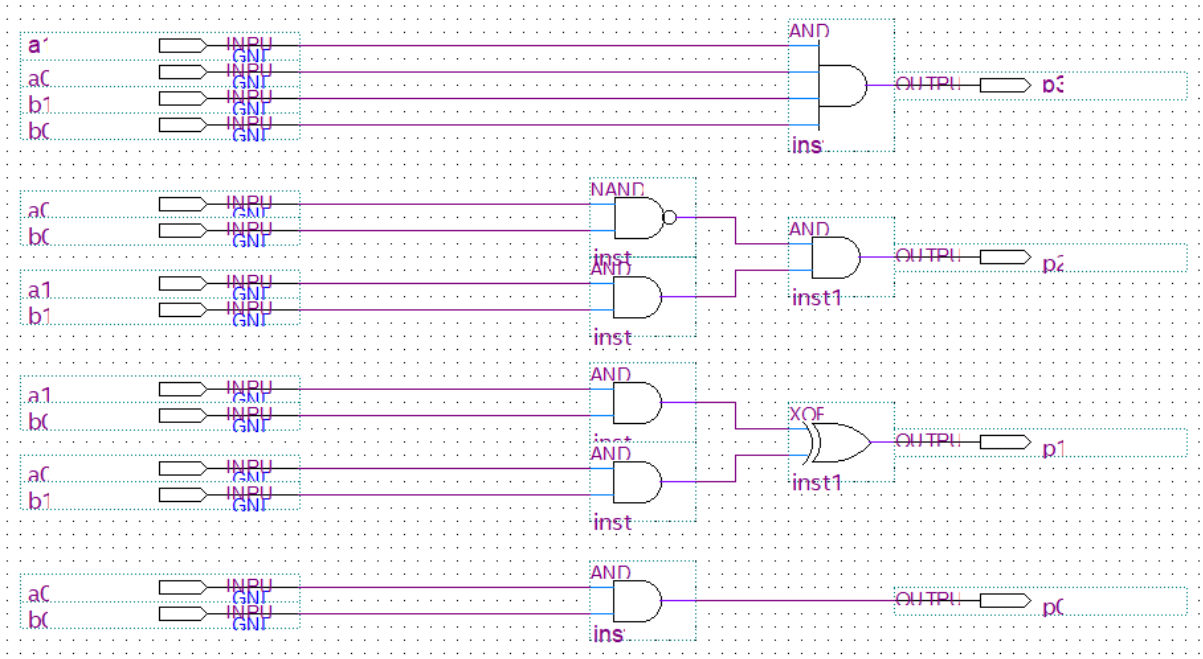

Figure 5: Reduced gate circuit for 2-bit multiplier

The 2-bit multiplier circuit can be reduced to eight gates. First, p3 adopts a 4-AND gate, reducing the total by two. Then, recognizing the symmetry in p1, a 2-XOR gate is used on the two AND pairs, reducing the total by another four. However, p0 and p2 are already optimized. The VHDL implementation becomes:

```
LEDG(3) <= a0 AND b0 AND a1 AND b1;
LEDG(1) <= (a0 AND b1) XOR (b0 AND a1);
```

3. Reducing the Number of Gates for the 2-Bit Adder

Table 2: c2 K-map

c2		a_1a_0			
		00	**01**	**11**	**10**
b_1b_0	**00**	0	0	0	0
	01	0	0	1	0
	11	0	1	1	1
	10	0	0	1	1

Table 3: c1 K-map

c1		a_1a_0			
		00	**01**	**11**	**10**
b_1b_0	**00**	0	0	1	1
	01	0	1	0	1
	11	1	0	1	0
	10	1	1	0	0

Table 4: c0 K-map

c0		a_1a_0			
		00	**01**	**11**	**10**
b_1b_0	**00**	0	1	1	0
	01	1	0	0	1
	11	1	0	0	1
	10	0	1	1	0

After K-map reduction, the equations for each output are as follows:

Table 5: The minimum amount of gates for the 2-bit adder

Output	K-Map Equation	Gates	# Gates
c2	$a_1b_1 + a_1a_0b_0 + a_0b_1b_0$	3 AND, 1 OR	4
c1	$a_1'a_0'b_1 + a_1'b_1b_0 + a_1'a_0b_1'b_0 + a_1a_0b_1b_0 + a_1b_1'b_0' + a_1a_0'b_1'$	1 AND, 2 XOR (Based on Lab 1)	3
c0	$a_0b_0' + a_0'b_0$	1 XOR	1

4. Results From Section 4.1.2

Table 6: Voltage measurements for AND gate

	Voltage for one resistor (V)	Voltage for two resistors (V)
V1	3.010	2.903
V2	1.941	1.938
vt	4.951	4.841

Table 7: Voltage measurements for OR gate

	Voltage for one resistor (V)	Voltage for two resistors (V)
V1	3.009	2.895
V2	1.940	1.939
Vt	4.949	4.834

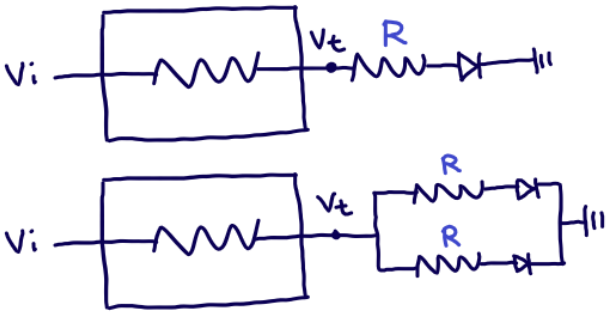

Figure 6: Single vs. parallel resistors

Vt is lower in the two-resistor case because the two branches run in parallel, reducing the effective resistance of each resistor. Since the power supply itself has some resistance, there is a voltage divider that shifts in favour of the power supply. Therefore, a larger voltage drop is experienced by the power supply instead of the circuit in the branched scenario, reducing the measured Vt. Theoretically, Vt would increase or stay the same if larger resistors were used in the branches.

5. Block-diagram for 4-bit Multiplier

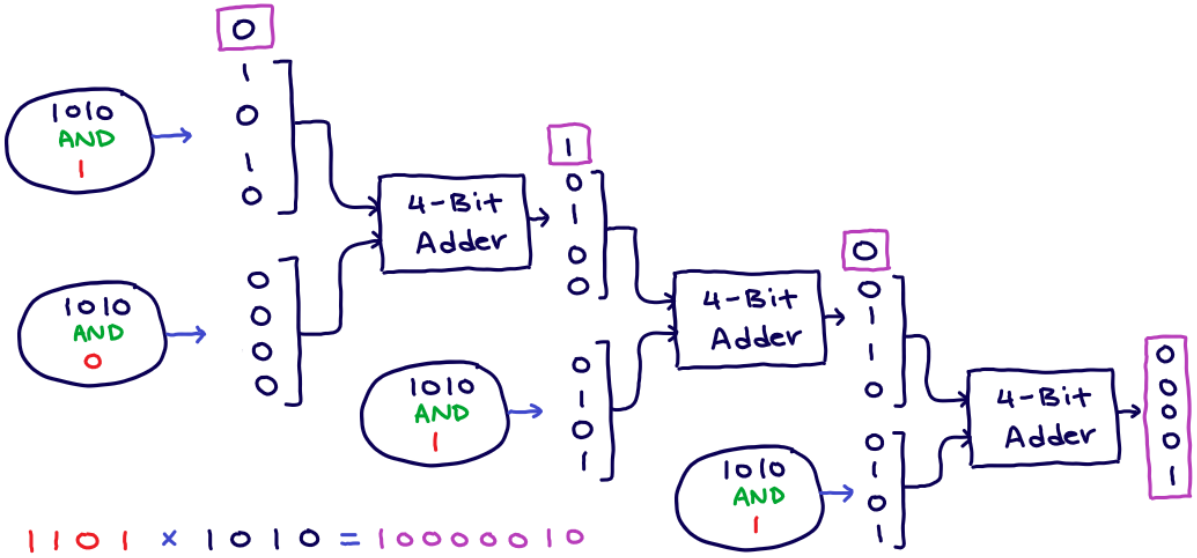

Figure 7: The 4-bit multiplier using three 4-bit adder modules

The diagram in Figure 7 shows how two 4-bit numbers can be multiplied together. At each stage, the least significant bit is saved as the output, and the four most significant bits are put into the next module. This serves to shift the decimal point one space to the right. At each shift, the first number is AND'ed with the corresponding digit of the second number to simulate local (1-bit) multiplication. The last bit of the first input (top left) is automatically saved and an extra 0 is appended in front because a previous addition with zero is not necessary.