ECE 375 Prelab for lab 6

External Interrupts

Lab Time: Friday 4 - 6

Faaiq Waqar

PreLab Questions

To complete this prelab, you may find it useful to look at the full ATmega128 datasheet. If you consult any online sources to help answer the pre lab questions, you must list them as references in your prelab.

1. In computing, there are traditionally two ways for a microprocessor to listen to other devices and communicate: polling and interrupts. Give a concise overview/description of each method, and give a few examples of situations where you would want to choose one method over the other.

Reference Used for Problem: https://www.geeksforgeeks.org/difference-between-interrupt-and-polling/

Polling: Polling s a non-hardware based mechanism that uses a protocol in which the CPU will check steadily over time whether or not the device requires some kind of attention. Essentially the polling unit will ask the device over and over whether or not it requires CPU support, and the CPU in turn will check to provide that resource.

Interrupts: An interrupt is a hardware based mechanism in which the computing device sends a signal to the CPU that it requires some kind of indicated attention, based on the type of interrupt signal. An interrupt is not time bounded. An interrupt will have the CPU stop its current process and effectively respond to the interrupt signal by passing control to an interrupt handler

When to Use What: Because of the nature of the two handling methods, it would likely be best to use interrupts in on command situations. That is when perhaps, you would like to use a button press or a specified signal interrupt in a program to take control and terminate the program when you want to. This is also useful in non-termination objectives where the objective is moreso to count at specific times. The polling method could be good in comparative methodology, perhaps when we hope to establish an asymptote on data presses or are using the method to track the best way to track for multiple occurrences in a short time frame.

2. Describe the function of each bit in the following ATmega128 I/O registers: EICRA, EICRB, and EIMSK. Do not just give a brief summary of these registers; give specific details for each bit of each register, such as its possible values and what function or setting results from each of those values. Also, do not just directly paste your answer from the datasheet, but instead try to describe these details in your own words.

EICRA: External Interrupt Control Register A. EICRA contains 8 bits, all with initial values set to 0, defining it al low level interrupts. Defined for external interrupt 3 - 0 sense control bits, activated by the external pints INT3:0. These pulses will generate a readable interrupt on EIRCA

EICRB: External Interrupt Control Register B. EICRB contains 8 bits, all with initial values set to 0, defining it al low level interrupts. Defined for external interrupt 7 - 4 sense control bits, activated by the external pints INT7:4. These pulses will generate a readable interrupt on EIRCB

EIMSK: External Interrupt Mask Register. This register, when an interrupt bit is written in, and the interrupt but in the status register is set to one, will trigger an interrupt request even if the pin is enabled as an output. This will provide a way to generate a software interrupt.

3. The ATmega128 microcontroller uses interrupt vectors to execute particular instructions when an interrupt occurs. What is an interrupt vector? List the interrupt vector (address) for each of the following ATmega128 interrupts: Timer/Counter0 Overflow, External Interrupt 5, and Analog Comparator.

Resource External Used: https://whatis.techtarget.com/definition/interrupt-vector

What is an interrupt vector: An interrupt vector is the addressable memory location in program memory of the interrupt handler, which prioritizes the specified interrupts and saves them

Timer/Counter0 Overflow: Vector number 17, Program address $0020

External Interrupt 5: Vector number 7, Program address $000C

Analog Comparator: Vector number 24, Program address $002E

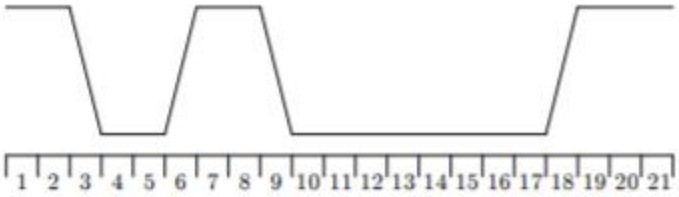

Figure 1: Sample Input to External Interrupt

4. Microcontrollers often provide several different ways of configuring interrupt triggering, such as level detection and edge detection. Suppose the signal shown in Figure 1 was connected to a microcontroller pin that was configured as an input and had the ability to trigger an interrupt based on certain signal conditions. List the cycles (or range of cycles) for which an external interrupt would be triggered if that pin's sense control was configured for: (a) rising edge detection, (b) falling edge detection, (c) low level detection, and (d) high level detection. Note: There should be no overlap in your answers, i.e., only one type of interrupt condition can be detected during a given cycle.

a. rising edge detection: [6,6] + [18,18]
b. falling edge detection: [3,3] + [9,9]
c. low level detection: [4,5] + [10,17]
d. high level detection: [1,2] + [7,8] + [19,21]