Part 2 : MOSFET Characteristics

1.ID vs VGS

1.1)

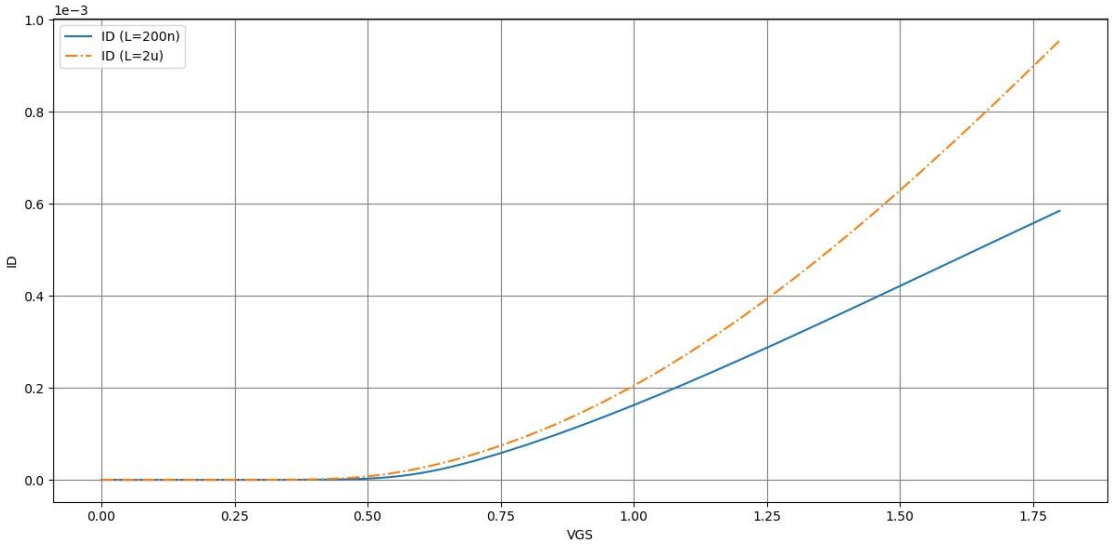

Figure 1 plot Id vs VGS for NMOS (ADT)

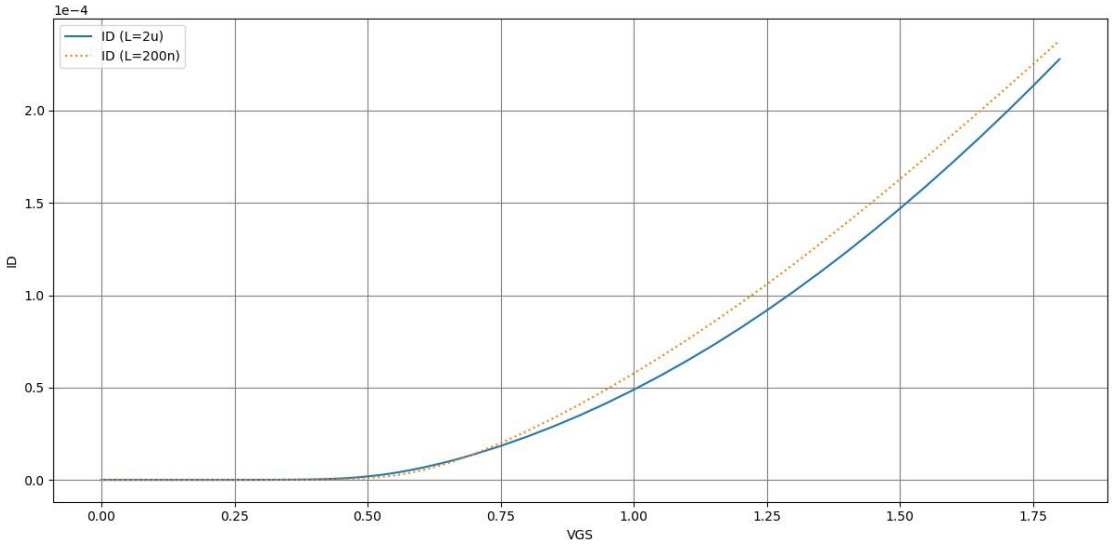

Figure 2 plot Id vs VGS for PMOS (ADT)

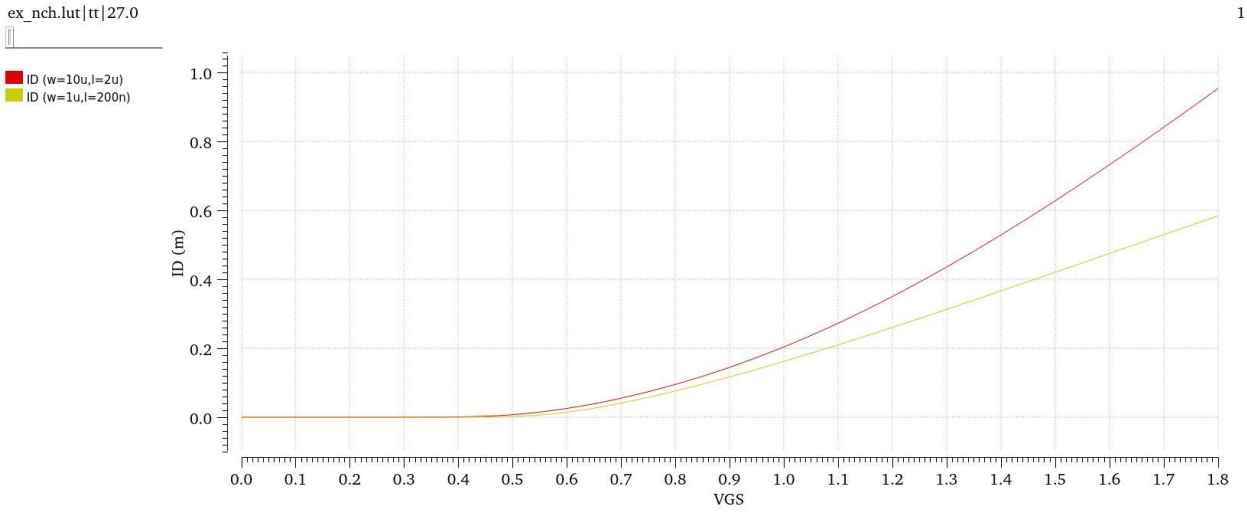

Figure 3 plot Id vs VGS for NMOS (Sizing Assistant)

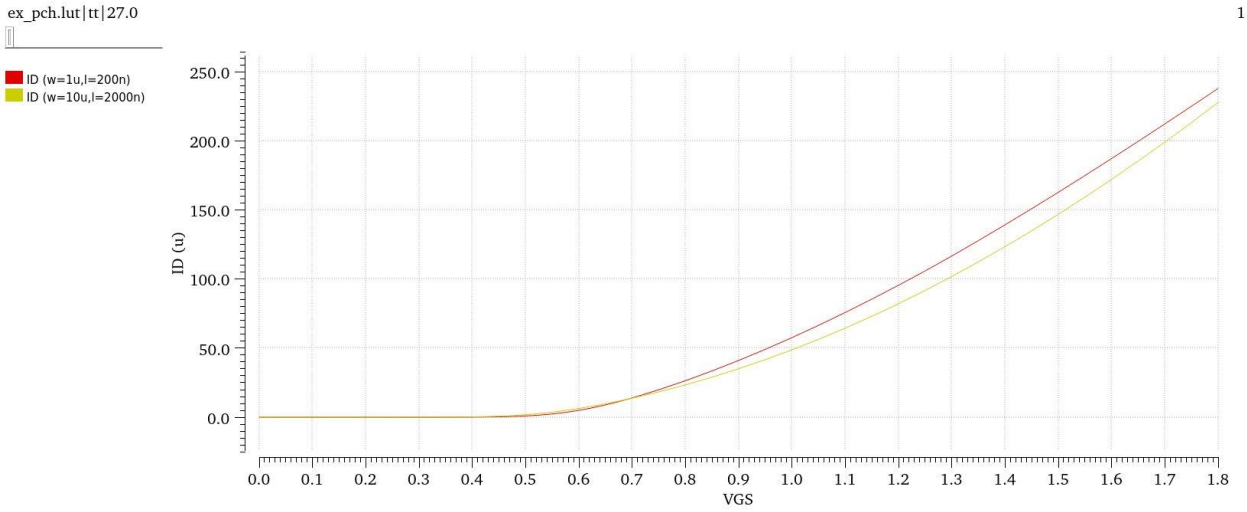

Figure 4 plot Id vs VGS for PMOS (Sizing Assistant)

1.2)

• Which one has higher current? Why?

• Is the relation linear or quadratic? Why?

•The higher current in a long channel device compared to a short channel device can be attributed to a few factors. In a long channel device, the assumption is made that the electric field is primarily one-dimensional (1D) and controlled only by the gate voltage. This allows for stronger gate control over the channel and results in a higher current.
On the other hand, in a short channel device, the electric field becomes two-dimensional (2D) due to the influence of both the gate voltage and the drain voltage. This 2D electric field distribution limits the strength of gate control over the channel and reduces the drain current.

Additionally, long channel NMOS has higher current than the short channel (as expected) that is because short channel effects (velocity saturation and mobility degeneration).

•The drain current in short channel devices is often considered to have a linear relationship with respect to the gate-to-source voltage (VGS). This linear relationship is due to the presence of velocity saturation, which limits the increase in current.

The drain current in long channel devices is often considered to have a quadratic relationship with respect to VGS. The drain current (ID) in a long channel device can be approximated by the equation:

ID = (1/2) (W/L) $\mu C_{ox}(V_{gs} - V_{th})^2$.

1.3)

3) Comment on the differences between NMOS and PMOS.

• Which one has higher current? Why?

• What is the ratio between NMOS and PMOS currents at VGS = VDD?

• Which one is more affected by short channel effects?

•the higher current in an NMOS (n-type MOSFET) compared to a PMOS (p-type MOSFET) can be attributed to the difference in carrier mobility between electrons and holes. Electrons generally have higher mobility compared to holes in semiconductor materials. This higher mobility allows electrons to move more easily through the channel, resulting in higher current flow in NMOS devices.

•the ratio between the current of an NMOS (ID_n) and the current of a PMOS (ID_p) device is influenced by the mobility of electrons and holes. When the NMOS and PMOS devices have the same channel length, width, and gate-to-source voltage (V_{GS}) bias, the current ratio can be approximated using the ratio of electron mobility (μ_n) to hole mobility (μ_p).

The approximate ratio of $ID_n$to ID_p is given by:

$$\frac{ID_n}{ID_p} \approx \frac{\mu_n}{\mu_p}$$

From the figure (11) get values of current at $V_{GS} = V_{DD}$

$$\frac{ID_n}{ID_p} = \frac{5.75504}{1.37295} = 4.19 \quad \text{(Long channel)}$$

$$\frac{ID_n}{ID_p} = \frac{3.53177}{1.42872} = 2.47 \quad \text{(short channel)}$$

•short channel effect appears strongly in case of NMOS more than case of PMOS

2. gm vs VGS

2.1)

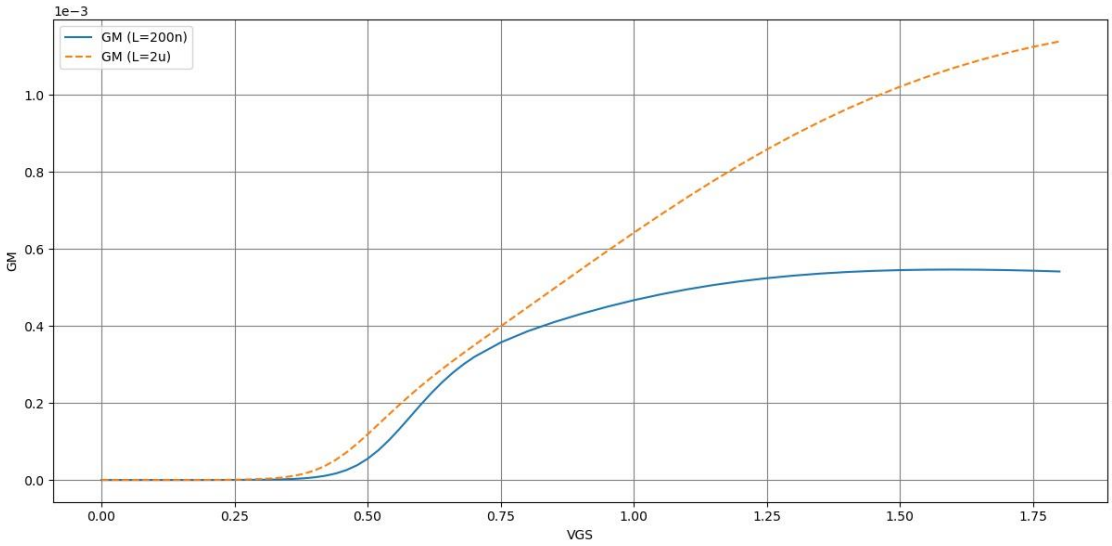

Figure 5 plot gm vs VGS for NMOS (ADT)

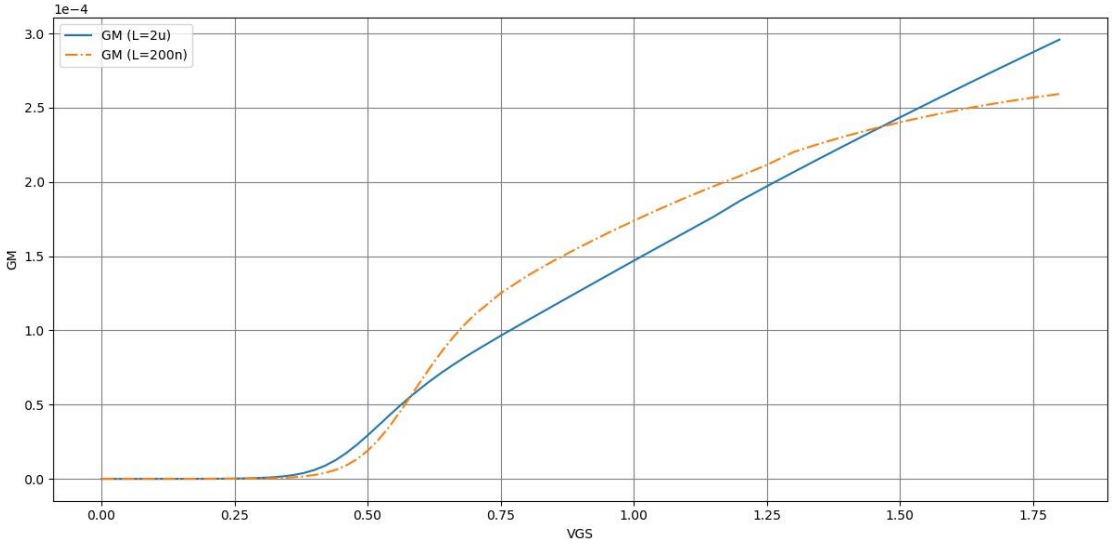

Figure 6 plot gm vs VGS for PMOS (ADT)

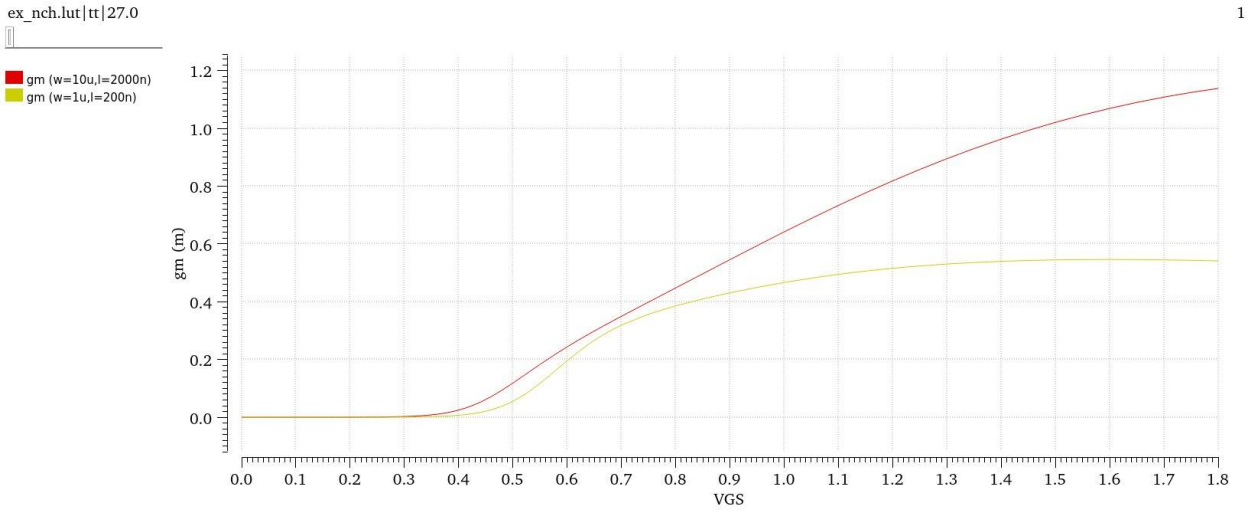

Figure 7 plot gm vs VGS for NMOS (Sizing Assistant)

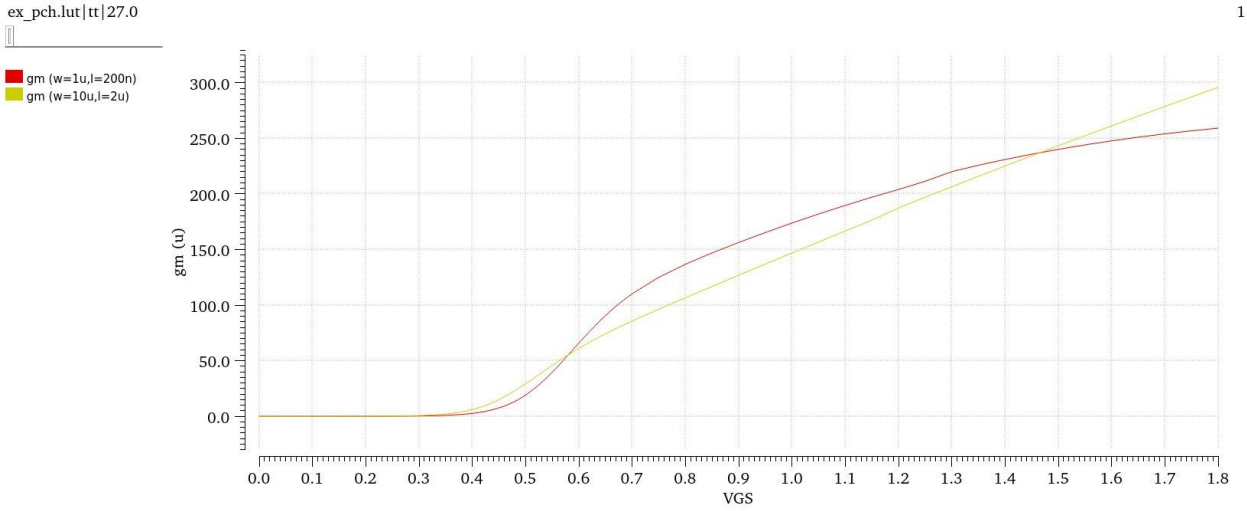

Figure 8 plot gm vs VGS for PMOS (Sizing Assistant)

2.2)

• Does gm increase linearly? Why?

• Does gm saturate? Why?

• transconductance (gm) represents the derivative of current drain, expressed as gm =$\frac{\partial I_d}{\partial v_{GS}}$. In the case of long channel devices, gm exhibits a linear relationship with the gate voltage, gm ∝ VGS. On the other hand, for short channel devices, gm can be approximated as a step function, where gm = constant. This behavior arises from the linear correlation between drain current and VGS.

•the transconductance (gm) exhibits saturation behavior specifically in the case of short channel MOSFETs. In this scenario, gm is considered to behave as a step function, indicating that it reaches a maximum value and remains constant for higher gate voltages. This saturation effect is due to the influence of short channel effects.

3. ID vs VDS

3.1)

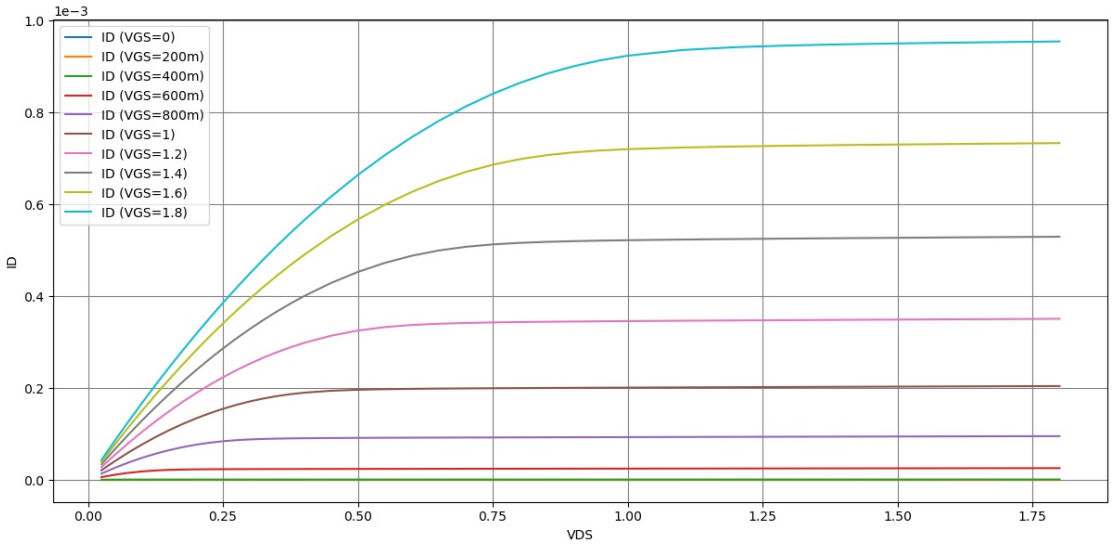

Figure 9 plot Id vs VDS for NMOS long channel (ADT)

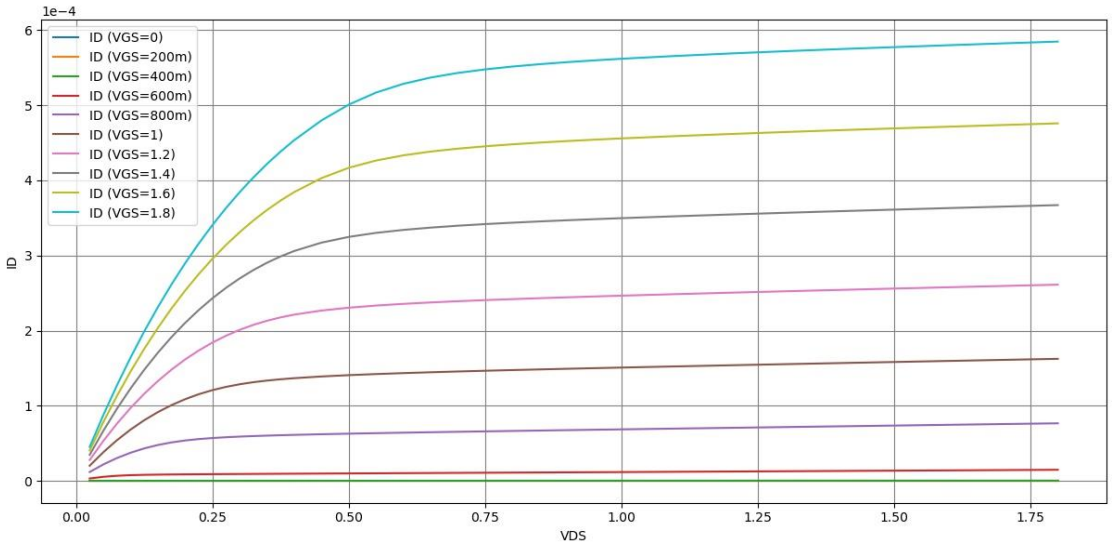

Figure 10 plot Id vs VDS for NMOS short channel (ADT)

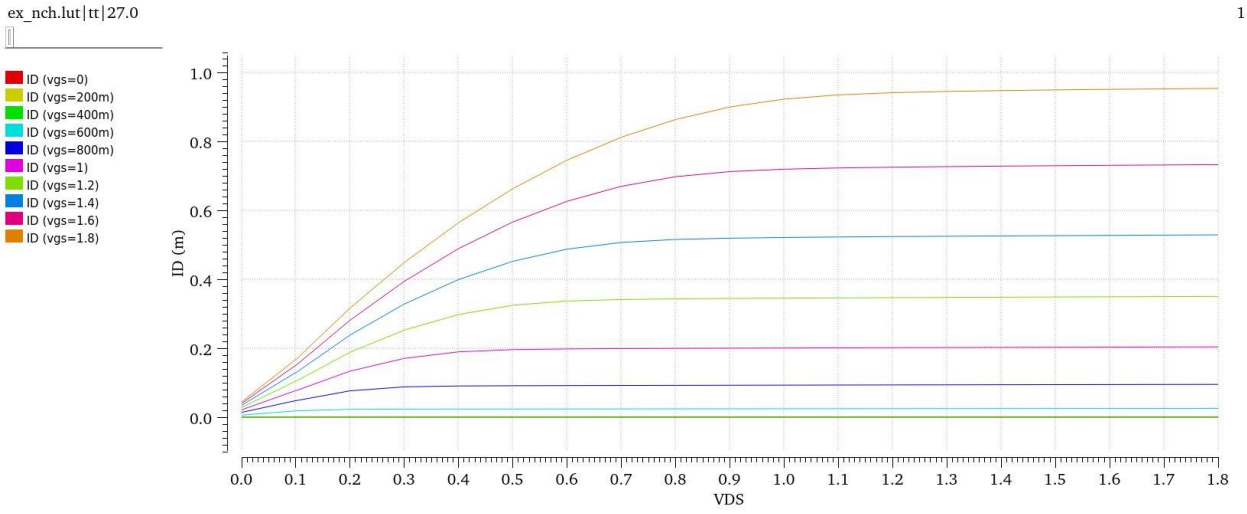

Figure 11 plot Id vs VDS for NMOS long channel (Sizing Assistant)

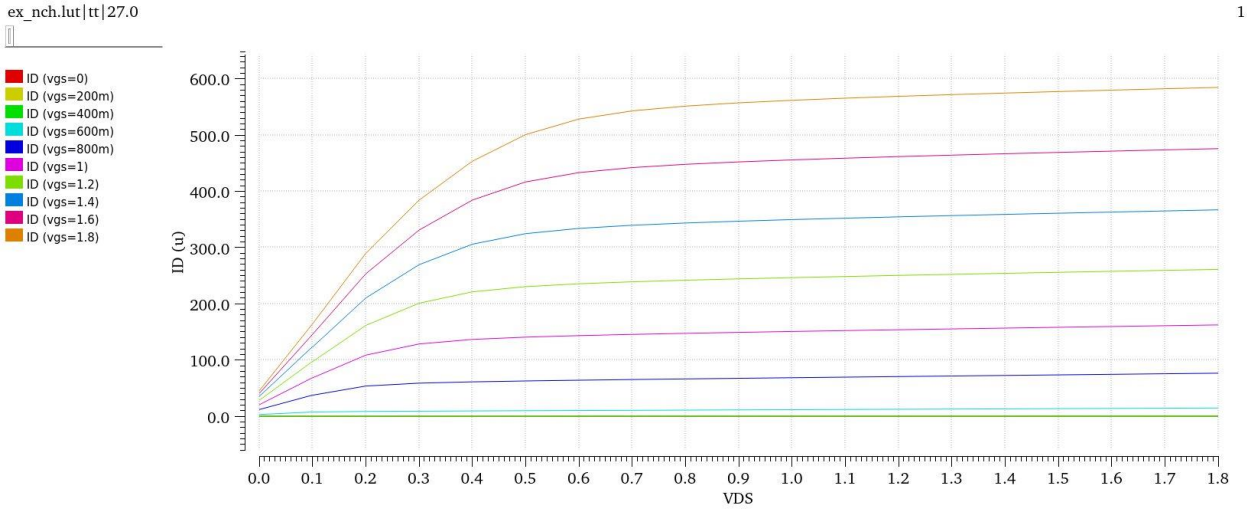

Figure 12 plot Id vs VDS for NMOS short channel (Sizing Assistant)

3.2)

Comment on the differences between short channel and long channel results.

- Which one has higher current? Why?
- Which one has higher slope in the saturation region? Why?

•long channel MOSFETs exhibit higher current compared to short channel MOSFETs. This disparity arises from several factors. Firstly, the width of the depletion region is wider in short channel MOSFETs compared to long channel MOSFETs. Additionally, the drain induced barrier lowering effect contributes to the difference in current. Furthermore, the gate voltage has a reduced level of control over the drain current in short channel MOSFETs. These combined factors result in the observed disparity in current between the two types of MOSFETs.

•long channel MOSFETs exhibit a higher slope in the saturation region compared to short channel MOSFETs. This difference is evident when observing the distinct steps during the gate voltage sweep for each type of device. In long channel MOSFETs, the steps follow a quadratic, whereas in short channel MOSFETs, they follow a linear. This disparity in step behavior is primarily attributed to the dominant influence of velocity saturation effects in short channel MOSFETs.

4. [Optional] gm and ro in Triode and Saturation

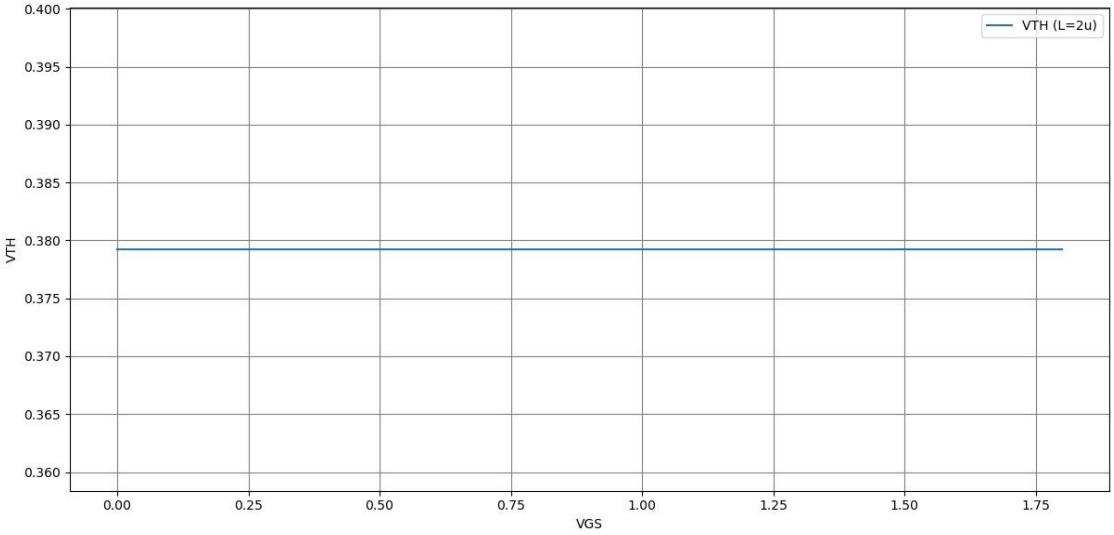

Figure 13 plot VTH vs VGS

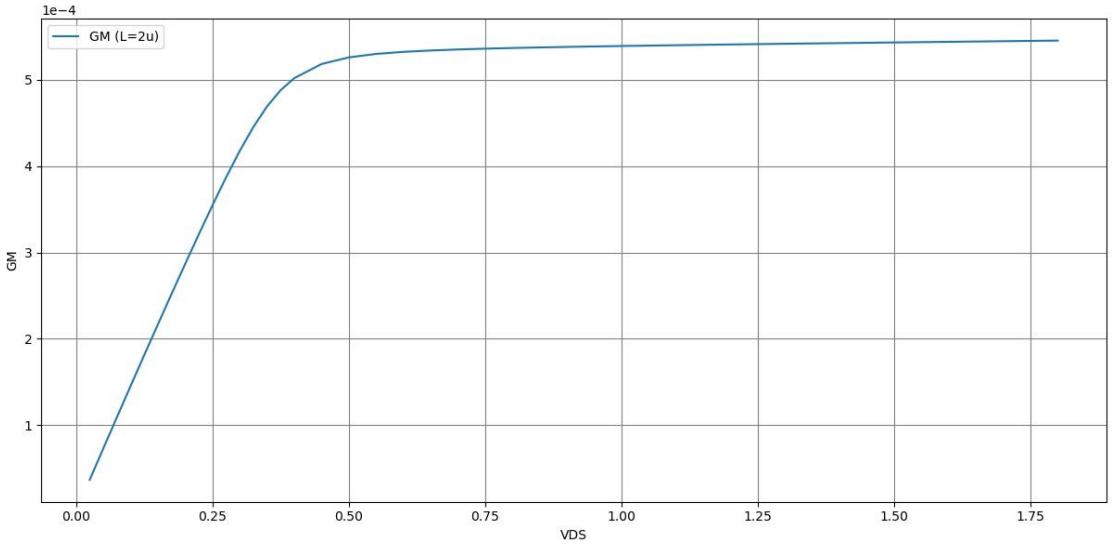

Figure 14 plot gm vs VDS for NMOS (ADT)

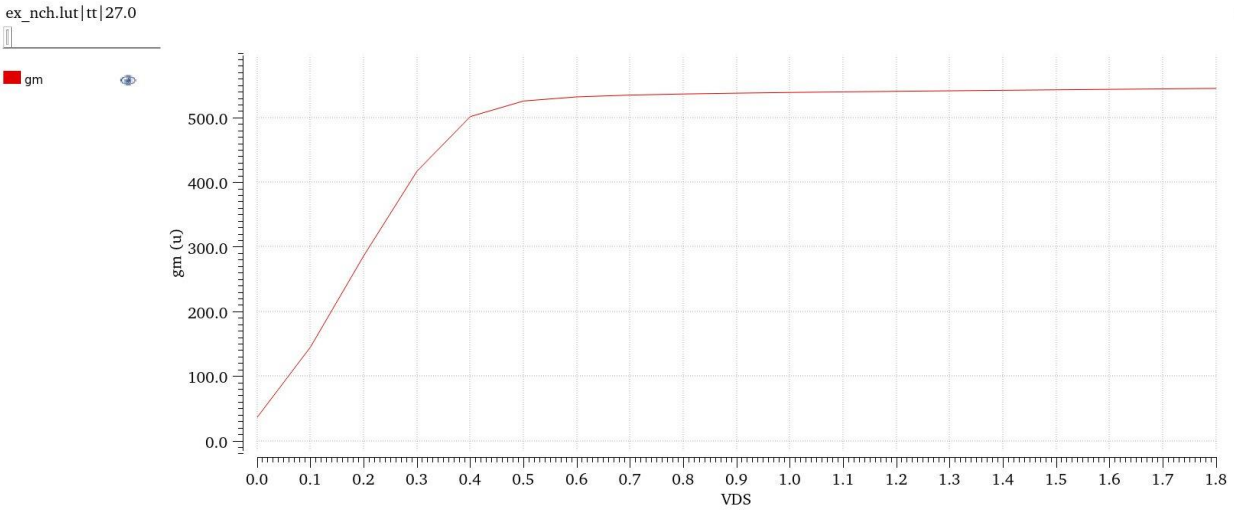

Figure 15 plot gm vs VDS for NMOS (Sizing Assistant)

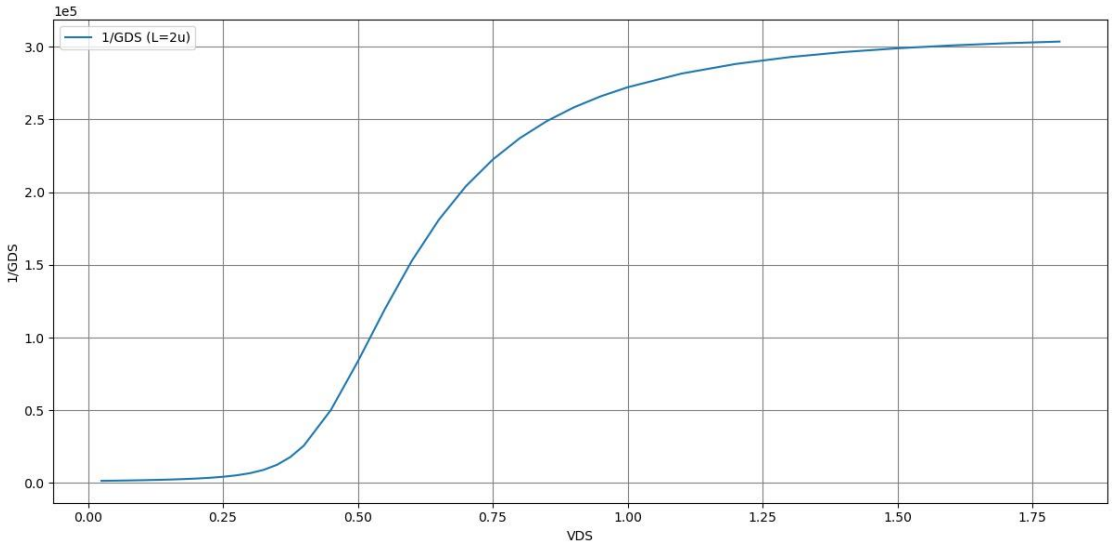

Figure 16 plot ro vs VDS for NMOS (ADT)

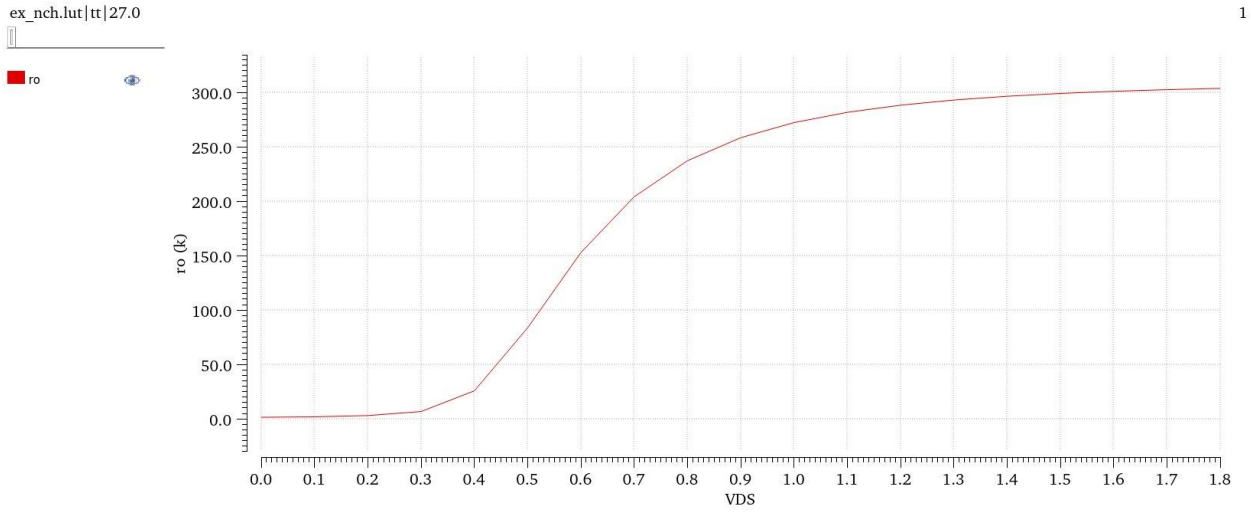

Figure 17 plot ro vs VDS for NMOS (Sizing Assistant)

From the graph of we found the value of $V_{TH} = 0.38V$. $V_{GS} \approx 0.38 + 0.5 \approx 0.9V$

4.2) 2) Comment on the variation of gm vs VDS.

• In the first part of the curve, is the relation linear? Why?

• Does gm saturate? Why?

• Where do you want to operate the transistor for analog amplifier applications? Why?

•I found from graph the relationship in the first part of curve is linear, before $V_{DS} = 0.5V$ because of the transistor is in triode region $I_D \alpha V_{DS}^2$ it's quadratic relation

$I_D = K_n(V_{OV} * V_{DS} - \frac{V_{DS}^2}{2})$.

• Then gm saturates because gm gets in saturation region

$I_D = {K_n}/{2} * {V_{OV}}^2(1 + \gamma V_{DS})$.at some point gm depend on V_{DS} semi linear so gm will be constant.

• for analog amplifier we should use transistor in saturation region where I_D is mostly depend with V_{GS} and little effect with V_{DS}(channel length modulation).

3) Comment on the variation of ro vs VDS.

• Does ro saturate just after the transistor enters saturation similar to gm? Why?

• Does ro increase if the transistor is biased more into saturation?

• Should we operate the transistor at the edge of saturation?

• Where do you want to operate the transistor for analog amplifier applications? Why?

•r_o will take time before it saturates because of little depend on channel length modulation as r_o increase with channel length modulation This means that small changes in drain-source voltage (V_{DS}) will not cause significant changes in the drain current (Ids) flowing through the transistor in saturation

resistance (r_o) becomes relatively high and remains relatively constant in this region.

•r_o will increase as we farther go into saturation region due to channel length modulation.

•The edge of saturation will satisfy both regions (triode-saturation)

Saturation: at this region where $r_o$is almost constant, $r_o$will increase due to channel length modulation as we go farther into sat region until a point short channel effect makes it decrease.

Triode: in this region current depend on V_{DS} quadratic it's not ideal if we want to use it as VCCS.

• for analog amplifier we should use transistor in saturation region where I_D is mostly depend with V_{GS} and little effect with V_{DS}(channel length modulation).