Part 1: Exploring Sizing Tradeoffs Using SA

1) We want to design a simple current mirror with the following specs.

Parameter	
Input Current	$10\mu A$
Output Current	$20\mu A$
% Change in Current for $\Delta V_{out} = 1V$	$<10\%$
Current direction (source/sink)	Sink

Answer the following:

2) The % Change in current translates to a spec on the $\lambda = 1/V_A$ of the device. How much is the required λ?

$$I_D = \frac{K}{2} V_{OV}^2 (1 + \gamma V_{DS}) = \frac{K}{2} V_{OV}^2 (1 + \gamma V_{OUT})$$

$$\Delta I_D = \frac{K}{2} V_{OV}^2 \, \gamma \, \Delta V_{OUT}$$

$$\frac{\Delta I_D}{I_D} = \frac{\gamma \Delta V_{OUT}}{1 + \gamma V_{OUT}} \approx \gamma \Delta V_{OUT} \quad \rightarrow \quad \gamma = 0.1$$

3) Sinking current means which device type? NMOS or PMOS?

NMOS.

4) The higher the g_m/I_D (the lower the V^*) the higher the headroom (the available swing), but the larger the area. Examine this trade-off using SA as shown below. Report L and W vs Vstar.

Figure 1 setup of SA

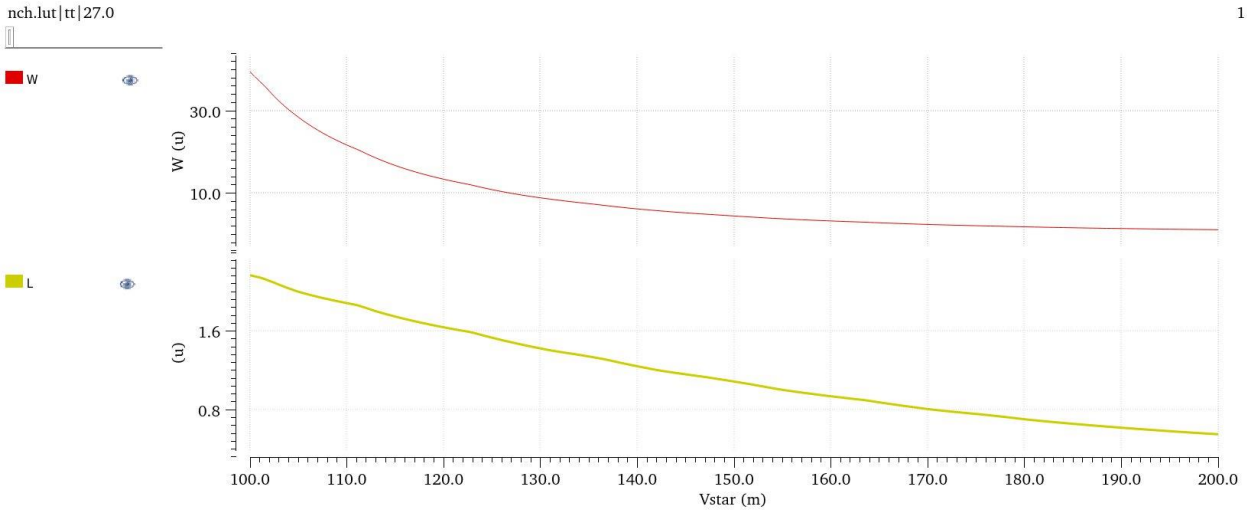


*Figure 2 plot w & l vs v**

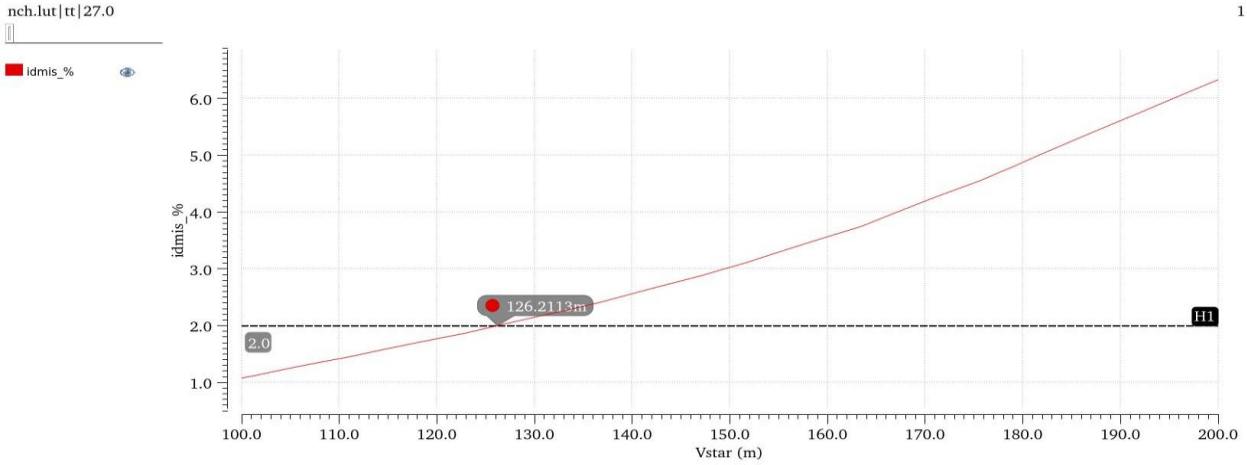


Figure 3 plot idmis vs vstar

- In my design I choose idmis = 2%, as shown in figure $V^* = 126.2113mV$.

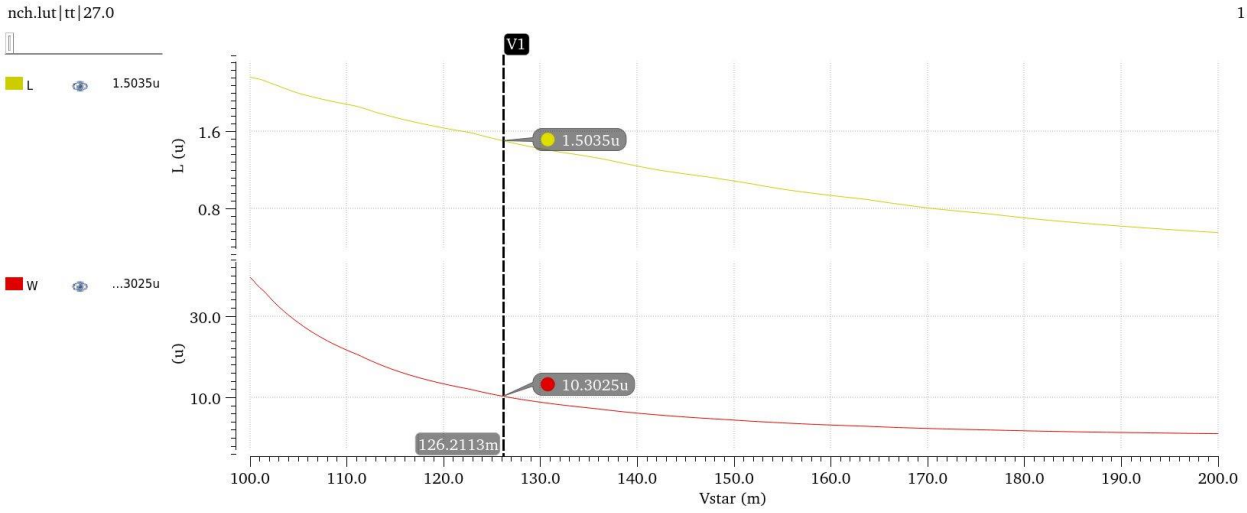


*Figure 4 get w & l at V**

• as shown in figure I get $W = 10.3025\mu m \quad L = 1.5035\mu m$.

• we can't previous design trade-offs exploration sweeps using a standard SPICE simulator, i.e., sweep Vstar at a constant, because γ has some dependence on L and Vstar so if vstar change we should change L to make γ const, but this cannot happen in simulator.

Part 2: Current Mirror Simulation

1. Design and OP (Operating Point) Analysis

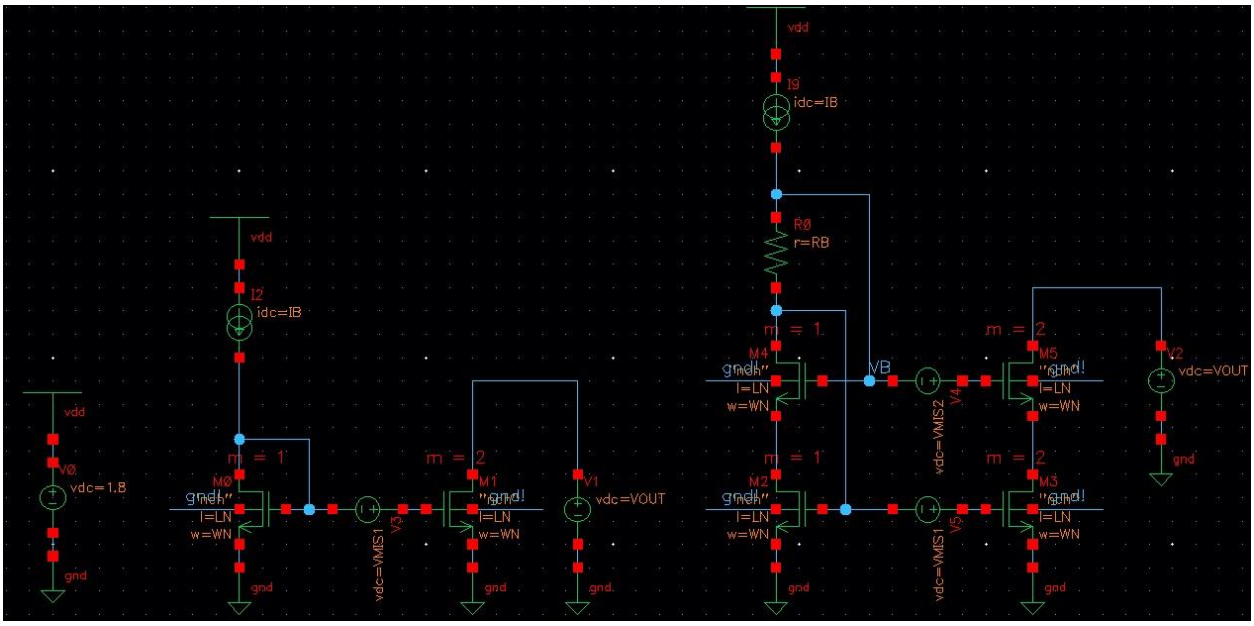


Figure 5 schematic

• $V_{DS2} \approx V_{DS3} \approx V^* + 50mV \approx 126.2113m + 50m = 176.2113mV.$

• $RB \approx \frac{\text{VDS2}}{I_B} \approx \frac{176.2113m}{10u} \approx 17.6\ K\Omega$ (range)

2) Perform DC sweep (not parametric sweep) for RB. Choose a reasonable sweep range given the rough value computed in the previous step. **Report** V_{DS3} vs R_B. **Choose** R_B to satisfy the $50mV$ saturation margin requirement. Is the selected R_B value larger or smaller than the rough analytical value? Why?

R_B value larger than the rough analytical value, because in the analytical results we ignored the body effect which causes Vth to be smaller than simulation and V_{GS} affected by Vth.

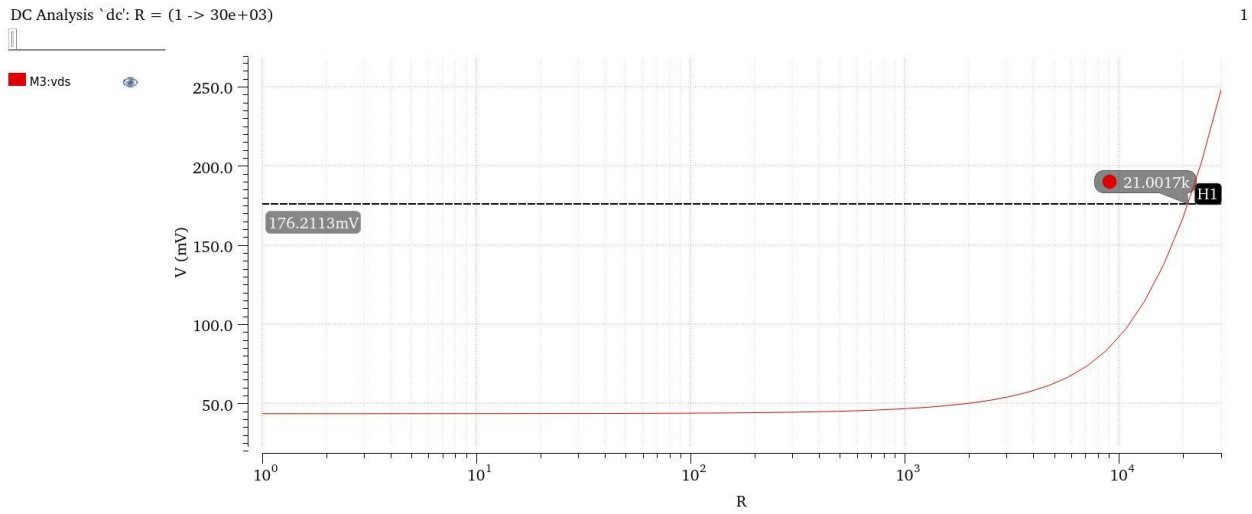


Figure 6 get value of RB

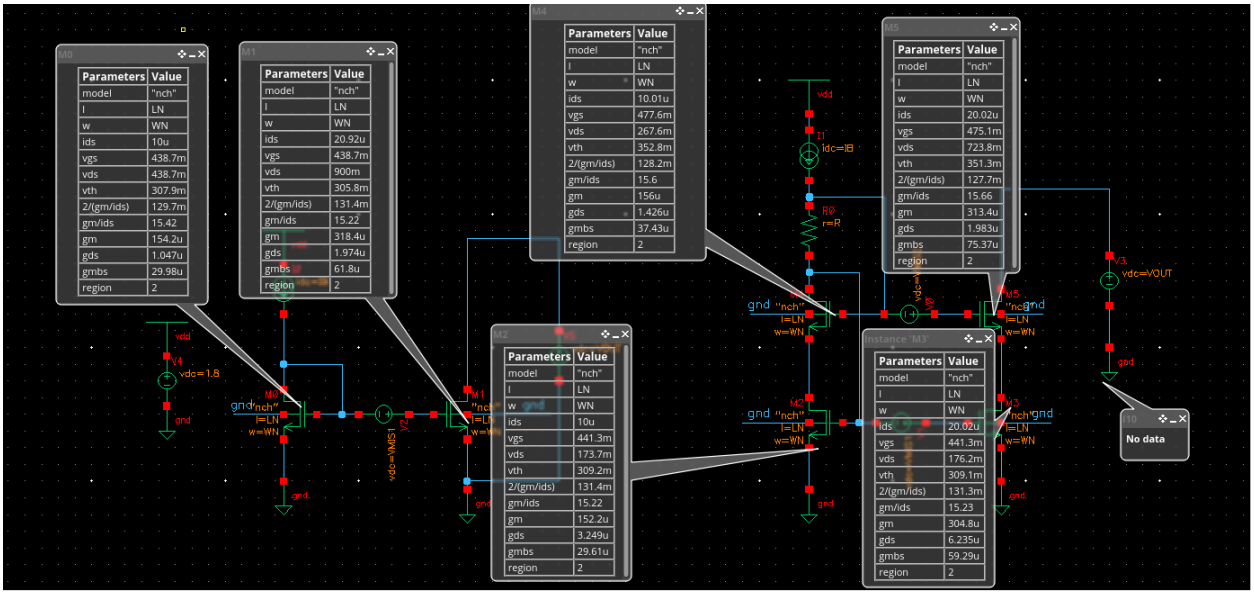


Figure 7 DC operating point

4)Do all transistors operate in saturation? Yes

2. DC Sweep (I_{out} vs VOUT)

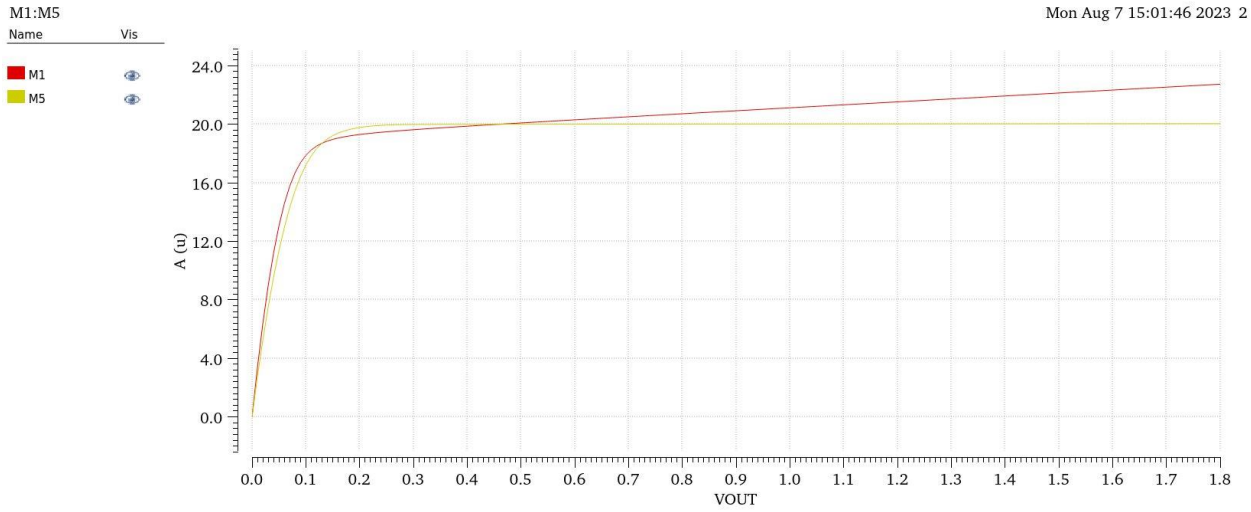


Figure 8 plot iout vs vout of two current mirrors

• As shown from previous analysis that wide sense current mirror is more stable (constant current value) with voltage variations despite simple current mirror which changed with V_{OUT} variations, in the simple mirror the current increase when $V_{OUT}(V_{DS})$ increases and exceed $2* I_B$ because V_{DS} isn't the same in M0 and M1 but in the second circuit they are the same that's why the current saturate.

• Because at this specific point, V_{DS} of the two mirror mosfets are the same so there won't be any mismatch error the mirroring will be more accurate as V_{DS} is the same and V_{GS} is the same.

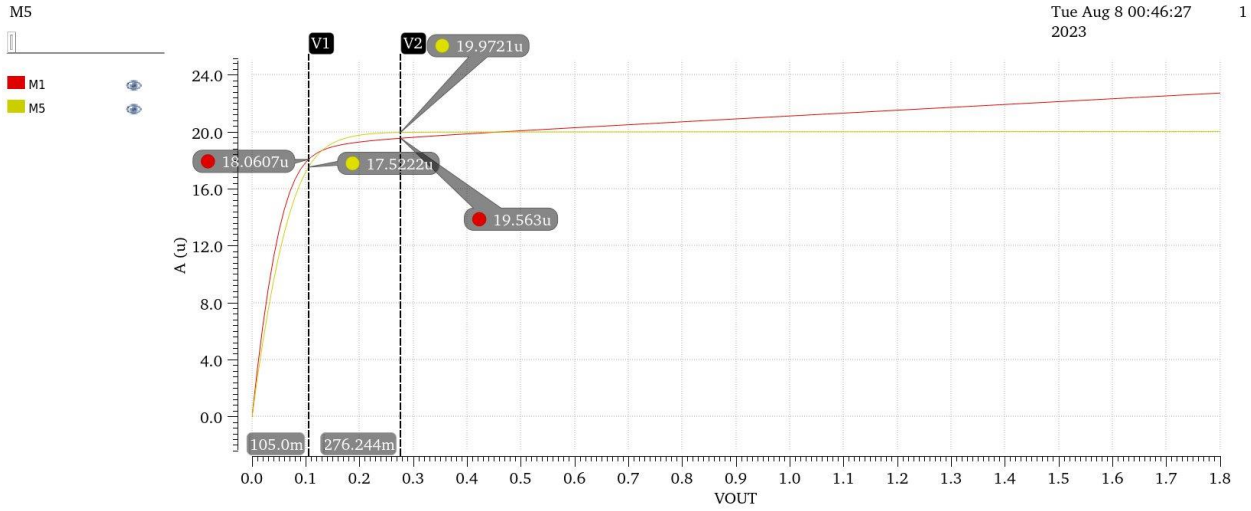


Figure 9 compliance from the plot

• as shown in figure compliance voltage of simple CM is approximately 105 mV and for wide swing CM is approximately 276.244 mV .

2)

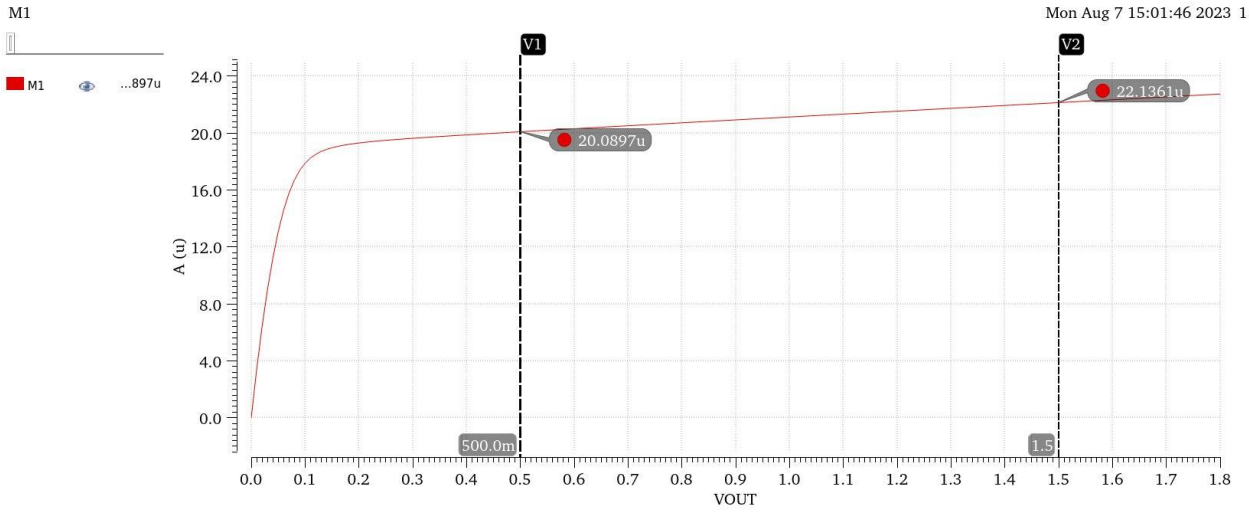


Figure 10 iout at vout equal 0.5 & 1.5

$$percentage\ change = \left(\frac{22.1361-20.0897}{20}\right) * 100 = 10\%$$

The Change in Current for $\boldsymbol{\Delta Vout}$ = $1V$ < 10% from part 1.

3)

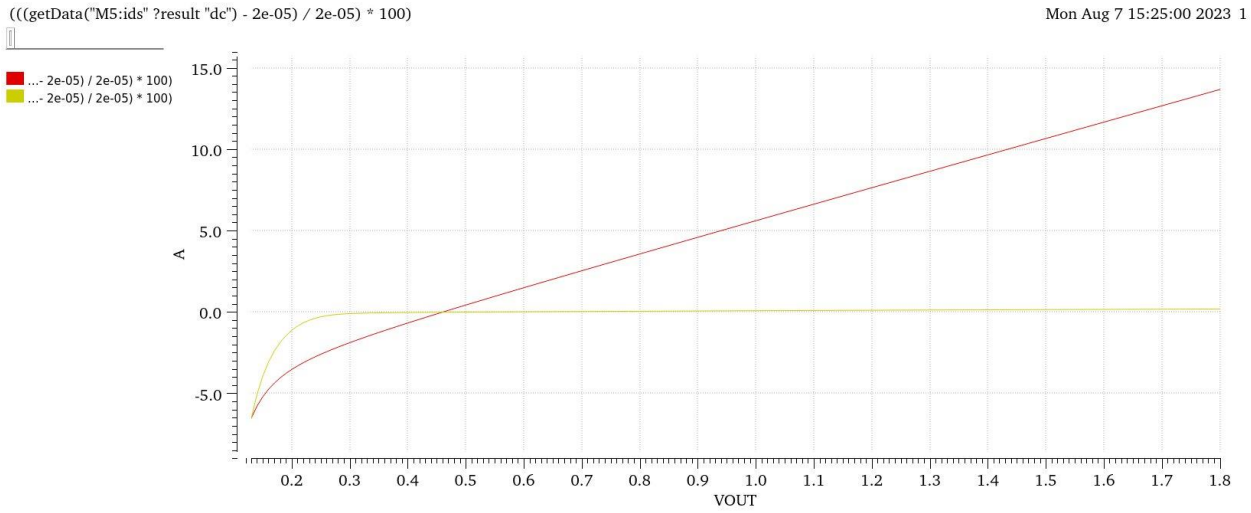


Figure 11 plot error of iout

•The wide-swing current mirror has better efficiency than the simple current mirror so the error in the wide-swing is less than the simple current mirror and the simple current mirror has lower Rout, and error of wide swing almost equal zero because the above 2 transistors make V_{DS} in the 2 transistors the same and have high output impedance.

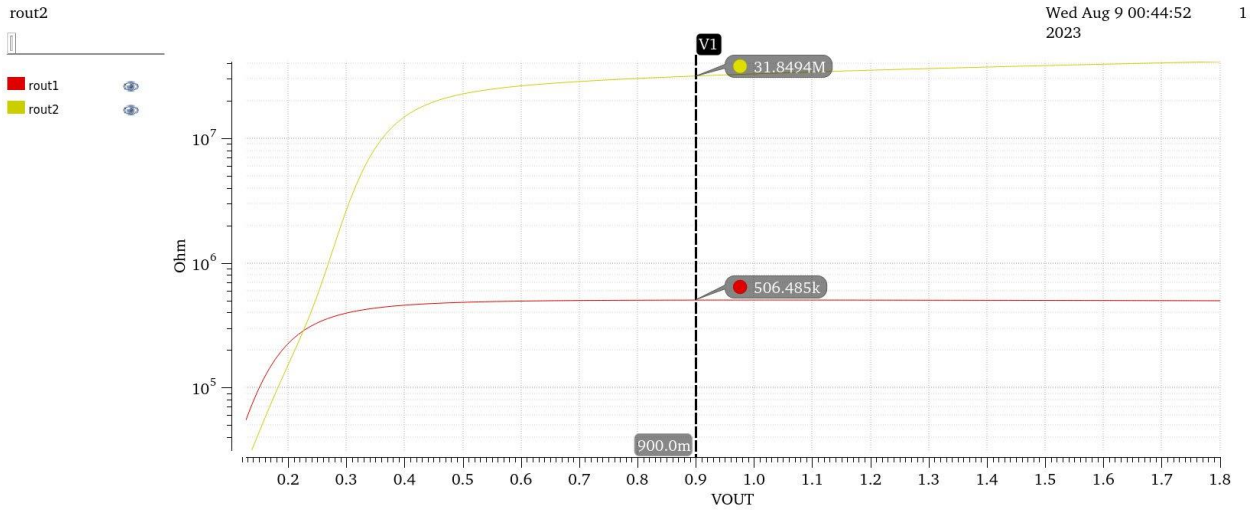


Figure 12 plot rout

• Rout of wide sense CM is more than that of simple CM because output of wide sense CM is cascaded which give high impedance while simple CM is only a single transistor, so its output impedance not boosted.

•yes, because V_{OUT} is the V_{DS} of the output mosfet so as V_{OUT} changes V_{DS} changes so the transistor either go deeper into saturation or towards the edge of saturation which will change the value of ro.

Hand analysis:

$$R_{OUT_{Simple}} = r_{o1} = \frac{1}{gds1} = \frac{1}{1.974\mu} = 506.5K\Omega$$

$$R_{OUT_{Wide}} = r_{o5}(1 + (gm5 + gmb5)r_{o3}) = 31.9M\Omega$$

	Simulator	Analytical
Simple CM	506.485KΩ	506.5KΩ
Wide swing CM	31.849MΩ	31.9MΩ

3. Mismatch

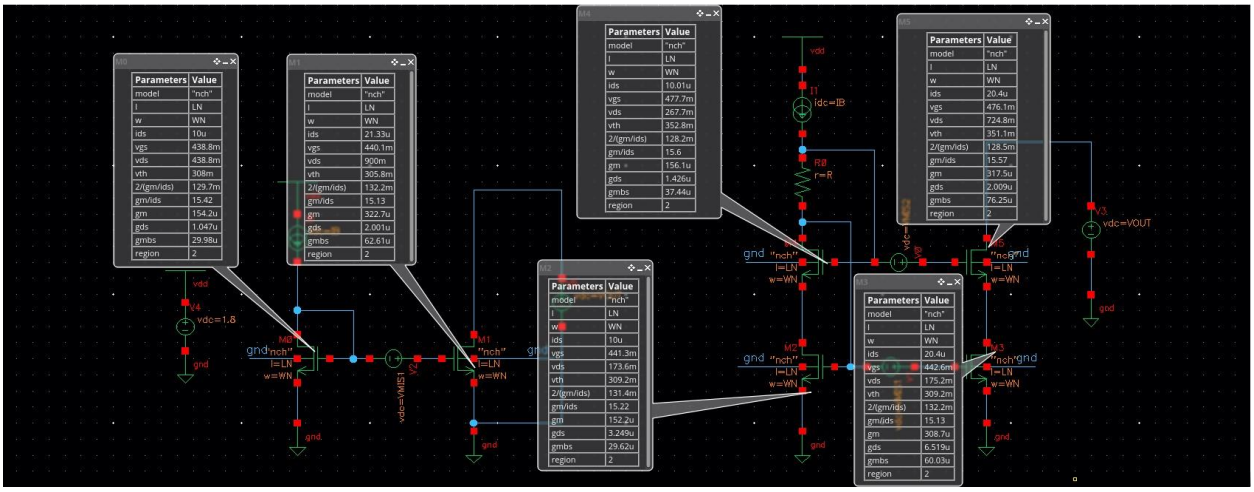
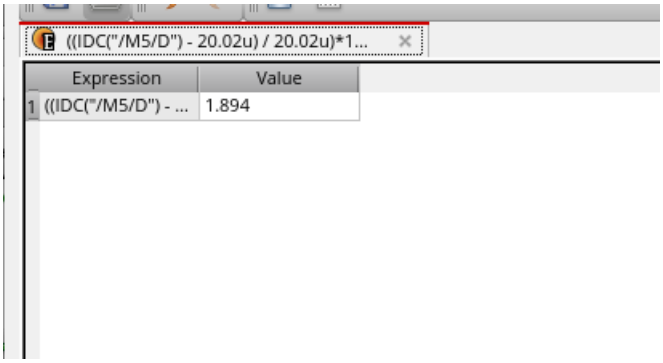


Figure 13 DC operating point at vmis1



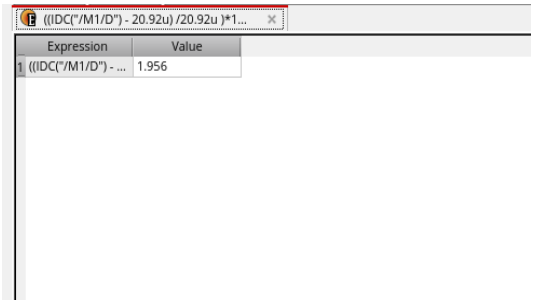


Figure 15 percentage error for simple mirror

Figure 14 percentage error from simulation for wide swing

$$\Delta I = G_M\,\Delta V = gm\,\Delta V = \frac{2\,I_D * \Delta V}{V^*}$$

$$\frac{AI}{I} = \frac{2\,\Delta V}{V^*} = \frac{2 * V_{MIS}}{V^*} * 100 = 2\%$$

	Simulator	Analytical
Percentage error wide swing	1.894%	2%
Percentage error simple	1.956%	2%

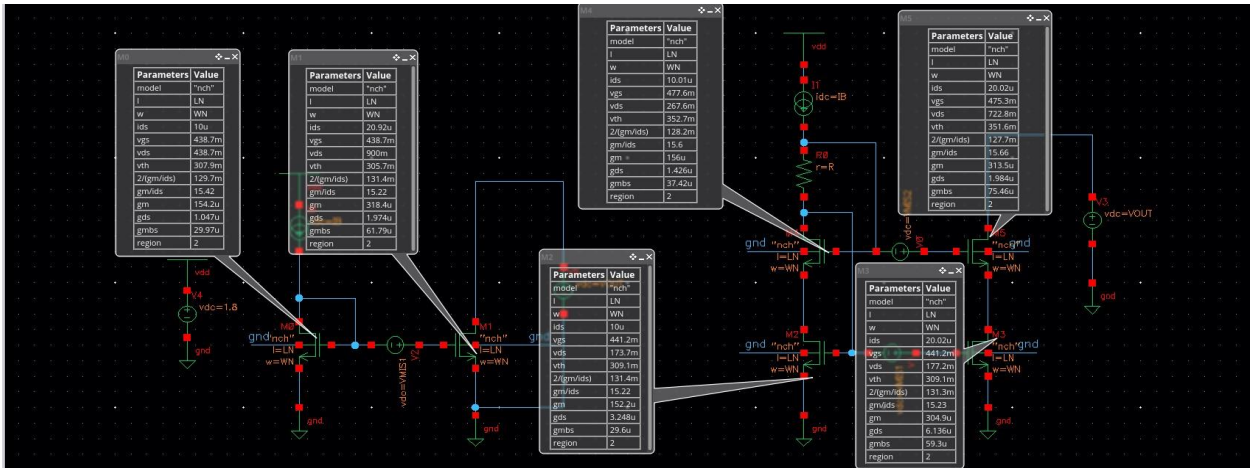


Figure 15 DC operating point at vmis2

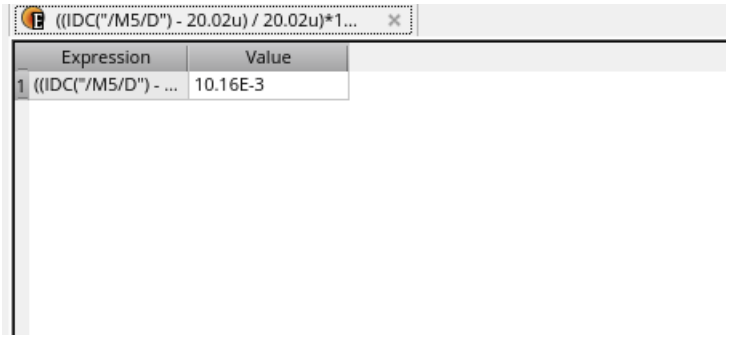


Figure 16 result of error

$$\frac{\Delta I}{I} = G_M \, \Delta V = \frac{gm5}{(1+(gm5+gmb5)r_{o3})} * \frac{V_{MIS2}}{I} * 100 = 0.03\%$$

	Simulator	Analytical
Percentage error	0.01%	0.03%

5-In simple mirror because the mismatch affects V_{GS} (strong volt), and I change directly but in the second cascode wide swing mirror the mismatch affects V_{DS} (the weakest volt).

6-For the mirror we should make it larger to increase the area and the mismatch decrease.