Analog IC Design
Lab 09 (Mini Project 01)
Two-Stage Miller OTA

PART 1: gm/ID Design Charts

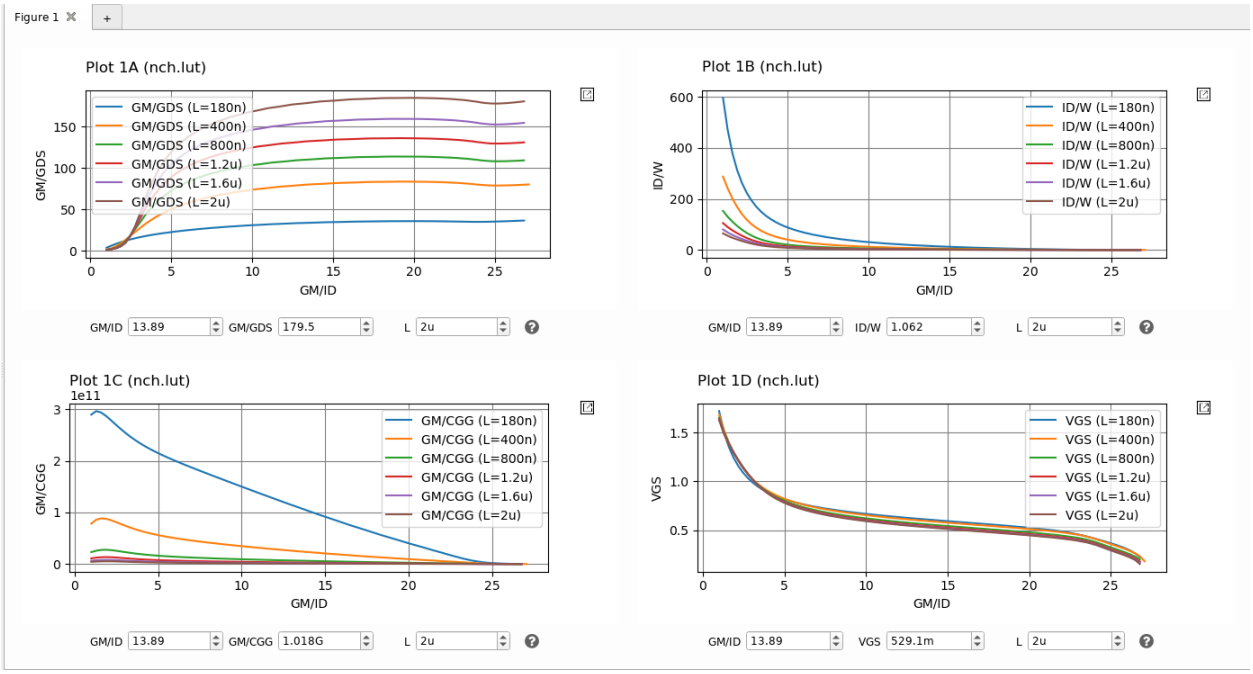


Figure 1 ADT Plots of NMOS.

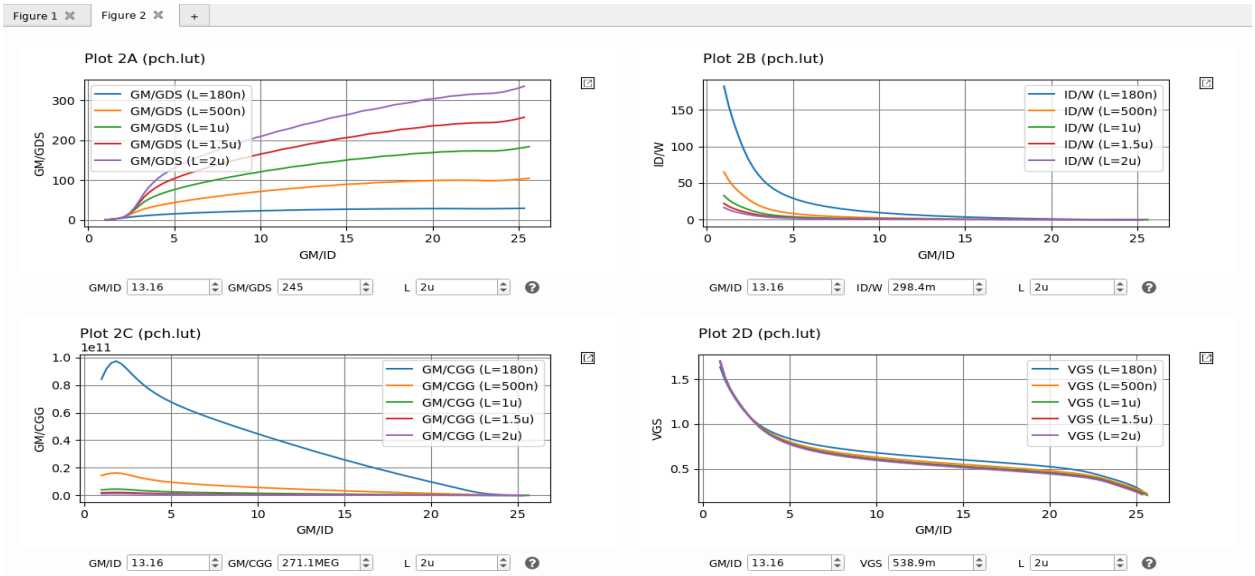


Figure 2 ADT Plots of PMOS.

PART 2: OTA Design

Technology	0.13um	0.18um
Supply voltage	**1.2V**	**1.8V**
Static gain error	**<= 0.05%**	**<= 0.05%**
CMRR @ DC	**>= 74dB**	**>= 74dB**
Phase margin (avoid pole-zero doublets)	>= 70°	>= 70°
OTA current consumption	**<= 60uA**	**<= 60uA**
CMIR – high	**>= 0.6V**	**>= 1V**
CMIR – low	**<= 0.2V**	**<= 0.2V**
Output swing	**0.2 – 1V**	**0.2 – 1.6V**
Load	5pF	5pF
Buffer closed loop rise time (10% to 90%)	**<= 70ns**	**<= 70ns**
Slew rate (SR)	$5V/\mu s$	$5V/\mu s$

1-Detailed design procedure and hand analysis. Justify why you used NMOS or PMOS input pair for each stage.

Since that the CMIR is closer to the ground rail, therefore I will use a PMOS input stage for the first stage.

Since I used a PMOS input stage for the first stage, the bias current will be a sourcing current source from upwards. Note that this bias current will also be biasing the second stage. So, the second stage input transistor will be a NMOS transistor to give me a common source stage and amplify the gain.

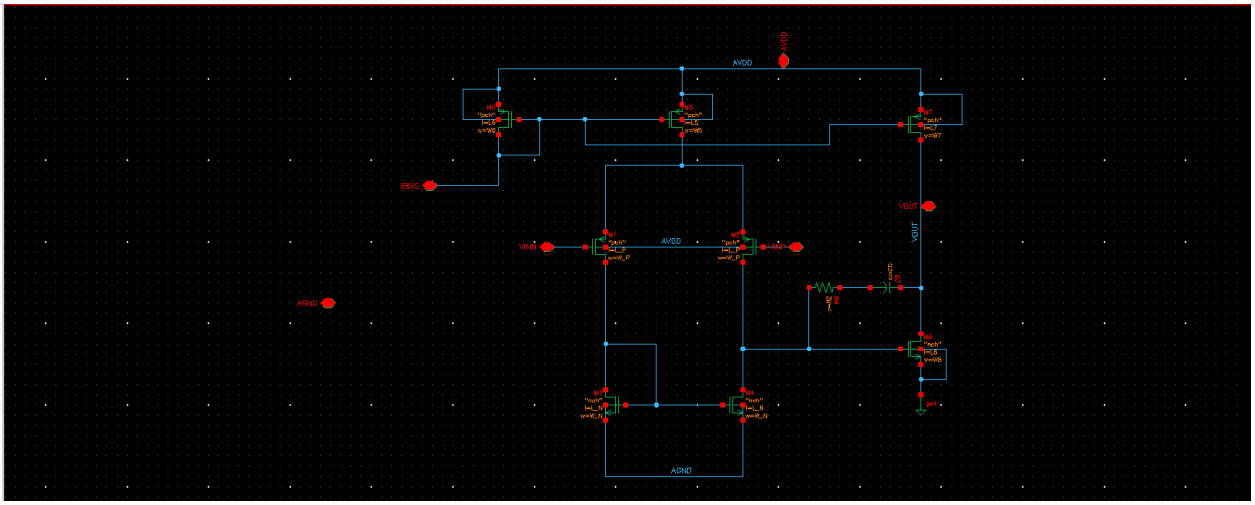


Figure 3 Schematic.

Design procedure:

1) Use a single 10uA DC current source and a single DC voltage source in your test bench. Design your own current mirrors and bias circuitry.

Here I will use a dc ideal current source then mirror the current for the first stage and the second stage with different widths for the mirror MOSFETS.

2)A reasonable starting point for C_C is $0.5C_L$. You may refine this choice by doing sweeps in simulation.

$$C_c = 0.5 * C_L = 2.5\ \text{pF}$$

3)Calculate the unity gain frequency (UGF) from the rise time requirement (t_{rise}=2.2τ). Hence, calculate $g_{m1,2}$.

$$t_{rise\ cl} = 2.2 * \tau_{CL} \leq 70ns \ \rightarrow\ \tau_{CL} \leq \frac{70n}{2.2} \rightarrow\ \tau_{CL} \leq 31.82ns$$

$$UGF = \frac{1}{\tau_{CL}}\ \ so\ UGF \geq 31.43M\ {}^{rad}/_{S}\ , i\ have\ C_C = 2.5PF$$

$$UGF = \frac{gm_{1,2}}{C_C}\ \ so\ gm_{1.2} \geq 78.57\mu S$$

4)From the SR requirement, calculate the current required in the first stage (I_{B1}):

SR=$I_{B1}C_C$. Given the total current budget, calculate the current of the second stage.

$$\boldsymbol{SR = \frac{I_{B1}}{C_C}\ \ \rightarrow\ \ I_{B1} = 12.5\mu A}$$

$$so\ I_{B2} = I_{Btotal} - I_{B1} = 60\mu - 12.5\mu = 47.5\mu A$$

5)**Calculate gm/ID of the first stage.**

$$\left(\frac{gm}{I_D}\right)_{1,2} \geq \frac{78.57\mu}{\frac{12.5}{2}} \geq 12.57$$

I will take $\left(\frac{gm}{I_D}\right)_{1,2} = 13.5\ so\ gm_{1,2} = 84.375\mu S.$

6)Show that the closed-loop gain for a buffer is $AvCL \approx 1 - 1\ AvOL$, where $AvOL$ is the open-loop gain. Given $AvCL$ gain error spec ($\%error$ = $|\ actual{-}ideal\ ideal\ |$ × 100), calculate the required DC gain in dB.

$$i\ have\ \varepsilon_s = \frac{1}{\beta A_{OL}} \leq 0.05\% \ \rightarrow\ A_{OL} \geq 2000(66.02dB)$$

7)Assign larger gain for the first stage (why?). Do not split the gain equally between the two stages. You may assume the first stage gain is twice that of the second stage (6dB difference).

$$A_{ol} = Gain_1 * Gain_2$$

$let\ Gain_1 = 2 * Gain_2$, because we design 1st stage for gain and 2nd stage for swing.

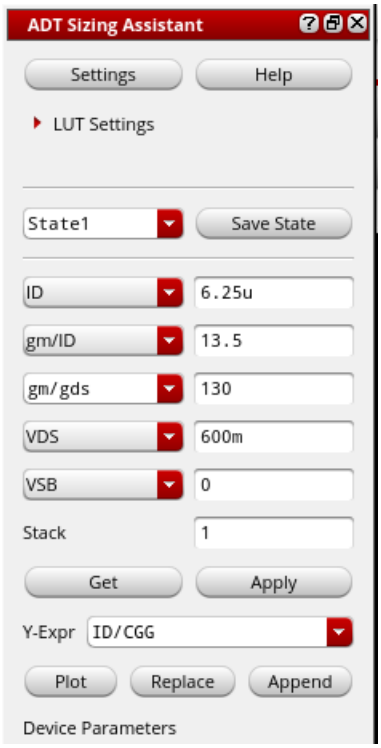
$so\ A_{v1} \geq 63.24 \quad and\ A_{v2} \geq 31.62$.

8)Given the 1st stage gain, calculate L (channel length) of the 1st stage input. You may assume input and load have the same gds.

$$\boldsymbol{A_{v1} = \frac{gm_{1,2} * r_{o1,2}}{2} \geq 63.24\ so\ \frac{gm_{1,2}}{gds_{1,2}} \geq 126.48\ \ will\ take\ it\ equal\ 130}$$

$$\boldsymbol{gds_{1.2}} = 650\ \mathrm{n}S$$

Using sizing assistant to get parameters.



#	Parameter	Value
1	ID	6.25u
2	L	890n
3	W	9.48u
4	VGS	553.5m
5	VDS	600m
6	VSB	0
7	gm/ID	13.35
8	Vstar	149.8m
9	fT	204.4M
10	gm/gds	129.7
11	VA	9.715
12	ID/W	659.3m
13	gm/W	8.804
14	AREA	8.437p
15	gm	83.46u
16	gmb	25.65u
17	gds	643.4n
18	ro	1.554M
19	VTH	413.2m
20	VDSAT	119m

$L_{1,2} = 890nm$

$W_{1,2} = 9.48\mu m$

$V_{GS} = 553.5mV$

$V_{DSAT} = 119mV$

Figure 4 Sizing M1.2

9)Given gds/ID of the first stage current mirror load, select L. Note that gds/ID slightly increases with gm/ID, which is not known yet. To get an estimate for L, you may ignore this dependence and assume a relatively large gm/ID for the load at this point (e.g., gm/ID = 15).

$$\boldsymbol{assume\ \left(\frac{gm}{I_d}\right)_{3,4} = 15\ ,i\ have\ branch\ current\ equal = \frac{12.5}{2} = 6.25\mu A}$$

$$\boldsymbol{so\ \ gm_{3,4} = 93.75\mu S\ \ \rightarrow \frac{gm_{3,4}}{gds_{3,4}} = 130}$$

I will take some margin in gain to be 140, using sizing assistant.

After using sizing assistant that generates $L_{3,4} = 1.3\mu m$.

10)Given the PM spec, calculate gm/ID of the second stage input transistor (Hint: assume $\omega_{p2}=4\omega_u$).

$$PM \geq 70 \; and \; UGF(W_u) \geq 31.43M \, {}^{rad}/_{S}$$

$$W_{P2} = 4 * W_u = 125.72M \, {}^{rad}/_{S}$$

$$\frac{gm_8}{CL} = 4 * \frac{gm_{1,2}}{C_C} \rightarrow \frac{gm_8}{gm_{1,2}} = 8 \rightarrow gm_8 = 8 * 84.375 = 675\mu S$$

$$\left(\frac{gm}{I_D}\right)_8 \geq 14.21 \quad .$$

11)Given the CMIR-high and Swing-high specs, calculate max vdsat for tail current source and output load. Take the lower value and assume V*= vdsat. Note that always V* > vdsat; thus, this assumption already adds some margin to make sure they are driven a little more into saturation. Now you have gm/ID of these two transistors. Note that these two transistors are identical (they form a current mirror; thus, they have same L and same gm/ID) except for the current (and width).

$$CMIR_{High} = VDD - V_{GS1} - V_{DSAT5} \geq 1V$$

$$V_{DSAT5} \leq 246.5mV$$

$$SWING_{High} = VDD - V_{DSAT7} = 1.6V \rightarrow V_{DSAT7} \leq 200mV$$

I will take the lower value which will satisfy both conditions which is V*=200 mV.

$$\left(\frac{gm}{I_D}\right)_{5.6.7} = \frac{2}{V^*} = 10$$

12)Use the CMRR spec to find gds of the tail current source (note that the second stage does not affect the CMRR). However, to complete this step you need gm of the current mirror load. This is not known yet, because we want VGS of 1st stage load = VGS of 2nd stage input. To break this deadlock, assume a relatively low gm/ID (e.g., gm/ID = 10) for first stage current mirror load1. Thus, get gds of tail current source.

$$CMRR = \frac{A_{vd}}{A_{vcm}} \geq 74dB \; so \; A_{vcm} \leq 12.62m$$

Assume $\left(\frac{gm}{I_D}\right)_{3,4} = 10 \rightarrow gm_{3,4} = 62.5\mu S$

$$A_{vcm}=\frac{1}{2*gm_{3,4}*r_{o5}} \leq 12.62m \rightarrow r_{o5} \leq 633K \; i \; will \; take \; it \; 500K$$

13)Tail current source and 2nd stage load must have the same L (they form a current mirror). Thus, get gds of the 2nd stage load (note that both gm and gds are proportional to ID).

$$i \; have \left(\frac{gm}{I_D}\right)_{5.6.7}$$

So $gm_5 = 125\mu S \quad and\ gm_6 = 100\mu S \quad and\ gm_7 = 475\mu S$

$gds6$ = 1.2584 uS $gds7$ = 5.9774 uS

I have $r_{o5} = 500K\Omega, using\ sizing\ assistant\ to\ get\ parameters.$

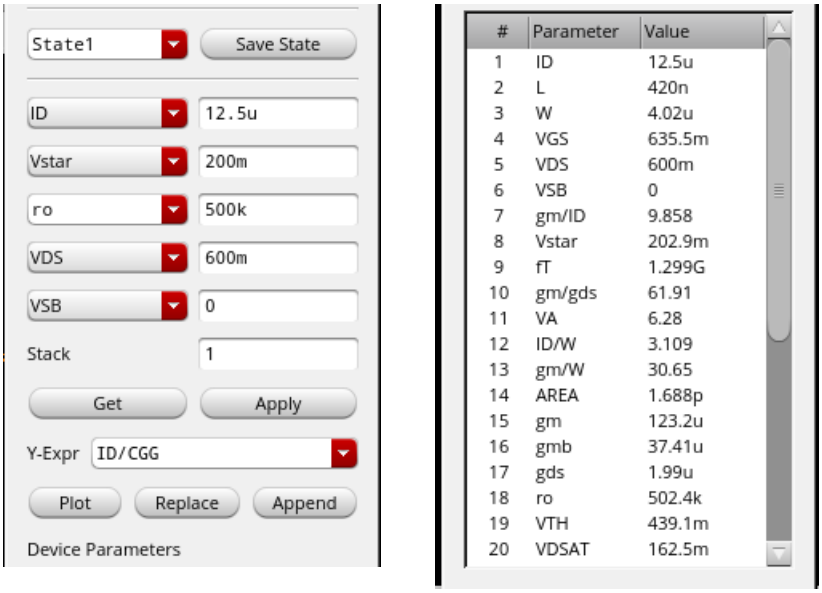


Figure 5 sizing M5

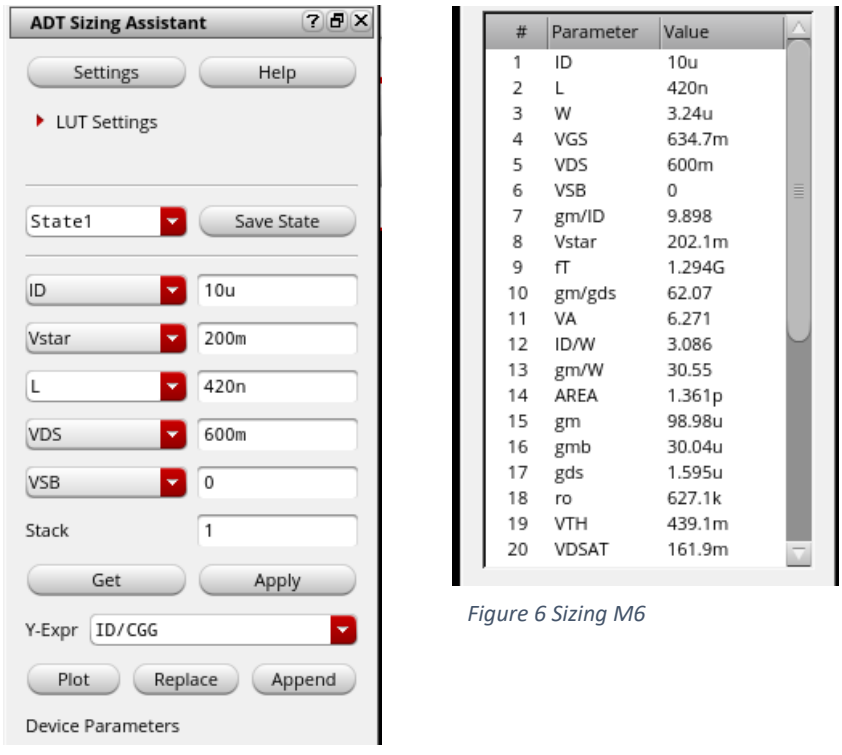
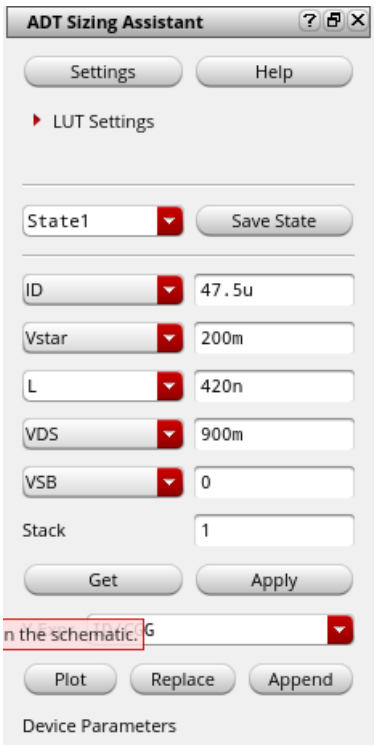


Figure 6 Sizing M6



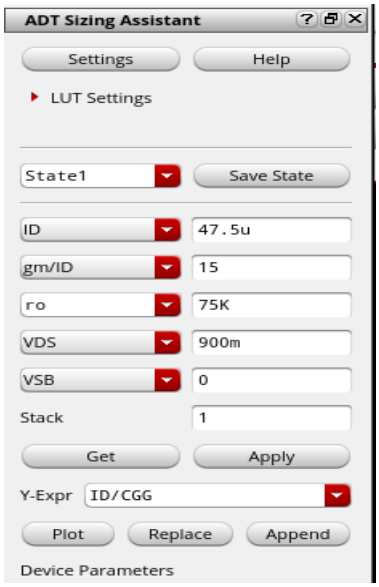
#	Parameter	Value
1	ID	47.5u
2	L	420n
3	W	15.01u
4	VGS	632.7m
5	VDS	900m
6	VSB	0
7	gm/ID	9.906
8	Vstar	201.9m
9	fT	1.326G
10	gm/gds	72.98
11	VA	7.368
12	ID/W	3.165
13	gm/W	31.35
14	AREA	6.304p
15	gm	470.5u
16	gmb	142.8u
17	gds	6.447u
18	ro	155.1k
19	VTH	439m
20	VDSAT	160.5m

Figure 7 Sizing M7

14)Given the 2nd stage gain, calculate gds and L of the 2nd stage input transistor. This transistor is now fully specified; thus, calculate its VGS.

$$Gain_2 = gm_8 * (r_{o7}||r_{o8}) = \frac{gm_8}{gds_7+gds_8}\ i\ have\ gm_8 = 675\mu S\ , gds_7 = 6.44\mu S$$

$r_{o8} \approx 75K\Omega$.



#	Parameter	Value
1	ID	47.5u
2	L	240n
3	W	5.23u
4	VGS	590.1m
5	VDS	900m
6	VSB	0
7	gm/ID	14.61
8	Vstar	136.9m
9	fT	9.026G
10	gm/gds	51.88
11	VA	3.551
12	ID/W	9.082
13	gm/W	132.7
14	AREA	1.255p
15	gm	693.9u
16	gmb	171.3u
17	gds	13.38u
18	ro	74.76k
19	VTH	471m
20	VDSAT	101.8m

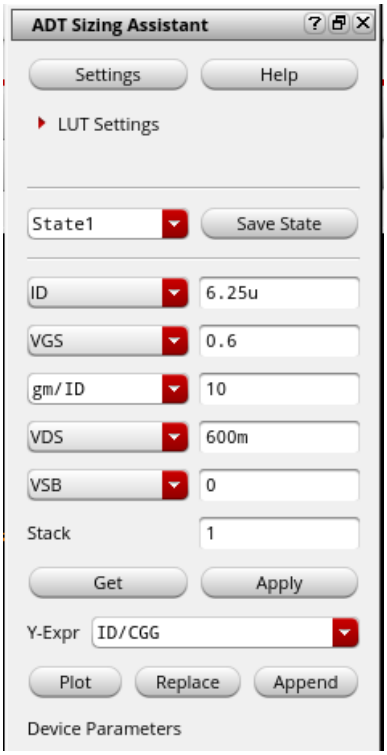
Figure 8 Sizing M8

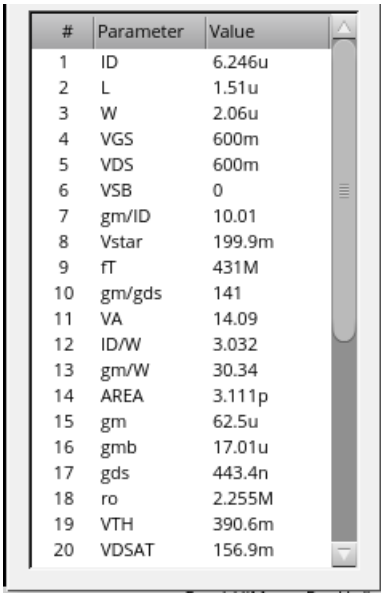
15)**Note that you need to avoid systematic offset. Use VGS charts to guarantee that 1st stage current mirror load and 2nd stage input transistor have the same VGS. Use this condition to determine the gm/ID of the current mirror load in the first stage. Check that the calculated gm/ID is larger than the one you assumed before (to guarantee that the CMRR is satisfied). Otherwise, re-iterate with the new gm/ID value (if the difference is large). If this step is not done properly, you will find that VOUT goes towards VDD or GND and one of the output transistors is out of saturation. In order to make sure that the systematic offset is cancelled, you can sweep the width of the current mirror load with fine step till VOUT is around VDD/2.**

$$\boldsymbol{gds_{3,4}} = 650\text{n}S$$

And I have $V_{GS3,4} = 590.1mV \approx 600mV$ *and current equal to* $6.25\mu A$

By using sizing assistant to get parameters.





#	Parameter	Value
1	ID	6.246u
2	L	1.51u
3	W	2.06u
4	VGS	600m
5	VDS	600m
6	VSB	0
7	gm/ID	10.01
8	Vstar	199.9m
9	fT	431M
10	gm/gds	141
11	VA	14.09
12	ID/W	3.032
13	gm/W	30.34
14	AREA	3.111p
15	gm	62.5u
16	gmb	17.01u
17	gds	443.4n
18	ro	2.255M
19	VTH	390.6m
20	VDSAT	156.9m

Figure 9 Sizing M3,4

16)Verify that your gm/ID choices do not violate the CMIR and the peak-to-peak output swing

$$\boldsymbol{CMIR_{LOW} = -V_{GS1} + V_{DSAT1} + V_{GS3} = 153.6mV < 200mV}$$

$$CMIR_{HIGH} = VDD - V_{GS1} - V_{DSAT5} = 1.1 > 1V$$

17)Choose Rz **to place the zero at infinity (some designers may move the LHP zero to the vicinity of the non-dominant pole to improve the PM). Do NOT place the LHP zero at a frequency less thanwp2.**

$$\boldsymbol{RZ = \frac{1}{gm_8} = 1.44K\Omega}$$

	$M_{1,2}$	$M_{3,4}$	M_5	M_6	M_7	M_8
Width	9.48μ	2.06μ	4.02μ	3.24μ	15.01μ	5.23μ
Length	$890n$	1.51μ	$420n$	$420n$	$420n$	$240n$
gm	84.375μ	62.5μ	125μ	100μ	470.5μ	693.9μ
I_D	6.25μ	6.25μ	12.5μ	10μ	47.5μ	47.5μ
gm/I_D	13.5	10	10	10	10	14.61
V_{DSAT}	119m	$156.9m$	$162.5m$	$161.9m$	$160.5m$	$101.8m$
V_{OV}	140.3m	$209.4m$	$196.4m$	$195.6m$	$193.7m$	$119.1m$
V^*	149.8m	$199.9m$	$202.9m$	$202.1m$	$201.9m$	$136.9m$

PART 3: Open-Loop OTA Simulation

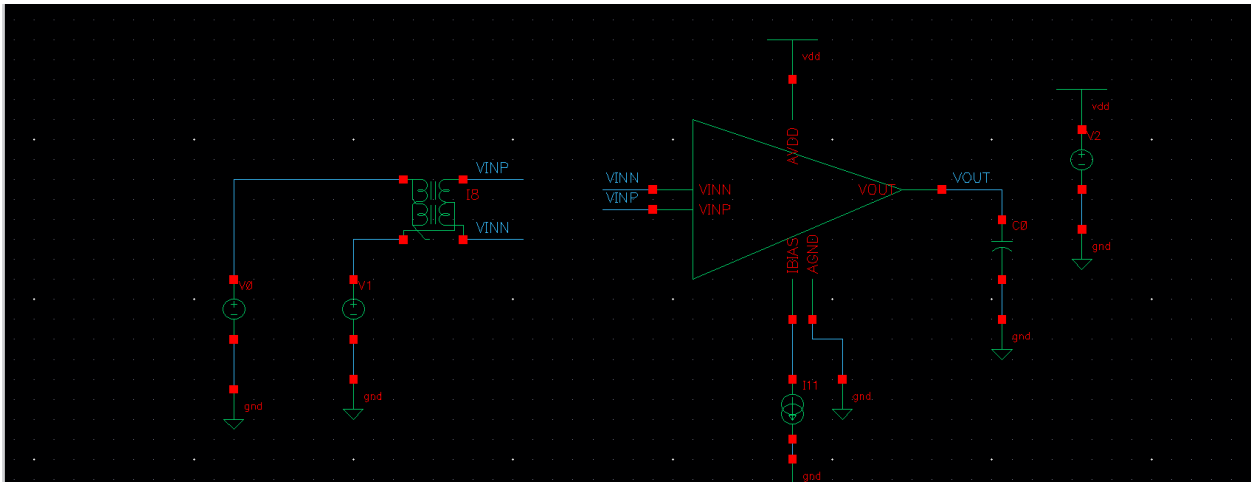


Figure 10 schematic Testbench.

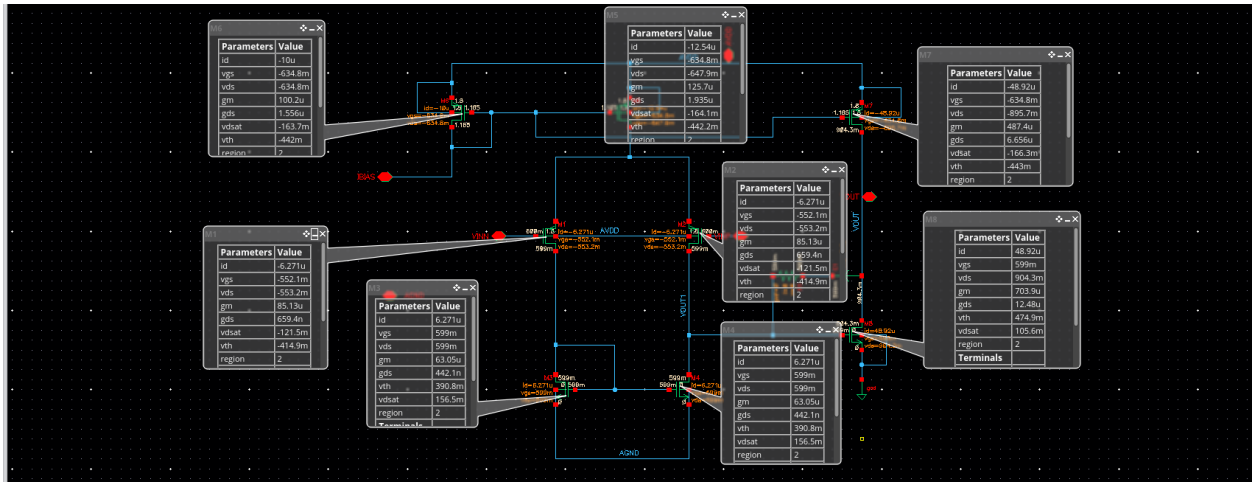


Figure 11 DC operating point.

• Is the current (and gm) in the input pair exactly equal? Yes.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
lab9_OTA_Open...	VDC("/I9/VOUT1")	599m			
lab9_OTA_Open...	VDC("/VOUT")	904.3m			

Figure 12 DC Voltages.

• What is DC voltage at the output of the first stage? Why?

$599mV$,because Dc voltage at output of 1st stage equals V_{GS} of current mirror load and Vgs of 2nd stage NMOS, and they must equal each other to avoid systematic offset and keep all MOSFETs in saturation.

• What is DC voltage at the output of the second stage? Why?

Dc voltage at output of 2nd stage equals V_{DS} of input NMOS which is $904.3mV$, this due to voltage drop on current mirror PMOS as shown in schematic which equal VDD-V_{DS}=1.8-895.7=$904.3mV$.

Diff small signal ccs:

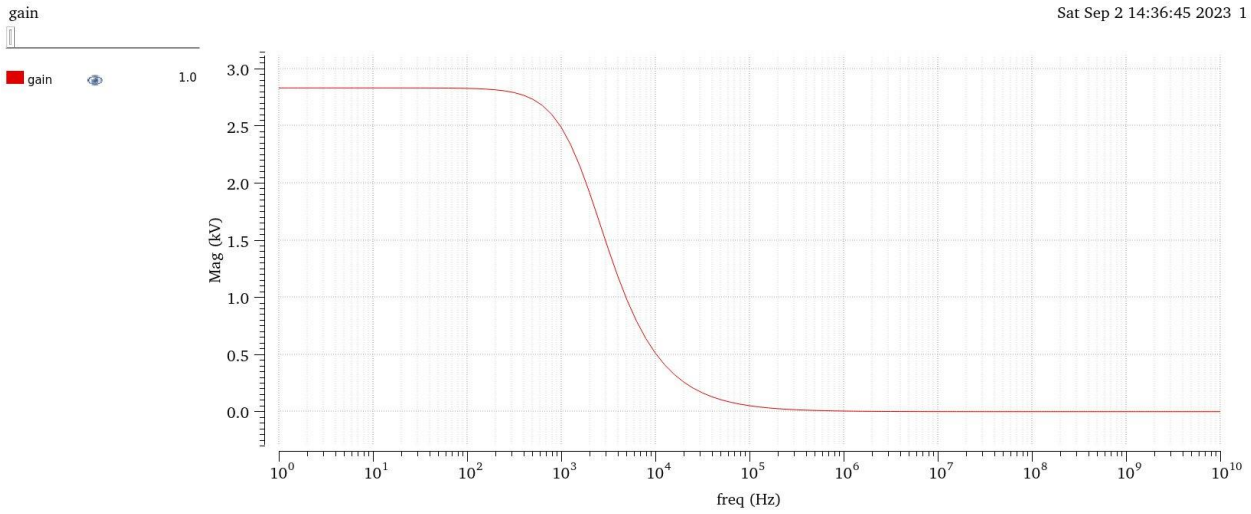


Figure 13 VOUT vs frequency.

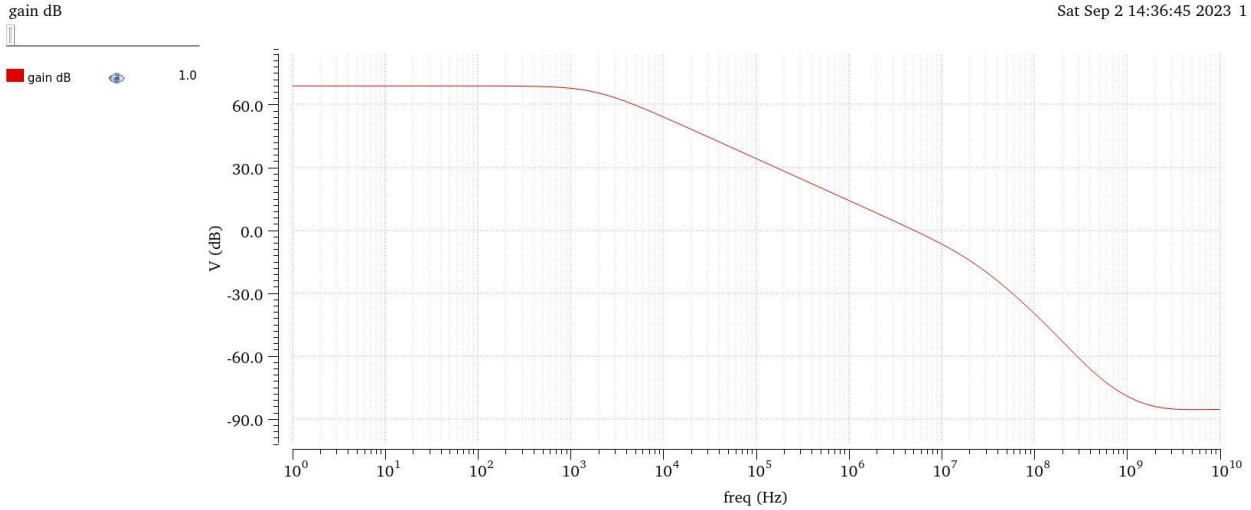


Figure 14 VOUT vs frequency in dB.

Outputs Setup | Results

Detail | Filter ... | Replace | (None)

7 rows

Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
lab9_OTA_Open...	gain				
lab9_OTA_Open...	gain dB				
lab9_OTA_Open...	DC gain	2.833K			
lab9_OTA_Open...	DC gain dB	69.05			
lab9_OTA_Open...	bandwidth	1.838K			
lab9_OTA_Open...	UGF	5.092M			
lab9_OTA_Open...	GBW	5.22M			

Figure 15 Results from simulator.

Hand analysis:

$$A_v = gain_1 * gain_2 = \frac{gm_1}{gds_2+gds_4} * \frac{gm_8}{gds_7+gds_8} = \frac{85.13\mu}{659.4n+442.1n} * \frac{703.9\mu}{6.656\mu+12.48\mu} =$$

$$77.29 * 36.78 = 2.843K = 69.076dB$$

$$BW = \frac{1}{2*\pi*ROUT_1*GM_2*ROUT_2*C_C} \approx 1.907KHZ.$$

$$GBW = BW * A_v = 1.907K * 2.843K = 5.42MHZ.$$

	Simulation	Hand analysis
Gain	2.833K	2.843K
Gain dB	69.05	69.07
Bandwidth	1.838K	1.907K
GBW	5.22M	5.42M
UGF	5.092M	5.42M

CM small signal ccs:

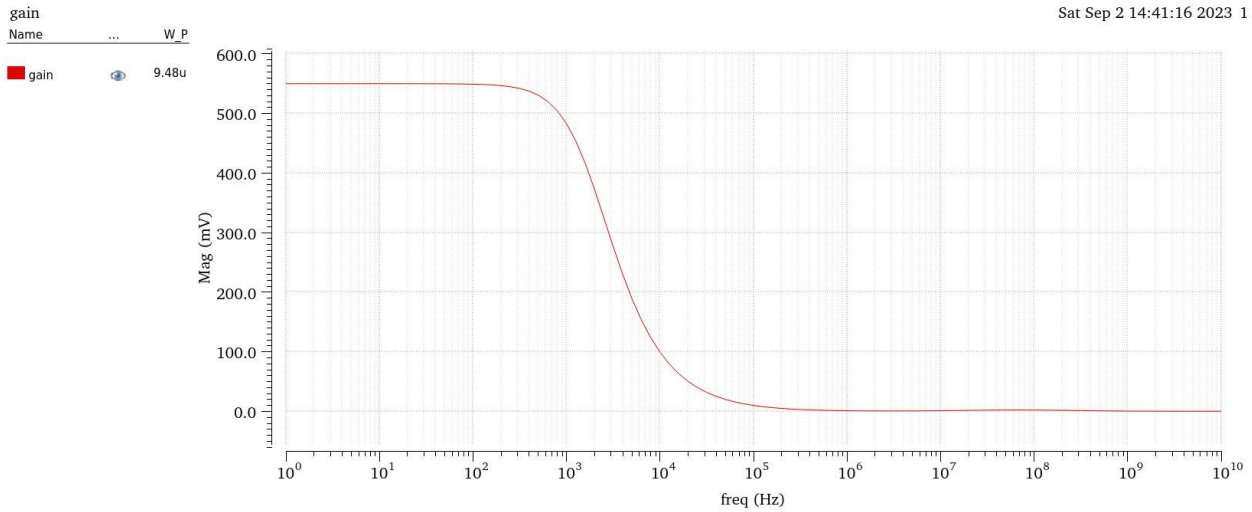


Figure 16 Plot Vout vs frequency Common mode.

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab9_OTA_Open...	gain				
lab9_OTA_Open...	gain dB				
lab9_OTA_Open...	DC gain	550m			
lab9_OTA_Open...	DC gain dB	-5.192			
lab9_OTA_Open...	bandwidth	1.838K			
lab9_OTA_Open...	GBW	1.013K			

Figure 17 Results from simulator.

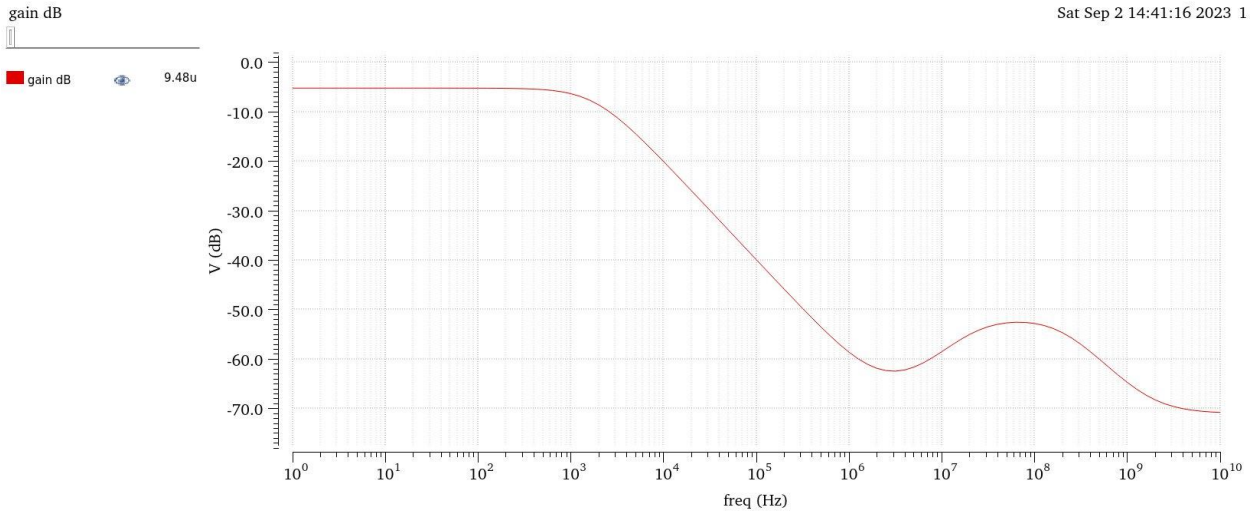


Figure 18 Plot VOUT vs frequency in dB.

Hand analysis:

$$A_{vCM1} = \frac{1}{2*gm_{3,4}*r_{o5}} = \frac{1}{2*63.05\mu*\frac{1}{1.935\mu}} = 15.345m$$

$$A_{vCM\_total} = A_{vCM1} * GM_2 * ROUT_2 = 15.345m * \frac{703.9\mu}{6.656\mu+12.48\mu} = 564m = -4.968dB.$$

	Simulation	Hand analysis
Gain	550m	564m
Gain dB	-5.192	-4.968

(Optional) CMRR:

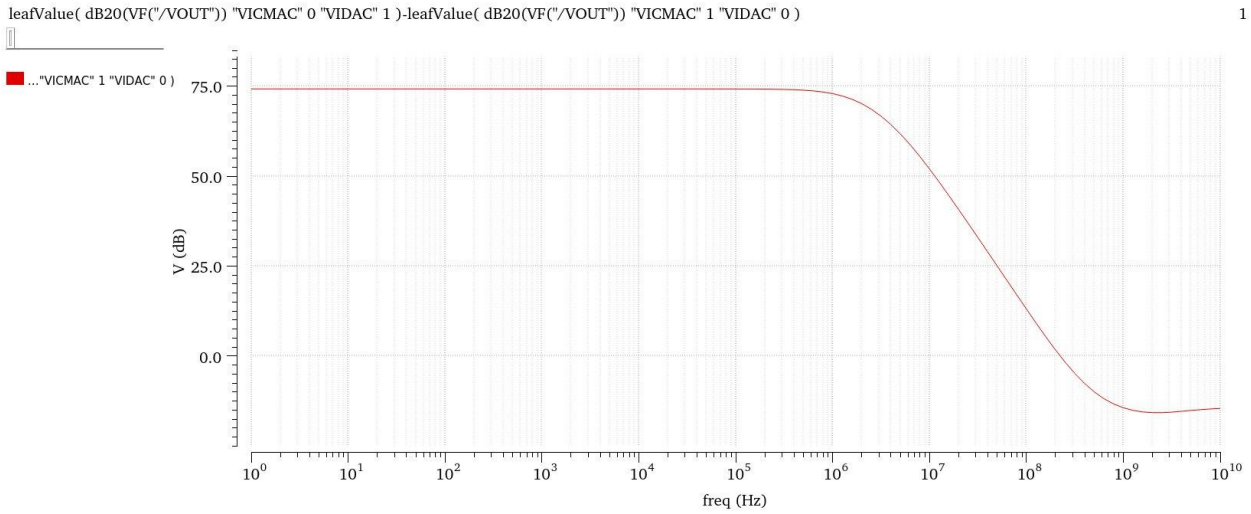


Figure 19 Plot CMRR.

Hand analysis:

$$CMRR = \frac{A_{vd}}{A_{vcm}} = 69.07dB + 4.968 = 74.04dB$$

	Simulation	Hand analysis
CMRR dB	74.242	74.04

(Optional) Diff large signal ccs:

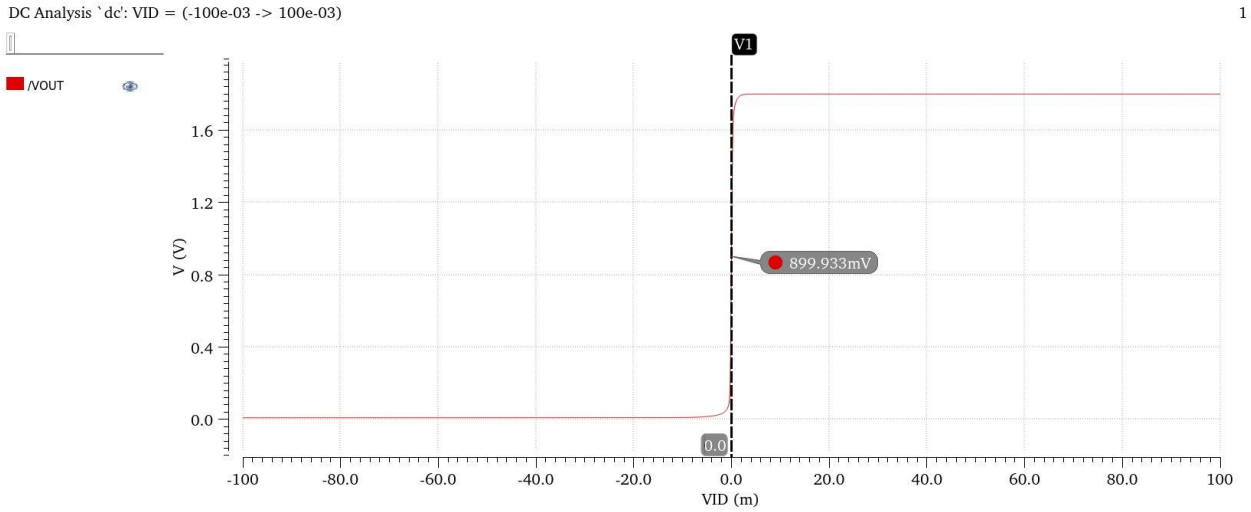


Figure 20 Plot VOUT VS VID.

From the plot $V_{OUT} = 899.933mV\ in\ DC\ operating\ point\ V_{OUT} = 903.4mV$

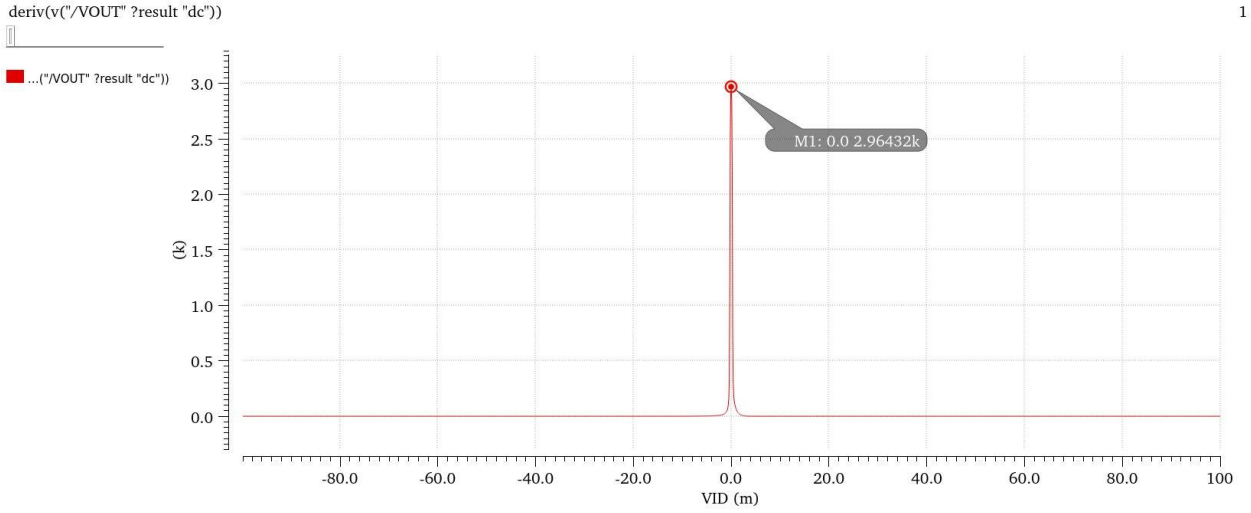


Figure 21 Plot derivative of VOUT vs VID.

	Derivative	A_{vd}
Peak	2.964K	2.833K

Comment:

The value of the derivative of the output signal at its peak is almost equal to the gain in dB.

CM large signal ccs (region vs VICM):

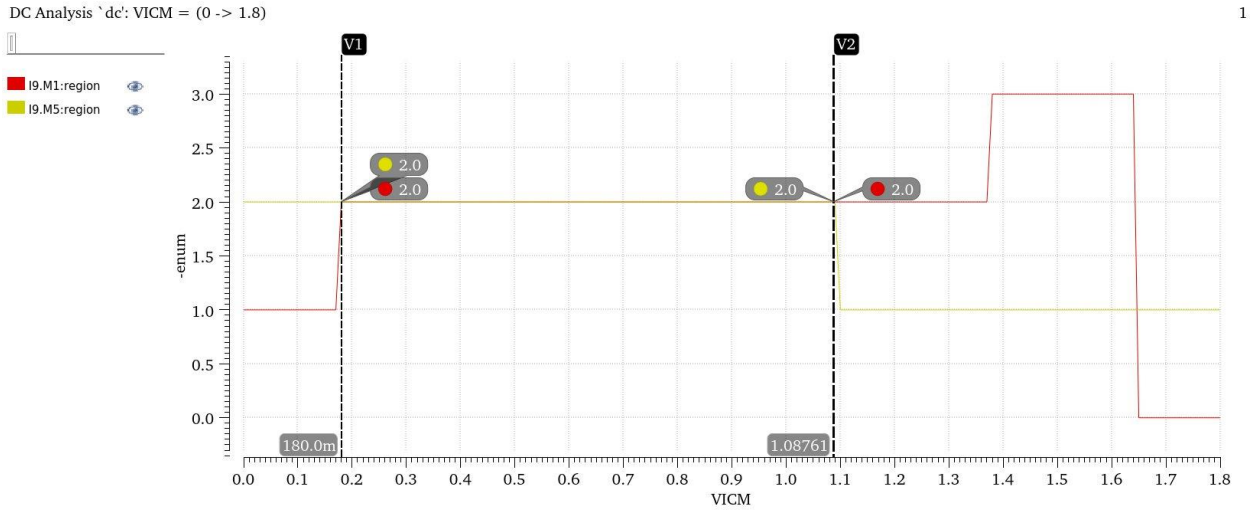


Figure 22 Plot regions vs VINCM.

Hand analysis:

$$CMIR_{low} = -\boldsymbol{V_{GS1} + V_{DSAT1} + V_{GS3}} = \boldsymbol{-552.1m + 121.5m + 599m = 168.4mV < 200mV}$$

$$CMIR_{HIGH} = VDD - V_{GS1} - V_{DSAT5} = 1.8 - 552.1m - 164.1m = 1.0838V > 1V$$

	Simulation	Hand analysis
$CMIR_{LOW}$	$180m$	$168.1m$
$CMIR_{HIGH}$	1.08761	1.0838

(Optional) CM large signal ccs (GBW vs VICM):

ymax(GBW)

	Expression	Value
1	ymax(GBW)	5.278E6

Figure 23 MAX GBW.

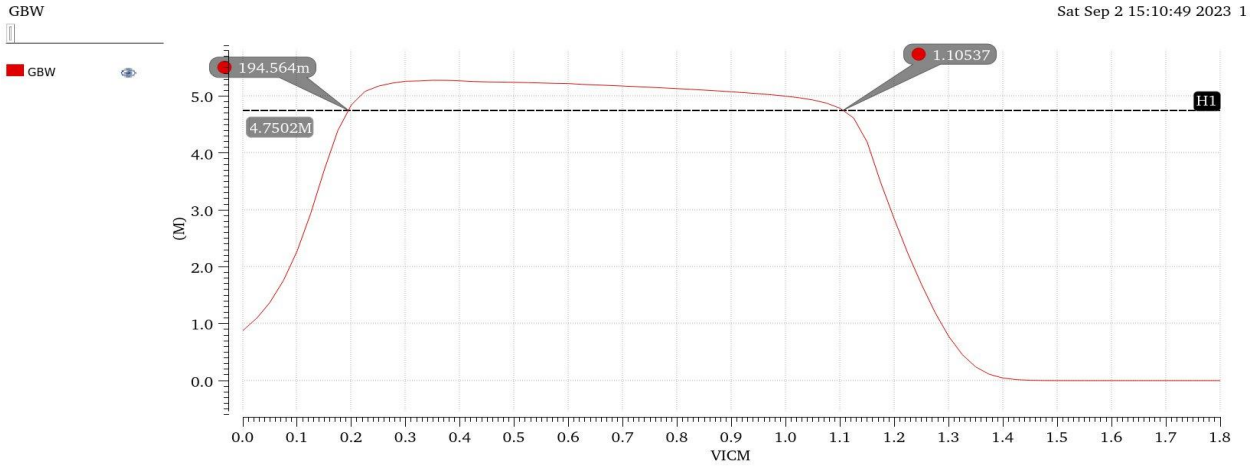


Figure 24 Plot GBW vs VINCM.

	$CMIR_{LOW}$	$CMIR_{HIGH}$
GBW method	$194.564m$	1.10537

PART 4: Closed-Loop OTA Simulation

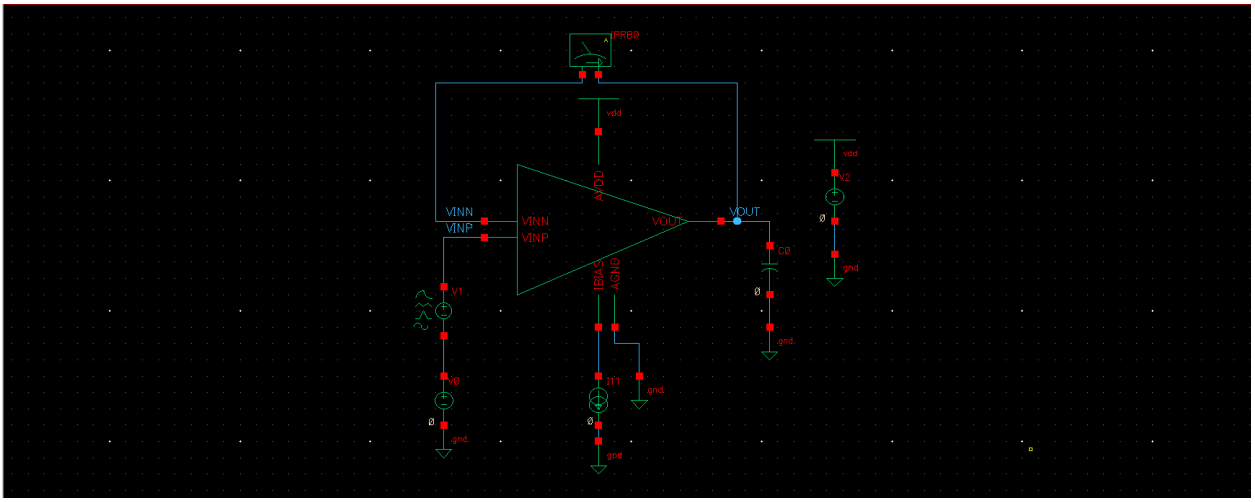


Figure 25 Schematic of Closed loop testbench.

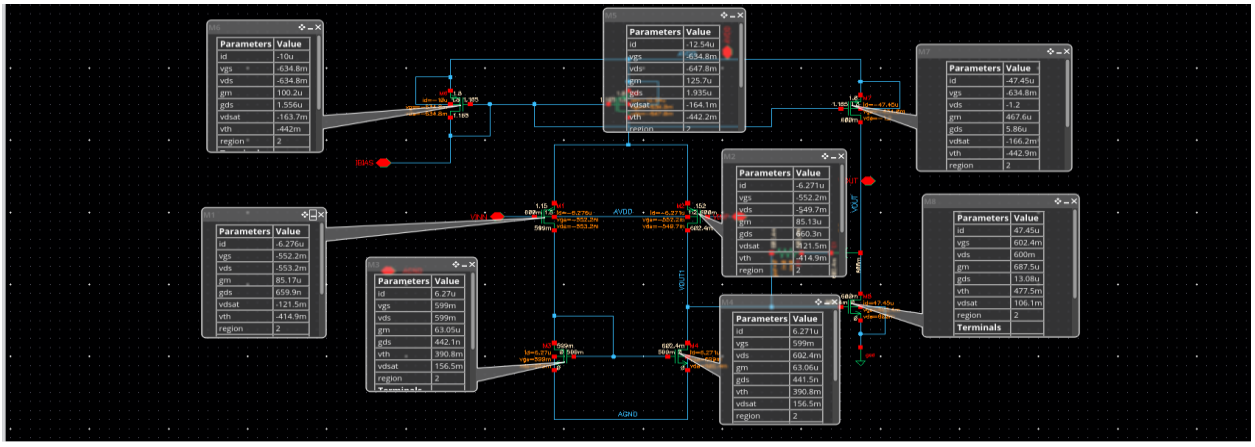


Figure 26 DC operating point.

• Are the DC voltages at the input terminals of the op-amp exactly equal? Why?

No, there is some difference in V_{DS} voltage due to V_{err} between two inputs of OTA.

• Is the DC voltage at the output of the first stage exactly equal to the value in the open-loop simulation? Why?

In closed loop → $V_{OUT1} = 602.4mV$.

In open loop → $V_{OUT1} = 599mV$.

They are not exactly equal, but they are very close to each other and that's due to the feedback that did the mismatch, due to V_{err} between two inputs of OTA.

• Is the current (and gm) in the input pair exactly equal? Why?

No, because there is some error in DC biasing voltage of input pair which make a small difference in drain current and gm, due to V_{err} between two inputs of OTA.

Loop gain:

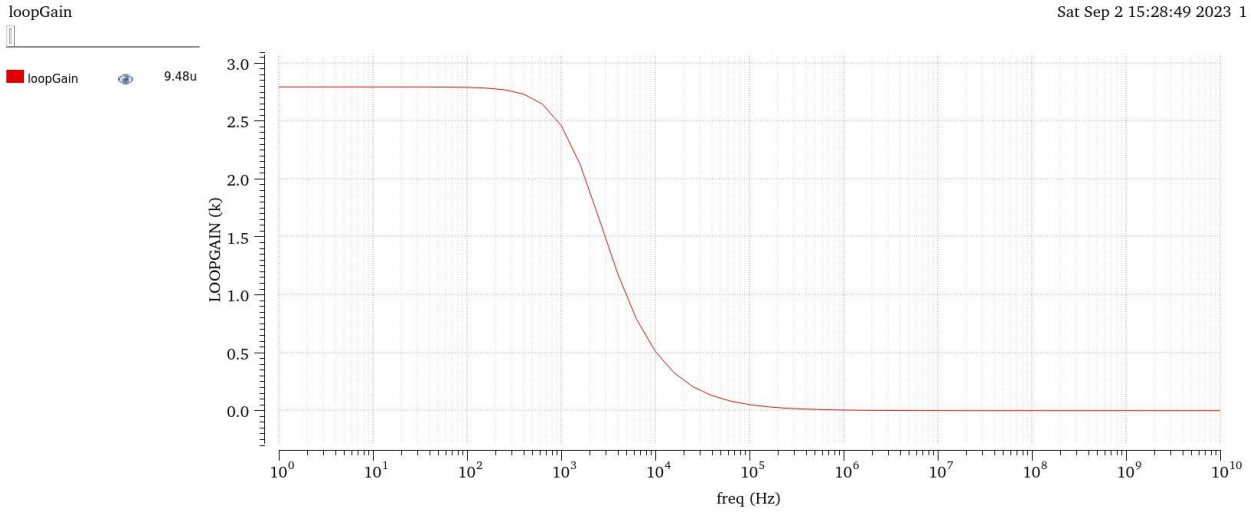


Figure 27 Loop gain vs frequency.

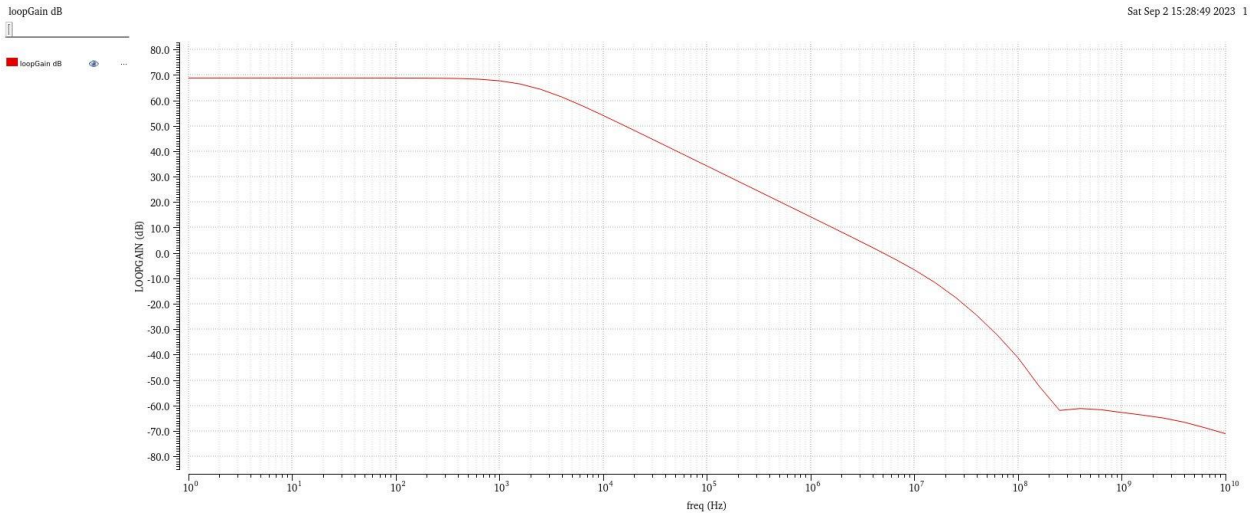


Figure 28 Plot loop gain in dB vs frequency.

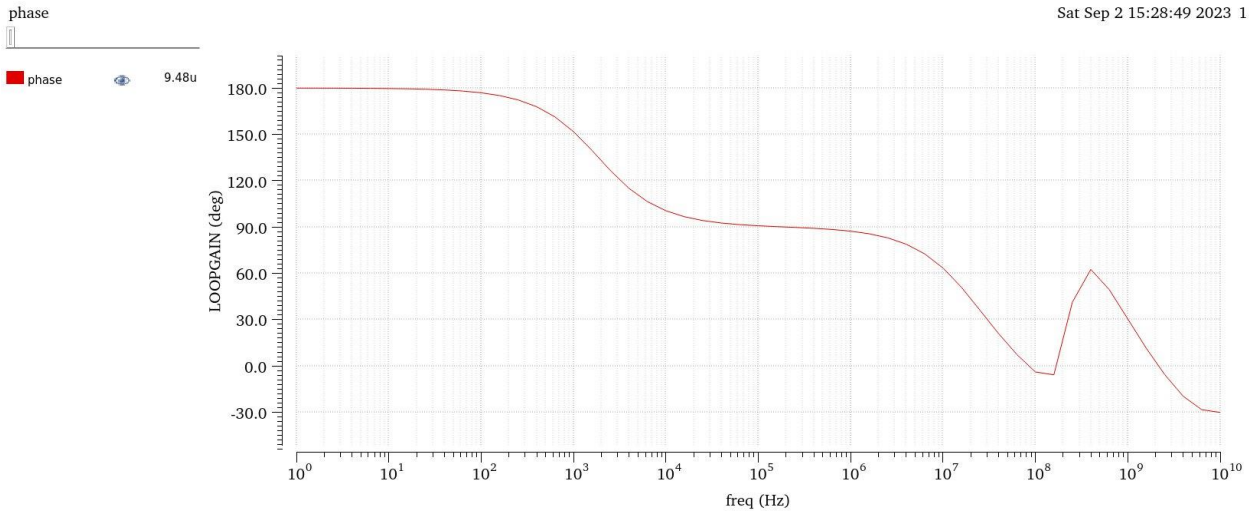


Figure 29 plot loop gain phase vs frequency.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
lab9_OTA_Open...	loopGain				
lab9_OTA_Open...	loopGain dB				
lab9_OTA_Open...	phase				
lab9_OTA_Open...	ymax(mag(getD...	2.762K			
lab9_OTA_Open...	ymax(dB20(mag...	68.82			
lab9_OTA_Open...	unityGainFreq(...	5.333M			
lab9_OTA_Open...	gainBwProd(ma...	5.273M			
lab9_OTA_Open...	PHASE margin	76.76			

Figure 30 results from simulator.

	Open loop	Feedback
Gain	2.833K	2.762K
Gain dB	69.05	68.82
GBW	5.22M	5.273M
UGF	5.092M	5.333M

Comment: The gain of closed loop is nearly the same as loop gain due to unity gain frequency but there some degradation in bandwidth of closed-loop due to the decrease in phase margin and decrease gain crossover Gx by compensating capacitor Cc, as the feedback network is a buffer and has B ideally=1, and product of gain and bandwidth is almost no change.

• Report PM. Compare with hand calculations. Comment.

$G_X = UGF = 2 * \pi * 5.333M = 33.508Mrad/s.$

$W_{P2} = 4 * W_U = 125.712Mrad/s$

$P_M = 90^o - tan^{-1}\left(\frac{G_X}{W_{P2}}\right) = 74.48°.$

Comment: The phase margin in the simulation and the hand analysis is very close to each other and it's equal to 76 degrees. First, it met the design spec needed. Secondly 76 degrees means critical damped response and it means fastest settling time and without overshot.

Hand analysis:

$$A_v = gain_1 * gain_2 = 2.806K = 68.96dB$$

$BW = \frac{1}{2*\pi*ROUT_1*GM_2*ROUT_2*C_C} \approx 1.932KHZ.$

$GBW = BW * A_v = 1.932K * 2.806K = 5.42MHZ.$

	Simulation	Hand analysis
Gain	2.833K	2.806K
BW	1.861K	1.932K
GBW	5.273M	5.42M
UGF	5.333M	5.42M

Slew rate:

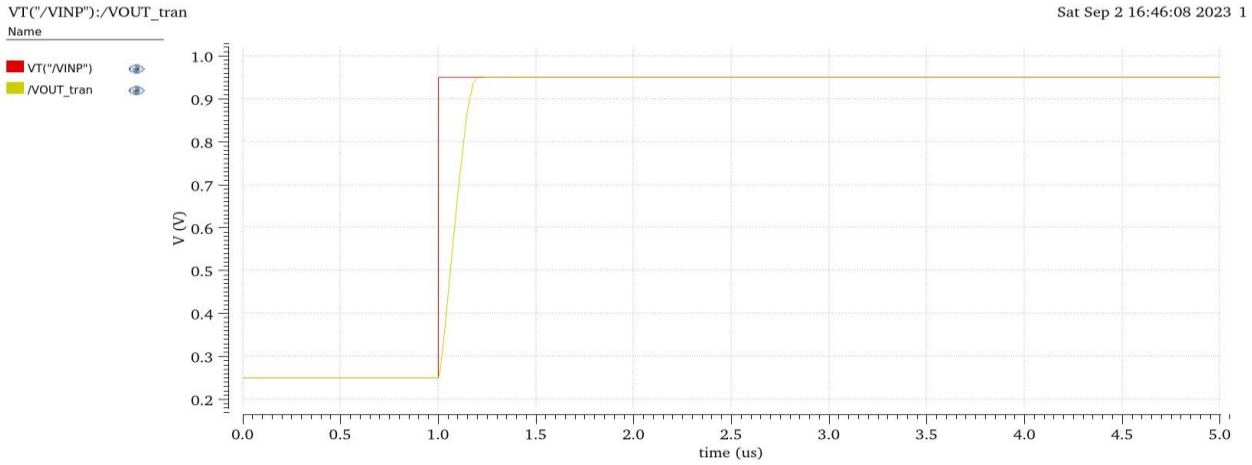


Figure 31 VOUT and VIN in Transient.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
lab9_OTA_Open...	VT("/VINP")				
lab9_OTA_Open...	/VOUT_tran				
lab9_OTA_Open...	slewRate(v("/VO...	4.942M			

Figure 32 SLEW RATE from simulator.

Hand analysis:

$$SR = \frac{I_{B1}}{C_C} = 5M$$

	Simulation	Hand analysis
Slew rate	4.942M	5M

Settling time:

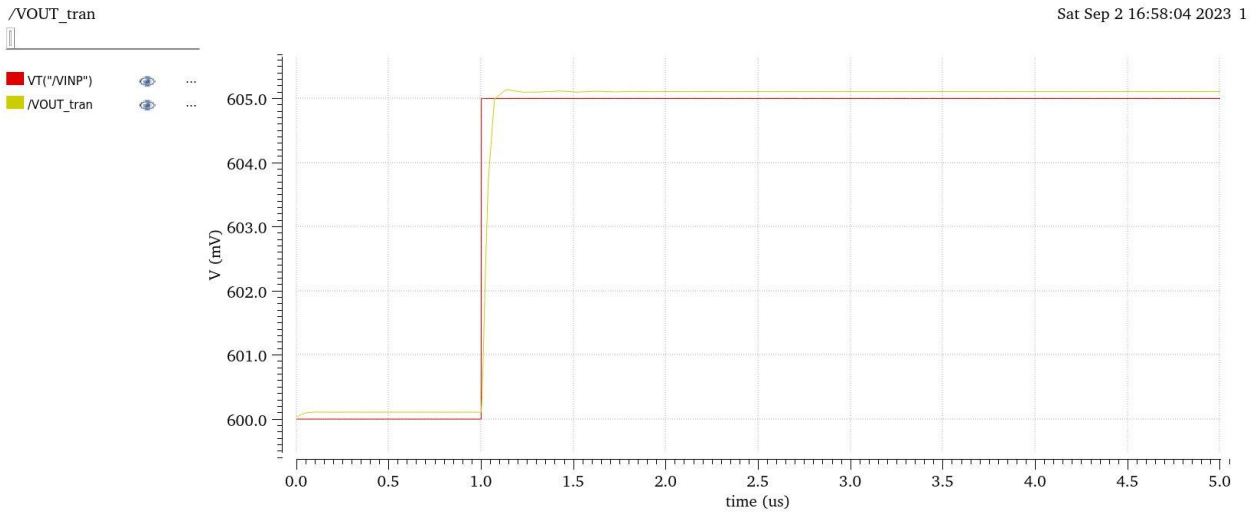


Figure 33 Setting time.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
lab9_OTA_Open...	VT("/VINP")				
lab9_OTA_Open...	/VOUT_tran				
lab9_OTA_Open...	riseTime(v("/VO...	52.18n			

Figure 34 Rise time from simulator.

Hand analysis:

I have $UGF = 2 * \pi * 5.333M = 33.508Mrad/s$.

$\tau = \frac{1}{UGF} = 29.84nS$.

$T_{rise} = 2.2 * \tau = 65.648nS$.

	Simulation	Hand analysis
Rise time	52.18n	65.648n

• Do you see any ringing? Why?

No there is no ringing in system because this system is a critical damped system with no ringing in time domain.

Specs achieved:

Spec	Required	Achieved
A_{vd}	$\geq 66dB$	$69.05dB$
CMRR	$\geq 74dB$	$74.242dB$
$V_{inCM-min}$	$\leq 0.2V$	$180mV$
$V_{inCM-max}$	$\geq 1V$	$1.08V$
GBW	$\geq 5MHz$	$5.22MHz$
Current Consumption	$\leq 60u$	60u
Phase Margin	≥ 70 degrees	76.76 degrees
Rise time	$\leq 70ns$	52.18ns
Slew Rate	$\geq 5MV/s$	$4.942\,MV/s$