Part 1: Low pass Filter

1.Transiant analysis:

1)Design:

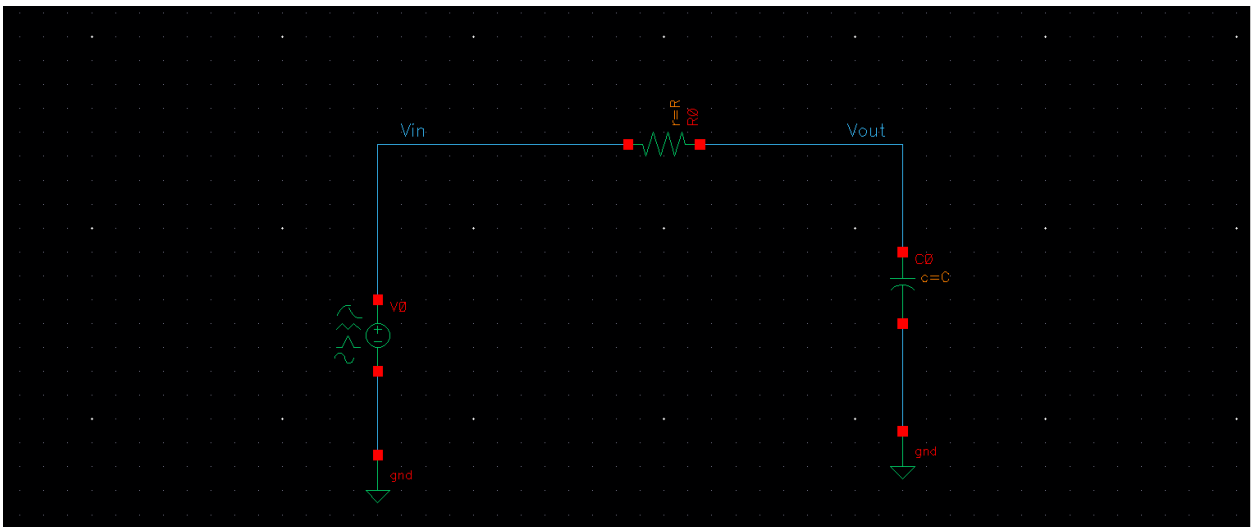

Figure 1Low pASS Filter Design

As $\tau = RC$ and $\tau = 0.3\ ns$ and R=1K Ω

$\therefore$ C=0.3 $\rho\mathcal{F}$

3)

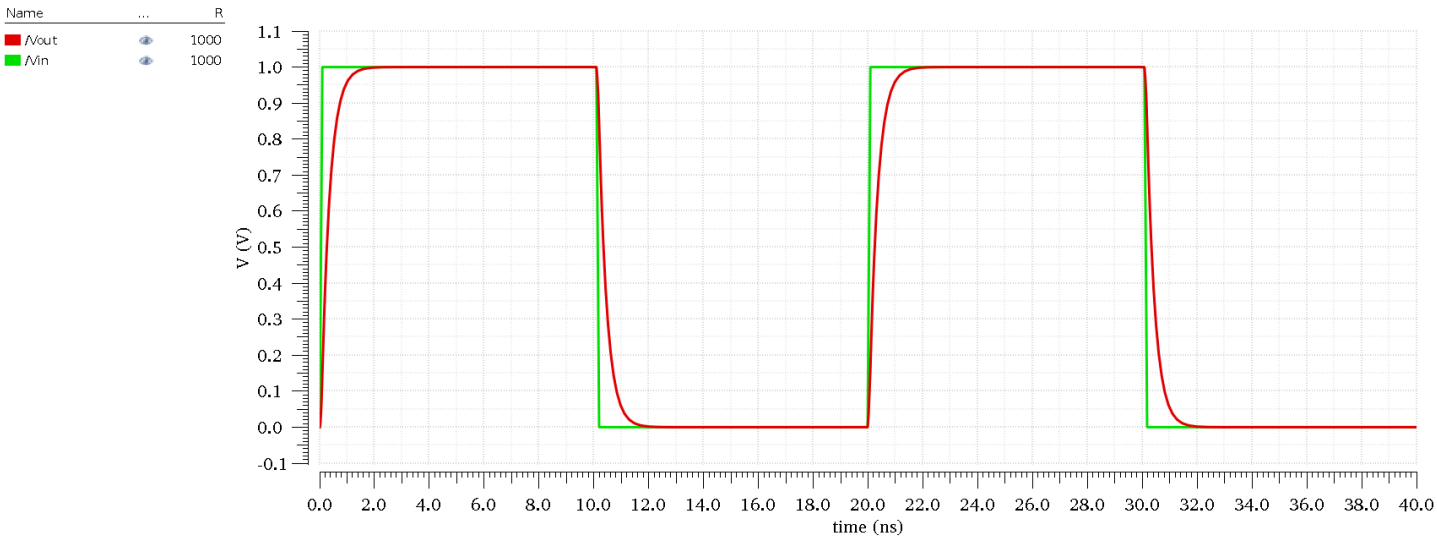

Figure 2 Transiant analysis

4)

Test	Output	Nominal	Spec	Weight	Pass/Fail
LAB01:LPF:1	Vout				
LAB01:LPF:1	Vin				
LAB01:LPF:1	rise time	661.8p			
LAB01:LPF:1	fall time	661.8p			

Figure 3 Simulator Results

*Analytic analysis for rise and fall time

At 90%

AS $V_O = V_{in}(1 - e^{\frac{T}{\tau}})$

0.9 $V_{in} = V_{in}(1 - e^{\frac{T}{\tau}})$

-0.1 $= -e^{\frac{T}{\tau}}$

$T_{90\%} = ln(10) * \tau = -ln(0.1) * \tau$

At 10%

AS $V_O = V_{in}(1 - e^{\frac{T}{\tau}})$

0.1 $V_{in} = V_{in}(1 - e^{\frac{T}{\tau}})$

-0.9 $= -e^{\frac{T}{\tau}}$

$T_{10\%} = -ln(0.9) * \tau$

-$T_{rise} = T_{fall} = T_{90\%} - T_{10\%}$ =2.2* τ=0.661ns=661ps

5)

	Simulation	Analytical
Rise time	661.8ps	661ps
Fall time	661.8ps	661ps

6)

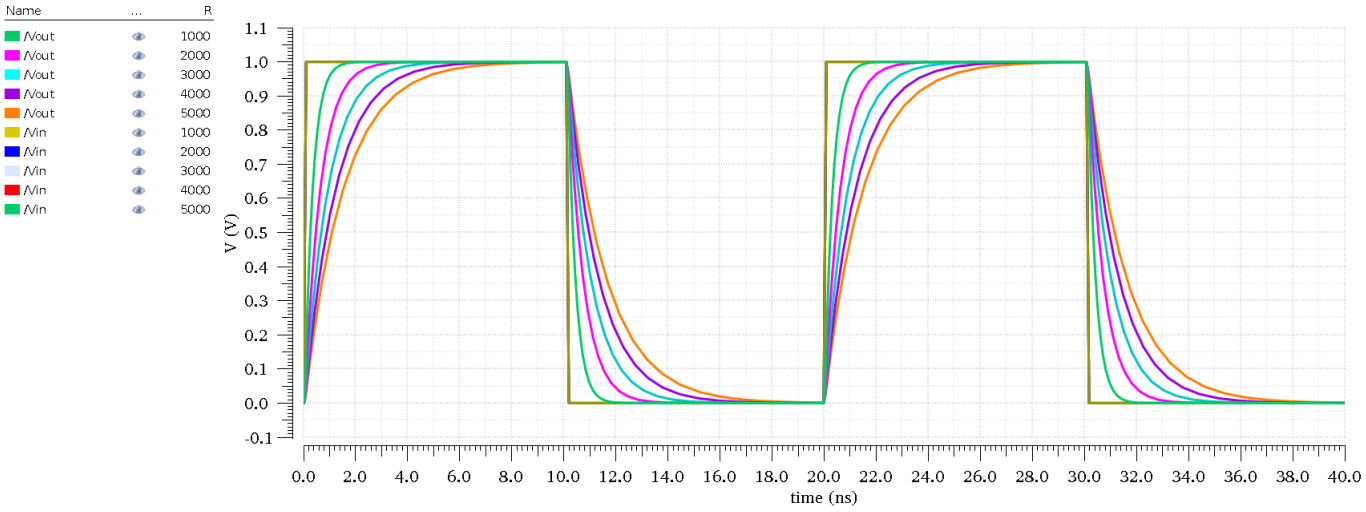

Figure 4 parametric sweep for resistance simulation results

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: R=1k						
1	LAB01:LPF:1	VT("/Vout")				
1	LAB01:LPF:1	Rise time	661.8p			
1	LAB01:LPF:1	Fall time	661.8p			
Parameters: R=2k						
2	LAB01:LPF:1	VT("/Vout")				
2	LAB01:LPF:1	Rise time	1.319n			
2	LAB01:LPF:1	Fall time	1.319n			
Parameters: R=3k						
3	LAB01:LPF:1	VT("/Vout")				
3	LAB01:LPF:1	Rise time	1.977n			
3	LAB01:LPF:1	Fall time	1.977n			
Parameters: R=4k						
4	LAB01:LPF:1	VT("/Vout")				
4	LAB01:LPF:1	Rise time	2.641n			
4	LAB01:LPF:1	Fall time	2.641n			
Parameters: R=5k						
5	LAB01:LPF:1	VT("/Vout")				
5	LAB01:LPF:1	Rise time	3.283n			
5	LAB01:LPF:1	Fall time	3.283n			

Figure 5 parametric sweep for resistance simulation results

Comment: as shown in both graphs when increase the value of the resistance rise time and fall time increases also due to their relation, and time constant of LPF increase so it's cut off frequency decreases follows the relation $\omega=\frac{1}{RC}$, and by decreasing cut off frequency of LPF it acts as an integrator at very high frequencies.

2. Ac analysis

1)

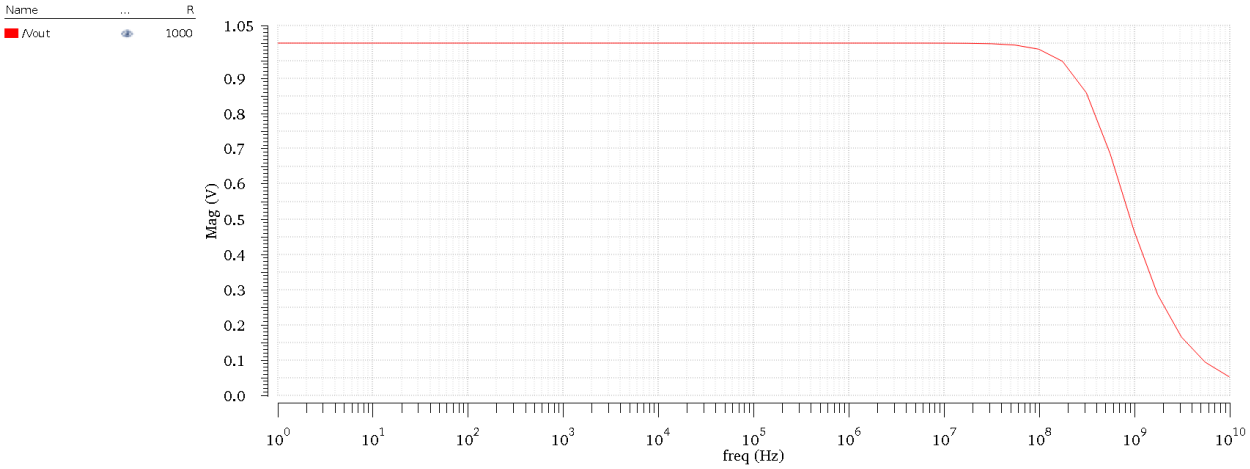

Figure 6 plot magnitude

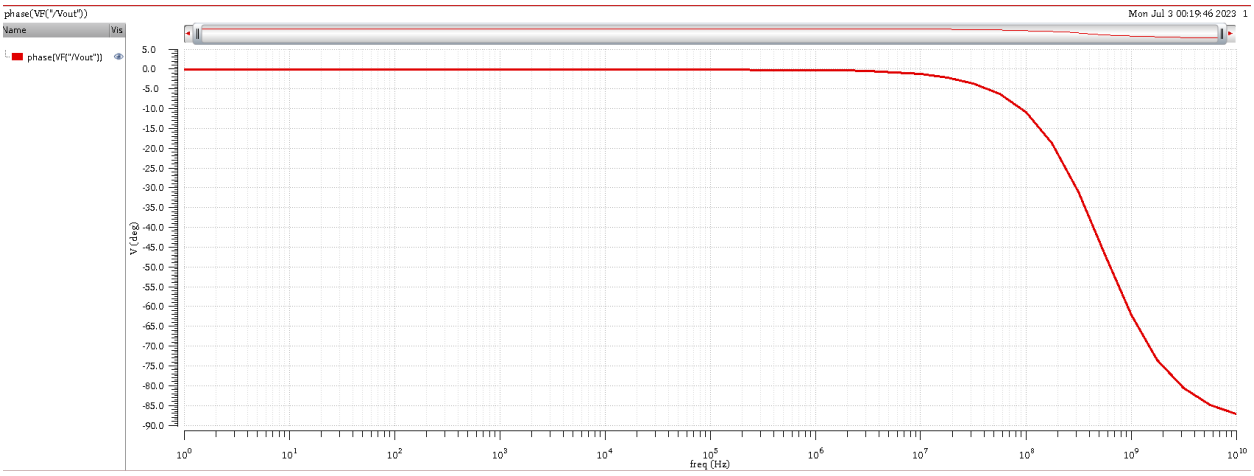

Figure 7 plot phase

2)

Test	Output	Nominal	Spec	Weight	Pass/Fail
LAB01:LPF:1	Vout				
LAB01:LPF:1	dB20(VF("/Vout"))				
LAB01:LPF:1	bandwidth(VF("/Vout") 3 "low")	531.4M			
LAB01:LPF:1	phase(VF("/Vout"))				
LAB01:LPF:1	DC gain	1			

Figure 8 Results from simulation (DC gain and Bandwidth)

*Analytic analysis:

Let s = jω. Then H(s)= $\frac{1/sC}{R+1/sC} = \frac{1}{1+sRC}$

- Then DC gain at s=0
- DC gain =1
- $\omega_c = \frac{1}{RC}$ $F_c = \frac{1}{2\pi RC}$ =530.516MHz

3)

	Simulator	Analytical
DC gain	1	1
Bandwidth	531.4M	530.516M

4)

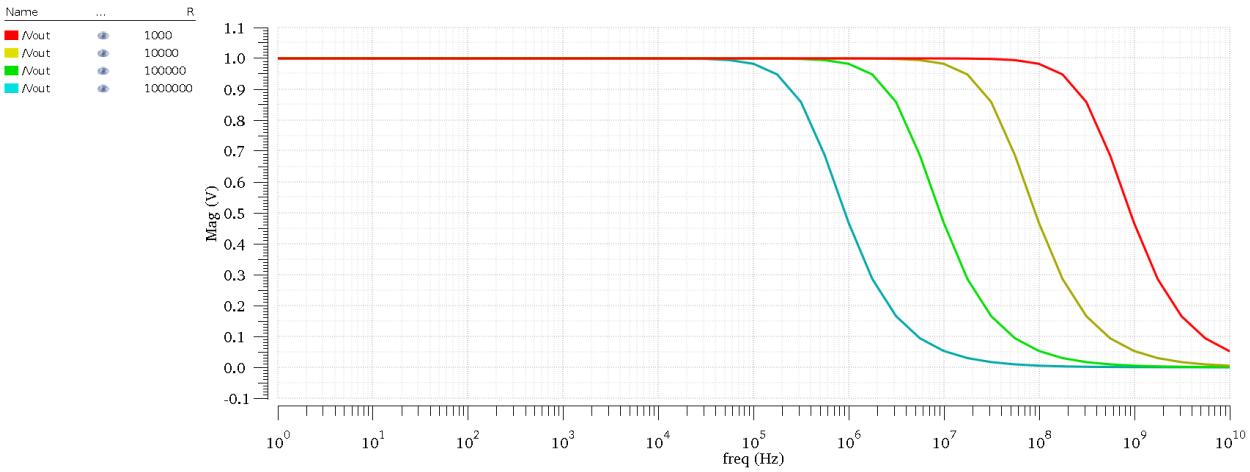

Figure 9 parametric sweep at resistance on ac analysis

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: R=1k						
1	LAB01:LPF:1	Vout				
1	LAB01:LPF:1	dB20(VF("/Vout"))				
1	LAB01:LPF:1	bandwidth(VF("/Vout") 3 "low")	531.4M			
1	LAB01:LPF:1	phase(VF("/Vout"))				
1	LAB01:LPF:1	DC gain	1			
Parameters: R=10k						
2	LAB01:LPF:1	Vout				
2	LAB01:LPF:1	dB20(VF("/Vout"))				
2	LAB01:LPF:1	bandwidth(VF("/Vout") 3 "low")	53.14M			
2	LAB01:LPF:1	phase(VF("/Vout"))				
2	LAB01:LPF:1	DC gain	1			
Parameters: R=100k						
3	LAB01:LPF:1	Vout				
3	LAB01:LPF:1	dB20(VF("/Vout"))				
3	LAB01:LPF:1	bandwidth(VF("/Vout") 3 "low")	5.314M			
3	LAB01:LPF:1	phase(VF("/Vout"))				
3	LAB01:LPF:1	DC gain	1			
Parameters: R=1M						
4	LAB01:LPF:1	Vout				
4	LAB01:LPF:1	dB20(VF("/Vout"))				
4	LAB01:LPF:1	bandwidth(VF("/Vout") 3 "low")	531.4k			
4	LAB01:LPF:1	phase(VF("/Vout"))				
4	LAB01:LPF:1	DC gain	1			

Figure 10 results of parametric sweep

Comment: as shown in the previous figures that by increasing the value of resistance cut off frequency of LPF decreases which follows this relation

- $F_c = \frac{1}{2\pi RC}$

Part 2 : MOSFET Characteristics

1.ID vs VGS

1.1)

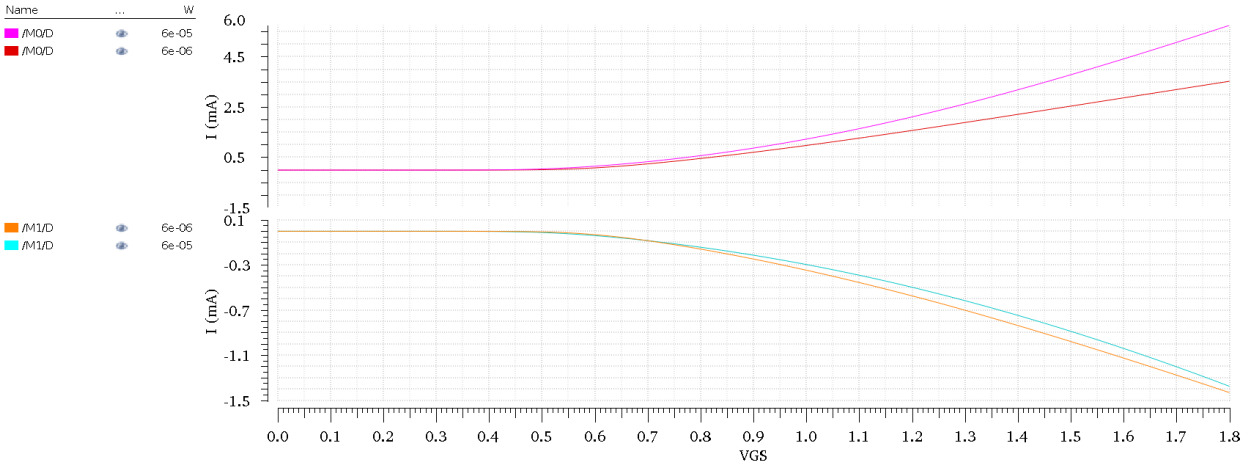

Figure 11 plot ID vs Vgs for both Nmos and Pmos

1.2)

•The higher current in a long channel device compared to a short channel device can be attributed to a few factors. In a long channel device, the assumption is made that the electric field is primarily one-dimensional (1D) and controlled only by the gate voltage. This allows for stronger gate control over the channel and results in a higher current.
On the other hand, in a short channel device, the electric field becomes two-dimensional (2D) due to the influence of both the gate voltage and the drain voltage. This 2D electric field distribution limits the strength of gate control over the channel and reduces the drain current.

Additionally, the depletion region in a short channel MOSFET is wider compared to a long channel MOSFET. This wider depletion region affects the drain current by reducing its value. The increased depletion region widens the depletion region capacitance, which increases the effective resistance of the channel, leading to a decrease in current.

•The drain current in short channel devices is often considered to have a linear relationship with respect to the gate-to-source voltage (VGS). This linear relationship is due to the presence of velocity saturation, which limits the increase in current.

The drain current in long channel devices is often considered to have a quadratic relationship with respect to VGS. The drain current (ID) in a long channel device can be approximated by the equation:

ID = (1/2) (W/L) $\mu C_{ox}(V_{gs} - V_{th})^2$.

1.3)

•the higher current in an NMOS (n-type MOSFET) compared to a PMOS (p-type MOSFET) can be attributed to the difference in carrier mobility between electrons and holes. Electrons generally have higher mobility compared to holes in semiconductor materials. This higher mobility allows electrons to move more easily through the channel, resulting in higher current flow in NMOS devices.

•the ratio between the current of an NMOS (ID_n) and the current of a PMOS (ID_p) device is influenced by the mobility of electrons and holes. When the NMOS and PMOS devices have the same channel length, width, and gate-to-source voltage (V_{GS}) bias, the current ratio can be approximated using the ratio of electron mobility (μ_n) to hole mobility (μ_p).

The approximate ratio of $ID_n$to ID_p is given by:

$$\frac{ID_n}{ID_p} \approx \frac{\mu_n}{\mu_p}$$

From the figure (11) get values of current at $V_{GS} = V_{DD}$

$$\frac{ID_n}{ID_p} = \frac{5.75504}{1.37295} = 4.19 \quad \text{(Long channel)}$$

$$\frac{ID_n}{ID_p} = \frac{3.53177}{1.42872} = 2.47 \quad \text{(short channel)}$$

•short channel effect appears strongly in case of NMOS more than case of PMOS.

2. gm vs VGS

2.1)

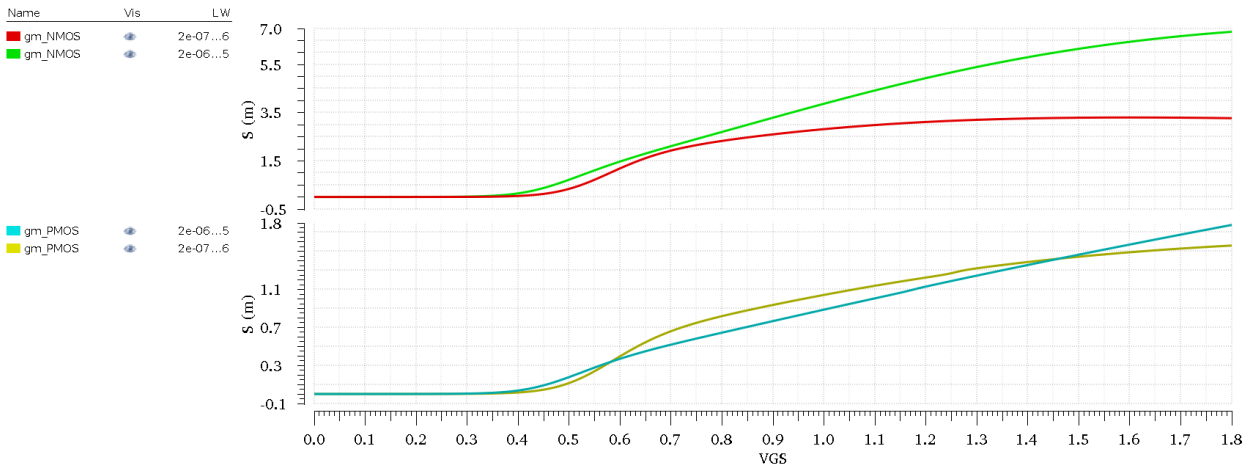

Figure 12 plot gm vs VGS for both nmos and pmos

2.2)

• transconductance (gm) represents the derivative of current drain, expressed as gm =$\frac{\partial I_d}{\partial v_{GS}}$. In the case of long channel devices, gm exhibits a linear relationship with the gate voltage, gm ∝ VGS. On the other hand, for short channel devices, gm can be approximated as a step function, where gm = constant. This behavior arises from the linear correlation between drain current and VGS.

•the transconductance (gm) exhibits saturation behavior specifically in the case of short channel MOSFETs. In this scenario, gm is considered to behave as a step function, indicating that it reaches a maximum value and remains constant for higher gate voltages. This saturation effect is due to the influence of short channel effects.

3. ID vs VDS

3.1)

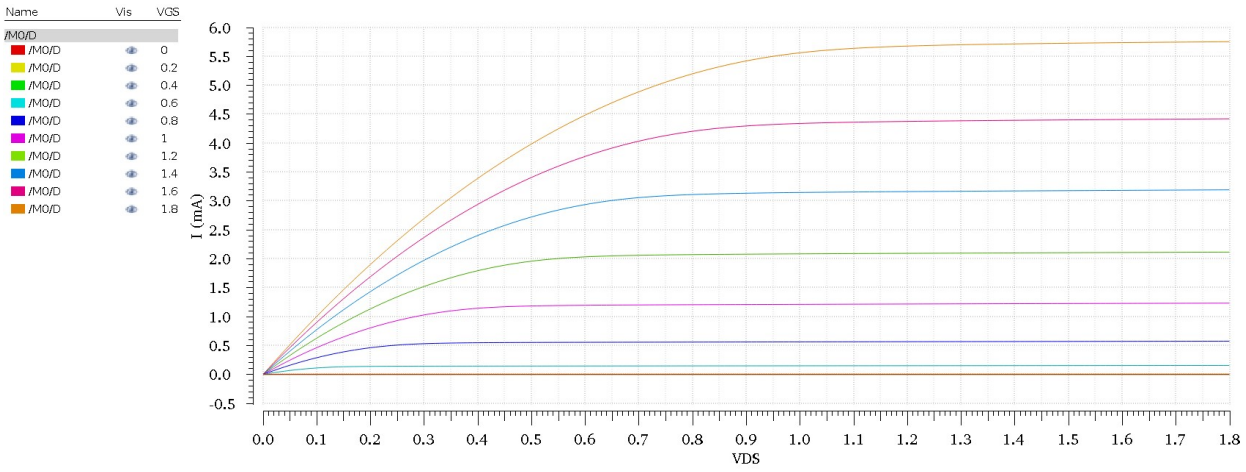

Figure 13 ID vs VDS for long channel and short channel NMOS

2.2)

•long channel MOSFETs exhibit higher current compared to short channel MOSFETs. This disparity arises from several factors. Firstly, the width of the depletion region is wider in short channel MOSFETs compared to long channel MOSFETs. Additionally, the drain induced barrier lowering effect contributes to the difference in current. Furthermore, the gate voltage has a reduced level of control over the drain current in short channel MOSFETs. These combined factors result in the observed disparity in current between the two types of MOSFETs.

•long channel MOSFETs exhibit a higher slope in the saturation region compared to short channel MOSFETs. This difference is evident when observing the distinct steps during the gate voltage sweep for each type of device. In long channel MOSFETs, the steps follow a quadratic, whereas in short channel MOSFETs, they follow a linear. This disparity in step behavior is primarily attributed to the dominant influence of velocity saturation effects in short channel MOSFETs.