Part 1: sizing chart

1) From the square law, we have

$$gm = \frac{2I_D}{V_{OV}} \rightarrow \quad V_{OV} = \frac{2I_D}{gm}$$

For a real MOSFET, if we compute Vov and 2 gm/ID they will not be equal. Let's define a new parameter called V-star (V^*) which is calculated from actual simulation data using the formula.

$$V^* = \frac{2I_D}{gm} \leftrightarrow gm = \frac{2I_D}{V^*}$$

The lower the $V*$ the higher the gm, but the larger the area and the lower the speed. An often-used sweet spot that provides good compromise between different trade-offs is V^* = 200mV.

2) Although the V^* is a nice parameter that is inspired by the square-law, it does not have an intuitive or a physical meaning (it is not an actual voltage in the circuit). We defined V^* to be able to define a relation between the gm and I_D. Thus, the real parameter that we should care about is the gm over I_D ratio (gm/ID).
3) There are many good things about using the gm/ID as a design knob:
4) a. The gm/ID gives a direct relation between the most important MOSFET parameter (gm) and the most valuable resource (ID). For example, a gm/ID = 10 S/A means you get 10 μS of gm for every 1 μA of bias current.
   b. The gm/ID is a normalized knob: it has a limited search range (typically from 5 to 25 S/A) independent of the technology or the device type.
   c. The gm/ID is intuitive because it tells you directly about the inversion level (bias point) and consequently all related trade-offs. For example, gm/ID = 5 S/A means strong inversion (SI), gm/ID = 15 S/A means moderate inversion (MI), and gm/ID = 25 S/A means weak inversion (WI).
   d. The gm/ID is an orthogonal knob: If we define the gm/ID then we define the inversion level (bias point). If you change ID or L while keeping gm/ID fixed, then the inversion level (bias point) is kept fixed. The W is treated as an output variable instead of being treated as an
   e. The higher the gm/ID (the lower the V^*) the higher the efficiency, but the larger the area and the lower the speed. An often-used sweet spot that provides good compromise between different trade-offs is gm/ID = 10 S/A (V^* = 200mV).

Parameter	Value
$\boldsymbol{A_v = g_m r_o}$[1]	50
$\boldsymbol{g_m}/I_D$	10 S/A
Supply ($\boldsymbol{V_{DD}}$)	1.8 V
Quiescent (DC) output voltage	$V_{DD}/2 = 0.9\ V$
Current consumption	20 μA

By using Sizing assistant, I have parameters $I_D = 20\mu A$ $\quad \frac{gm}{I_D} = 10\ {}^{S}/_{A}$

$\frac{gm}{gds} = 50$ $\quad V_{DS} = 0.9V$ $\quad V_{SB} = 0$

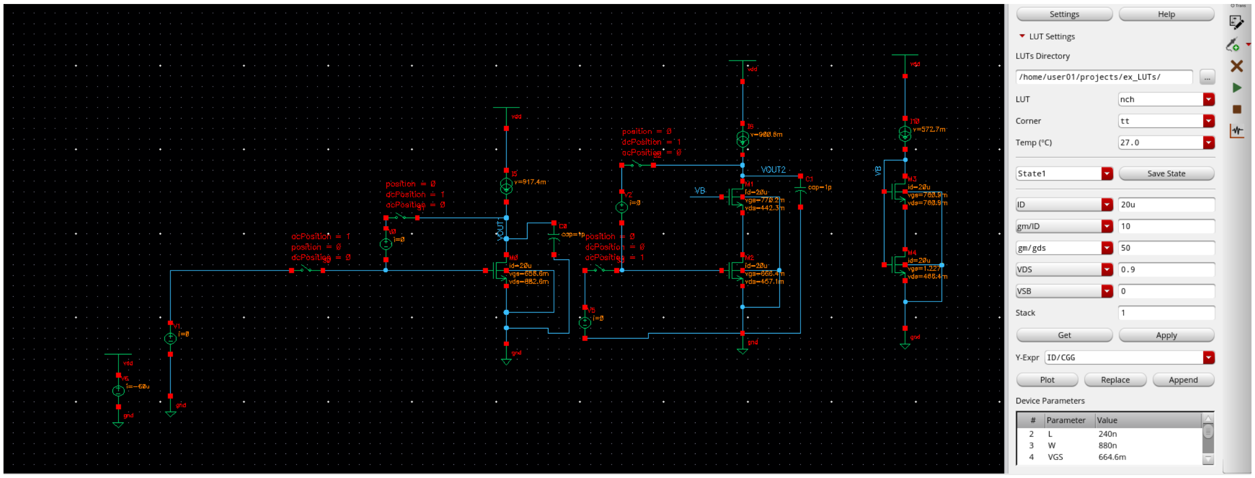

Figure 1 Sizing assistant results.

After using SA that generate the values of W,L and V_{GS}

$W = 880nm$ $\quad L = 240nm$ $\quad V_{GS} = 664.6mV$

Part 2: Cascode for Gain:

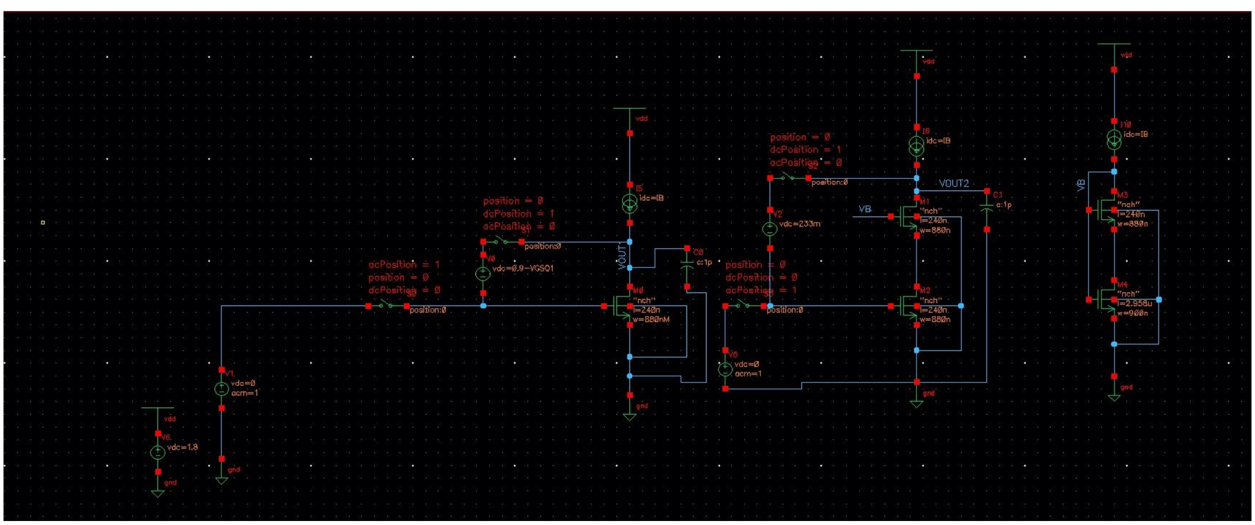

Figure 2 schematic

This parameter of schematic:

Use IB = 20μA. Use L and W as selected in Part 1 for M0, M1, M2, and M4. Use the same W for M3 but it will have a different L as will be shown later. Use CL = 1pF

In common source amplifier we have $V_{DS} = 0.9V$

In cascode amplifier we have for both transistor $V_{DS} = 0.45V$

$but\ upper\ NMOS\ has\ v_{SB}\ not\ equal\ zero\ because\ source\ of\ this\ trans\ not\ connecged\ to\ source,$

$it\ has\ V_{SB} = 0.45V$

$V_B = V_{GS2} + V_{DS1}$

Using sizing assistant to get this V_{GS2}

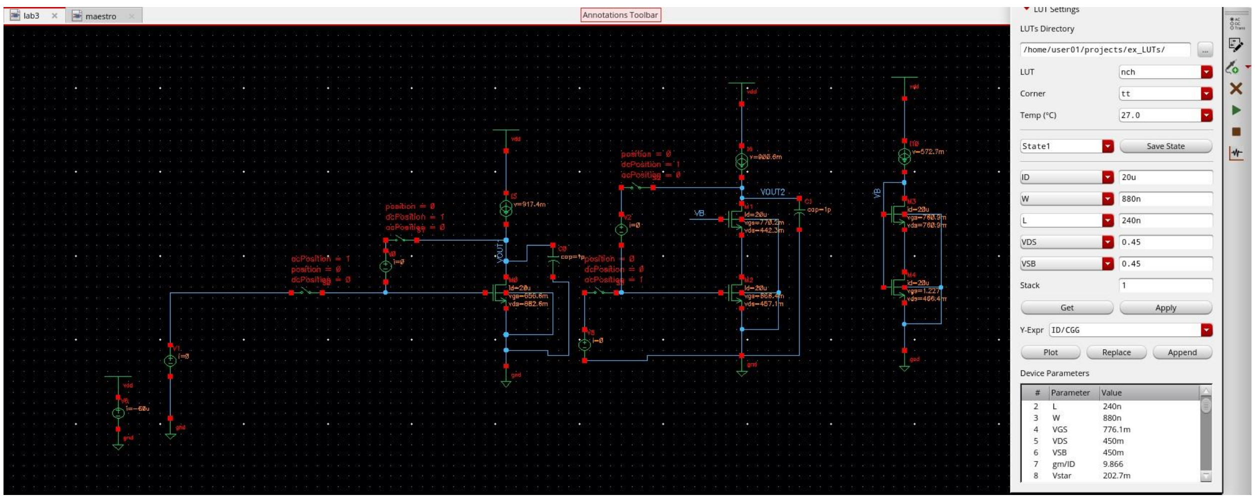

Figure 3 Sizing assistant of cascode amplifier

From SA we get $V_{GS2} = 776.1mV \quad then$

$V_B = V_{GS2} + V_{DS1}$ =0.45+0.776=1.226V

•M3 and M4 are used to generate the cascode bias voltage we want to get dimensions

Of M4 I want to get L and I have $V_B = V_{GS4,3} = 1.226V$

By ploting $V_{GS4,3}\ vs\ L\ using\ sizing\ assistant\ and\ trace\ L$

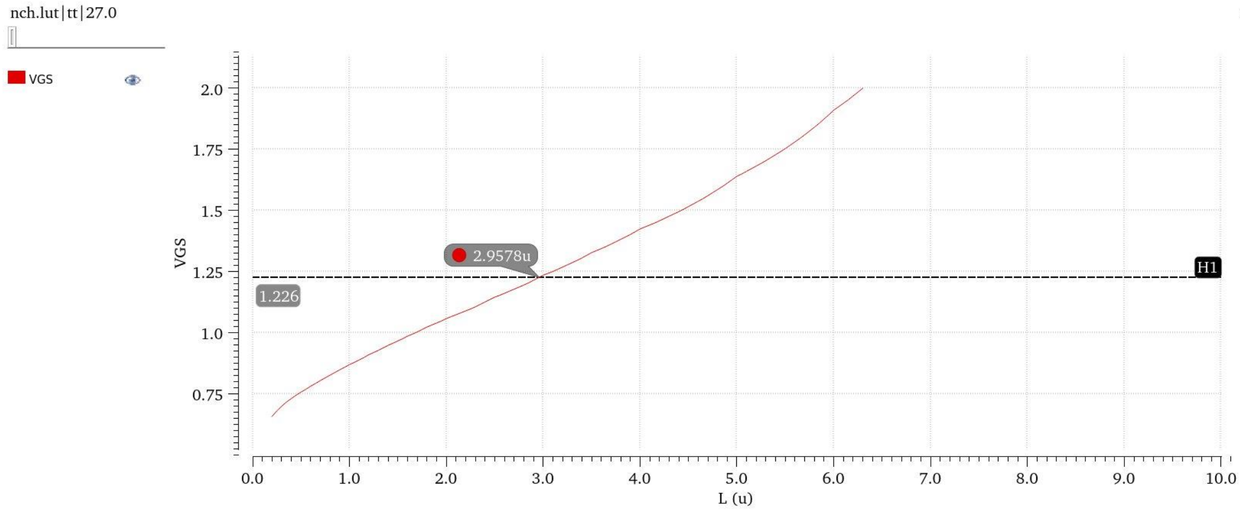

Figure 4 Trace to get L

After tracing L=2.9578μm

DC Analysis:

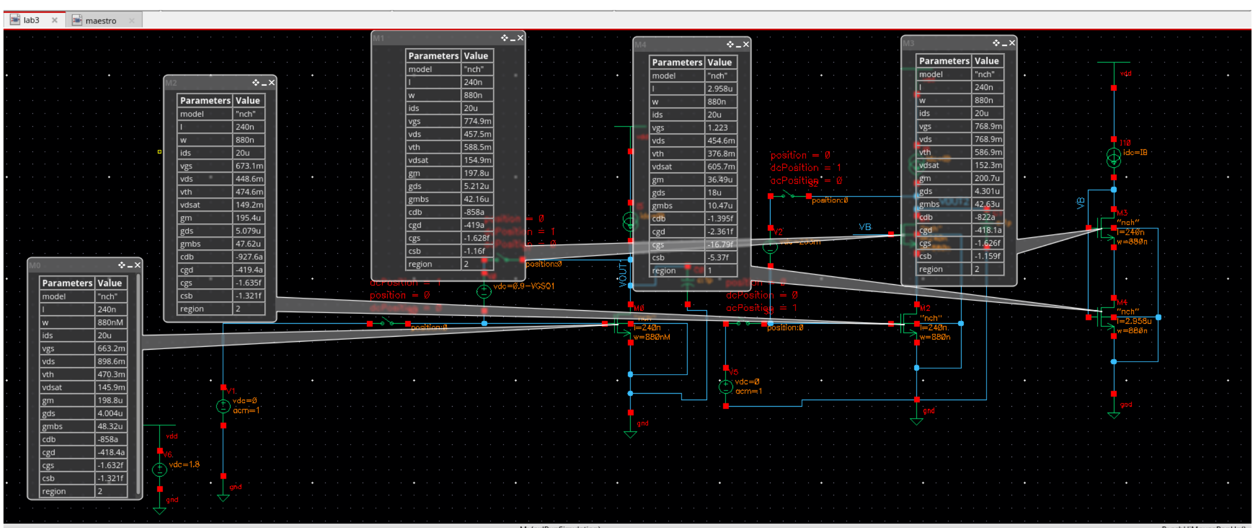

Figure 5 DC operting point

9) all transistors operate in saturation region expect M4(in my schematic) operate in triode because

$V_B = V_{GS} \qquad V_B = V_{DS1} + V_{DS2}$

Then $\quad V_{GS} > V_{DS} \;\; then\ M4(in\ my\ schmatic) is\ always\ in\ triode$

10)All transistors don't have the same threshold voltage even they have the same channel length L, this due to body effect we notice that M0 and M2(in my schematic) have VTH is almost the same, but M1 have different VTH because of body effect as source and bulk are not connected to each other so we will have voltage $Vsb\ between$ them which increase value of VTH.

11)gm >> gds .

gm > gmb .

$C_{gs} > C_{gd}$.

$C_{sb} > C_{db}$.

2. AC Analysis

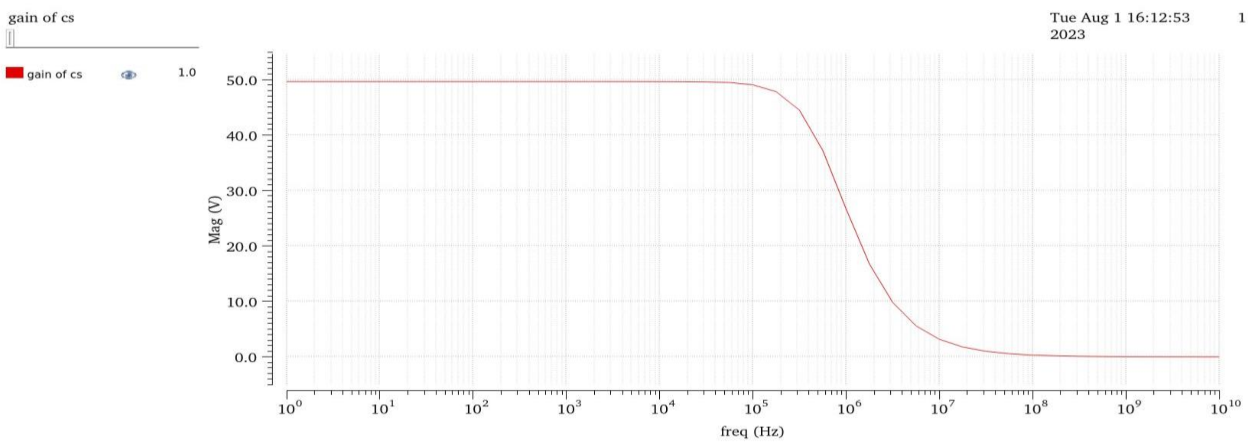

Figure 6 gain of common source

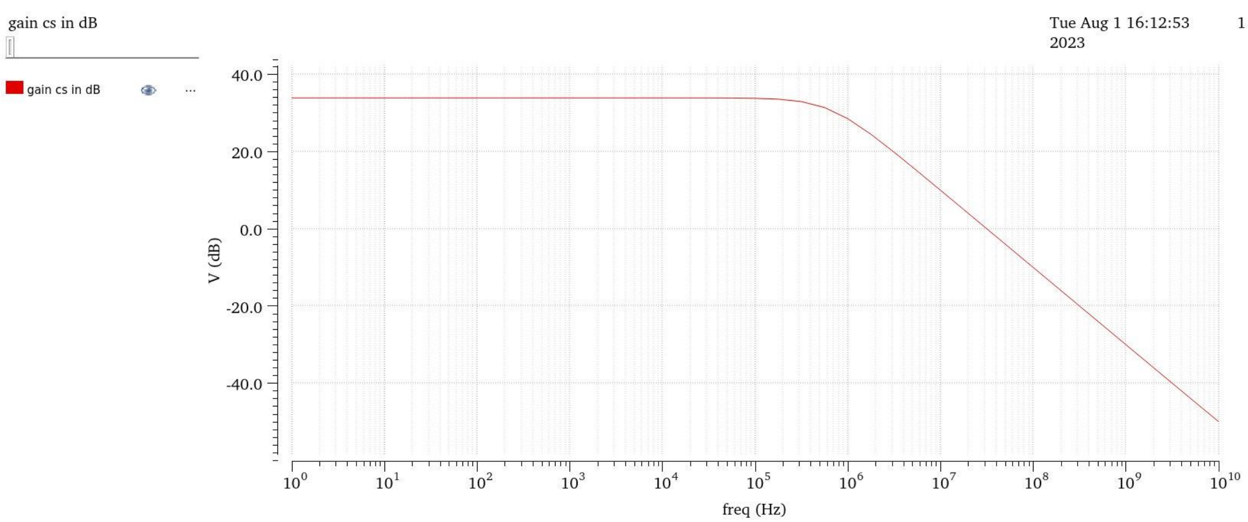

Figure 7 gain of common source in dB

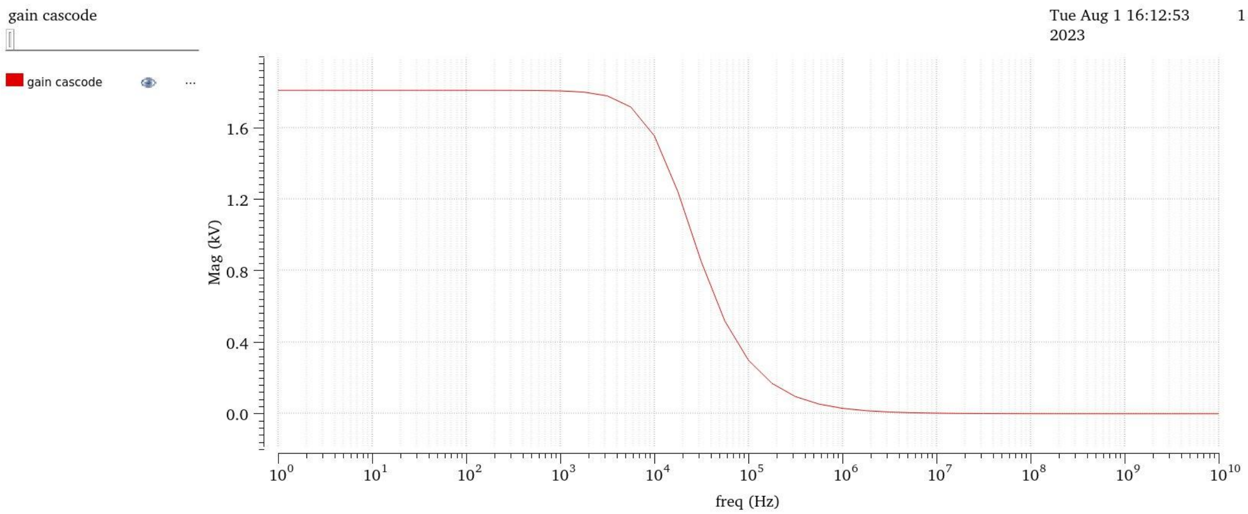

Figure 7 gain of cascode

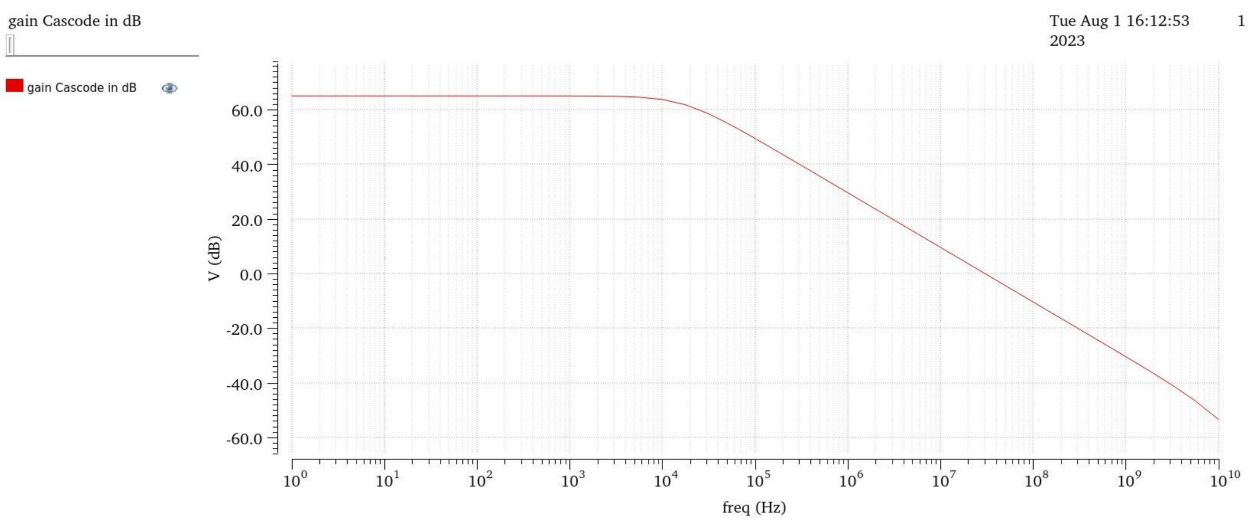

Figure 8 gain of cascode in dB

• from simulation we found:

$A_{vcs} = 49.65$

$A_{vcascode} = 1.809K$

Comment: cascode amplifier gain is greater than common source amplifier gain.

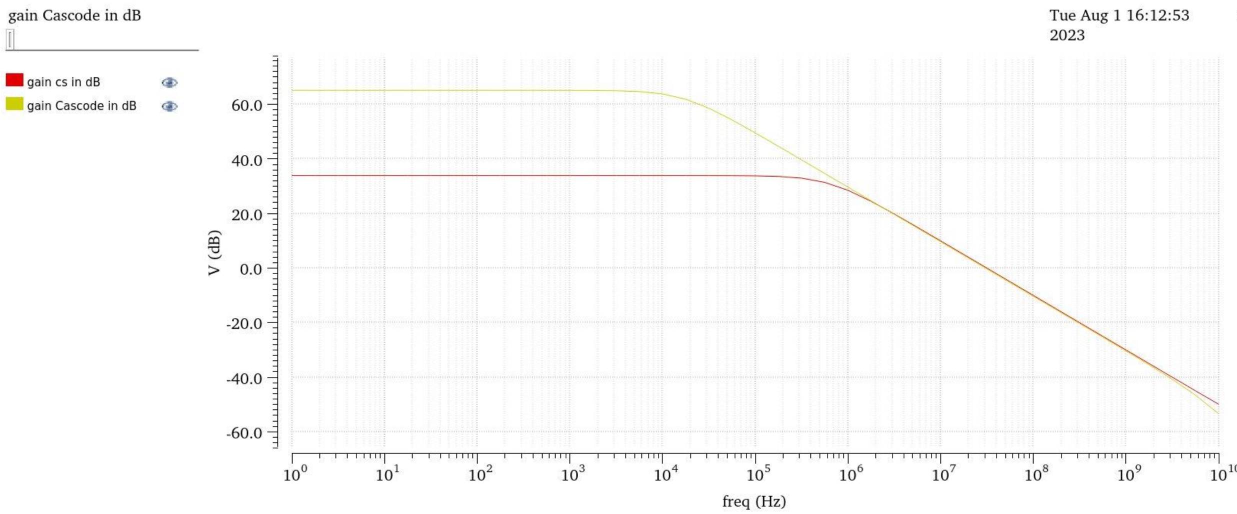

Figure 9 graph of cs and cascode bode plot on same graph

lab3_lab3_1	gain of cs				
lab3_lab3_1	gain cs in dB				
lab3_lab3_1	gain cascode				
lab3_lab3_1	gain Cascode in ...				
lab3_lab3_1	dc gain cs	49.65			
lab3_lab3_1	dc gain cs in dB	33.92			
lab3_lab3_1	dc gain cascode	1.809K			
lab3_lab3_1	dc gain cascode ...	65.15			
lab3_lab3_1	bandwidth cs	647.7K			
lab3_lab3_1	bandwidth casc...	16.84K			
lab3_lab3_1	gbw cs	32.24M			
lab3_lab3_1	gbw cascode	30.54M			
lab3_lab3_1	ugf cs	31.6M			
lab3_lab3_1	ugf cascode	30.92M			

Figure 10 results from adexl

RESULTS from ADEXL:

	Common source	Cascode amplifier
Gain	49.65	1.809K
Gain in dB	33.92	65.15
BW	647.7K	16.84K
GBW	32.24M	30.54M
UGF	31.6M	30.92M

Hand analysis:

$$|A_{VCS}| = gm1 * r_o = gm1 * \frac{1}{gds} = 198.8\mu * \frac{1}{4.004\mu} = 49.65$$

$$|A_{VCascode}| = gm1 * (r_{o1} + r_{o2} + (gm2 + gmb2) * r_{o1} * r_{o2})$$

$$=195.4\mu * \left(\frac{1}{5.079\mu} + \frac{1}{5.212\mu} + (197.8\mu + 42.16\mu) * \frac{1}{5.079\mu} * \frac{1}{5.212\mu}\right) = 1.847\mathrm{K}$$

$$\mathrm{BW_{CS}} = \frac{1}{2\pi * R * C} = \frac{1}{2\pi * \frac{1}{4.004\mu} * 10^{-12}} = 637.256\mathrm{KHZ}$$

$$\mathrm{BW_{Cascode}} = \frac{1}{2\pi * R * C} = \frac{1}{2\pi * 9452.405 * 10^{3} * 10^{-12}} = 16.838\mathrm{KHZ}$$

$$\mathrm{GBW_{CS}} = \mathrm{BW_{CS}} * \mathrm{Gain_{CS}} = 637.256\mathrm{K} * 49.65 = 31.64\mathrm{MHZ}$$

$$\mathrm{GBW_{Cascode}} = \mathrm{BW_{cascode}} * \mathrm{Gain_{Cascode}} = 1.847\mathrm{K} * 16.838\mathrm{K} = 31.1\mathrm{MHZ}$$

UGF$\approx GBW$

Comment:

As shown in previous results The cascode amplifier has a higher gain than the common source amplifier because the common base transistor in the cascode amplifier effectively multiplies the output resistance of the common source transistor. This is because the common base transistor has a very high output resistance, which is not affected by the input voltage because of higher resistance of cascode amplifier than common source,cascode has lower bandwidth as bandwidth.

	Simulator	Hand analysis
Gain CS	49.65	49.65
Gain Cascode	1.809K	1.847
BW CS	647.7K	637.256K
BW cascode	16.84K	16.838K
GBW CS	32.24M	31.64M
GBW Cascode	30.54M	31.1M
UGF CS	31.6M	31.64M
UGF Cascode	30.92M	31.1M

PART 3 [Optional]: Cascode for BW

1. OP Analysis

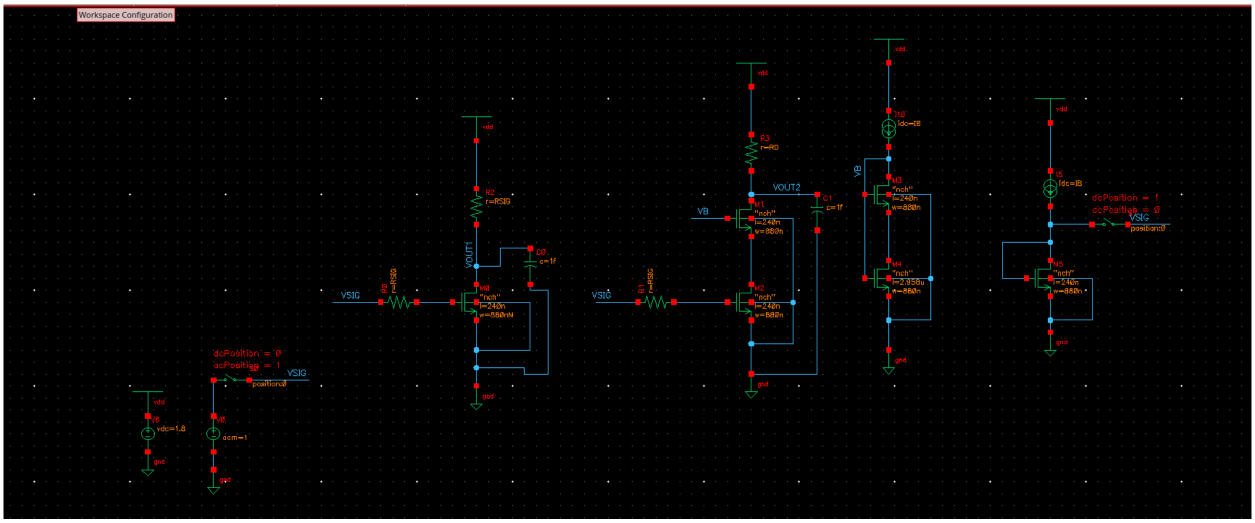

Figure 11 Schmatic

2) RD= $\frac{0.9}{20\mu} = 45K\Omega$

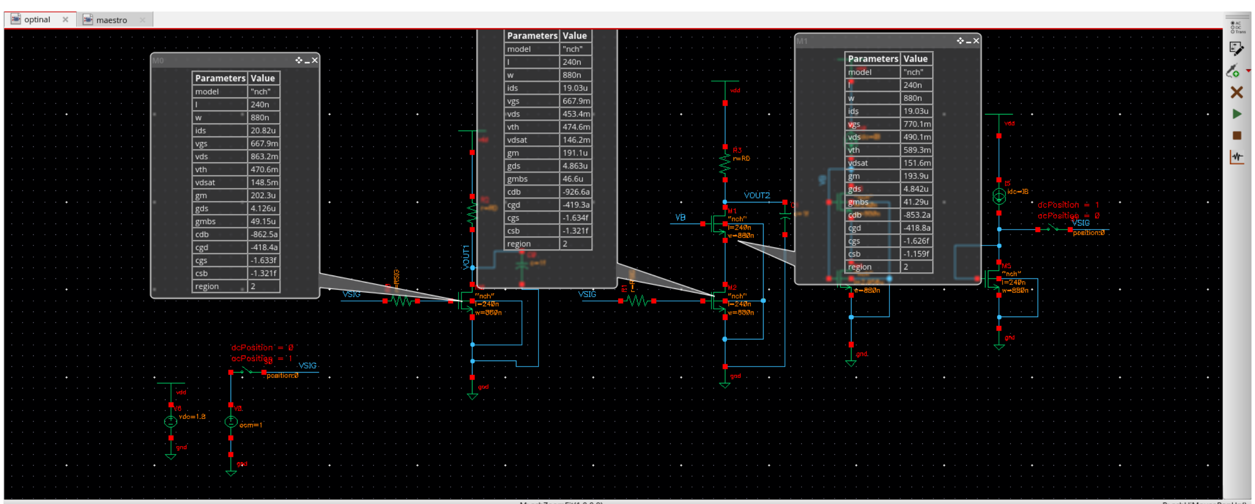

Figure 12 DC Operating point

3) as shown in figure all transistor operating in sat region (region 2).

2. AC Analysis

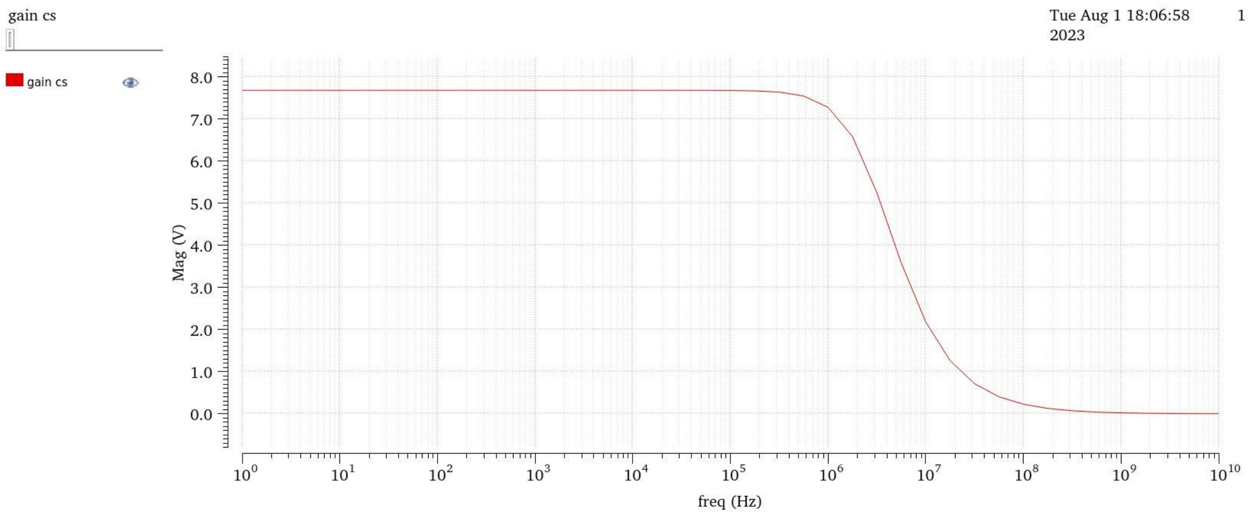

Figure 13 cs gain

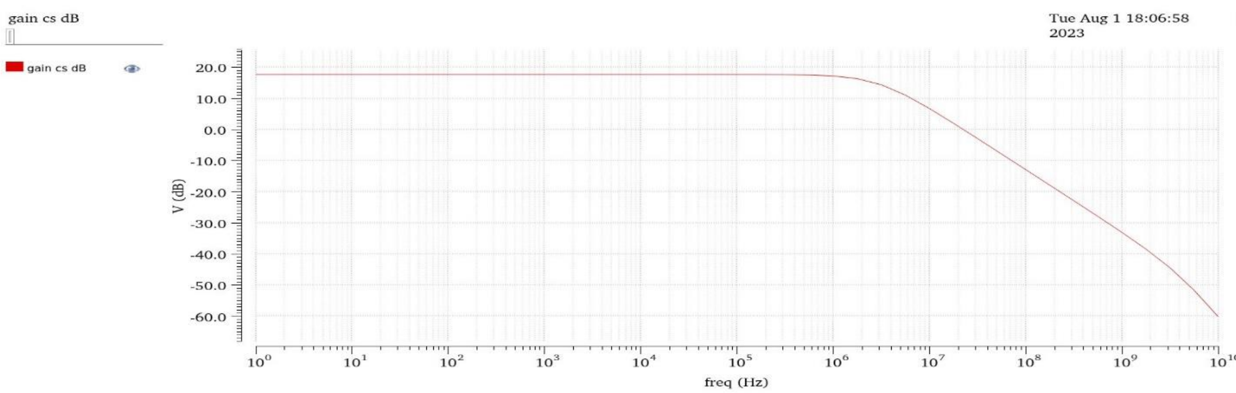

Figure 14 cs gain in dB

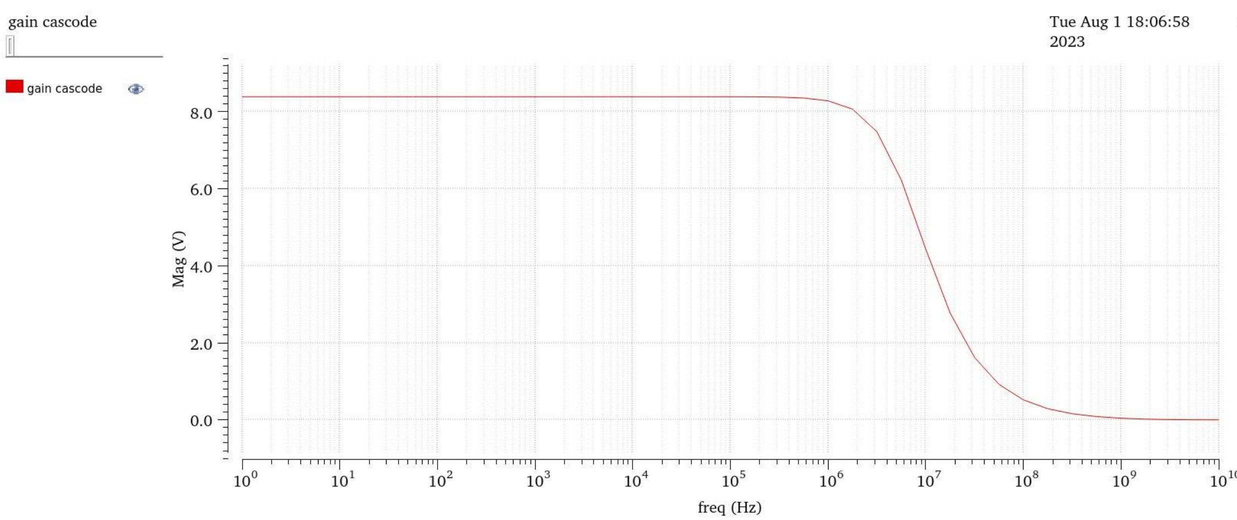

Figure 15 cascode gain

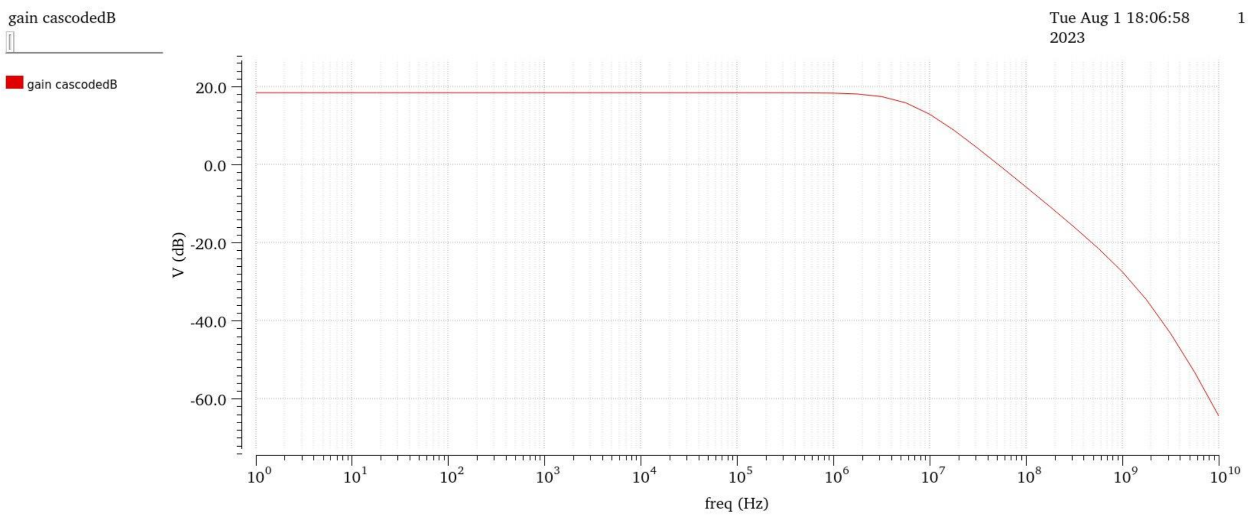

Figure 16 cascode gain in dB

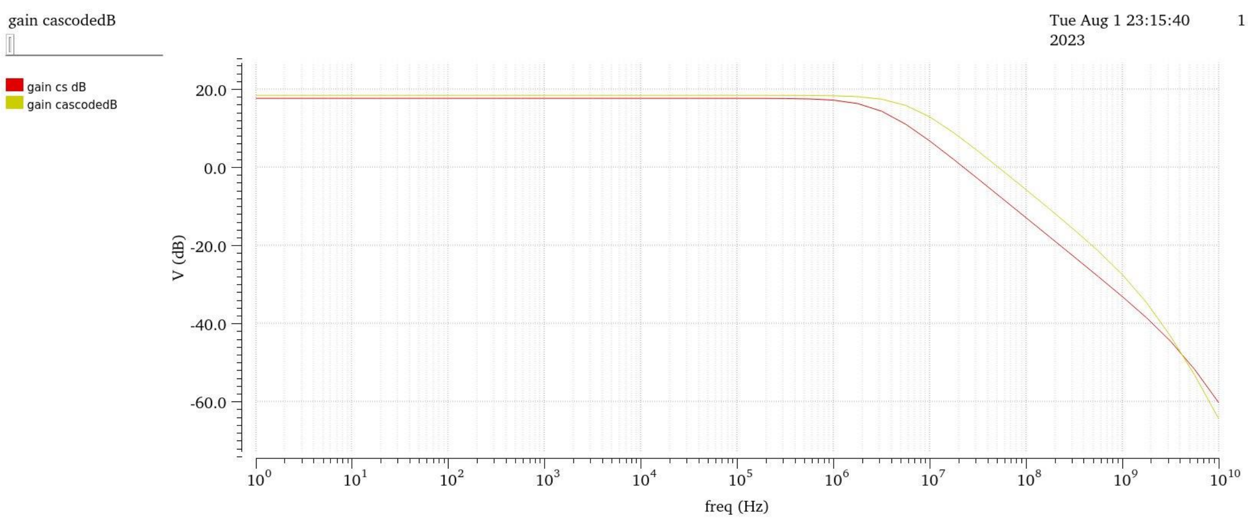

Figure 17 bode plot of cs and cascode

gain cs	expr	VF("/VOUT1")		
gain cs dB	expr	dB20(VF("/VOUT1"))		
gain cascode	expr	VF("/VOUT2")		
gain cascodedB	expr	dB20(VF("/VOUT2"))		
dc gain cs	expr	ymax(mag(VF("/VOUT1")))		7.678
dc gain cs dB	expr	ymax(dB20(VF("/VOUT1")))		17.71
dc gain cascode	expr	ymax(mag(VF("/VOUT2")))		8.391
dc gain cascode dB	expr	ymax(dB20(VF("/VOUT2")))		18.48
bandwidth cs	expr	bandwidth(VF("/VOUT1") 3 "low")	ymax(dB20(VF("/VOUT2")))	2.968M
bandwidth cascode	expr	bandwidth(VF("/VOUT2") 3 "low")		6.331M
gbw cs	expr	gainBwProd(VF("/VOUT1"))		22.84M
gbw cascode	expr	gainBwProd(VF("/VOUT2"))		53.27M
ugf cs	expr	unityGainFreq(VF("/VOUT1"))		24.41M
ugf cascode	expr	unityGainFreq(VF("/VOUT2"))		53.52M

Figure 18 results from adexl

	Common source	Cascode amplifier
Gain	7.678	8.391
Gain in dB	17.71	18.48
BW	2.968M	6.331M
GBW	22.84M	53.27M
UGF	24.41M	53.52M

Hand analysis:

$$|A_{VCS}| = gm1 * (r_o||RD) = gm1 * (\frac{1}{gds}||RD) = 202.3\mu * (\frac{1}{4.126\mu}||45K) = 7.678$$

$$|A_{VCascode}| = gm1 * RD||(r_{o1} + r_{o2} + (gm2 + gmb2) * r_{o1} * r_{o2})$$

$$=191.1\mu * 45K||\left(\frac{1}{4.863\mu} + \frac{1}{4.842\mu} + (193.9\mu + 41.29\mu) * \frac{1}{4.863\mu} * \frac{1}{4.842\mu}\right) = 8.56$$

the dominant pole the input pole instead of the output pole. I will use miller theorem

$$BW_{CS} = \frac{1}{2\pi*R*(C_{GS}+C_{GD}(1+A))} = \frac{1}{2\pi*10^6*10*(1.633*10^{-15}+418.4*10^{-18}(1+7.678))} = 3.024MHZ$$

$$A_0 = -gm_1 * (r_{o1}||R_{LFS})$$

$$R_{LFS} = \frac{1}{gm_2}(1 + \frac{RD}{r_{o2}})$$

$$A_0 = 1.16$$

$$BW_{Cascode} = \frac{1}{2\pi*R*(C_{GS}+C_{GD}(1+A))} = \frac{1}{2\pi*10^6*10*(1.634*10^{-15}+419.3*10^{-18}(1+1.16))} = 6.27MHZ$$

$$GBW_{CS} = BW_{CS} * Gain_{CS} = 3.024M * 7.678 = 23.2MHZ$$

$$GBW_{Cascode} = BW_{cascode} * Gain_{Cascode} = 6.27M * 8.56 = 53.67MHZ$$

UGF$\approx GBW$

	Simulator	Hand analysis
Gain CS	7.678	7.678
Gain Cascode	8.391	8.56
BW CS	2.968M	$3.024M$
BW cascode	6.331M	6.27M
GBW CS	22.84M	23.2M
GBW Cascode	53.27M	53.67M
UGF CS	24.41M	23.2M
UGF Cascode	53.52M	53.67M

Comment:

I used to calculate bandwidth open circuit theorem and miller theorem

I noticed the cascode gain doesn't change higher than common source is almost equal because when use RD has small value it is parallel to output impedance, so gain almost did not change.

For bandwidth we have dominant pole is input pole and when adding cascode miller theorem effect decreases on the input pole thus causing extension in bandwidth, this is reason for different in bandwidth.