Part 1: gm/ID Design Charts

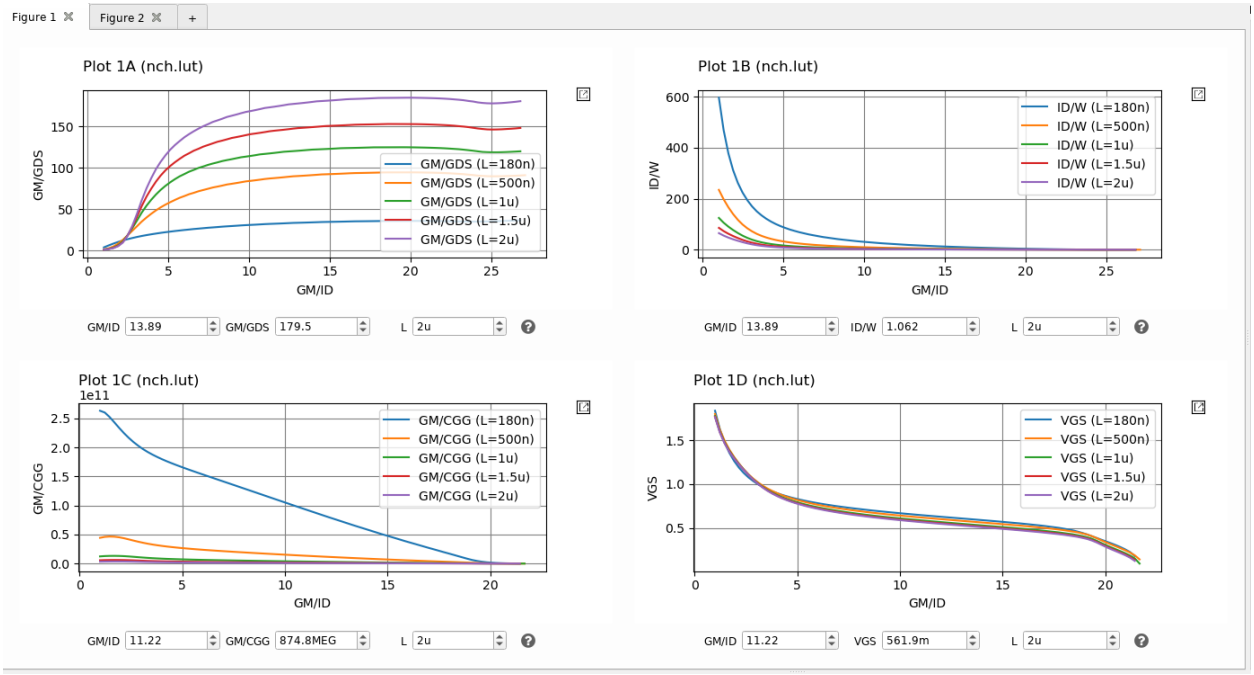

Figure 1 NMOS ADT

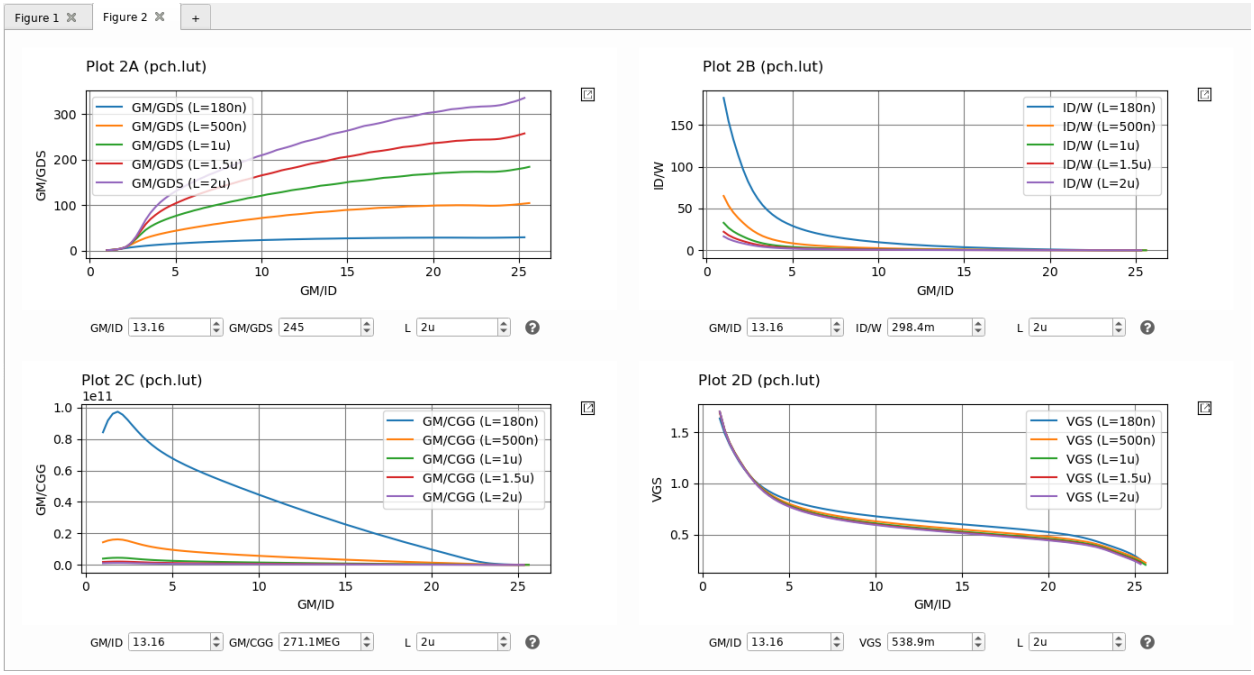

Figure 2 PMOS ADT

Part 2: OTA Design

Use the gm/ID methodology to design a diff input single-ended (SE) output operational transconductance amplifier (OTA) that achieves the following specs. Use an ideal external 10uA DC current source in your test bench (not included in the OTA current consumption spec), but design your own current mirror.

Technology	
Supply voltage	1.8V
Load	5pF
Open loop DC voltage gain	>= 34dB
CMRR @ DC	>= 74dB
Phase margin	>= 70°
OTA current consumption	<= 20uA
CM input range – low	<= 0.8V
CM input range – high	>= 1.5V
GBW	>= 5MHz

Commented [HO1]: CMRR is gm/gds higher than Av
Avdc + 40dB means gm/gds = 100 which is quite reasona

Design of NMOS input pair:

$$GBW = \frac{gm_{1,2}}{2\pi C_L} \geq 5MHZ \quad \rightarrow \quad gm_{1.2} \geq 157.07\mu S$$

$$i\ have\ current\ in\ input\ pair\ equal\ 10\mu A \ \rightarrow \ \frac{gm_{1,2}}{I_D} \geq 15.7$$

$$assume\ the\ load\ current\ mirror\ has\ the\ same\ r_o\ of\ input\ pair\ so\ A_v = gm_{1.2} * \frac{r_o}{2} \geq 50.12$$

$$so\ gm_{1.2} * r_o \geq 100.24 \quad \rightarrow \ gds_{2,4} \leq 1.57\mu S$$

$$i\ will\ take\ \frac{gm_{1.2}}{gds_{2,4}} = 110 \quad \frac{gm}{I_D} = 20$$

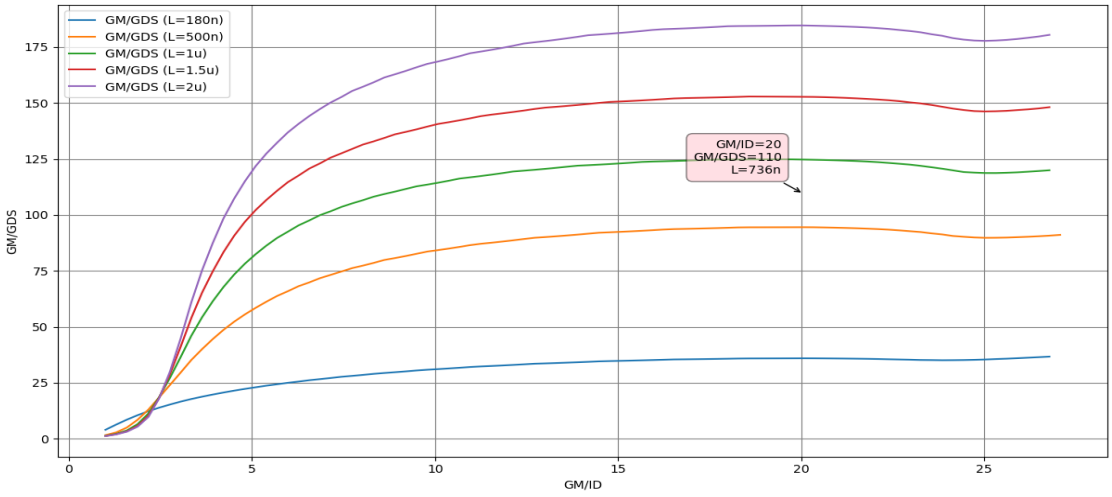

Figure 3 get length of input pair from ADT.

From ADT $L_{1,2} = 736nm$

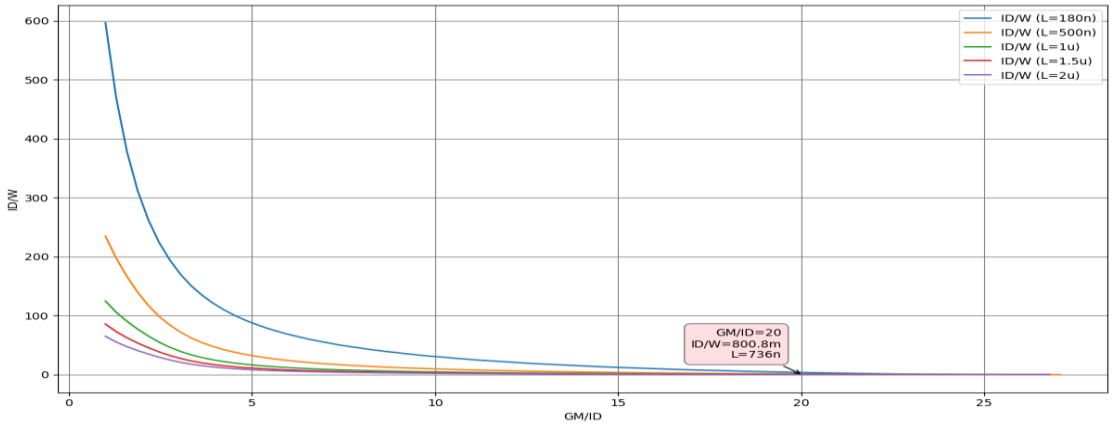

Figure 4 get w of pmos from ADT.

$$\frac{I_D}{W_{1,2}} = 800.8m \quad \rightarrow \quad W_{1,2} = 12.49\mu m$$

Design of PMOS Current Mirror Load:

Initially, assume $\frac{gm_{3,4}}{I_d} = 15 \;\; so \; gm_{3,4} = 150\mu S$

$\frac{gm_{3,4}}{gds_{3,4}} \rightarrow gds_{3,4} \leq 1.57\mu S \;\; \frac{gm_{3,4}}{gds_{3,4}} \geq 95.54 \quad i \; will \; take \; it \; 100$

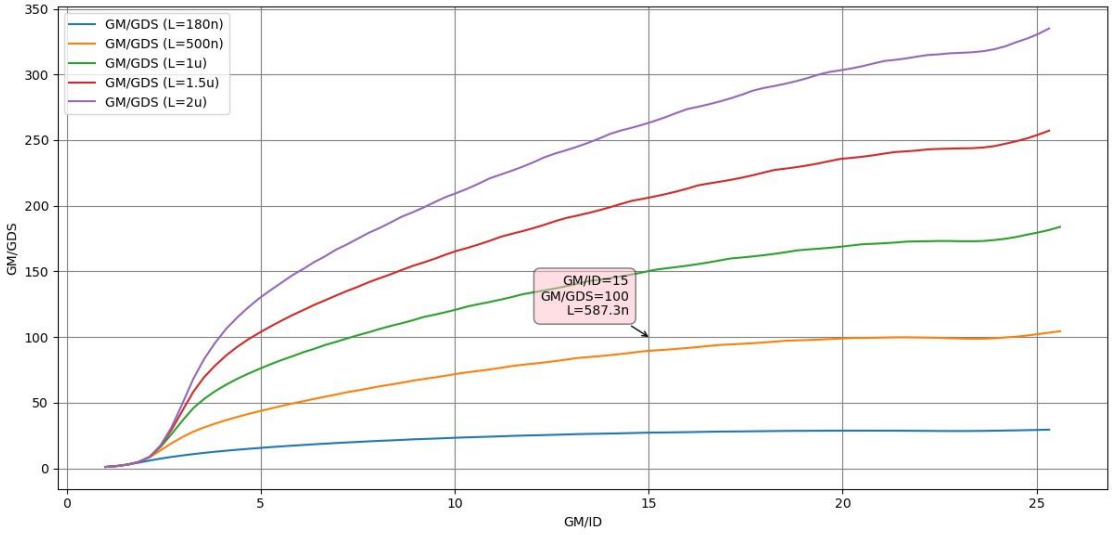

Figure 5 get L of PMOS from ADT.

From ADT $L_{3,4} = 587.3nm$

I have $CMRR_{HIGH} = V_{DD} - V_{GS3} - V_{DSAT1} + V_{GS1} \geq 1.5$

From ADT get value of V_{DSAT1}

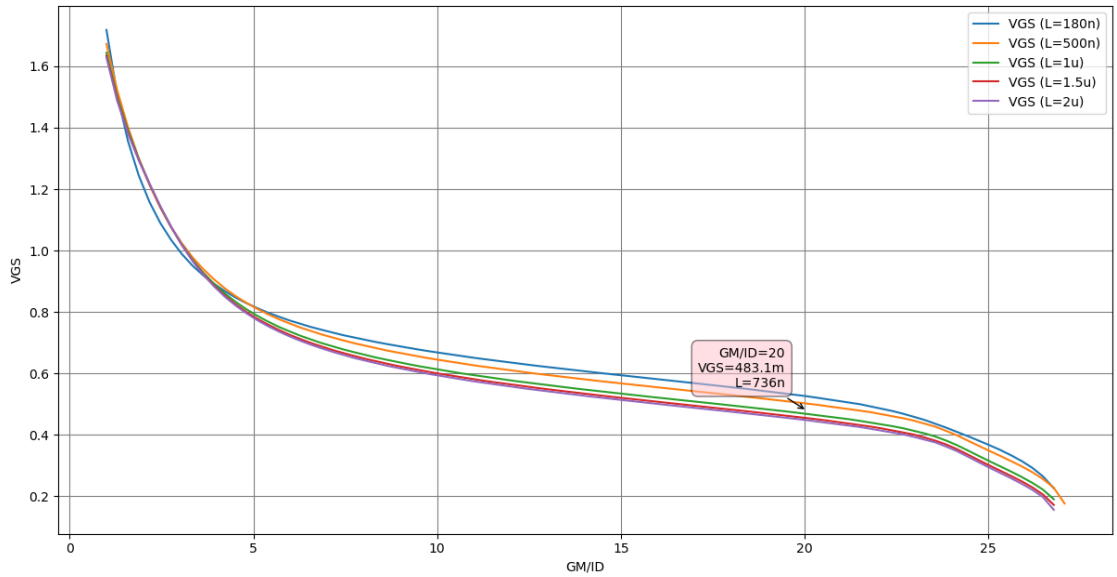

Figure 6 get vgs of NMOS input pair

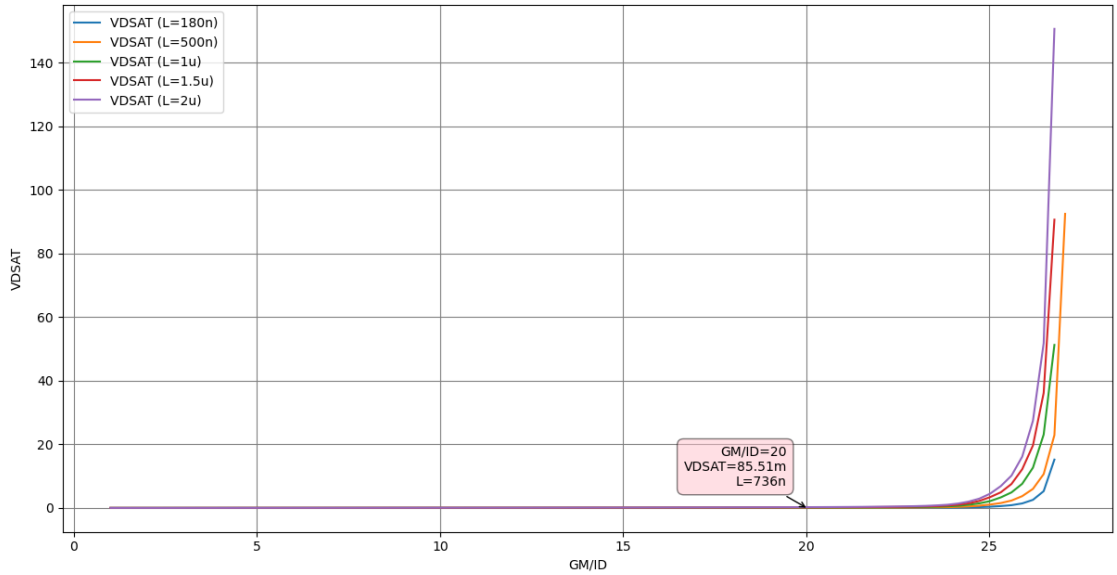

Figure 7 get vdsat of input pair NMOS.

So $V_{GS3,4MAX} = 697.59mV$

From this value of $V_{GS3,4}$ $get\ the \min of\ \frac{gm}{ID}$

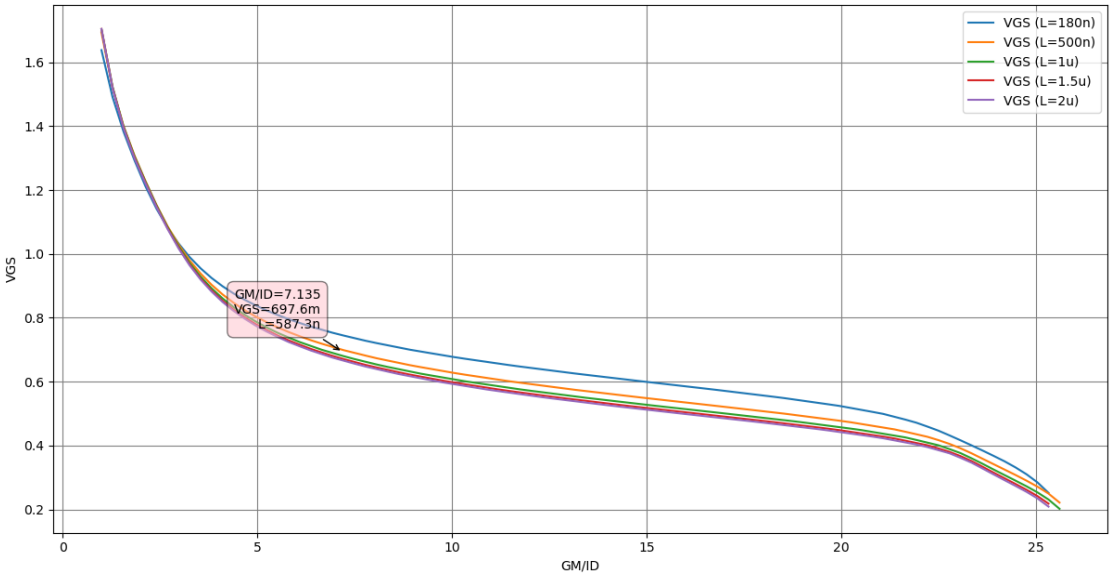

Figure 8 get min of gm/ID.

$$\frac{gm}{I_{D\ MIN}} = 7.135 \quad i\ will\ take\ \frac{gm}{ID} = 7.5$$

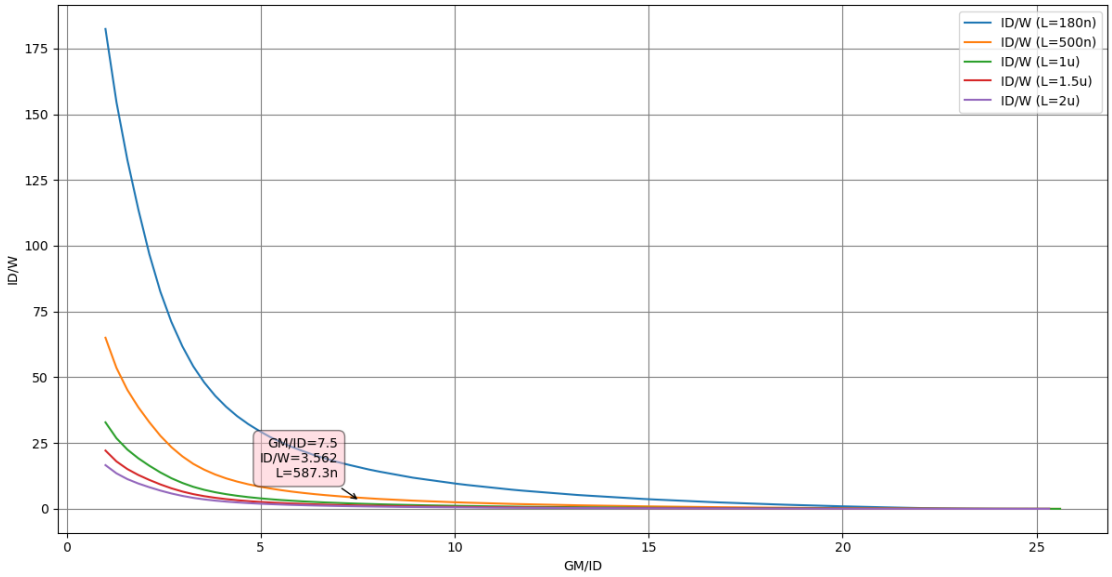

Figure 9 get w of PMOS

$$\frac{I_D}{W_{3,4}} = 3.562 \quad \rightarrow \quad W_{3,4} = 2.8\mu m$$

Design of Tail Current Mirror:

$CMRR = \frac{A_V}{A_{CM}} \geq 74$ So $A_{CM} \leq -40dB$

$A_{CM} = \frac{1}{2*gm_{3,4}*R_{SS}} \leq 0.01 \rightarrow gds_5 \leq 1.8\mu S$

Initially, assume $\frac{gm_5}{I_d} = 15$ $so\ gm_5 = 300\mu S$

So $\frac{gm_5}{gds_5} \geq 166.67$ $i\ will\ take\ it\ equal\ 175$

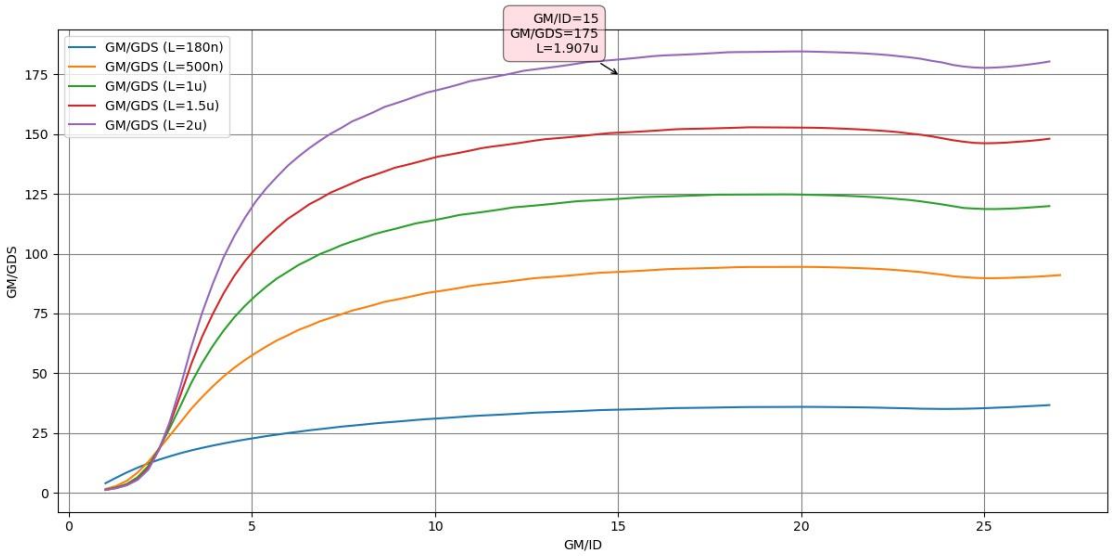

Figure 10 get L of NMOS5.

From ADT $L_{5,6} = 1.907\mu m$

I have $CMRR_{LOW} = V_{GS1} + V_{DSAT5} \geq 0.8$

$V_{DSAT5} \geq 316.9mV$

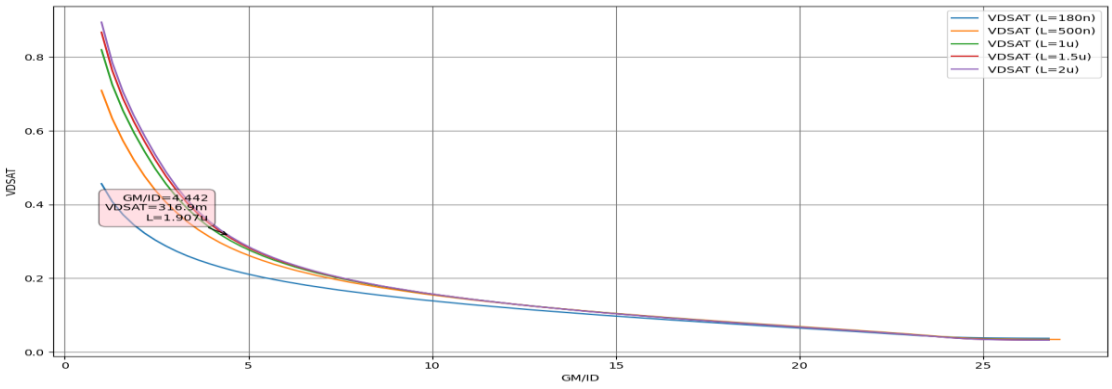

Figure 11 get min gm/ID of NMOS5

$\frac{gm}{I_{D\ MIN}} = 4.442 \quad i\ will\ take\ \frac{gm}{ID} = 13$

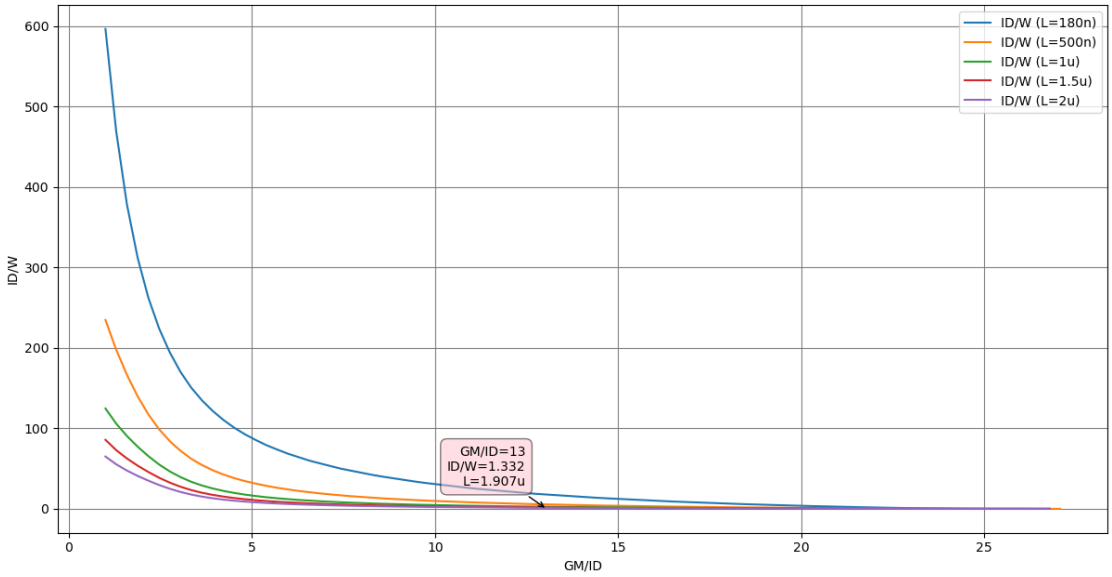

Figure 12 get w of NMOS_5.

$\frac{I_D}{W_5} = 1.332 \quad \rightarrow \quad W_5 = 7.5\mu m$

$W_6 = {}^{W_5}/_2 = 3.75\mu m$

	M1	M2	M3	M4	M5	M6
Width	12.49μ	12.49 μ	2.8 μ	2.8 μ	7.5 μ	3.75 μ
Length	736n	736n	587.3n	587.3n	1.907 μ	1.907 μ
gm	200 μ	200 μ	75 μ	75 μ	260 μ	130 μ
ID	10 μ	10μ	10 μ	10 μ	20 μ	10 μ
Gm/ID	20	20	7.5	7.5	13	13
V^*	0.1	0.1	0.266	0.266	0.154	0.154
V_{OV}	87m	87m	258.7m	258.7m	254.7m	255m
V_{DSAT}	85.5m	85.5m	208.5m	208.5m	166.2m	165.8m

Part 3: Open-Loop OTA Simulation[1]

Schematic of the OTA with DC node voltages clearly annotated.

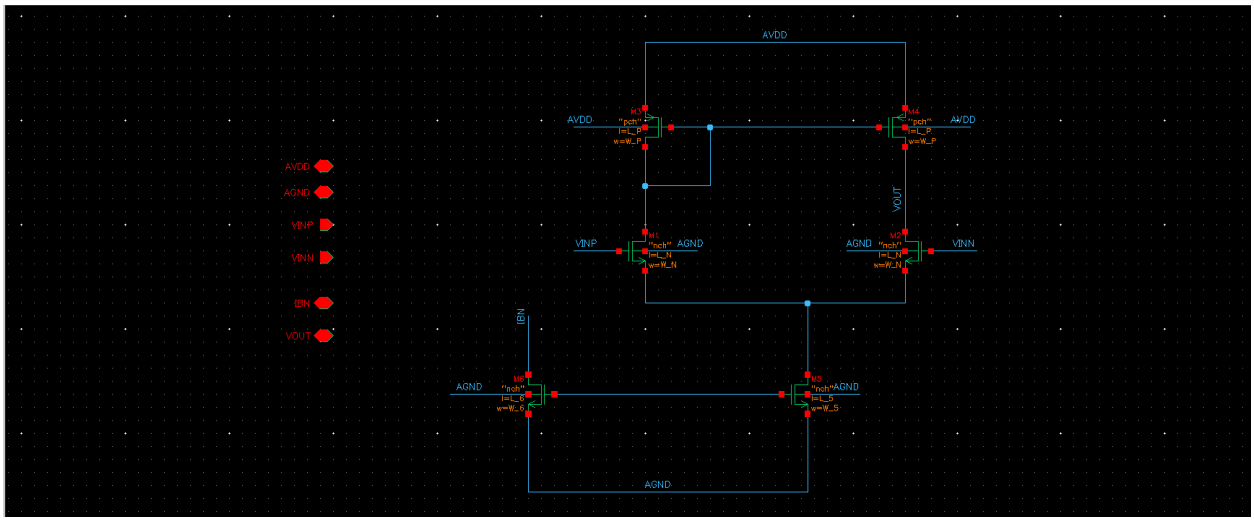

Figure 13 OTA Circuit schematic.

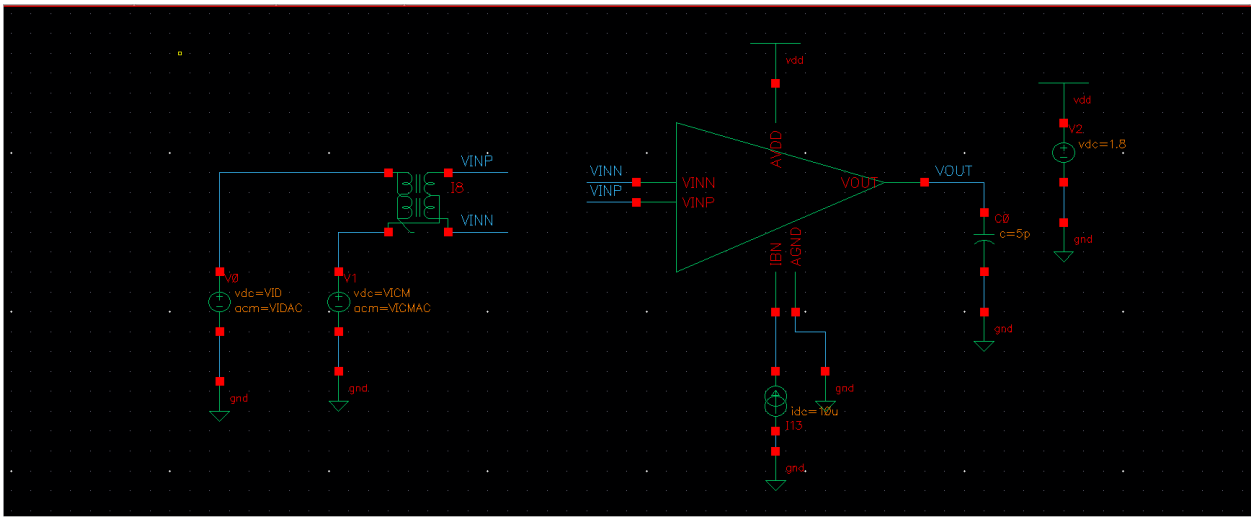

Figure 14 OTA Testbench.

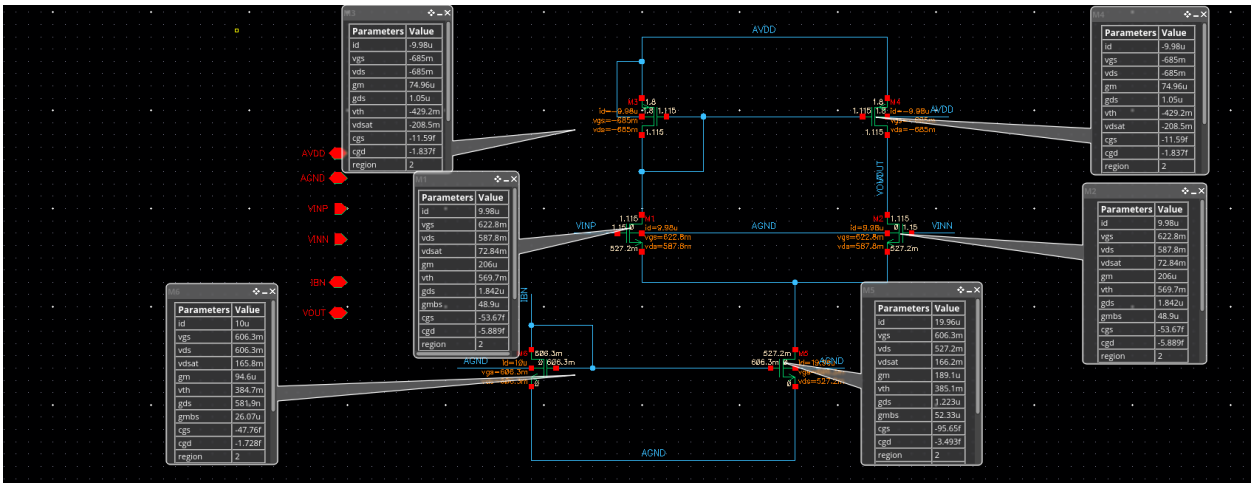

Figure 15 DC Operating point.

Is the current (and gm) in the input pair **exactly** equal? YES.

What is DC voltage at V_{OUT}? Why? 1.156V, The DC voltage of V_{OUT} is the same as VICM node V_F (the node of the diode connection). that's because V_{OUT} follows the V_F.

V_{OUT}=$VDD - V_{DS4} = 1.8 - 0.685 = 1.115V$.

Diff small signal ccs:

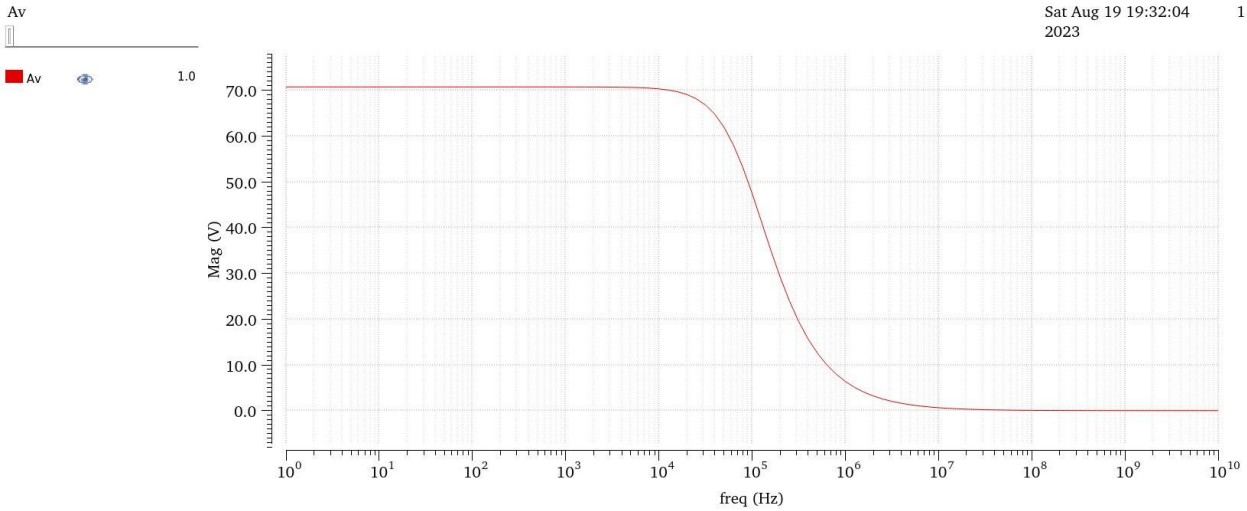

Figure 16 plot gain vs frequency.

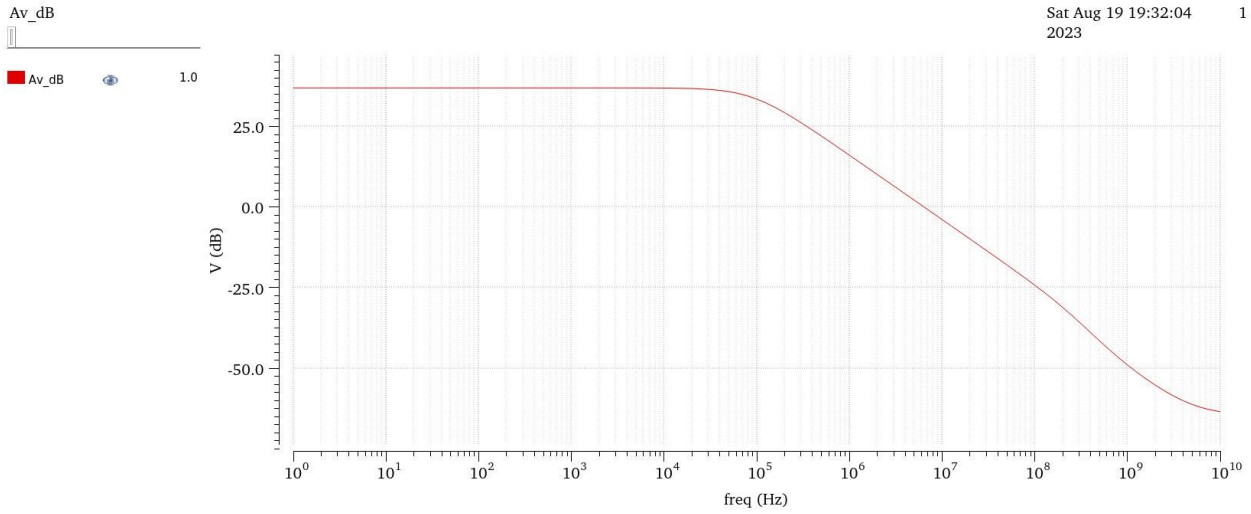

Figure 17 plot gain vs frequency in dB.

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab7_OTA_5T_1	Av				
lab7_OTA_5T_1	Av_dc mag	70.73			
lab7_OTA_5T_1	Av_dB				
lab7_OTA_5T_1	Av_dc mag dB	36.99			
lab7_OTA_5T_1	bw	90.66K			
lab7_OTA_5T_1	ugf	6.429M			
lab7_OTA_5T_1	gbw	6.428M			

Figure 18 results from simulator.

Hand analysis:

$$A_V = gm_1 * (r_{o2} || r_{o4}) = 206\mu * (\frac{1}{1.842\mu} || \frac{1}{1.05\mu}) = 71.23$$

GBW=$\frac{gm_{1,2}}{2\pi C_L} = \frac{206\mu}{2*\pi*5p} = 6.55MHZ$

$$BW = \frac{GBW}{Gain} = 92KHZ$$

	Simulator	Hand analysis
DC gain	70.73	71.23
DC gain dB	36.99	37
Bandwidth	90.66KHZ	92KHZ
GBW	6.428MHZ	6.55MHZ
UGF	6.429MHZ	6.55MHZ

CM small signal ccs:

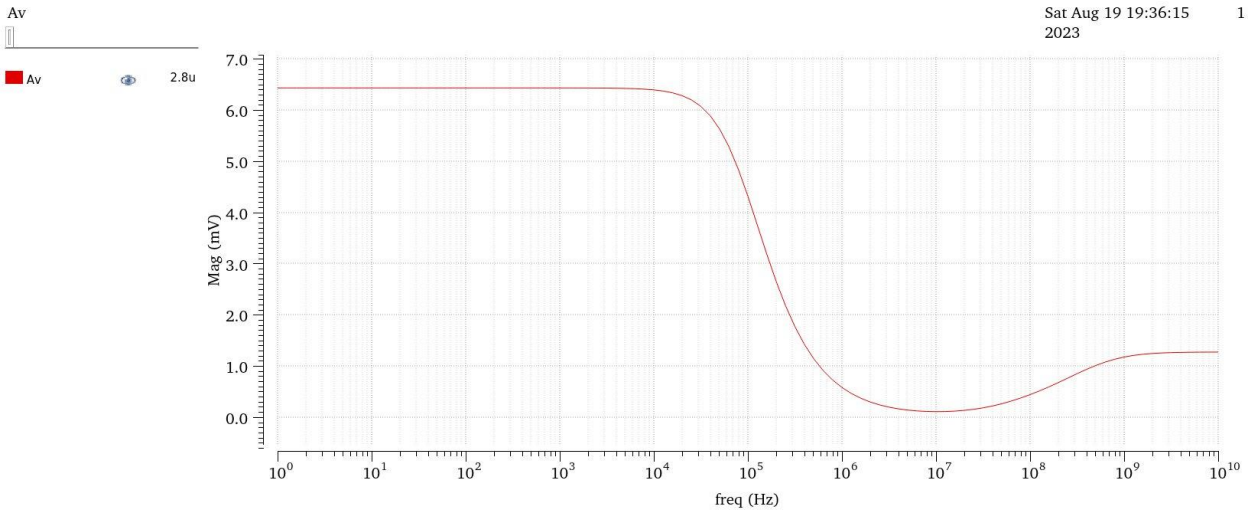

Figure 19 plot cm gain vs frequency.

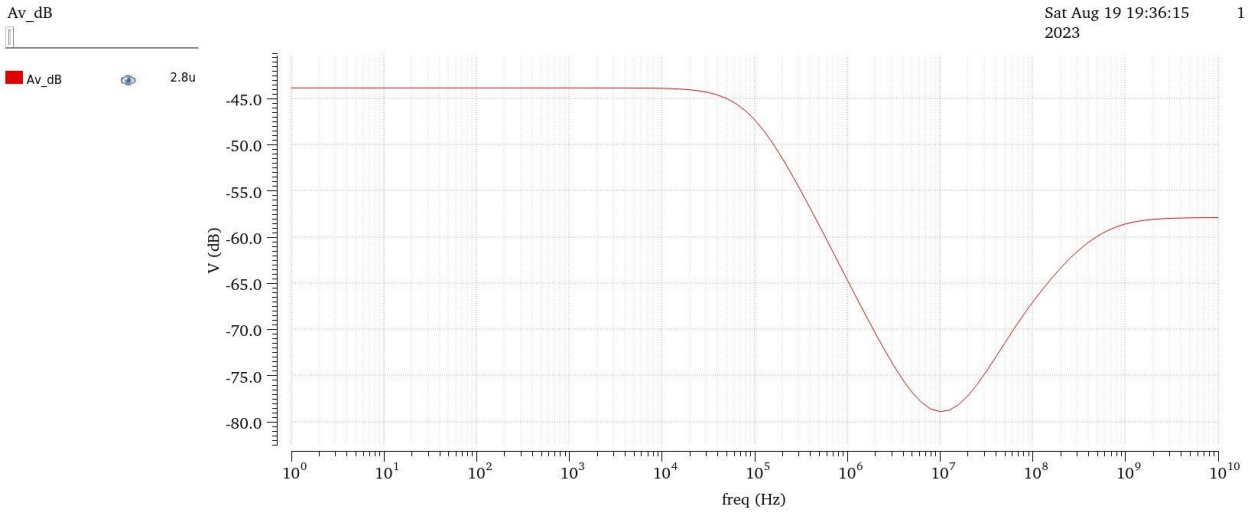

Figure 20 plot cm gain vs frequency in dB.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
lab7_OTA_5T_1	Av				
lab7_OTA_5T_1	Av_dc mag	6.438m			
lab7_OTA_5T_1	Av_dB				
lab7_OTA_5T_1	Av_dc mag dB	-43.83			
lab7_OTA_5T_1	bw	90.68K			
lab7_OTA_5T_1	gbw	585.1			

Figure 21 results from simulator.

Hand analysis:

$$A_{VCM} = \frac{1}{2*gm_{3.4}r_{o5}} = \frac{1}{2*74.96\mu*{}^{1}/_{1.223\mu}} = 8.15m = -41.8\,dB.$$

	Simulator	Hand analysis
DC gain in dB	-43.8	-41.8

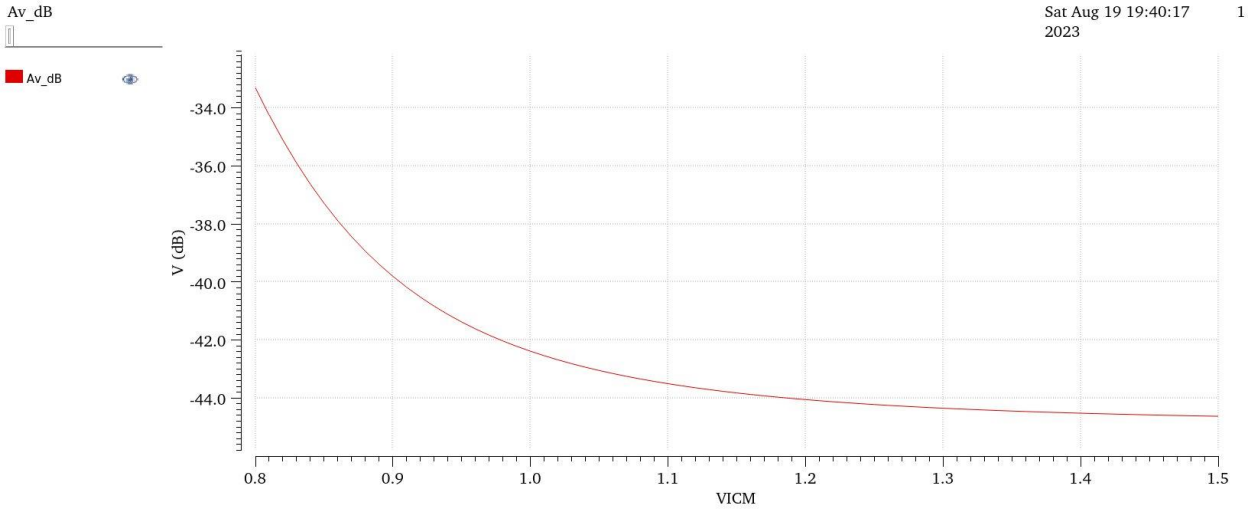

Figure 22 plot AVCM vs VINCM.

Comment: Av_{cm} decreases by increasing VI_{cm} we increase VDS_5 of the current mirror (VGS_1) so we increase its output resistance Rss and Av_{cm} is inversely proportional with Rss so it decreases.

CMRR:

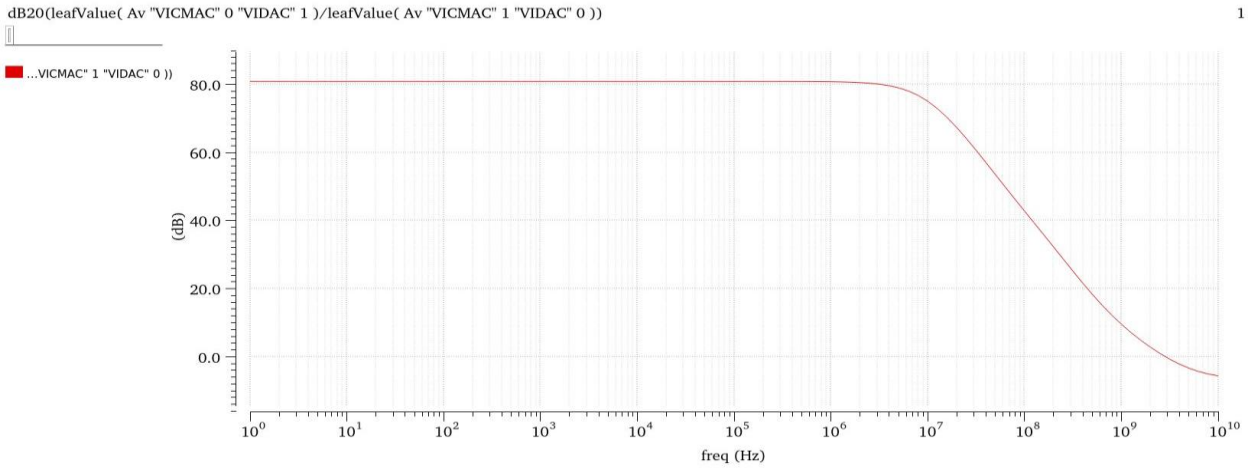

Figure 23 plot CMRR in dB vs frequency.

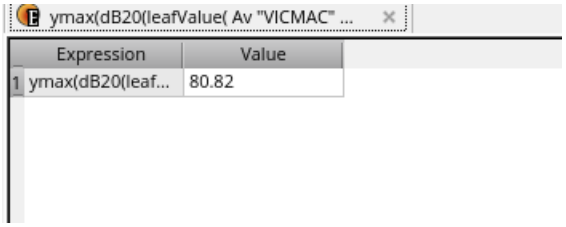

Figure 24 CMRR Value from simulator.

Hand analysis:

$$CMRR = \frac{A_{Vd}}{A_{Vcm}} = \frac{71.23}{8.15m} = 78.83\ dB.$$

	Simulator	Hand analysis
CMRR	80.82	78.83

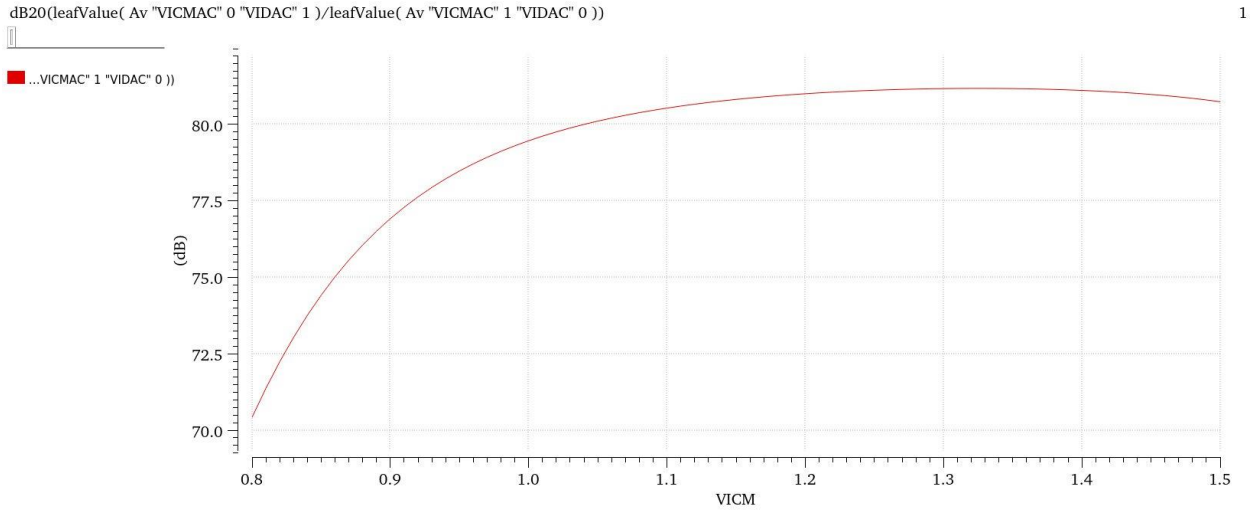

Figure 25 CMRR vs VICM.

- Comment: At first CMRR increases by increasing V_{icm} because R_{ss} of the mirror transistor increases and that degrades A_{vCM} but at higher values it decreases again as V_{icm} proportional with V_{GD1}(V_{icm}=$V_{GD1} - V_{GS3} + V_{DD}$) and V_{GS3} is constant so V_{GD1}increases and the condition of saturation is $V_{GD1} < V_{TH}$ so the input pair transistor is pushed towards the triode (not deeper into saturation) so r_{o1} decreases so CMRR decreases again (A_{vd} decreases).

Diff large signal ccs:

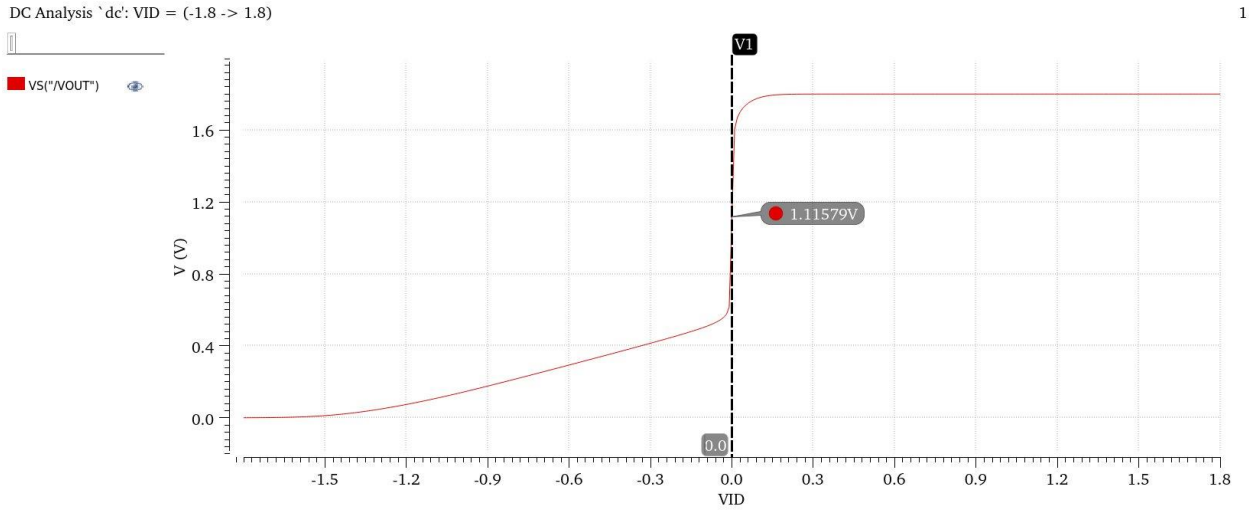

Figure 26 plot Vout vs Vid.

- From the plot, what is the value of V_{OUT} at VID = 0? Why?

From the plot, the value of V_{OUT} at Vid=0 is equal to VI_{CM} because that means that we don't inject any differential signal and we are only running a DC simulation with V_{DC}=VIN_{CM} so V_F =VI_{CM} so it's exactly the same as in requirement (1) that Vout follow V_F.

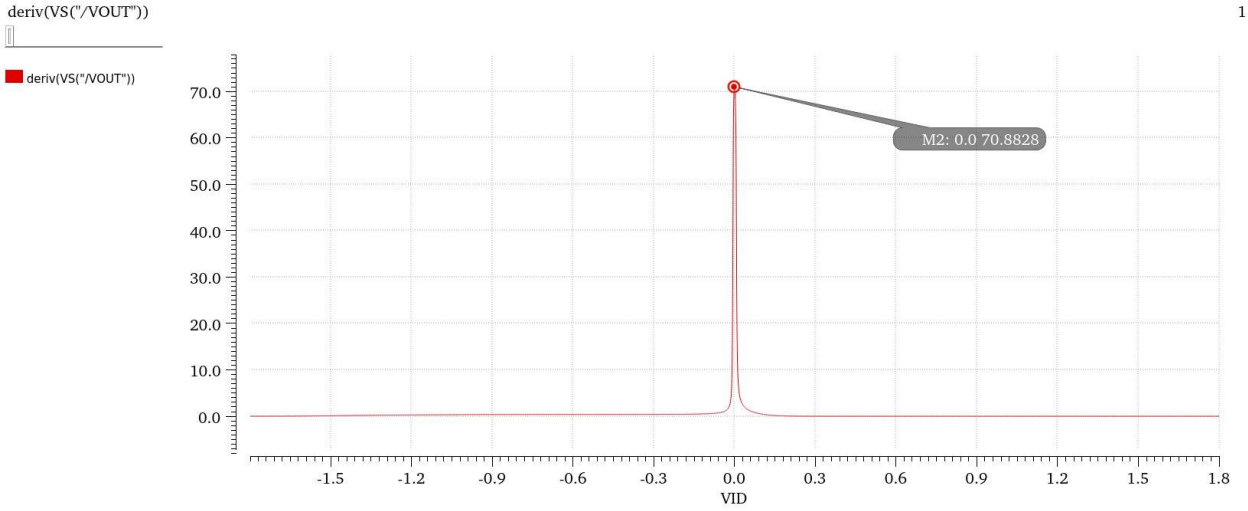

Figure 27 plot derivative of vout vs VID.

The derivative of V_{OUT} vs V_{ID} is the differential gain, the peak of the curve is almost exactly equal to the differential gain Ao of the circuit.

	Differential gain	PEAK
DC gain	70.73	70.88

CM large signal ccs (region vs VICM):

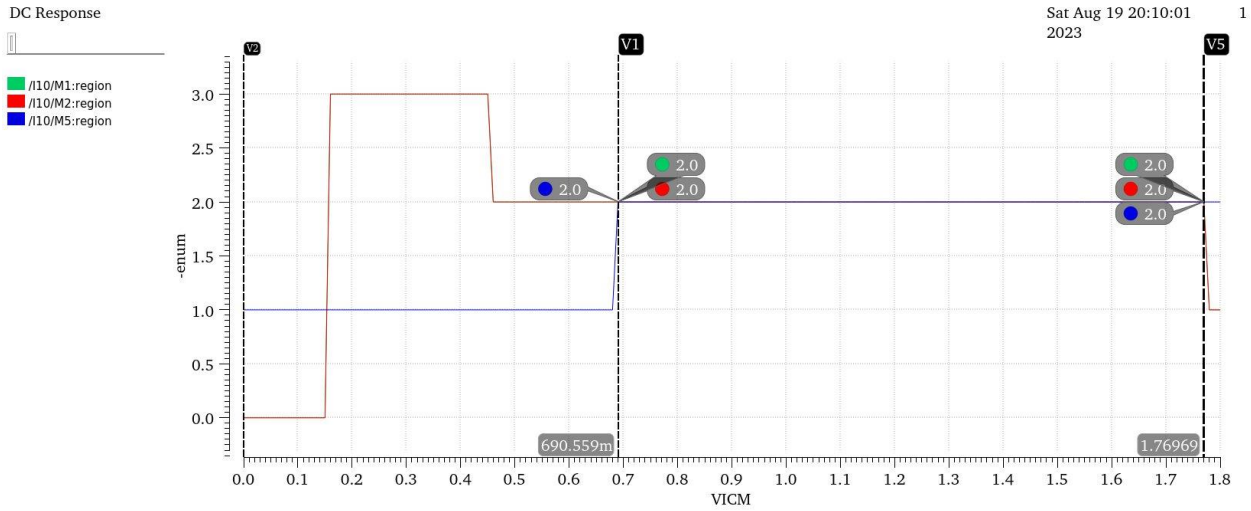

Figure 28 Plot regions vs VICM

$$CMIR_{RANGE} = 1.76969 - 690.599m = 1.08V$$

Hand analysis:

$$CMIR_{LOW} = V_{GS1} + V_{DSAT5} = 622.8m + 166.2m = 789mv$$

$$CMIR_{HIGH} = V_{DD} - V_{GS3} - V_{DSAT1} + V_{GS1} = 1.8 - 685m - 72.84m + 622.8m = 1.665v$$

$$CMIR_{RANGE} = 1.665 - 789m = 876mv$$

	Regions	Hand analysis
Min	690.6m	789m
Max	1.77	1.665
Range	1.08	876m

(Optional) CM large signal ccs (GBW vs VICM):

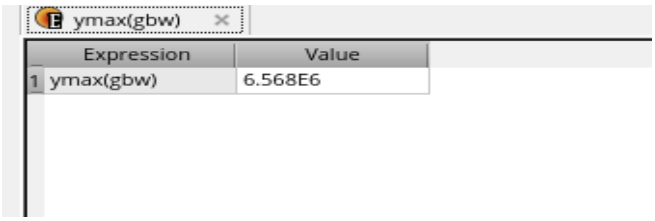

Figure 29 get max value of GBW.

$$GBW_{90\%} = 6.568 * 0.9 = 5.9112M$$

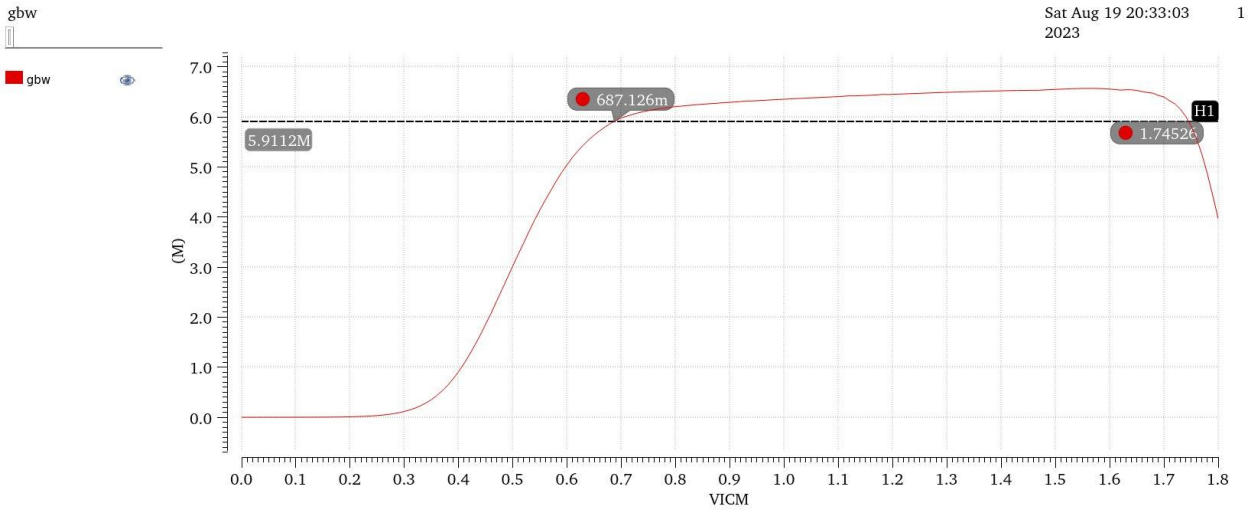

Figure 30 plot GBW VS VINCM.

$$CMIR_{RANGE} = 1.74526 - 687.126m = 1.058V$$

	Regions	GBW
MIN	690.6m	687.126m
MAX	1.77	1.74526
RANGE	1.08	1.058

The GBW is way better than the regions as the regions first is a simulation parameter only and second has a very sharp edged between transitions while the GBW is a logical and experimental way to tell the valid range and leaves the designer to his own estimation whether he accepts 90% of the output or maybe less.

PART 4: Closed-Loop OTA Simulation

DC point

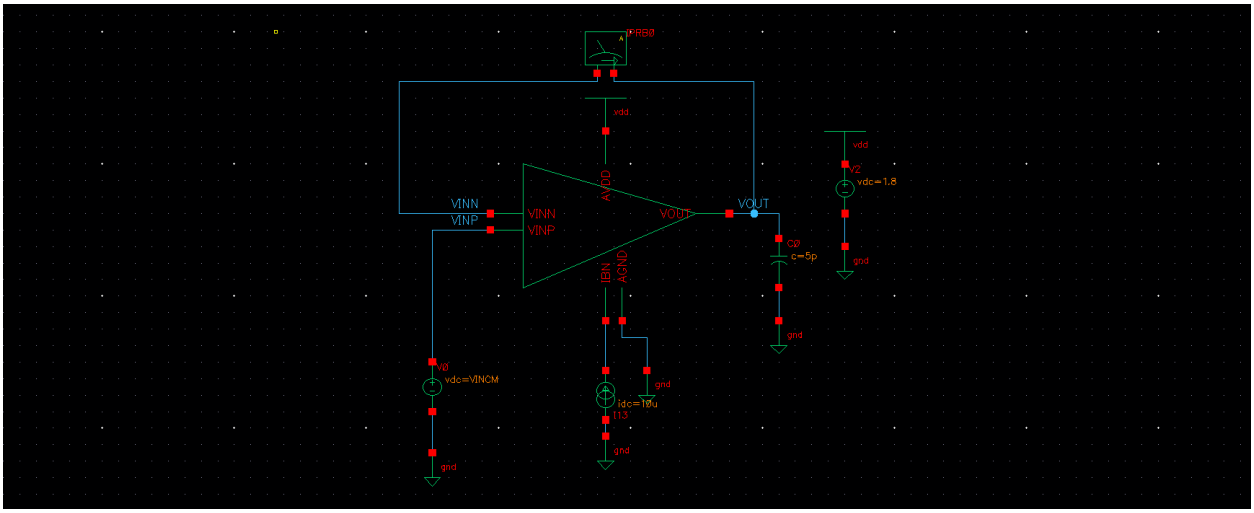

Figure 31 schematic of closed loop OTA.

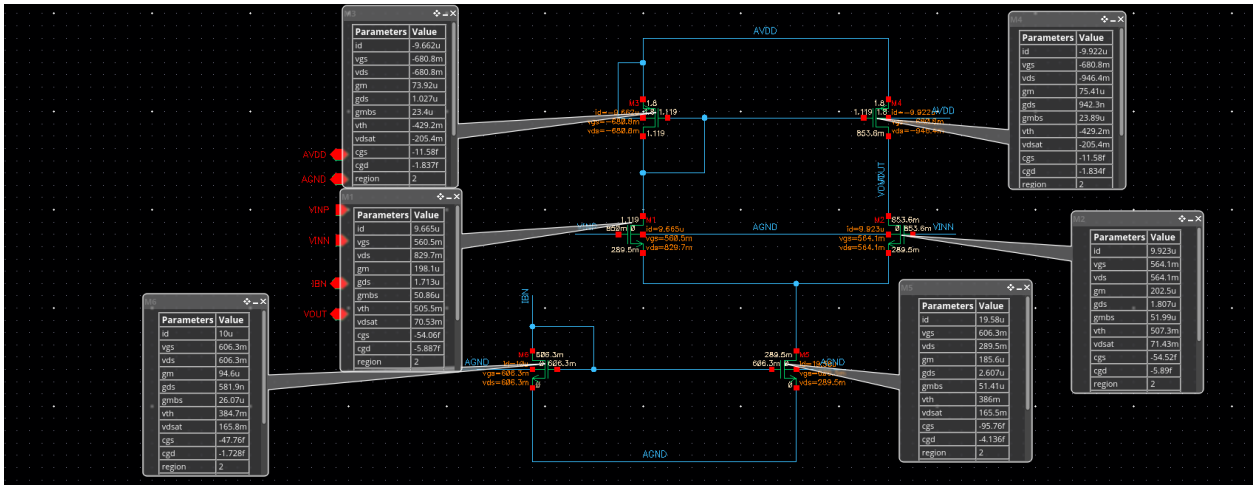

Figure 32 DC Operating point.

Comment: NO, the current and gm of the input pair is not exactly equal the 5T-OTA in a closed-loop unity gain buffer, the output voltage will change a little bit from the input common mode level just to match the input voltage. The non-zero differential input voltage will cause the imbalance of the two sides of the differential pair. This imbalance is just like the mismatch, it will make a small mismatch in the gm and current of the sides of the differential pair which we will calculate in the next step.

Mismatch calculations:

$\Delta_{ID} = 9.923 - 9.665 = 0.258\mu A$

$\Delta_{gm} = 202.5 - 198.1 = 4.4\mu S$

$$mismatch\ ID = \frac{\Delta_{ID}}{ID_{part1}} = \frac{0.258}{9.98} * 100 = 2.585\%$$

$$mismatch\ gm = \frac{\Delta_{gm}}{gm_{part1}} = \frac{4.4}{206} * 100 = 2.136\%$$

Loop gain

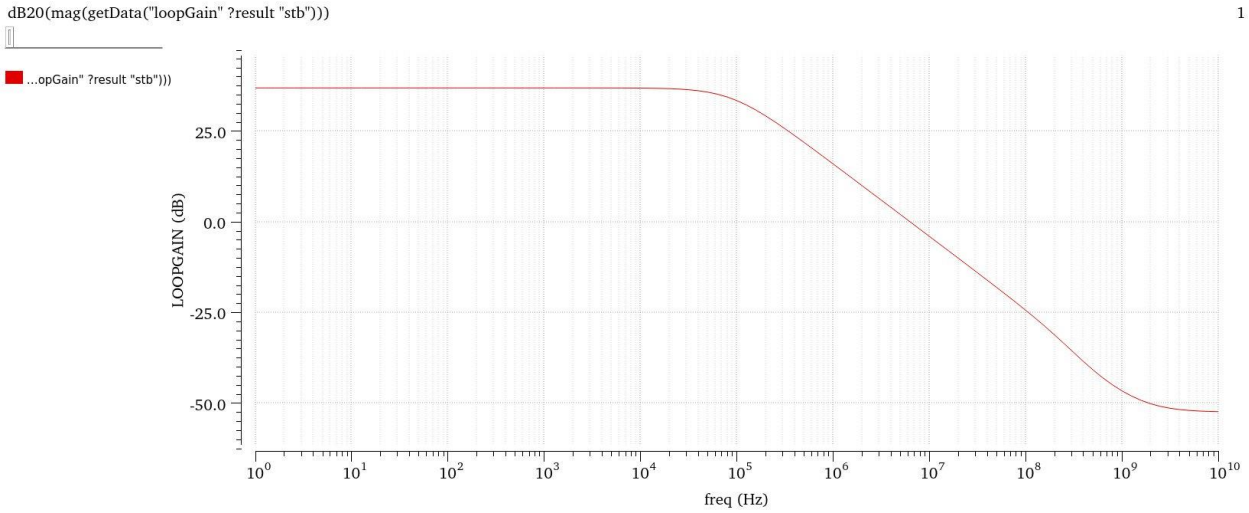

Figure 33 plot Loop gain vs frequency

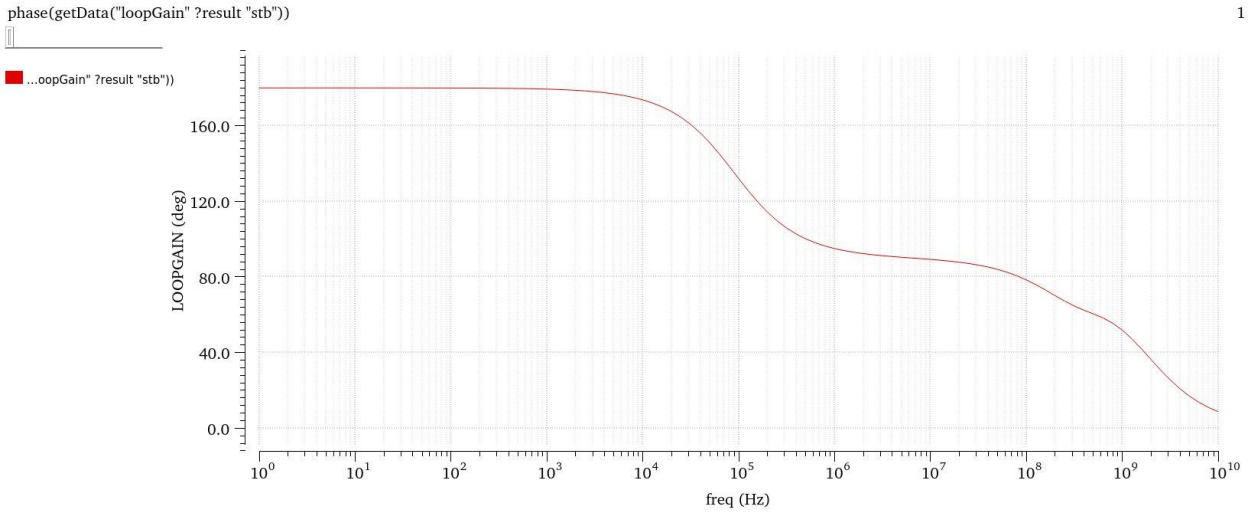

Figure 34 plot phase of loop gain vs frequency.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Filter	Filter	Filter	Filter	Filter	Filter
lab7_OTA_5T_cl...	/VOUT				
lab7_OTA_5T_cl...	DC gain	70.44			
lab7_OTA_5T_cl...	DC gain dB	36.96			
lab7_OTA_5T_cl...	GBW	6.365M			

Figure 35 Results from simulator

	Open loop	Loop gain
DC gain	70.73	70.44
DC gain in dB	36.99	36.96
GBW	6.428M	6.365M

Hand analysis:

$$A_V = gm_1 * (r_{o2}||r_{o4}) = 198.1\mu * (\frac{1}{1.807\mu} \,||\, \frac{1}{942.3n}) = 72.04$$

GBW=$\frac{gm_{1,2}}{2\pi C_L} = \frac{202.5\mu}{2*\pi*5p} = 6.446MHZ$

	Simulator	Hand analysis
DC gain	70.44	72.04
DC gain in dB	36.96	37.15
GBW	6.365M	6.446M

Comment: The DC gain and GBW are almost the same in the closed loop as the open loop as the feedback network is just a wire (buffer) so the loop gain is equal to B*AOL and B=1 so the results are almost the same.

Part 5 (optional): Effect of Mismatch on CMRR

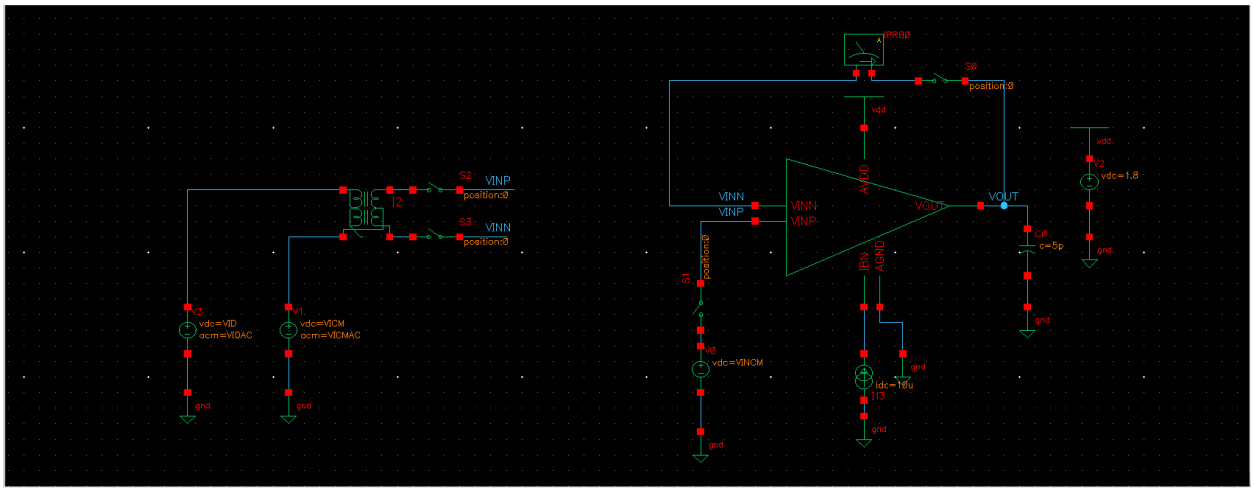

Figure 36 schematic.

1) CM small signal ccs:

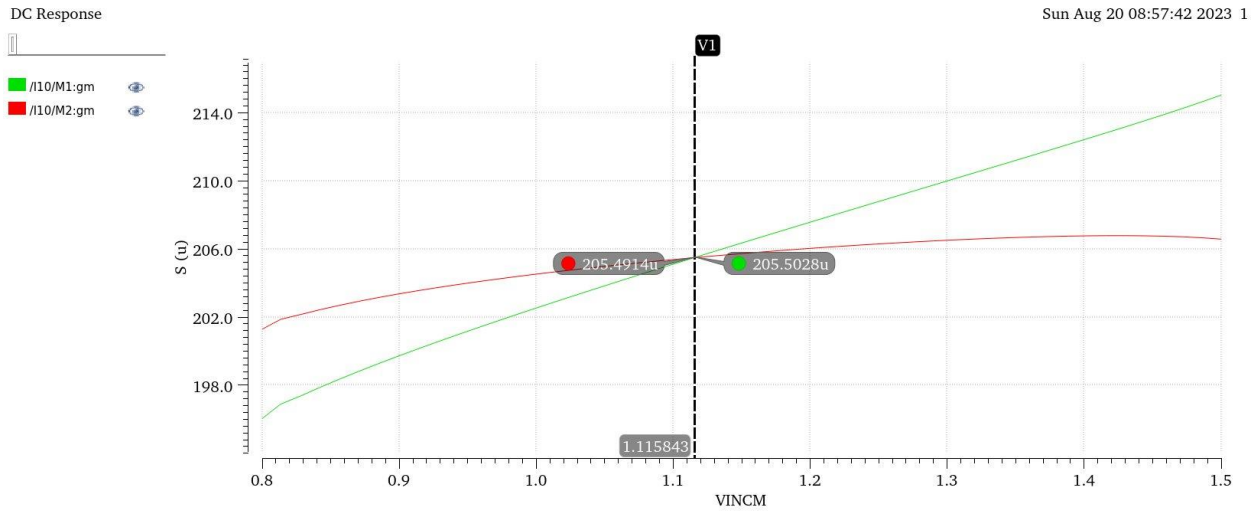

Figure 37 Plot gm vs VINCM.

• The two gm's intersect (are equal) at a specific VIN. Why? What is AV_{CM} at this value.

At 1.115843 V the two curves intersect because at this point there is no mismatch.