# Part 1: Differential Amplifier Design

1) We want to design a resistive loaded differential amplifier with the specifications below.
**NOTE:** that the bias current is split between two transistors; each transistor gets $I_D = 20\mu A$.

| Parameter | |
|---|---|
| **Supply ($V_{DD}$)** | $1.8V$ |
| **Bias current ($I_{SS}$)** | $40\mu A$ |
| **Differential gain** | $8$ |
| **CM output level**[1] | $V_{DD}/3$ |
| **Load capacitance** | $1pF$ |

[1] Note that $I_{SS}R_D = 2V_{out-CM}$ must be smaller than $(V_{DD} - V_{dsat3})$ for proper large signal characteristics, why?

2) Since the output level is closer to the ground rail, we will use a PMOS input stage. Assume the PMOS will not be placed in a dedicated well to save the area. Assume we will use a simple current mirror for biasing.

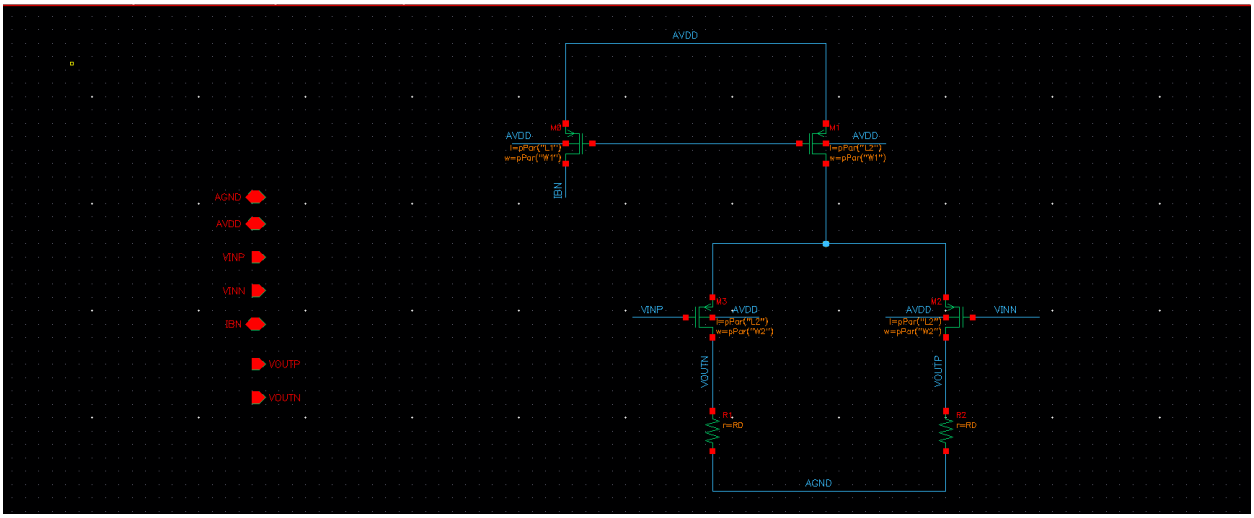


*Figure 1 schematic*

•**Choose $R_D$** to meet the CM output level spec. $R_D = \frac{V_{RD}}{I} = \frac{0.6}{20\mu} = 30K\Omega$.

•The differential amplifier gain is given by

$$|A_v| \approx g_m(R_D||r_o)$$

•We will choose $L$ to set $r_o \gg R_D \rightarrow r_o = 10 \times R_D$.

$$|A_v| \approx 0.91 \times g_m R_D = 0.91 \times 2\frac{I_D}{V^*} \times R_D = 1.82\frac{V_{RD}}{V^*}$$

•**Choose $V^*$** to meet the differential gain spec.

$$\boldsymbol{V^* = \frac{1.82V_{RD}}{A_V}}$$

•Assume we will set $V_{DS}$ of the tail current source to $300mV$ to allow more output swing. **Report the input pair sizing using SA.**

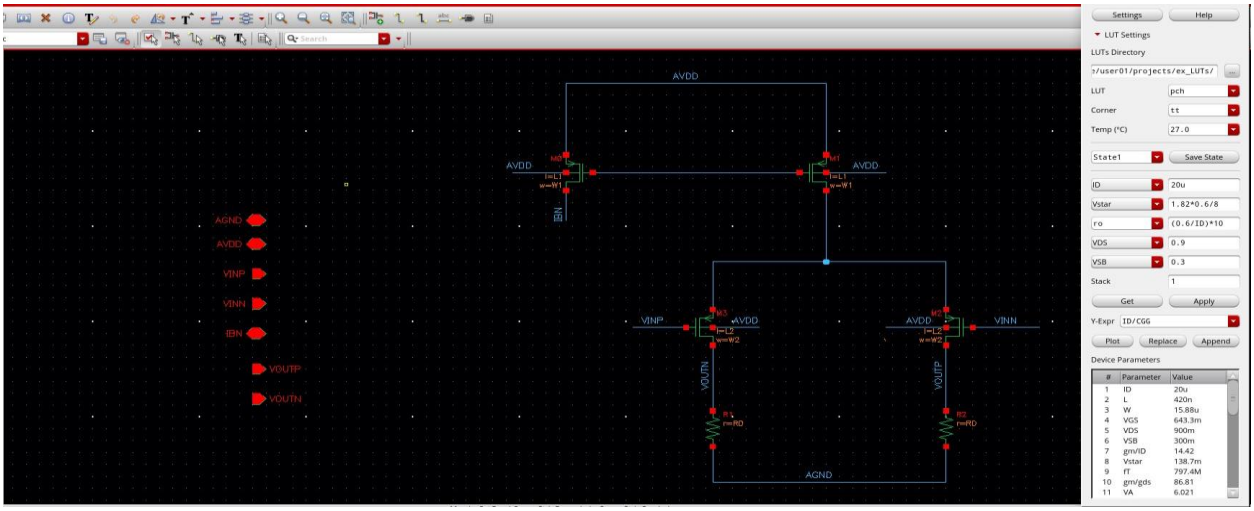


*Figure 2 sizing assistant parameters.*

From sizing assistant parameters is $W = 15.88\mu m \quad L = 420nm. \quad V_{TH} = 533.7mV$

•Give the above assumption, calculate the CM input level. **Calculate** the min and max CM input levels. Is the selected CM input level in the valid range?

$$VINCM_{LEVEL} = 1.8 - 300m - VGS_{DIFF} = 1.8 - 300m - 643.3m = 856.7mV$$

$$VINCM_{MIN} = V_{RD} - V_{TH} = 0.6 - 527.4m = 72.6mV$$

$$VINCM_{MAX} = V_{DD} - V^* - VGS_{DIFF} = 1.8 - 138.7m - 643.3m = 1.0202V$$

Yes, CM input level in the range.

•The tail current source has the following specifications:

| **Parameter** | |
|---|---|
| **Input current** | $20\mu A$ |
| **Percent mismatch:** $\boldsymbol{\sigma(I_{out})/I_{out}}$ | $\leq 2\%$ |
| **Compliance voltage** | $\leq 200mV$ |
| **Area** | Minimize |

10)

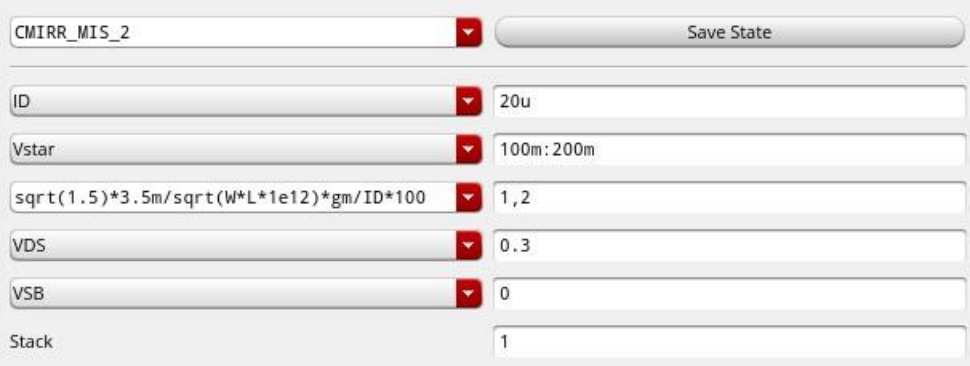


*Figure 3 sizing assistant.*

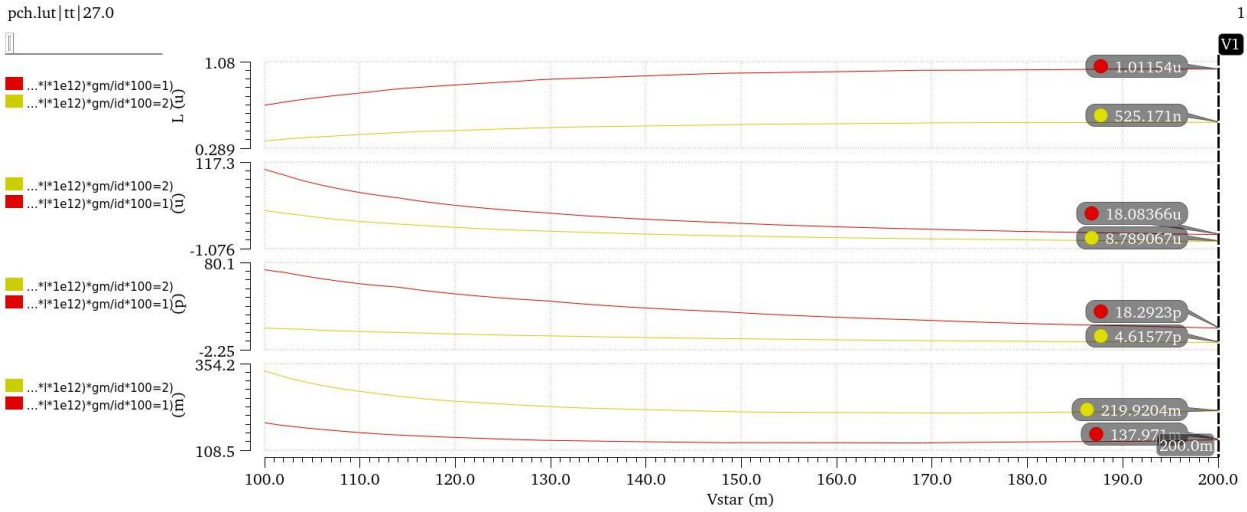


*Figure 4 plot parameters vs v**

•As seen in the plot, for a given mismatch requirement, the minimum area is achieved at the max $V^*$. Similarly, for a given area requirement, the minimum mismatch is achieved at the max $V^*$. That's why current mirrors are commonly biased in strong inversion.

•Given the compliance voltage spec, **report** the above figure with a cursor added to the selected design point.

From the graph $W = 8.79\mu m \quad L = 525.171nm$

# Part 2: Differential Amplifier Simulation

## OP simulation

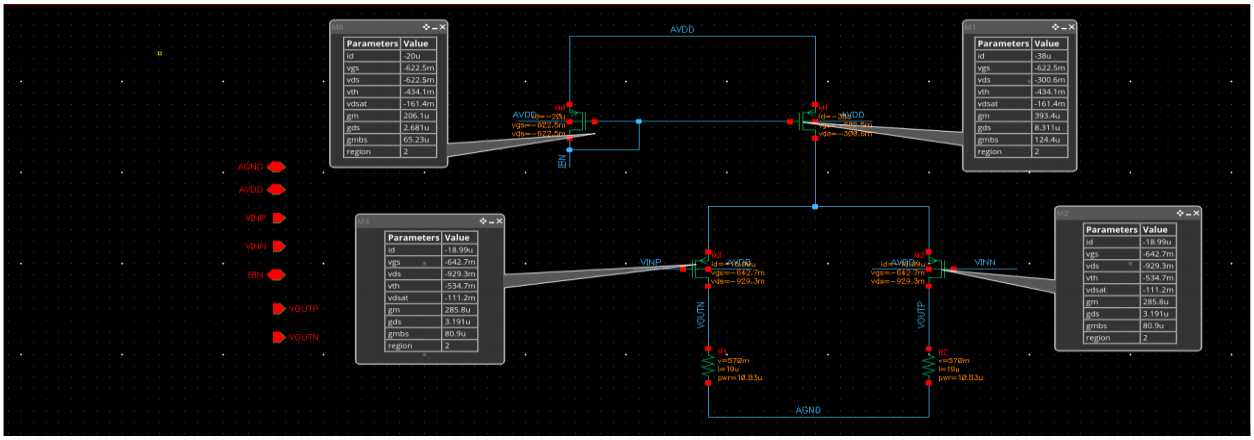


*Figure 5 DC Operating point*

All transistors operate in saturation.

## Diff small signal ccs

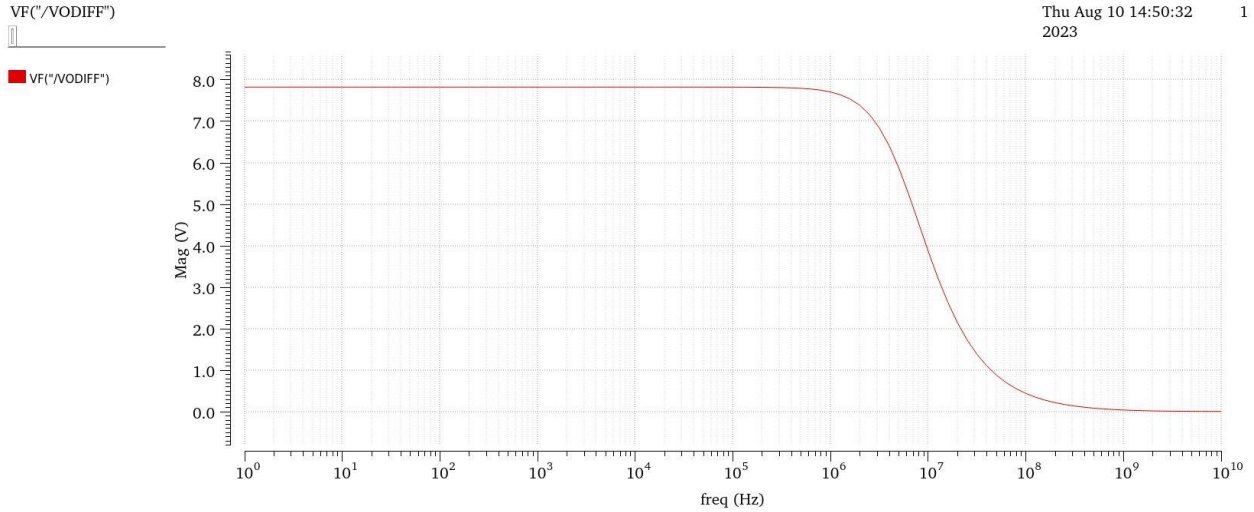


*Figure 6 plot VODIFF vs frequency*

| Name | Type | Details | Value | Plot | Save | Spec |
|---|---|---|---|---|---|---|
| | expr | VF("/VODIFF") | | ☑ | ☐ | |
| | expr | ymax(mag(VF("/VODIFF"))) | 7.827 | ☑ | ☐ | |
| | expr | dB20(VF("/VODIFF")) | | ☑ | ☐ | |
| | expr | ymax(dB20(VF("/VODIFF"))) | 17.87 | ☑ | ☐ | |
| | expr | bandwidth(VF("/VODIFF") 3 "low") | 5.697M | ☑ | ☐ | |

ymax(dB20(VF("/VODIFF")))

*Figure 7 results from simulator*

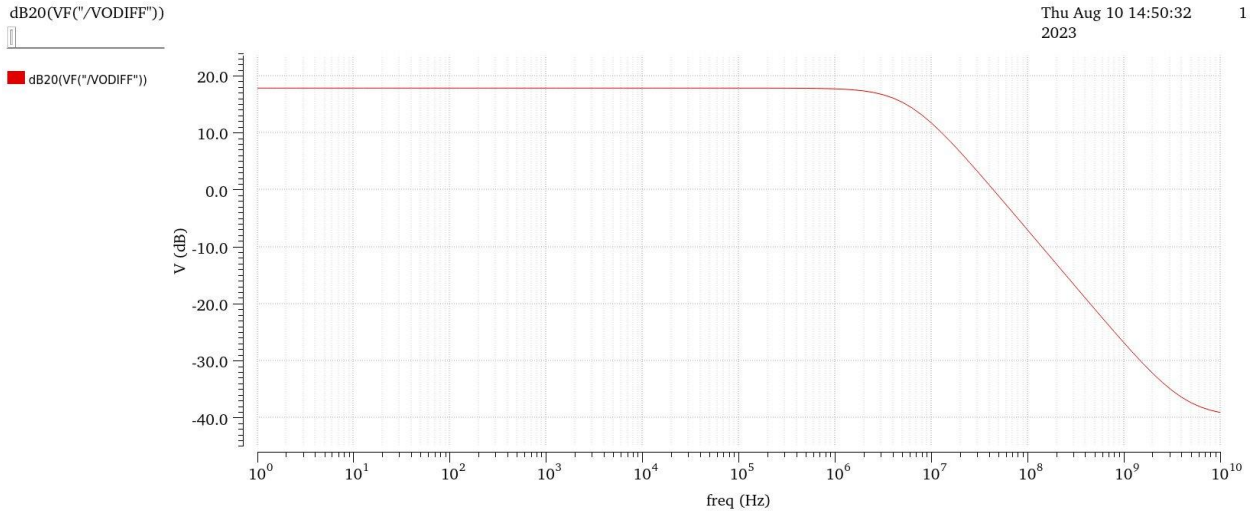


*Figure 8 plot VODIFF vs frequency in dB*

Hand analysis:

$$A_{Vd} = gm(R_D||r_o) = 285.8\mu * (30K \,||\, \frac{1}{3.191\mu}) = 7.825$$

$$bandwidth = \frac{1}{2\pi(R_D||r_o)*(C_{gd}+C_{db}+C_L)} = 5.67MHZ$$

| | Simulator | Analytical |
|---|---|---|
| Gain | 7.827 | 7.825 |
| bandwidth | 5.697MHZ | 5.67MHZ |

## CM small signal ccs

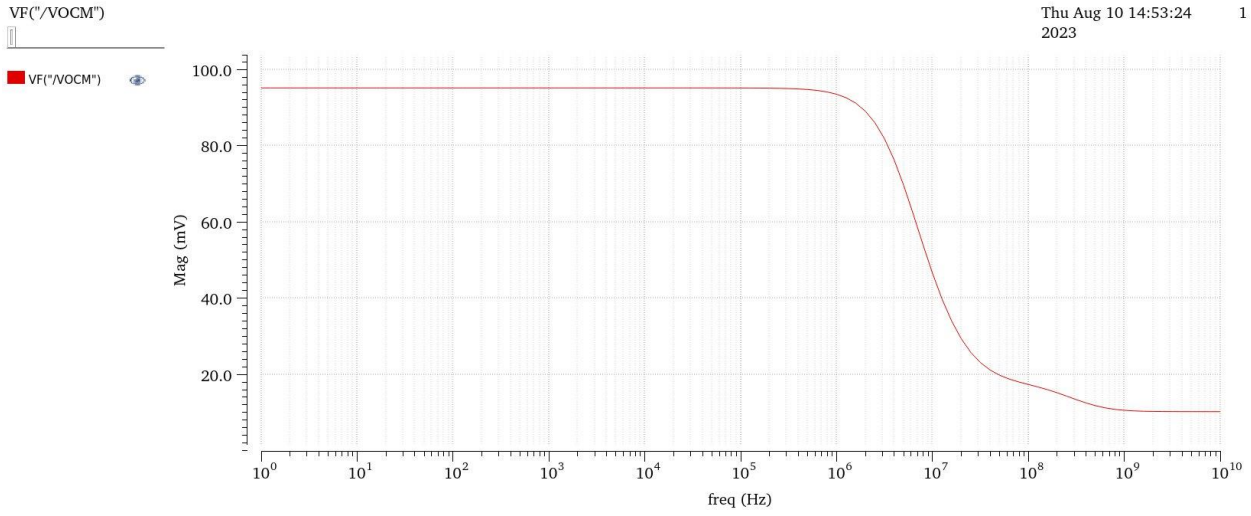


*Figure 9 plot VOCM vs frequency*

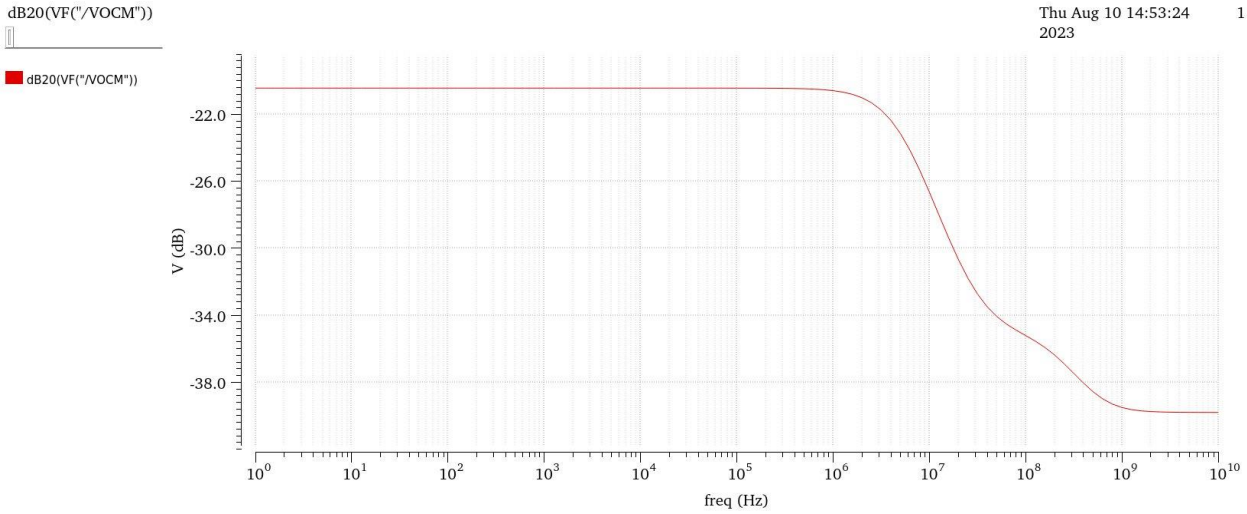


*Figure 10 plot VOCM vs frequency*

| Test | Output | Nominal | Spec | Weight | Pass/Fail |
|---|---|---|---|---|---|
| Filter | Filter | Filter | Filter | Filter | Filter |
| LAB06_Different... | VF("/VOCM") | | | | |
| LAB06_Different... | ymax(mag(VF("/... | 95.16m | | | |
| LAB06_Different... | dB20(VF("/VOC... | | | | |
| LAB06_Different... | ymax(dB20(VF("... | -20.43 | | | |
| LAB06_Different... | bandwidth(VF("/... | 5.388M | | | |

*Figure 11 results from simulator*

Hand analysis:

$$A_{VCM} = \frac{gm\, R_D}{1+2(g_m+g_{mb})r_{o1}} = 96m$$

| | Simulator | Analytical |
|---|---|---|
| Gain | 95.16m | 96m |

•Yes, the gain is smaller than one as expected to reject the CM signal.

• The system first faces the dominant pole which gives the -20db/dec that the graphs shows Then it faces a zero which tries to increase the slope which shows the slight increase in slope at about 10^7 Hz then comes the non-dominant pole which decreases the slope again, because tail current source is shunted by capacitance so at high frequency another pole due to this capacitance come to action which effects on bode plot and also impedance increases.

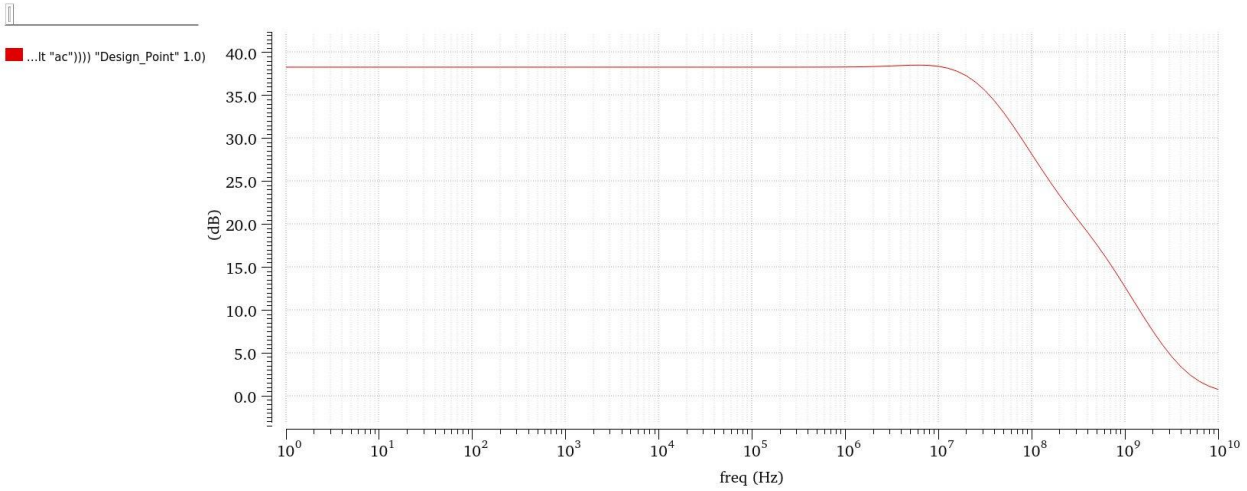


*Figure 12 plot Avd/Avcm*

From simulator CMMR = 38.2852dB

$$CMMR = \frac{A_{vd}}{A_{vcm}} = \frac{\left(g_m(R_D||r_o)\right)}{\left(\frac{g_m R_D}{1+2(g_m+g_{mb})R_{ss}}\right)} = 81.5 = 38.223\text{dB}.$$

| | Simulator | Analytical |
|---|---|---|
| CMMR | 38.2852dB | 38.223dB |

the same reason for the variations of AVCM because the system faces dominant pole then it faces a zero which slightly increase the slope then face another pole which continue to the end, due to capacitance which shunt Rss and decrease impedance and come into action with pole.

## Diff large signal ccs

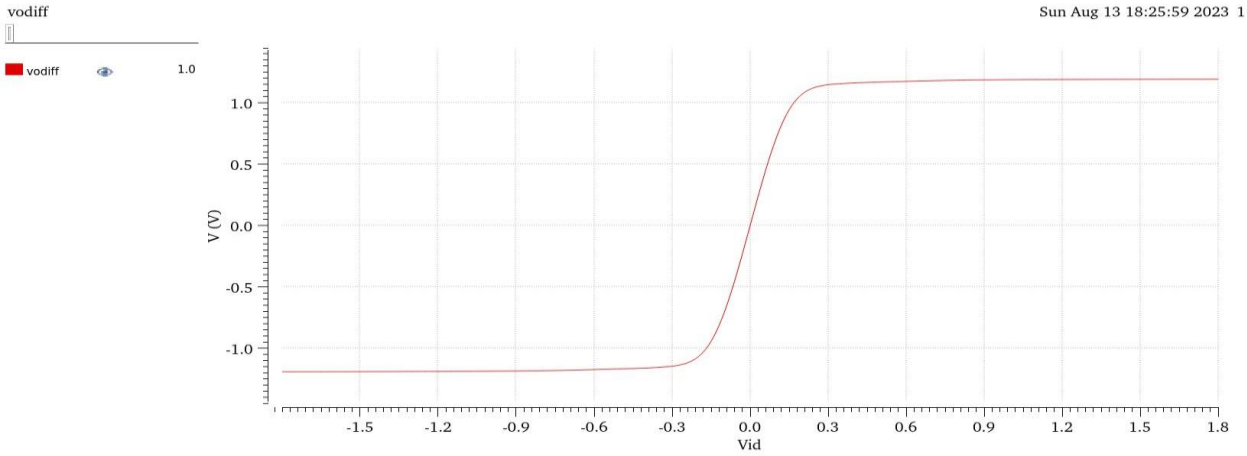


*Figure 13 plot VODIFF vs Vid*

The analytical range:

$-I_{SS}\,R_D \;\rightarrow\; I_{SS}R_D \quad -1.2 \;\rightarrow 1.2$

The simulator range:

-1.194 → 1.194

## CM large signal ccs (region vs VICM)

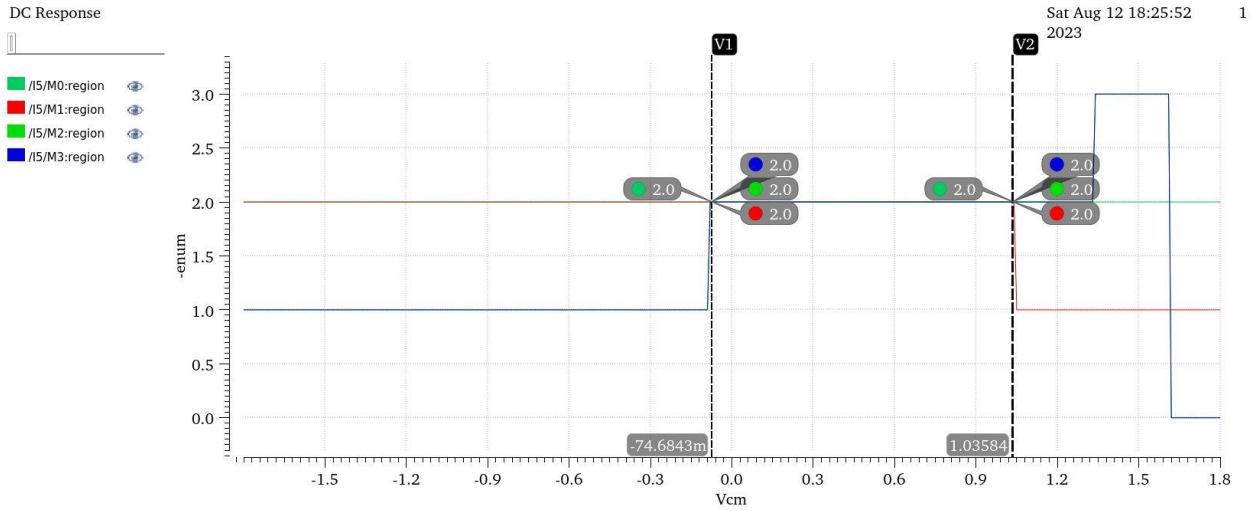


*Figure 14 plot regions*

I have the negative input range to get minimum input why?

Because we haven't current equal 20$\mu A$ exactly so drop in resistance not equal exactly 0.6V and when we do simulator range of $V_{incm}$ by $V^*$ and simulator calculate it using $V_{DSAT}$

From simulator range from

-74.6843$mV$ *but we start sweep from zero i will take zero as* min *value to* 1.03584 $mV$

From part one $VINCM_{MIN} = V_{RD} - V_{TH} = 0.6 - 527.4m = 72.6mV.$

$VINCM_{MAX} = V_{DD} - V^* - VGS_{DIFF} = 1.8 - 138.7m - 643.3m = 1.0202V$

The range from simulator = 1.03584-0=1.03584V

The range if used the minimum -74.6843 =1.03584+74.6843=1.11 V.

The range hand analysis =1.0202-72.6m=0.9476 V

| | Simulation | Hand analysis |
|---|---|---|
| Max | 1.03584 | 1.0202 |
| Min | 0 &&-74.6843 I will take zero as minimum because starts from zero | 72.6m |
| rang | 1.03584 if I take negative min value the range will be 1.11 | 0.9476 V |

## CM large signal ccs (GBW vs Vicm)

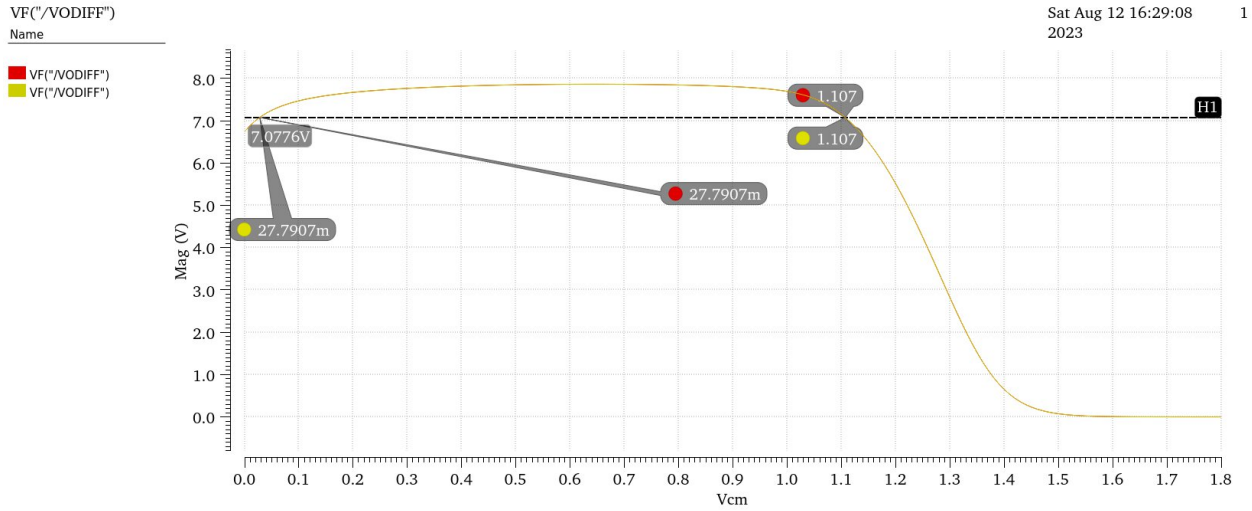


*Figure 15 plot VODIFF vs Vicm*

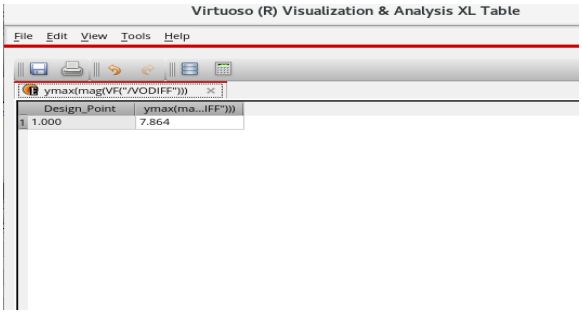


*Figure 16 max output Vodiff*

$$VODIFF_{90\%} = 0.9 * 7.864 = 7.0776V$$

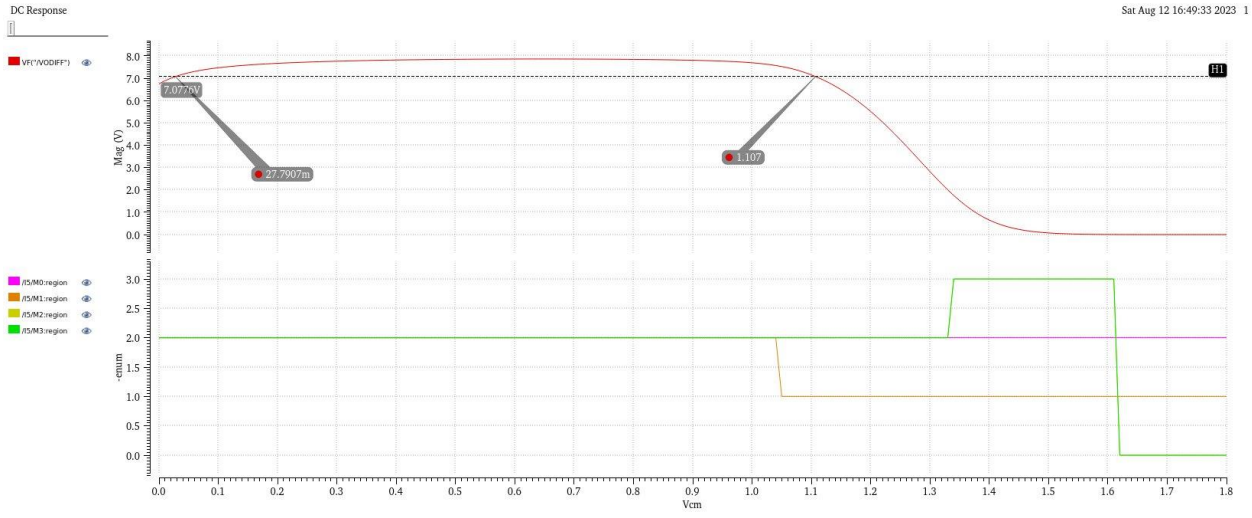


*Figure 17 plot VODIFF and regions vs VCM*

From the graph the $CM_{range}$ $1.1078 - 27.7907m = 1.08V$

From plot of regions $CM_{range}$ $1.03584 + 74.6843m = 1.11V$ when I plot regions, I found min is this negative -74.6843 but the sweep required starts from zero.
From plot of regions $CM_{range}$ $1.03584 - 0 = 1.03584V$ Because sweep starts from zero, I will take it as min value.

| | GBW | Regions |
|---|---|---|
| Range | 1.08V | 1.03584 V<br>1.1 V if we take vmin equal -74m |

The GBW is way better than the regions as the regions first is a simulation parameter only and second has a very sharp edged between transitions while the GBW is a logical and experimental way to tell the valid range and leaves the designer to his own estimation whether he accepts 90% of the output or maybe less.