

Analog IC Design

Lab 11 (Mini Project 02)

Fully-Differential Folded Cascode OTA

PART 1: gm/ID Design Charts

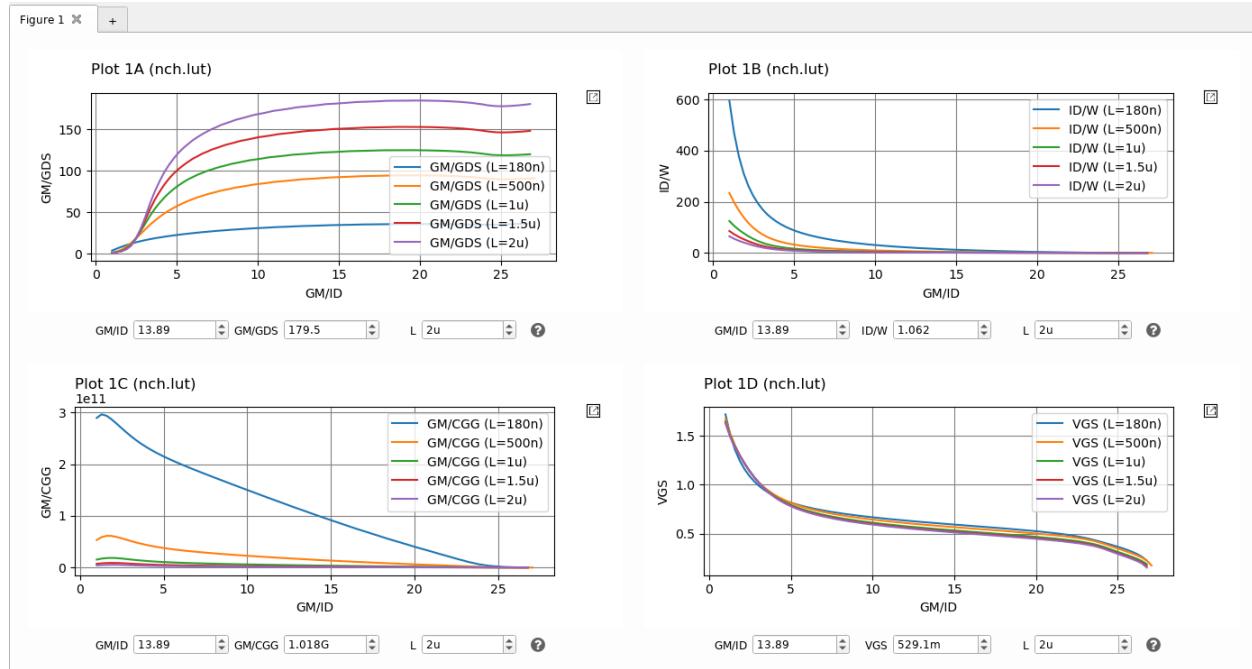


Figure 1 ADT plots of NMOS.

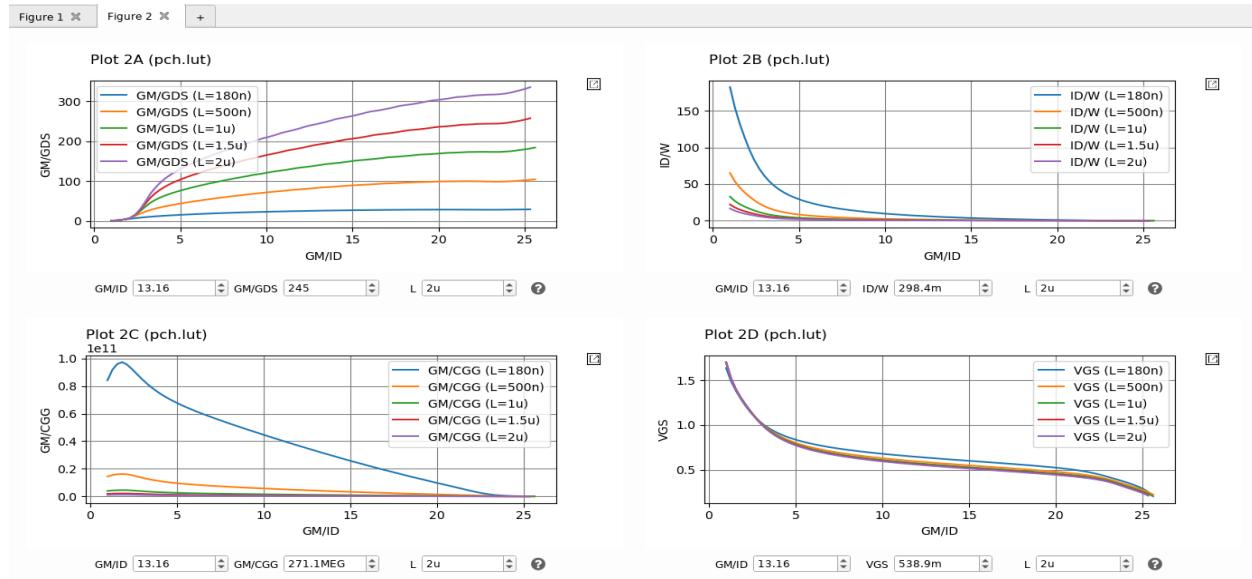


Figure 2 ADT Plots of PMOS.

PART 2: OTA Design

Design a fully differential folded cascode OTA with capacitive feedback that meets the specifications below.

The current consumed in the biasing branches (current mirrors) is not included in the specifications.

Technology	0.13um	0.18um
Supply voltage	1.2V	1.8V
Closed loop gain	2	2
Phase margin	$\geq 70^\circ$	$\geq 70^\circ$
OTA current	$\leq 80\mu A$	$\leq 80\mu A$
CMFB circuit current	$\leq 40\mu A$	$\leq 40\mu A$
CM input range – low	≤ 0	≤ 0
CM input range – high	$\geq 0.6V$	$\geq 1.1V$
Differential output swing	0.6Vpk-to-pk	1.2Vpk-to-pk
Load	1pF	1pF
DC Loop gain	50dB	60dB
Closed loop bandwidth	10MHz	10MHz

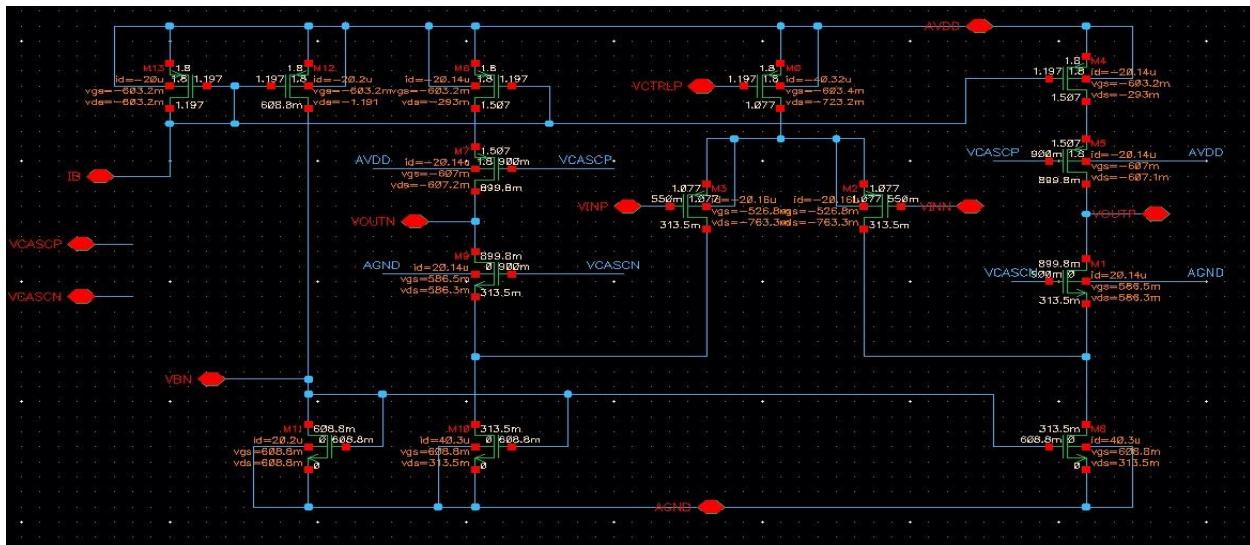


Figure 3 Schematic of folded OTA.

Suggested Design Procedure:

- 1) From the CMIR spec you will find that you need a PMOS input stage as shown in the schematic above.
- Input Pair | Tail Current Source → PMOS, because of CM input range which is 0-1.1 near to GND rail.
- 2) The OTA current will be divided as follows: ISS = 40uA for the input pair (CS), and 40uA for the cascode branches (CG). The NMOS current sources in the bottom needs to sink 80uA (2 x 40uA). For more details on how to select the folded cascode current split check this paper: "[Optimum Split Ratio for Folded Cascode OTA Bias Current: A Qualitative and Quantitative Study](#)" DOI: [10.1109/ICM48031.2019.9021755](https://doi.org/10.1109/ICM48031.2019.9021755).
- 3) Since this is a relatively difficult design, we will directly assume values for L and gm/ID (or V*) based on designer's experience and folded cascode trade-offs matrix.
 - For the input pair use short L and bias it in MI or WI, e.g., L = 0.2um and gm/ID = 15. This maximizes the GBW (good efficiency) and minimizes the input capacitive loading (avoid reducing the DC LG).

You will have to tune your gm/ID to achieve the CL bandwidth spec.

For PMOS Input pair

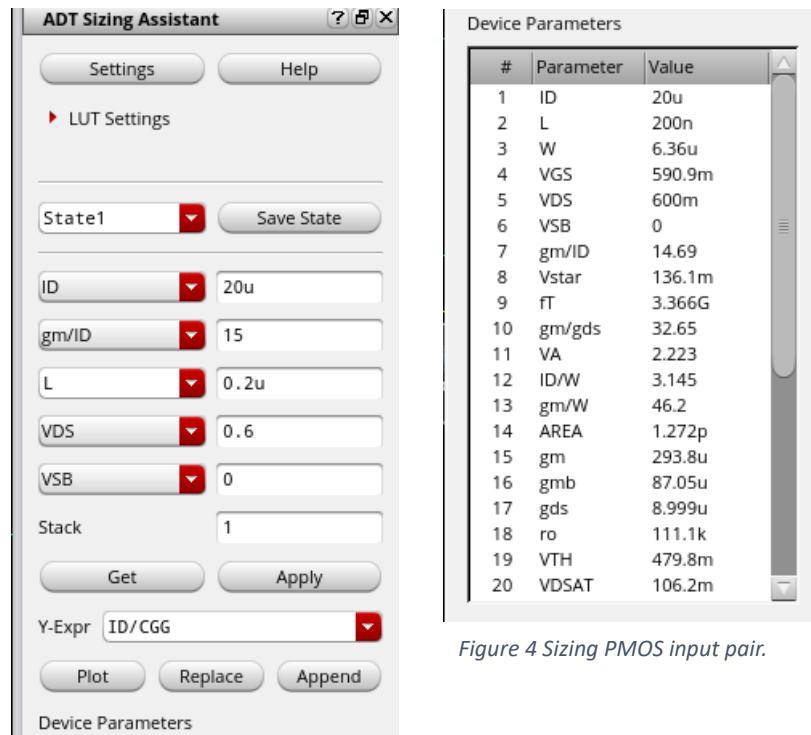


Figure 4 Sizing PMOS input pair.

- For the current source transistors use relatively long L and bias them in SI, e.g., L = 1um and gm/ID = 10. These transistors contribute significant offset and noise. A large gm will not help the gain but will increase the noise.

Sizing M13,12,11,10,9

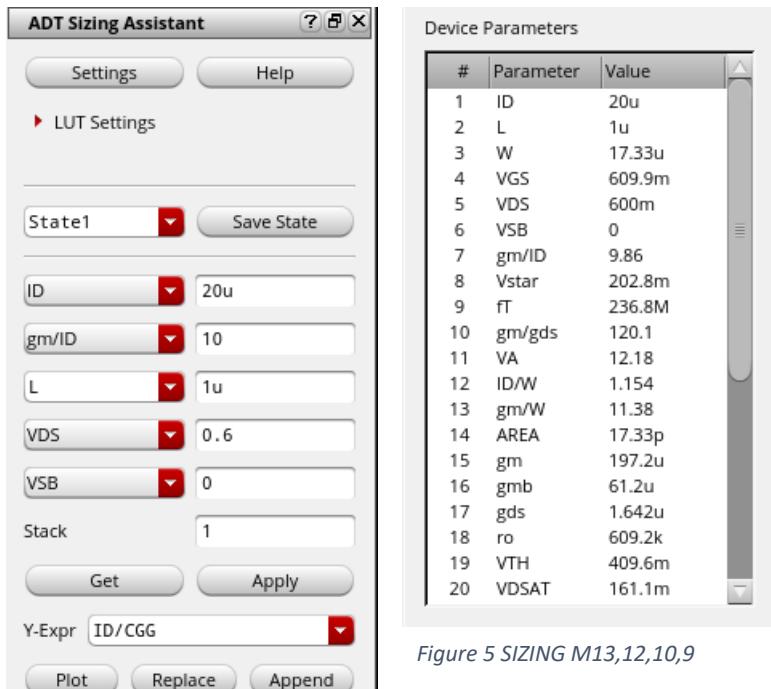


Figure 5 SIZING M13,12,10,9

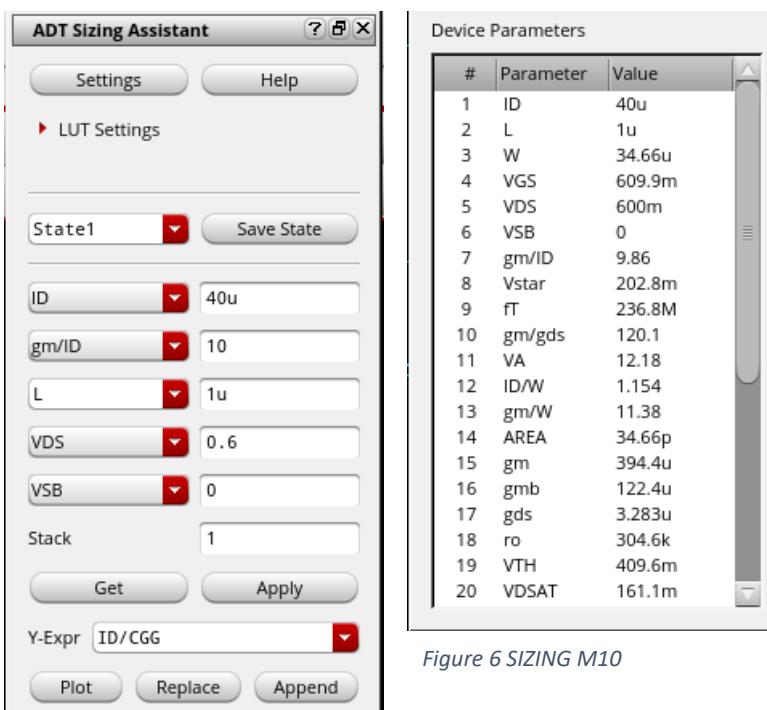


Figure 6 SIZING M10

Sizing M2,3,4

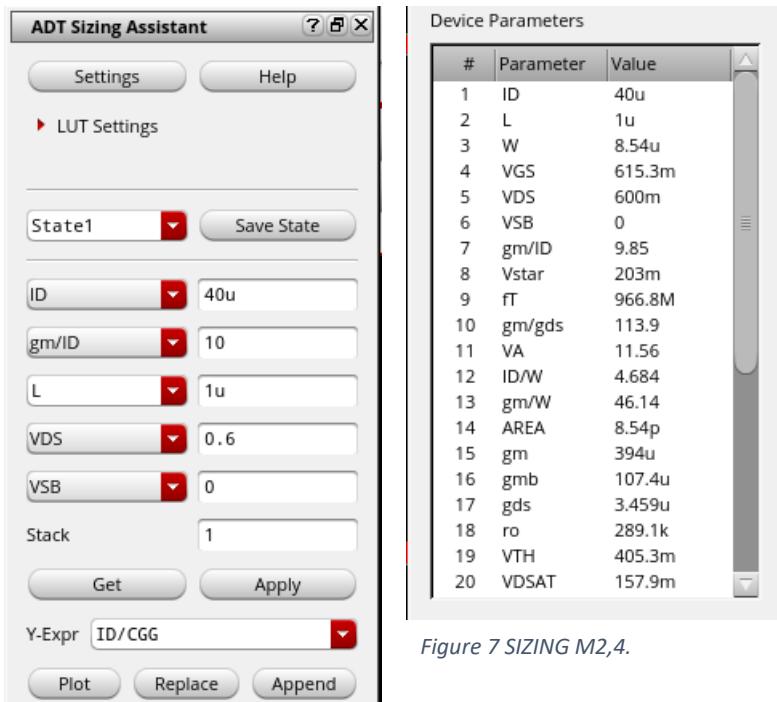


Figure 7 SIZING M2,4.

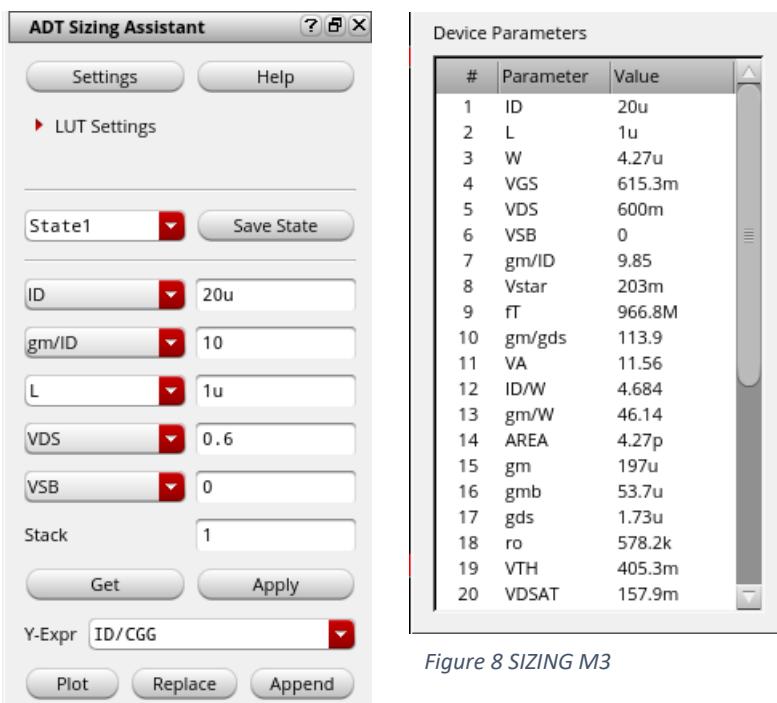


Figure 8 SIZING M3

- For the cascode transistors use moderate L and bias them in MI or WI, e.g., L = 0.5um and gm/ID = 15. These transistors do not contribute significant offset and noise, so they don't need to be large. A large gm helps the gain and doesn't increase the noise.

CASCODED TRANSISTORS

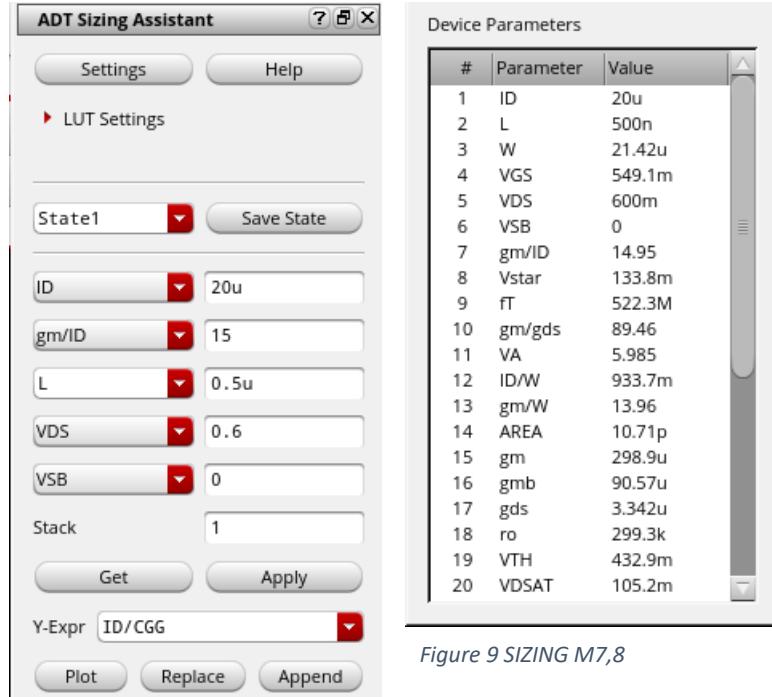


Figure 9 SIZING M7,8

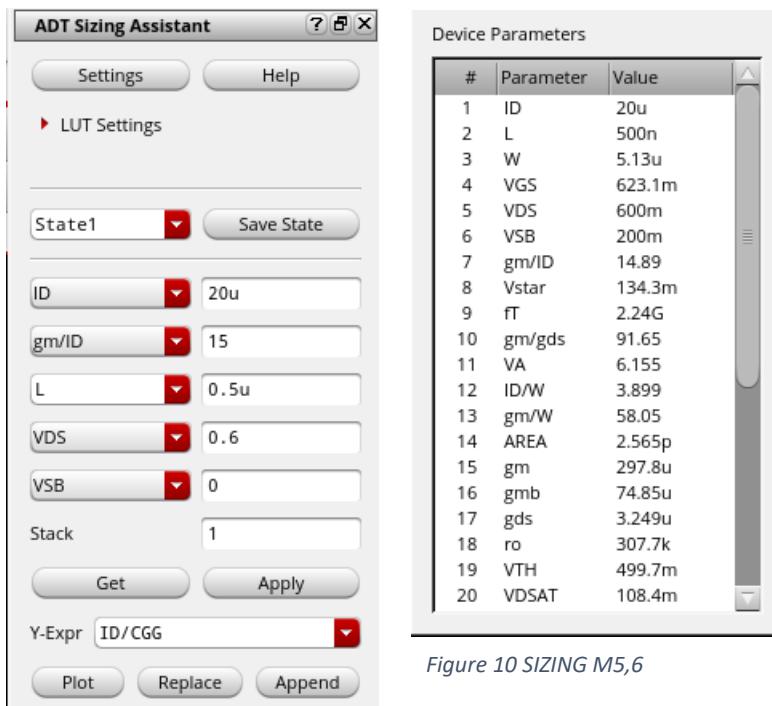


Figure 10 SIZING M5,6

- These assumptions greatly simplify the design process and can be later tuned in simulations (taking the trade-offs matrix into consideration) to achieve exact specifications.

When I have got loop gain wasn't achieved so I have scaled sizing of cascaded transistors by 4.2

$$\text{So } L_{cascode} = 0.5\mu * 4.2 = 2.1\mu m$$

$$W_{7,8} = 21.42\mu * 4.2 = 89.964\mu m$$

$$W_{5,6} = 5.13\mu * 4.2 = 21.546\mu m$$

- 4) From the assumed V^* , select suitable biasing for the cascode transistors (VCASCP and VCASCN).

Hint: Set $VCASCN \approx VGSN + V^*$ and $VCASCP \approx VDD - |VGSP| - V^*$

$$V_{CASCN} = V_{GS5,6} + V_{2,4}^* = 824.7mV.$$

$$V_{CASCP} = V_{DD} - V_{GS7,8} - V_{9,11}^* = 989mV.$$

PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

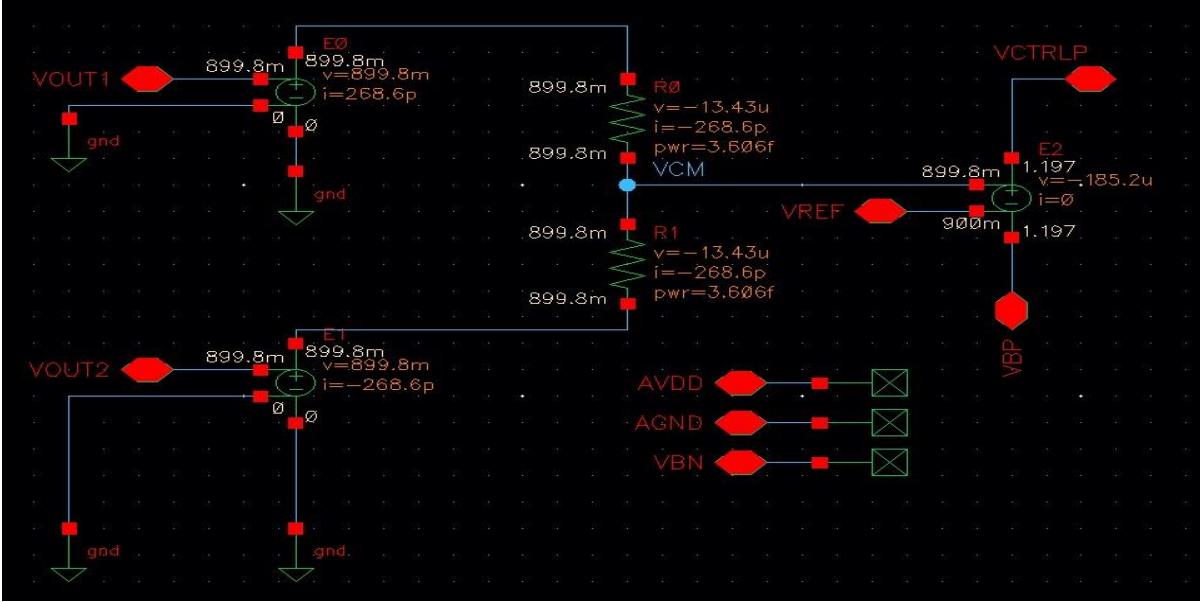


Figure 11 Schematic behavioral.

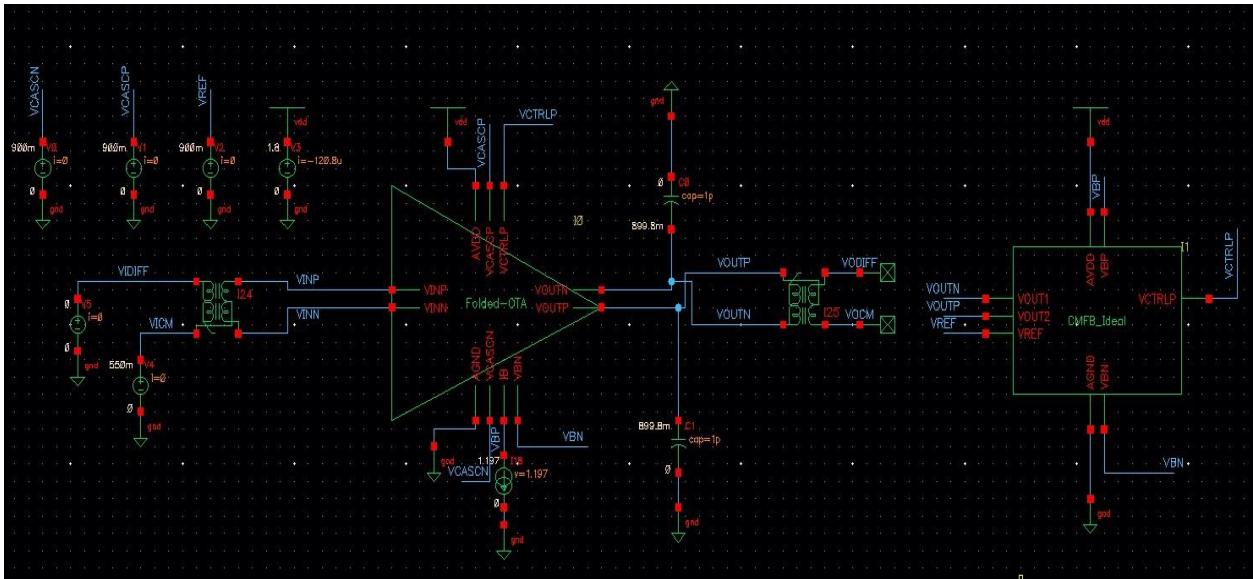


Figure 12 TESTBENCH.

- Set VICM in the middle of the CMIR.
- Select VREF to maximize the symmetrical output swing.

I will set $V_{CM} = 550mV$ $V_{REF} = 900mV$.

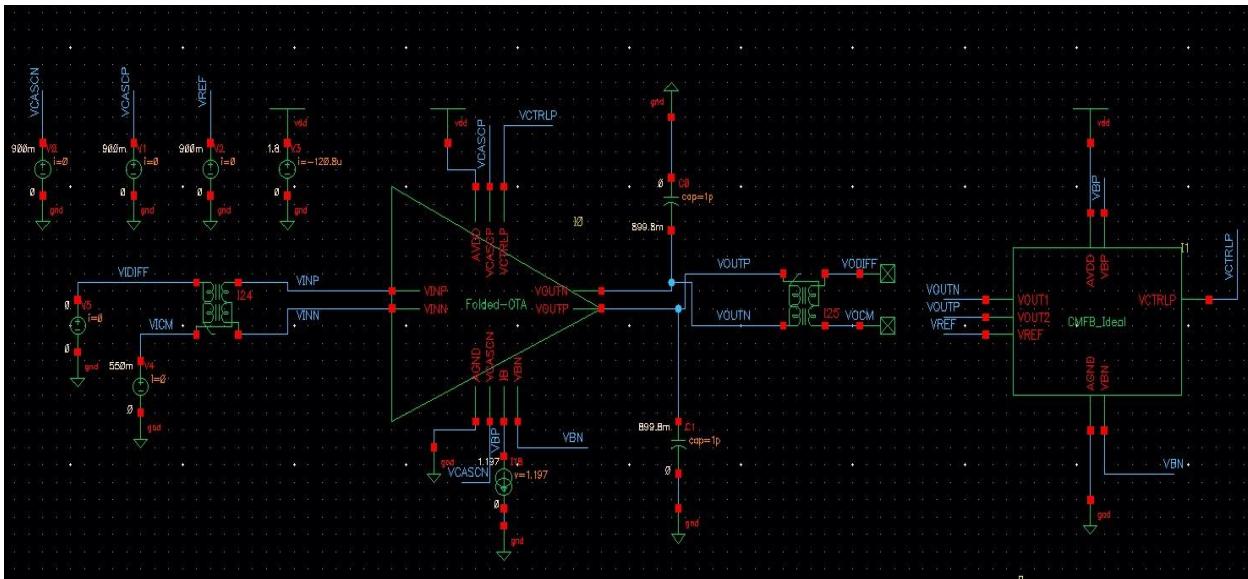


Figure 13 Testbench Schematic.

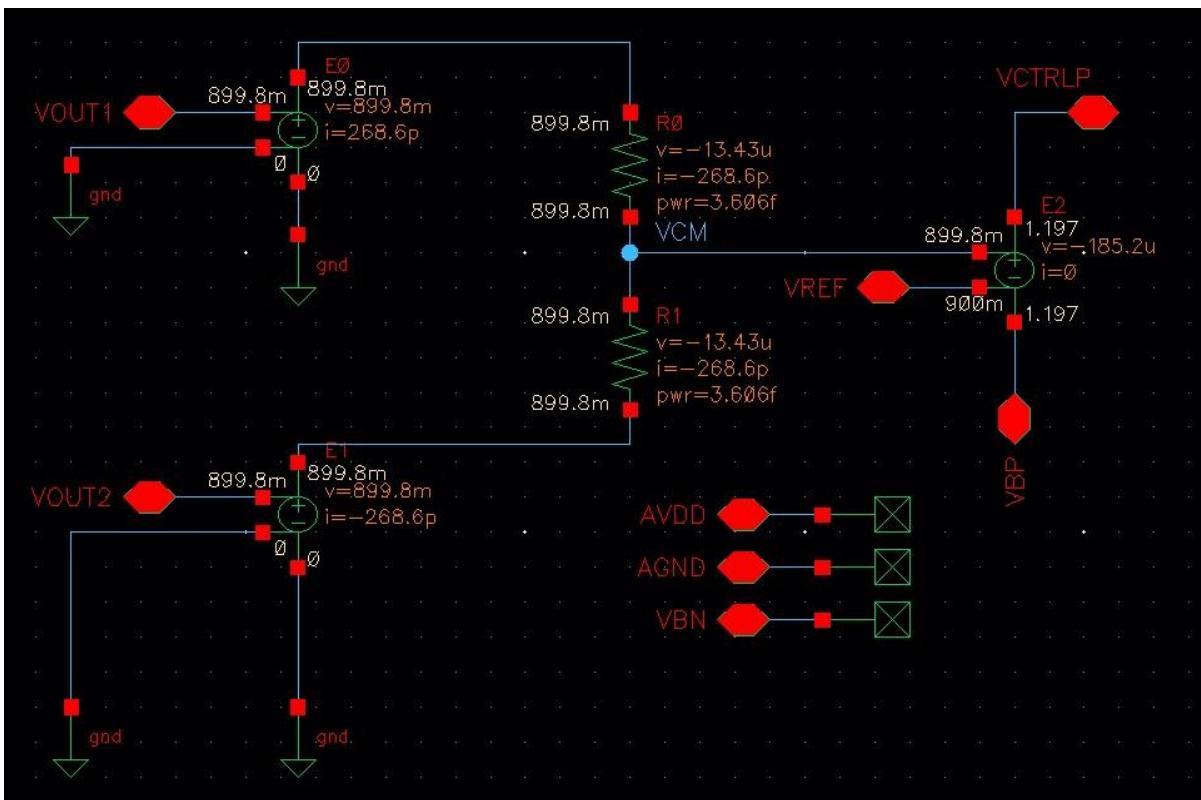


Figure 14 DC Operating point in behavioral schematic.

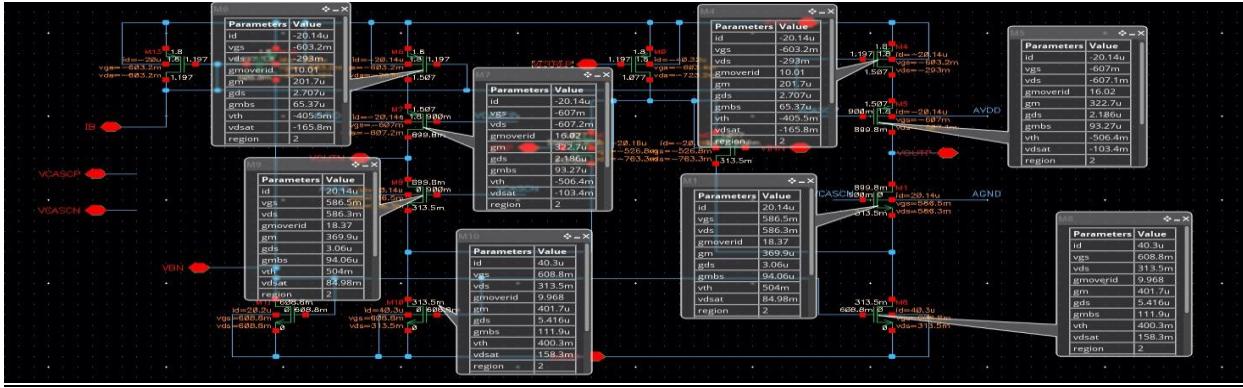


Figure 15 DC OPERATING POINT.

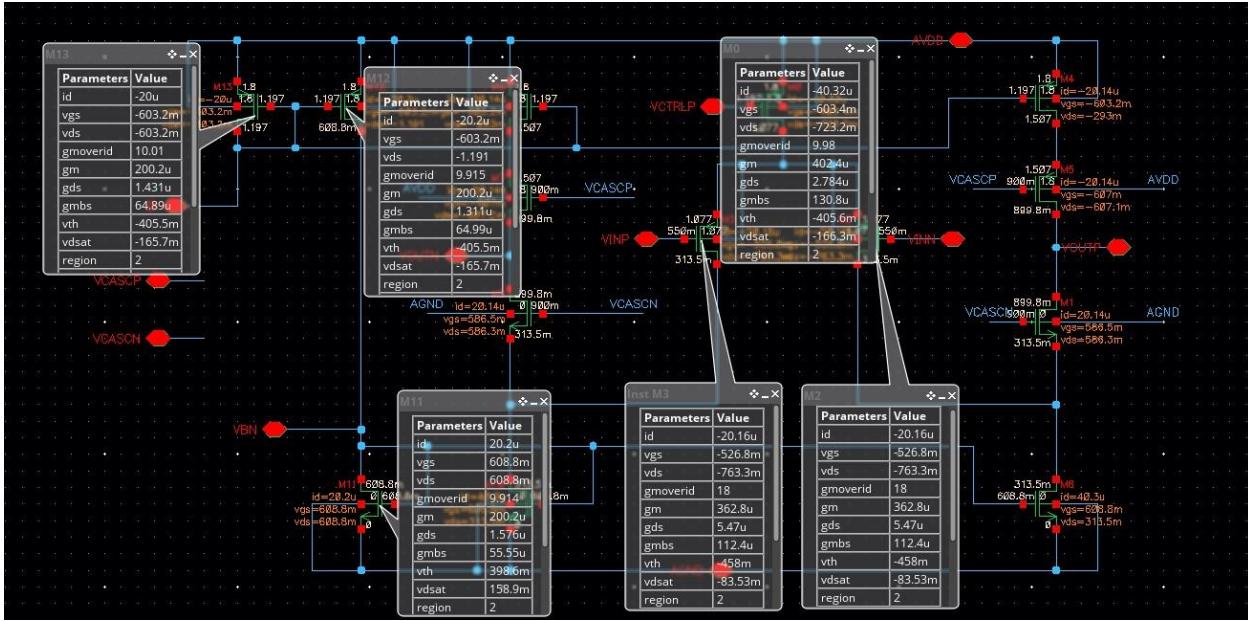


Figure 16 DC OPERATING POINT.

- What is the CM level at the OTA output?

$$V_{OCM} = 898.8mV \approx V_{REF}.$$

- What are the differential input and output voltages of the error amplifier? What is the relation between them?

$$\text{Differential input} = V_{REF} - V_{CM} = 900 - 898.8 = 0.2mV$$

$$\text{Differential output} = V_{CTRLP} - V_{BP} = 1.197 - 1.197 = 0V$$

Differential input voltage is the error voltage between common mode voltage and VREF “desired CM voltage”, and differential output is the bias voltage to tail current source to set CM DC voltage, and the relation between them is the gain of error amplifier.

Diff small signal ccs:

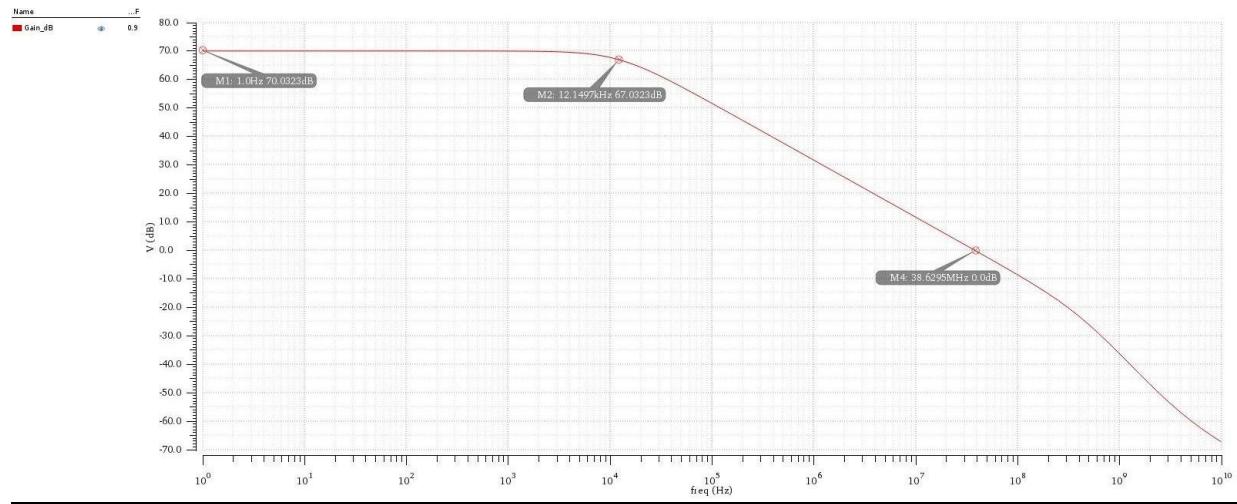


Figure 17 plot gain vs frequency in dB.

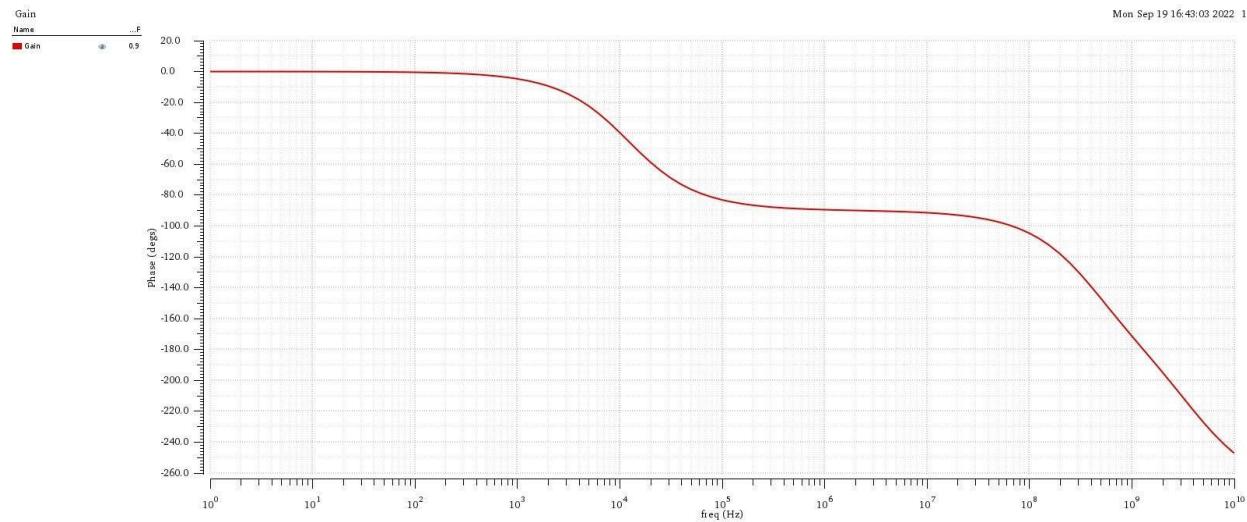


Figure 18 plot phase vs frequency.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Lab_11:CMFB_TB:1	Gain				
Lab_11:CMFB_TB:1	Gain_dB	[]			
Lab_11:CMFB_TB:1	Ao	3.174k			
Lab_11:CMFB_TB:1	Ao_dB	70.03			
Lab_11:CMFB_TB:1	BW	12.17k			
Lab_11:CMFB_TB:1	UGF	38.74M			
Lab_11:CMFB_TB:1	GBW	38.71M			
Lab_11:CMFB_TB:1	PM	84.35			

Figure 19 Results from simulator.

Note: check the schematic to know numbering of mosfets.

Hand analysis:

$$R_{OUT} = (r_{o1} * (1 + (gm_1 + gmb_1) * (r_{o8} || r_{o2}))) || (r_{o5} * (1 + (gm_5 + gmb_5) * r_{o4}))$$

$$Gain = gm_2 * R_{OUT} = 3.4K = 70.62dB.$$

IO.M1:cdd IO.M5:cdd	
IO.M1:cdd	IO.M5:cdd
1 22.52E-15	69.41E-15

Figure 20 values of parasitic caps.

$$C_{OUT} = C_{dd1} + C_{dd5}$$

$$bandwidth = \frac{1}{2\pi R_{OUT} * (C_L + C_{OUT})} = 12.54MHz.$$

$$GBW = Gain * Bandwidth = 42MHz.$$

To calculate the phase margin:

$$W_{pnd} = \frac{W_T}{3} = \frac{gm_1}{6\pi C_{gg}} = 456.3M.$$

$$Phase\ margin = 90^\circ - \tan^{-1} \left(\frac{W_U}{W_{pnd}} \right) = 85^\circ.$$

	Simulation	Hand analysis
DC gain	3.174K	3.4K
DC gain dB	70.03	70.62
Bandwidth	12.17K	12.54K
GBW	38.71M	42M
UGF	38.74M	42M
PM	84.35	85

PART 4: Open-Loop OTA Simulation (Actual CMFB)

- The 40uA current is divided between the four CMFB branches. You may assume L = 1um and gm/ID = 15 for all transistors with unknown L or gm/ID for simplicity (note that L and gm/ID for some transistors are already known, why?).
 - We need CD (source followers) to buffer the OTA output. This avoids loading the OTA with the sensing resistors¹.
 - The sensing resistors are chosen such that the max current flowing through them (when diff signal is max) is less than the CD bias current. This avoids starving the CD when the diff output signal has its maximum excursion.
 - The CD introduces DC shift. Thus, the input to the error amplifier is not Vocm. Instead, it is Vocm + |VGSP|. Thus, you need to set VREF to VREF + |VGSP|. A better approach is to apply VREF to an identical CD buffer, so that it experiences the same |VGSP| shift.
-
- The CMFB limits the output swing. Max Vout is VDD – V* – |VGSP|. One reason why we selected PMOS CD is to avoid increasing VTH by body effect (increasing VTH will limit output swing even more).
 - The output range now is from 2V* to VDD – V* – |VGSP|. Select Vocm to be around the middle of this range to have maximum symmetric output swing (it will be different from the value selected in the behavioral model).
 - The output of the CD buffer is close to VDD; thus, we select NMOS input for the error amplifier.

¹ Note that this type of CMFB will have a limited linear range and may affect the output swing specification.

- The error amplifier is a simple differential amplifier with diode connected loads. We don't need high gain from the error amplifier, but we need low impedance nodes to avoid deteriorating the stability of the CMFB loop.
- The bias point output of the error amplifier is equal to $VDD - |VGSP|$. That's why we use the error amplifier output to control the PMOS current source in the folded OTA rather than the NMOS current source.
- Note that we select the non-inverting error amplifier output to maintain -ve feedback in the CMFB loop.

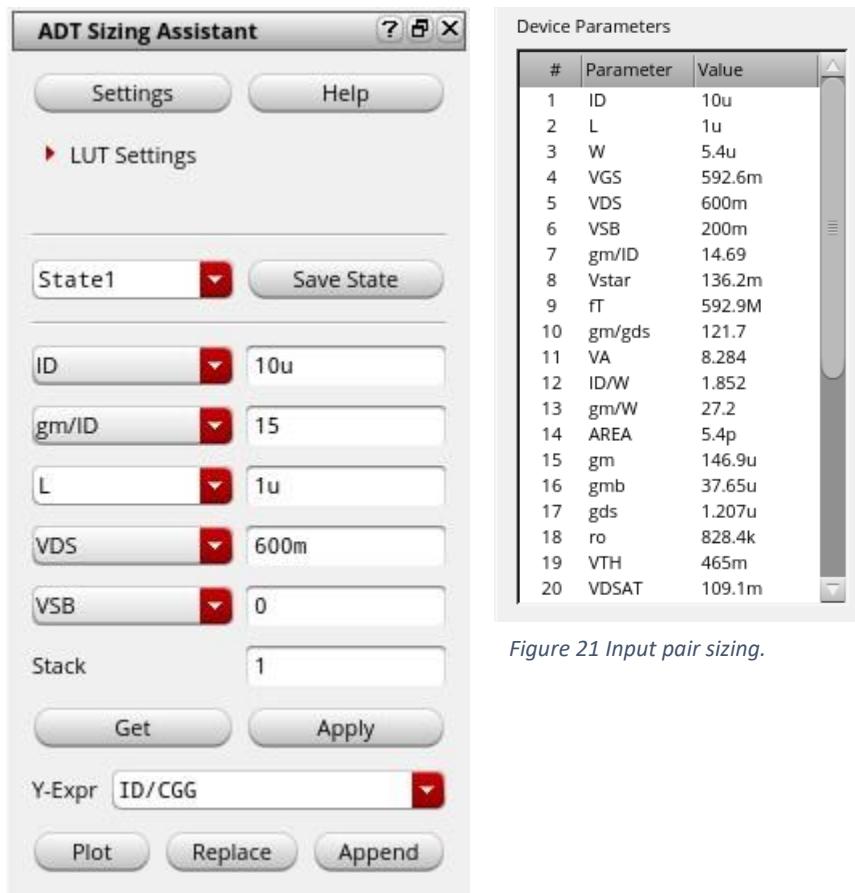


Figure 21 Input pair sizing.

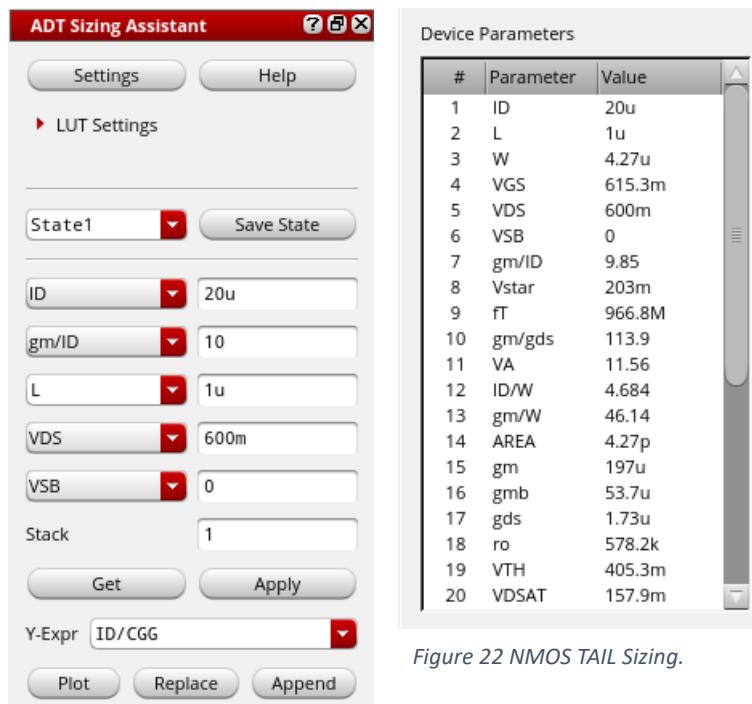


Figure 22 NMOS TAIL Sizing.

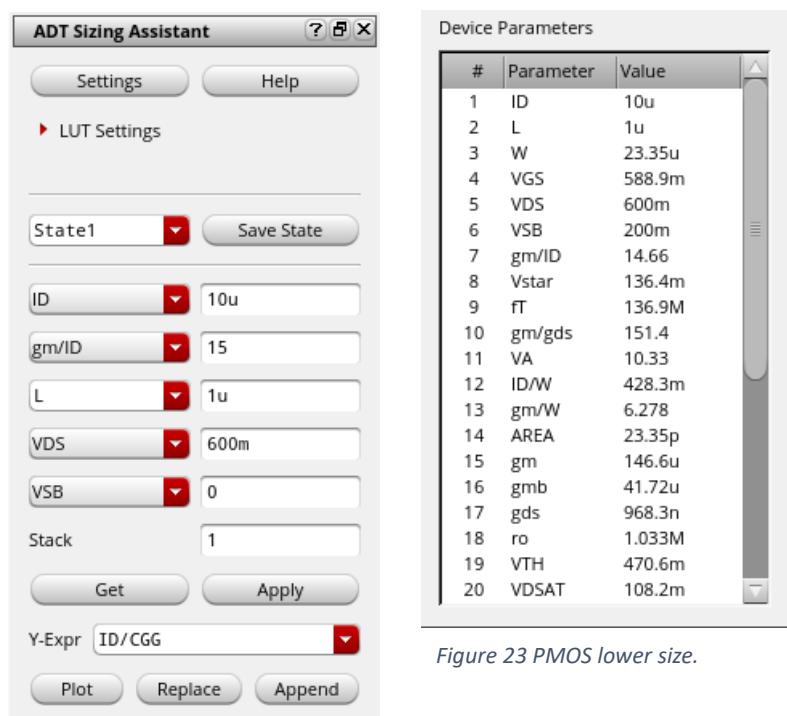


Figure 23 PMOS lower size.

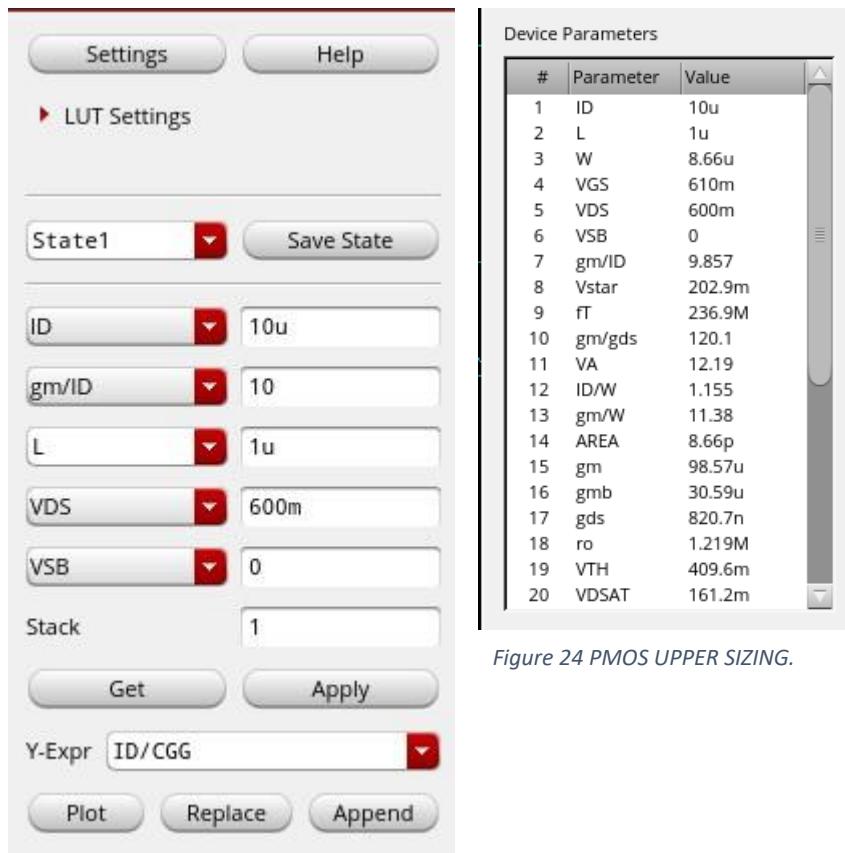


Figure 24 PMOS UPPER SIZING.

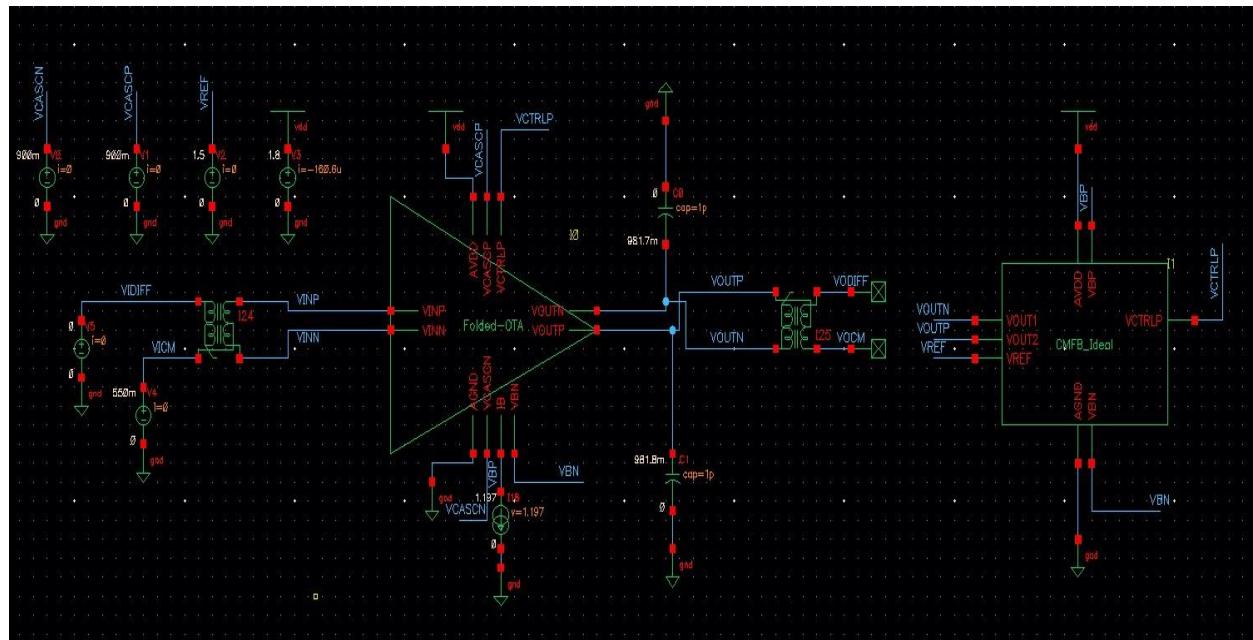


Figure 25 DC operating point of testbench.

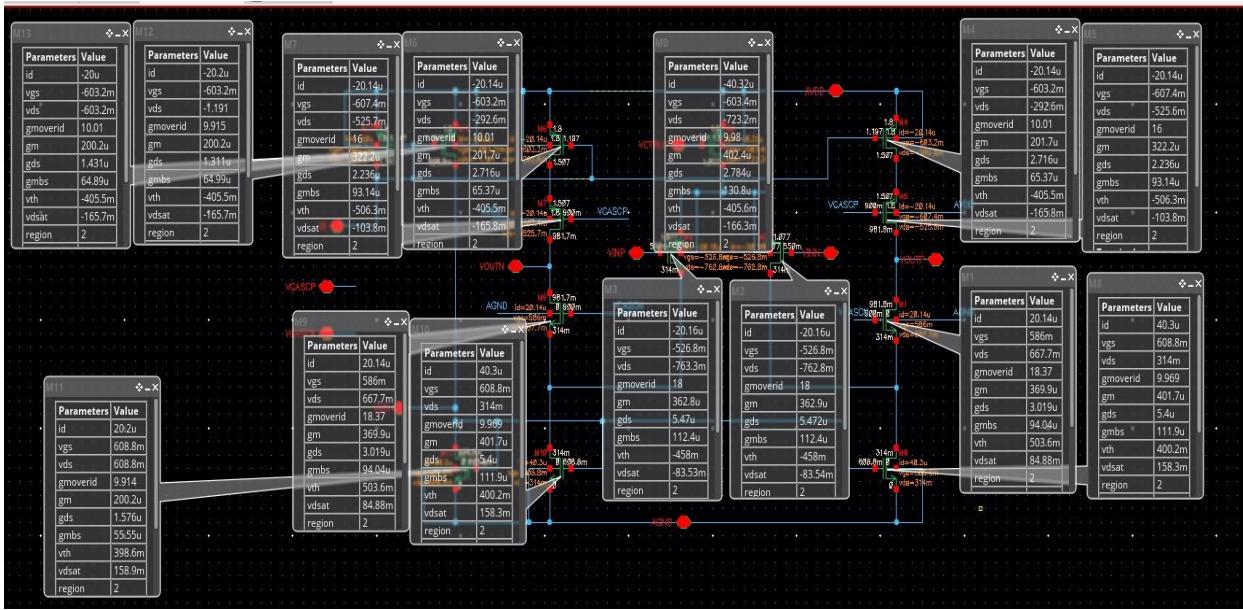


Figure 26 DC operating point of folded cascode.

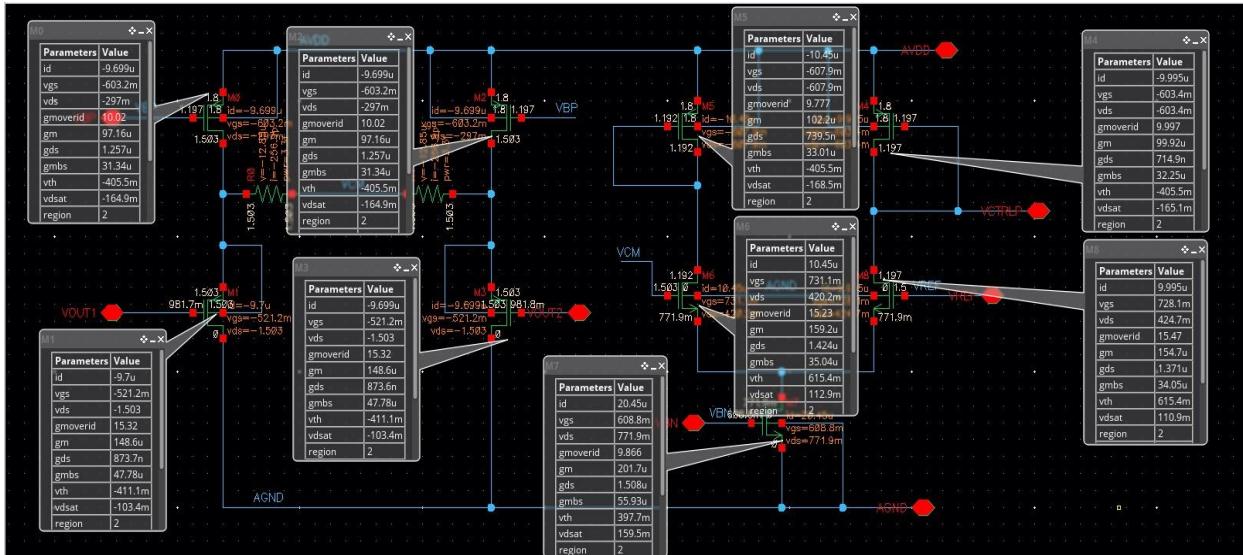


Figure 27 DC Operating point of actual CMFB.

- What is the CM level at the OTA output? Why?

$$V_{OCM} = 981.7mV.$$

I need V_{OCM} to be equal 900mV so i used $V_{REF} = V_{OCM} + V_{GSP} = 1.5V$.

as we have settled VREF to achieve this output level due to PMOS common drain stage, this will compensate the dc shift of the actual CMFB circuit.

- What are the differential input and output voltages of the error amplifier? What is the relation between them?

$$\text{Differential input} = V_{CM} - V_{REF} = 1.503 - 1.5 = 3mV.$$

$$\text{Differential output} = V_{CTRLP} - V_{BP} = 1192.1m - 1196.8m = 4mV.$$

Differential input voltage is the error voltage between common mode voltage and VREF “desired CM voltage”, and differential output is the bias voltage to tail current source to set CM DC voltage, and the relation between them is the gain of error amplifier.

Diff small signal ccs:

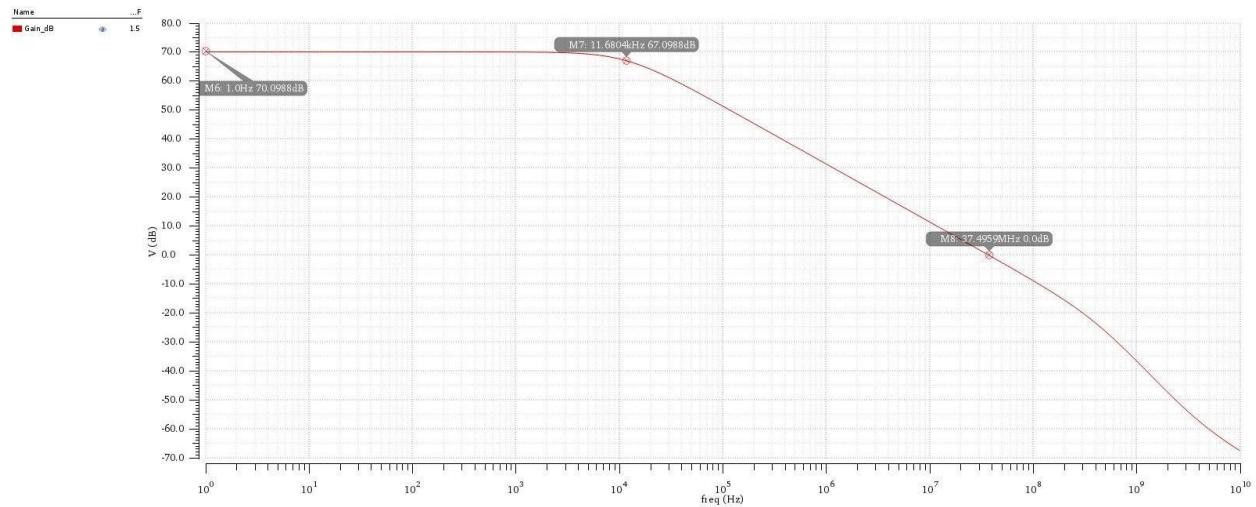


Figure 28 plot gain vs frequency in dB.

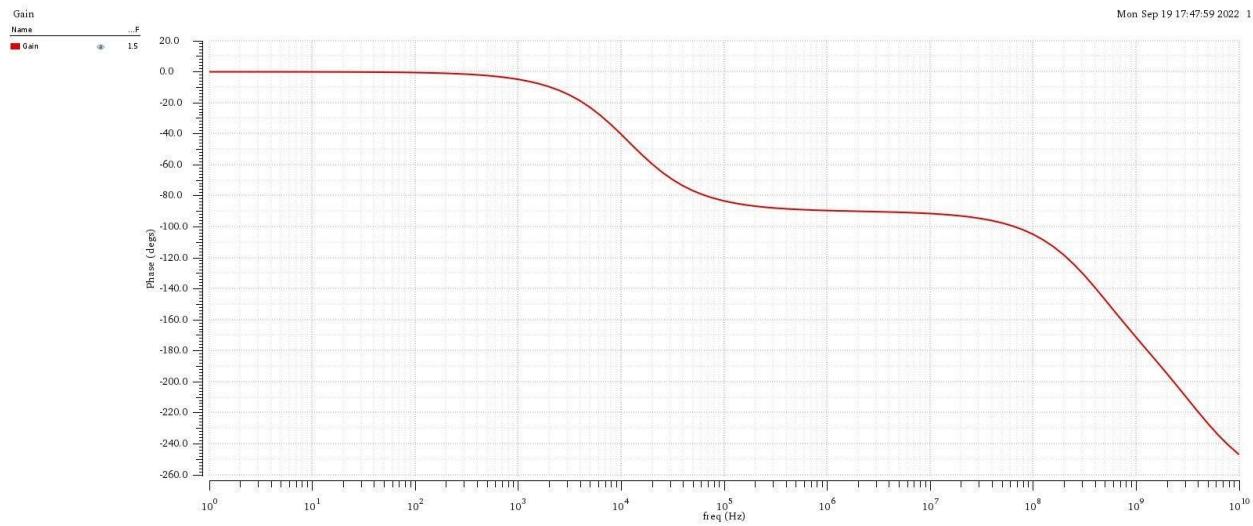


Figure 29 plot phase vs frequency.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Lab_11:CMFB_TB:1	Gain				
Lab_11:CMFB_TB:1	Gain_dB				
Lab_11:CMFB_TB:1	Ao	3.198k			
Lab_11:CMFB_TB:1	Ao_dB	70.1			
Lab_11:CMFB_TB:1	BW	11.71k			
Lab_11:CMFB_TB:1	UGF	37.69M			
Lab_11:CMFB_TB:1	GBW	37.55M			
Lab_11:CMFB_TB:1	PM	84.45			

Figure 30 Results from simulator.

PART 5: Closed Loop Simulation (AC and STB Analysis)

Note that the CM DC level provided before the input balun is useless because it is blocked by the capacitor.

Note that we use two baluns at the output to allow stability analysis. We divide the output to diff and CM and break the diff/CM loops by OV dc sources, then we combine them again to VOUTN and VOUTP to close the feedback loop. We use a 2pF input capacitance and 1pF feedback capacitance to provide a closed loop gain = 2. Note that you need to connect VOUTN to VINP and VOUTP to VINN to maintain negative feedback. We use large resistors across the feedback capacitance to close the loop in DC. This will set $V_{ICM} = V_{OCM}$.

Instead in using two voltages sources with zero V I used two probes like previous Laps.

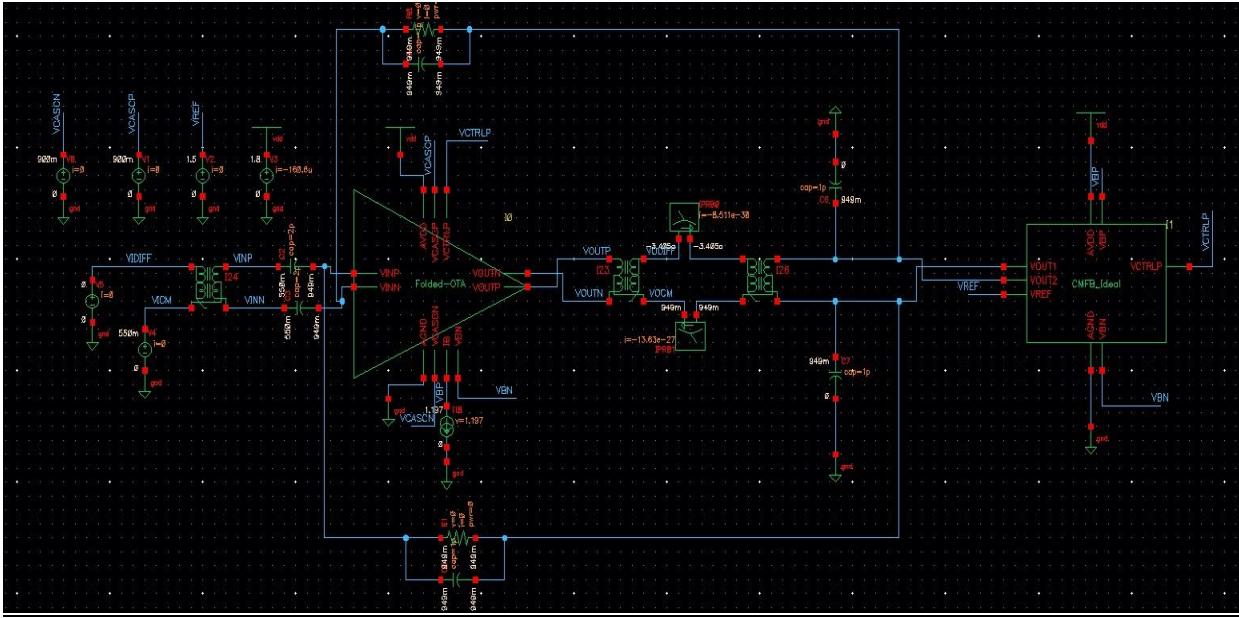


Figure 31 testbench with feedback.

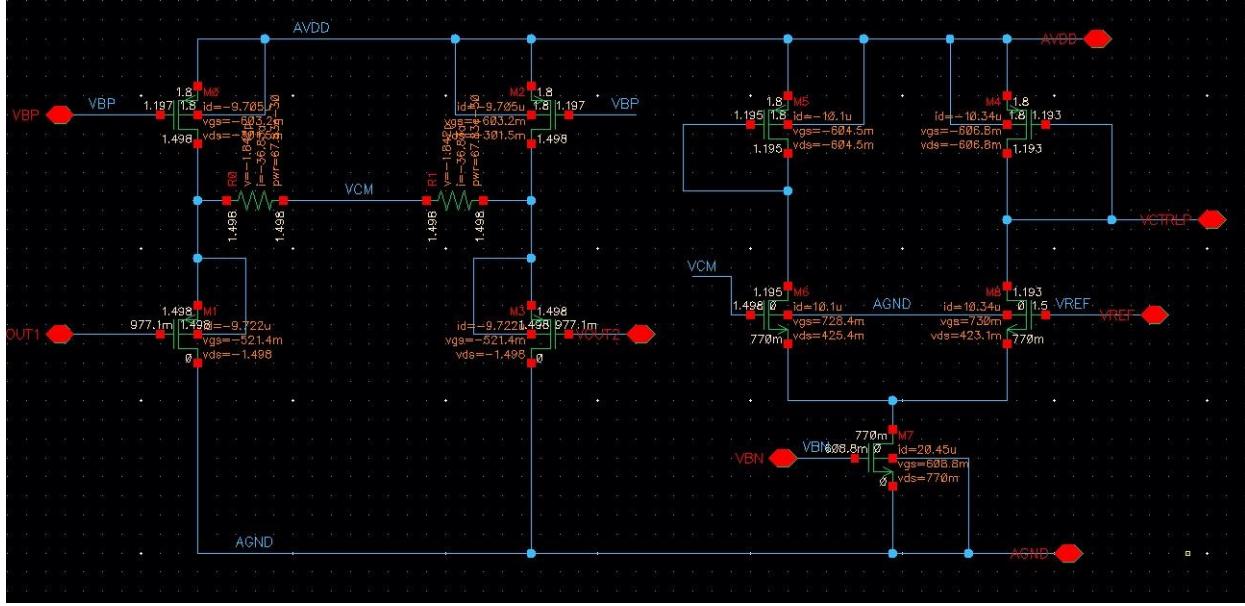


Figure 32 Actual CMFB.

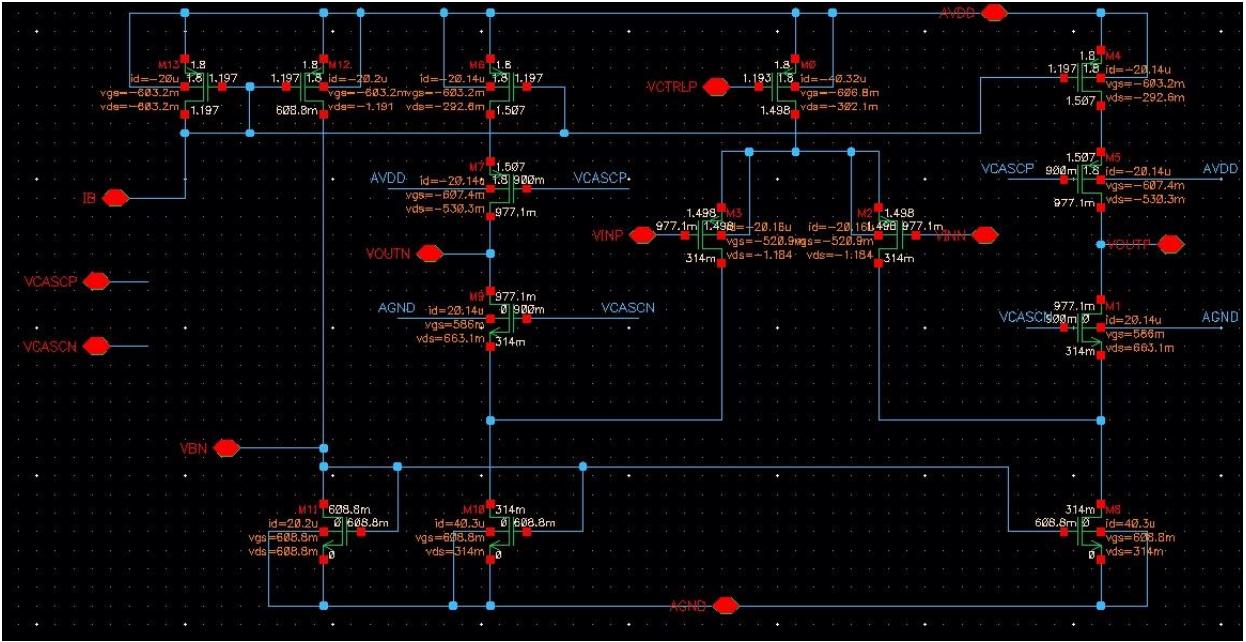


Figure 33 FOLDED CASCODE DC OPERATING POINT.

What is the CM level at the OTA output? Why?

$V_{OCM} = 949mV$ his is what I designed the circuit too keep common mode level at about 0.9 V and I do it by setting $V_{REF} = 1.5V$, due to CD stage in sensing branch of CMFB circuit.

What is the CM level at the OTA input? Why?

$V_{INCM} = 949mV$ is equal to V_{OCM} as this connection is buffer.

Differential closed-loop response:

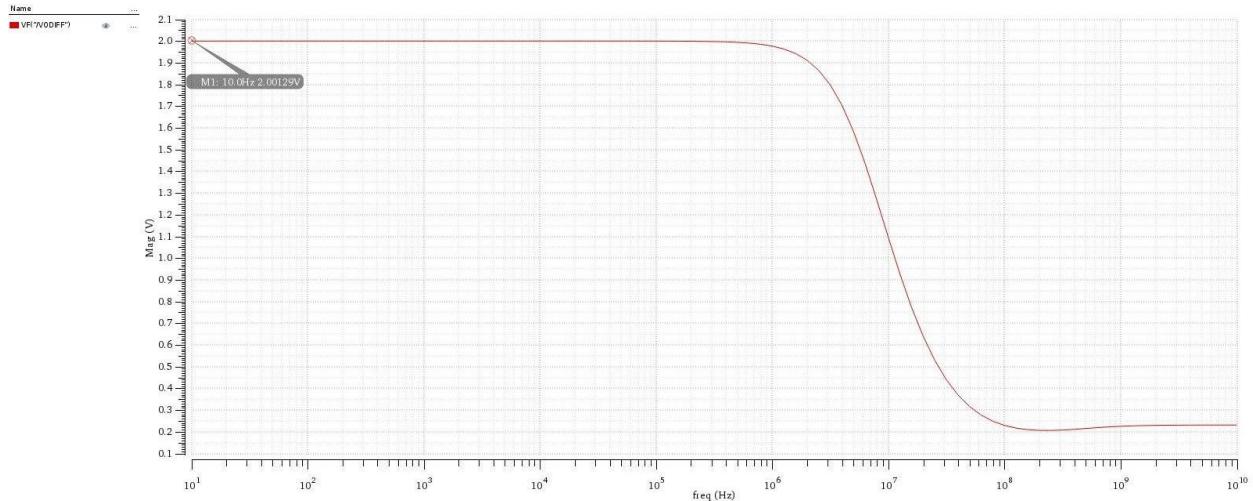


Figure 34 plot gain vs frequency in dB.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Lab_11:Closed_Loop:1	VF("/VODIFF")	✓			
Lab_11:Closed_Loop:1	BW_cl	10.23M			
Lab_11:Closed_Loop:1	GBW_cl	20.53M			

Figure 35 Results from simulator.

As shown in figures:

$$DC \text{ Closed Loop Gain} = 2.001 \approx 2$$

$$bandwidth = 10.23MH \approx 10MHz.$$

The specs in closed loop gain and closed loop bandwidth are satisfied.

Differential and CMFB loops stability (STB analysis):

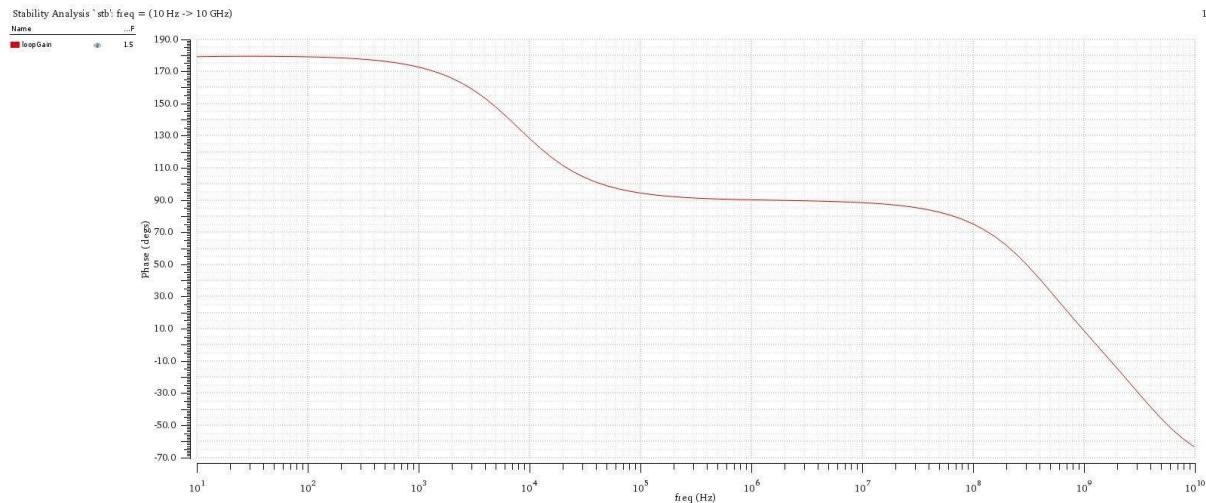


Figure 36 Differential loop gain phase.

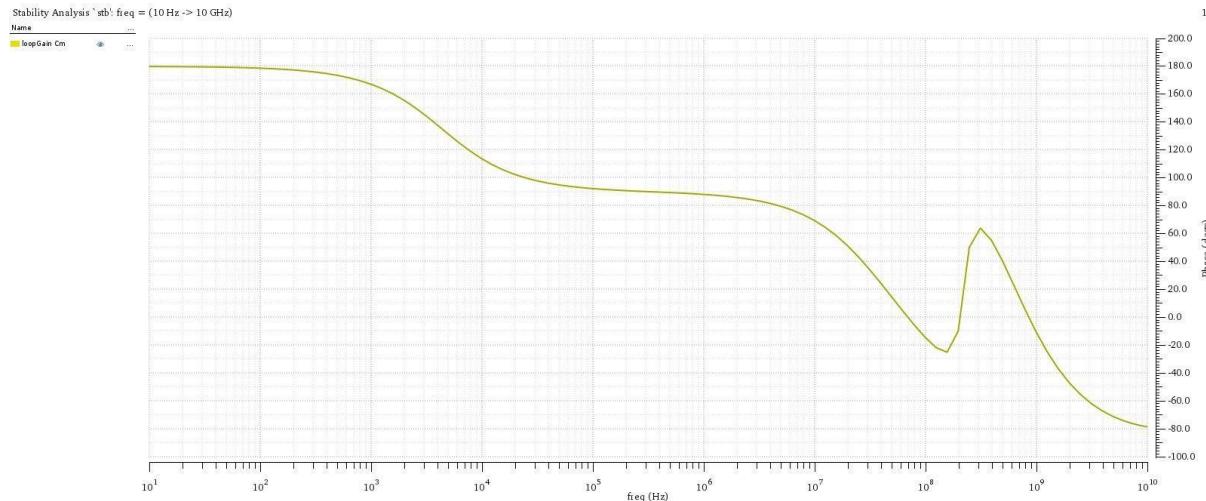


Figure 38 CM loop gain phase.

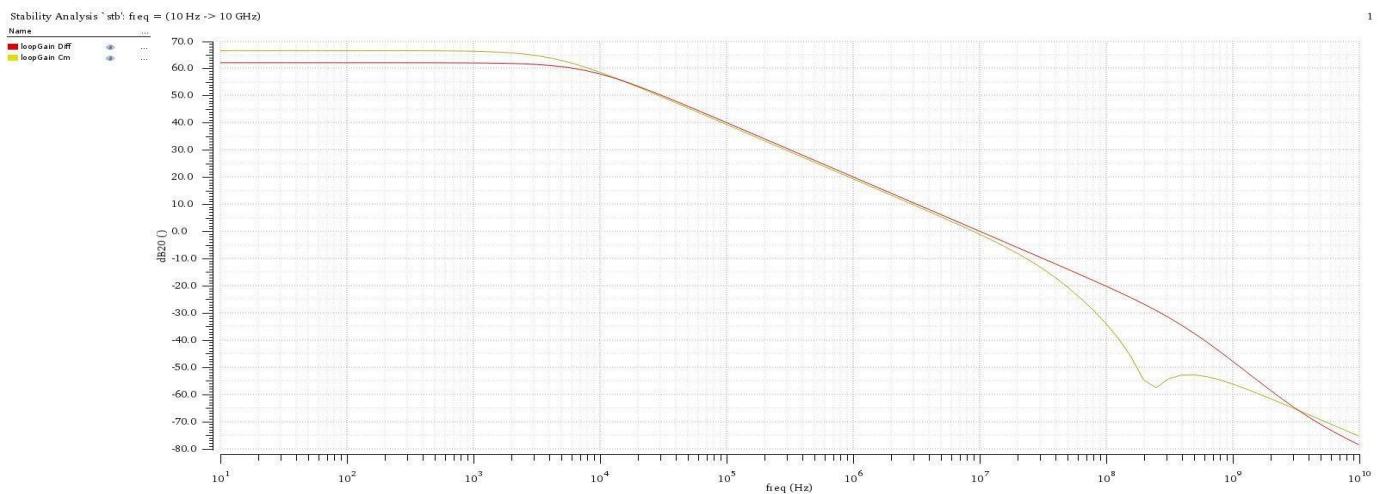


Figure 37 Diff and CM gain overlaid.

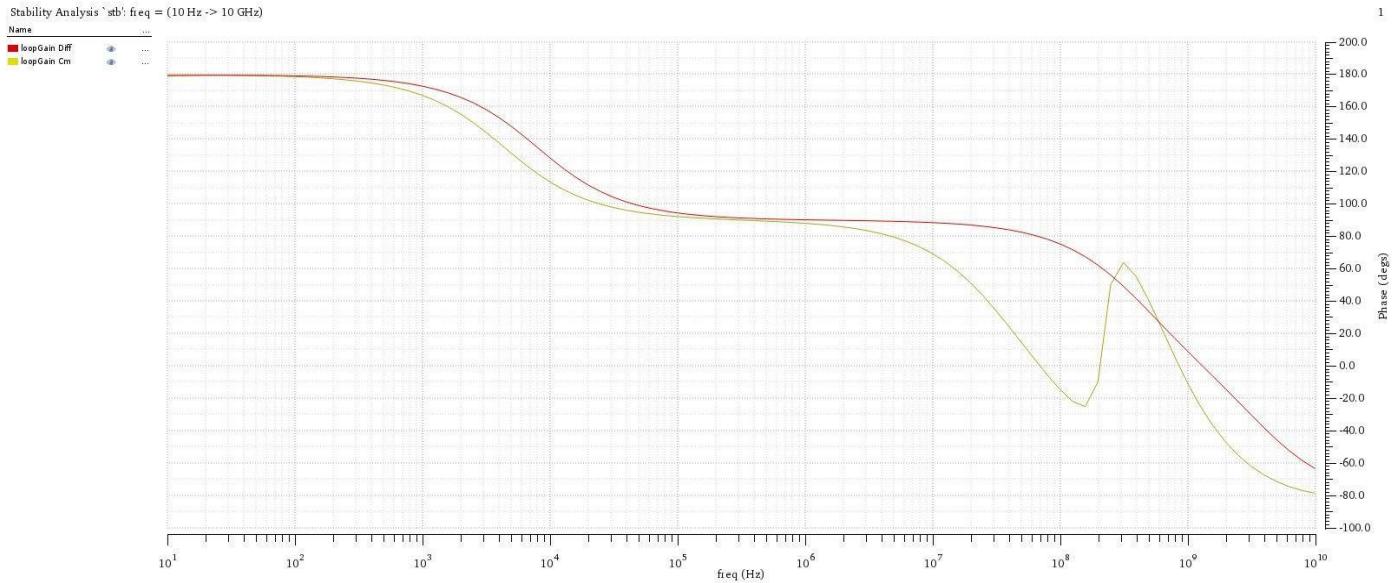


Figure 39 DIFF and CM PHASE overlaid.

Firstly the differential gain equal 62dB I want it to be equal 60 dB after tuning the results is below.

Differential results:

ymax(mag(getData("loopGain" ?result "stb"))))	1.002E3
ymax(dB20(mag(getData("loopGain" ?result "stb")))))	60.02
bandwidth(mag(getData("loopGain" ?result "stb")) 3 "low")	8.411E3
gainBwProd(mag(getData("loopGain" ?result "stb"))))	8.448E6
getData("/phaseMargin" ?result "stb_margin") (Deg)	87.03

Figure 40 Diff Results.

As shown in Figure $A_{DIFF} = 60.02 \approx 60dB$.

CM results:

ymax(mag(getData("loopGain" ?result "stb"))))	2.211E3
ymax(dB20(mag(getData("loopGain" ?result "stb")))))	66.89
bandwidth(mag(getData("loopGain" ?result "stb")) 3 "low")	5.730E3
gainBwProd(mag(getData("loopGain" ?result "stb"))))	12.70E6
getData("/phaseMargin" ?result "stb_margin") (Deg)	47.07

Figure 41 CM Results.

	Differential	Common mode
GBW	8.448M	12.7M
PM	87.03	47.07

As shown in table GBW of DIFF is lower than CM, PM of DIFF is higher than CM and in both is satisfied.

Comment: Differential more stable than common mode.

NOTE: The phase margin of the CM is 47 we might see a slight peeking in the transient run.

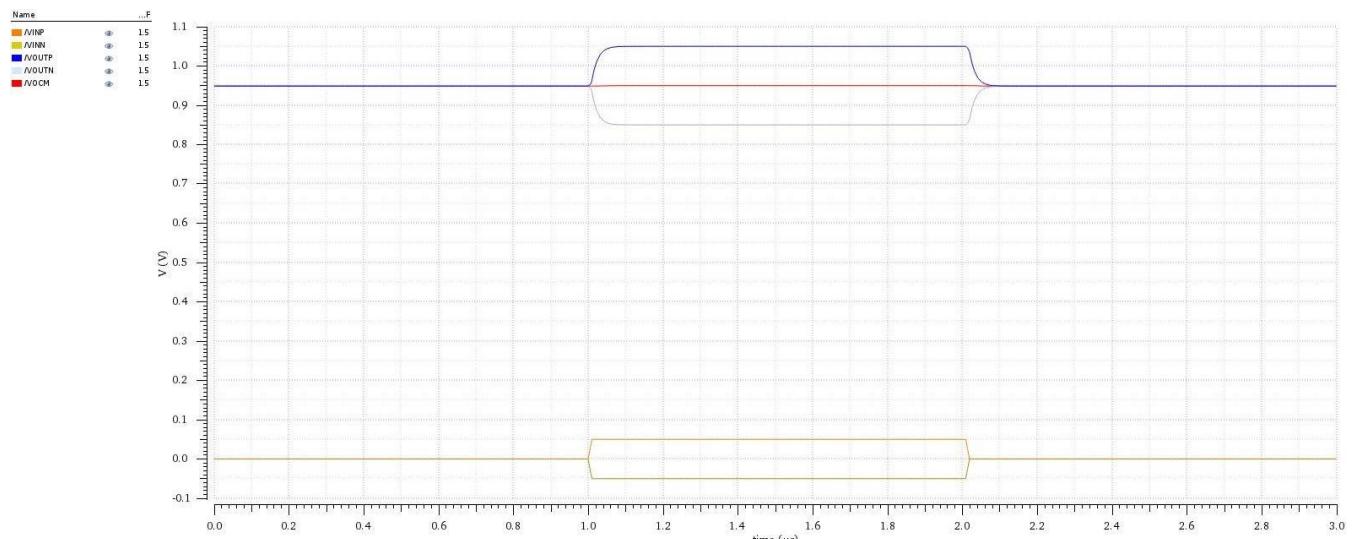
- $GBW_{CM} > GBW_{diff}$ as CM LG has higher gain.
- $PM_{CM} < PM_{diff}$ as $GBW \approx G_x \rightarrow G_{xCM} > G_{xdiff}$ and that make $PM_{CM} < PM_{diff}$.

	Open loop	Closed loop
DC LG	60.02dB	70.01 dB
GBW	8.448 M	37.55 M

Comment: The results are not the same as I calculated the values of the open loop LG and GBW by assuming that beta = 1/3 which is not so accurate as it should include the OTA parasitic capacitances.

PART 6: Closed Loop Simulation (Transient Analysis)

Plot the transient signals at VINP, VINV, VOUTP, VOUTN, and VOCM overlaid in the same figure.



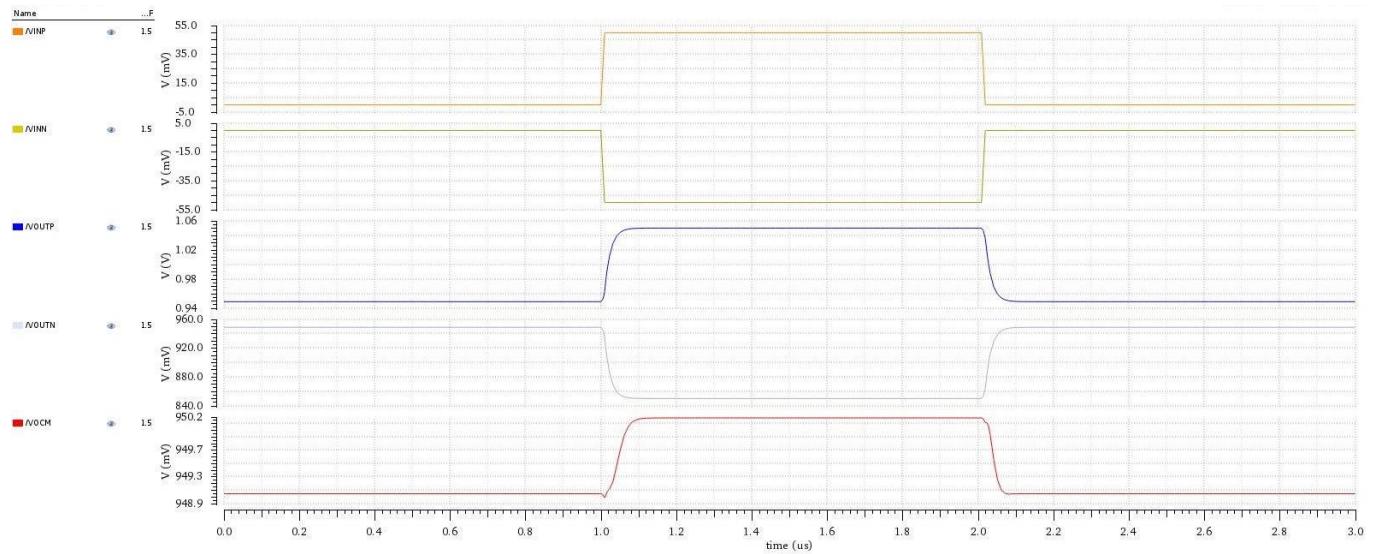


Figure 43 Transient signals.

Do you notice any differential/CM ringing? Are both loops stable with adequate PM?

Yes, there is some CM ringing as expected as the phase margin of the CM loop is 47.07 which is less than 76 but also, it's still stable.

Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.

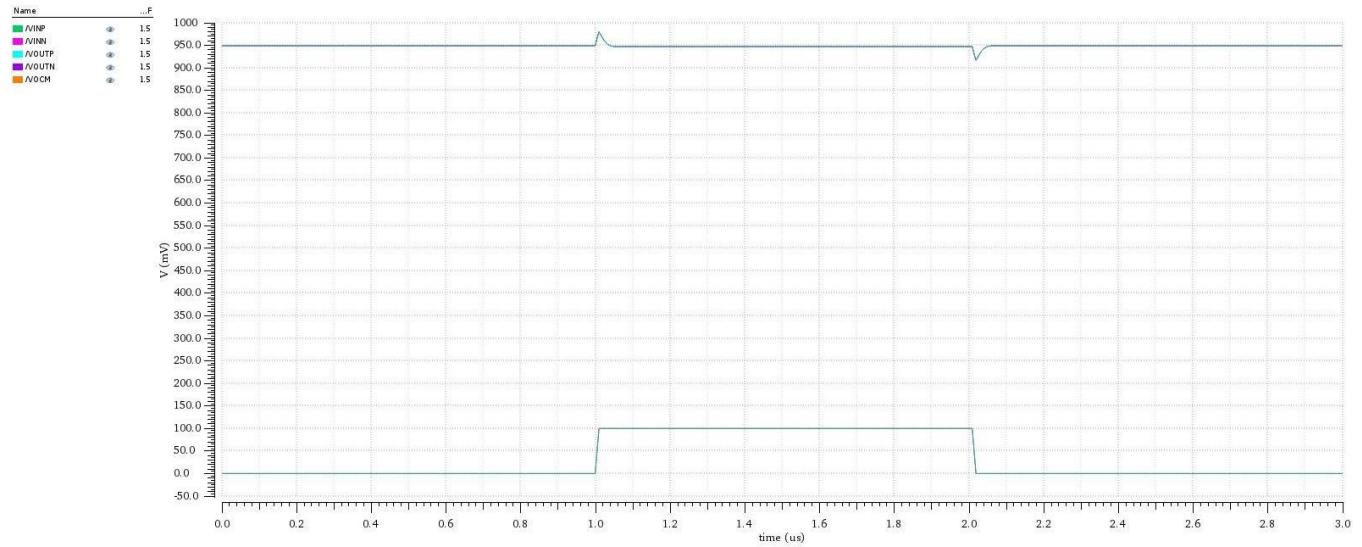


Figure 44 transient signals at common input.

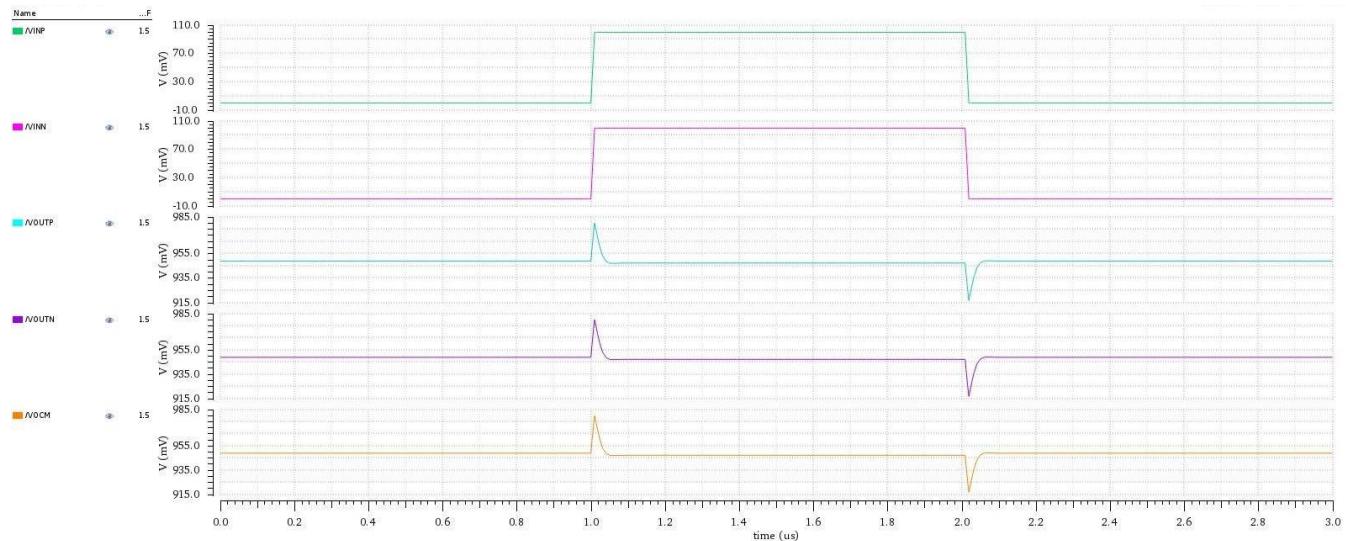


Figure 45 Transient signals.

Do you notice any differential/CM ringing? Are both loops stable with adequate PM?

There is a differential overshoot in VOUTP, VOUTN, VOCM.

Both loops are stable.

Phase margin of the differential loop is much bigger than that of the CM loop.

Output swing:

Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.

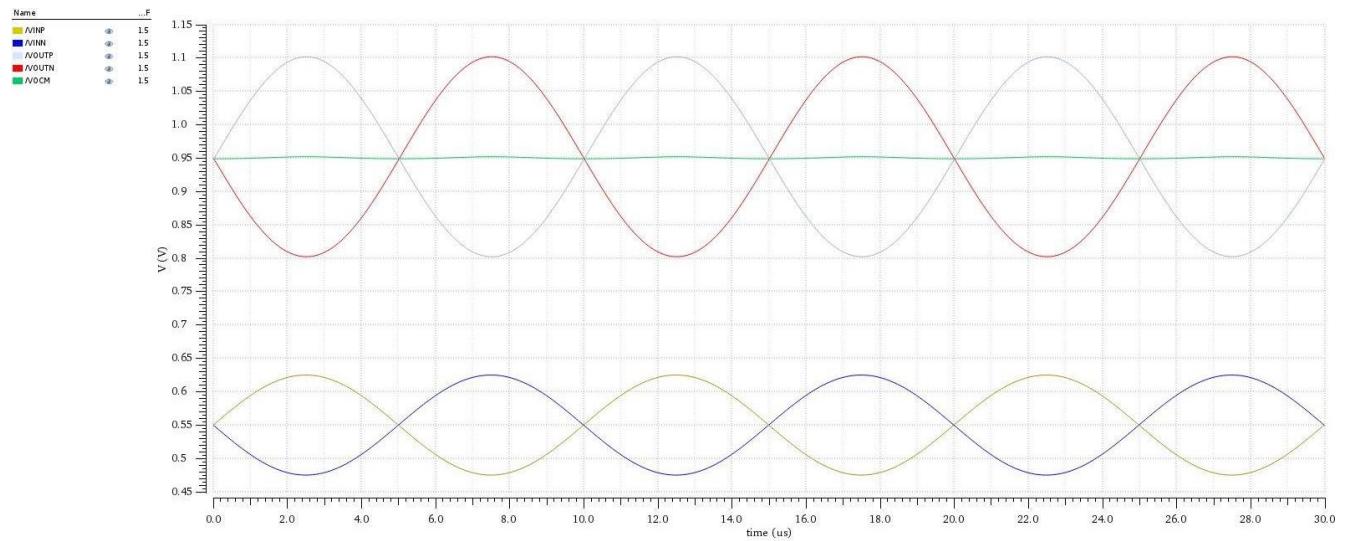


Figure 46 Transient signals.

Plot the transient signals at VIDIFF and VODIFF overlaid in the same figure.

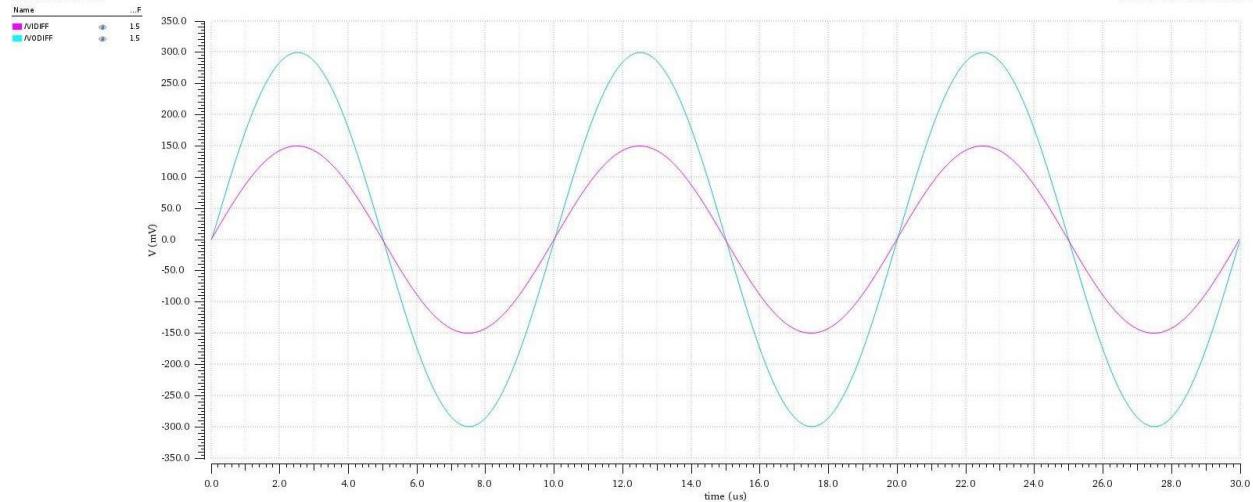


Figure 47 Transient signals.

Calculate the diff input and output peak-to-peak swings and the closed loop gain.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Lab_11:part_6:1	/VINP				
Lab_11:part_6:1	/VINN				
Lab_11:part_6:1	/VOUTP				
Lab_11:part_6:1	/VOUTN				
Lab_11:part_6:1	/VOCM				
Lab_11:part_6:1	/VIDIFF				
Lab_11:part_6:1	/VODIFF				
Lab_11:part_6:1	Vout_PTP	599.3m			
Lab_11:part_6:1	Vin_PTP	300m			
Lab_11:part_6:1	Av_cl	1.998			

Figure 48 Results from simulator.

$$A_{vcl} = \frac{V_{ODIFF\ Peak\ to\ peak}}{V_{INDIFF\ Peak\ to\ peak}} = 1.998 \approx 2$$

another check that the closed loop gain is satisfied.

CMIR Check:

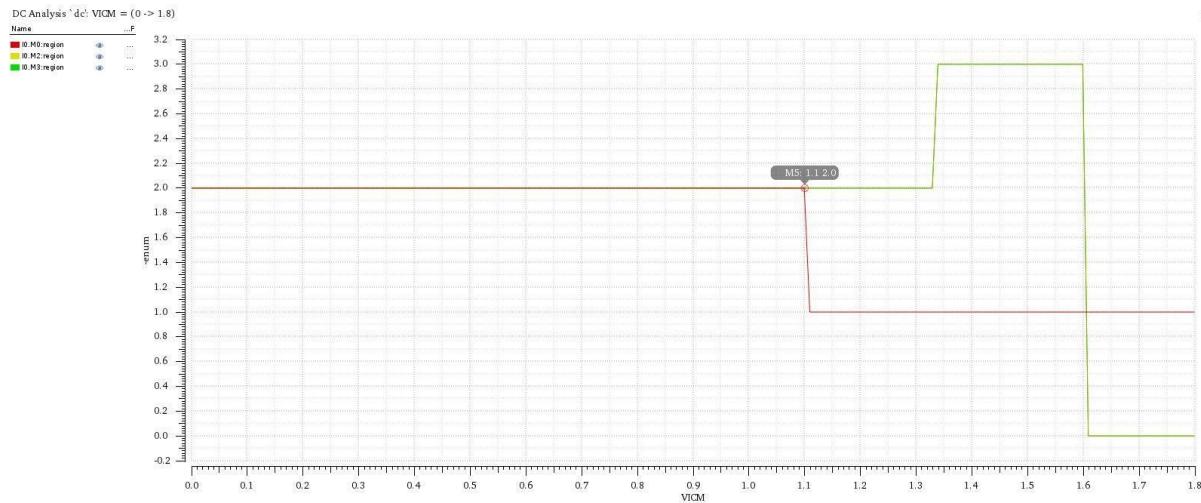


Figure 49 Regions of OTA vs VICM.

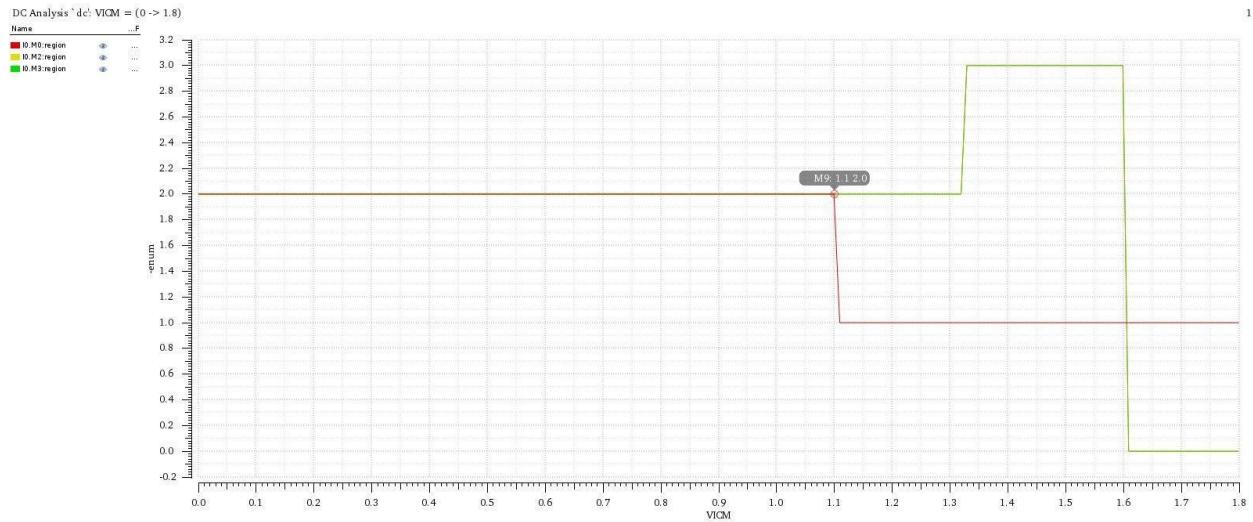


Figure 50 Regions vs VICM.

As shown the CMIR is satisfied $0 \rightarrow 1.12$

Spec	Required	Achieved
A_{cl}	2	1.998
Phase Margin	≥ 70	87.03
OTA Current	$\leq 80\mu$	80.6 μ
CMFB Circuit Current	$\leq 40\mu$	39.85 μ
CMIR-Low	≤ 0	0
CMIR-high	≥ 1.1	1.12
Differential Output Swing	1.2 Vpp	1.27VPP
DC Loop Gain	60 dB	60.02 dB
Closed Loop Bandwidth	10 MHz	10.23 MHz