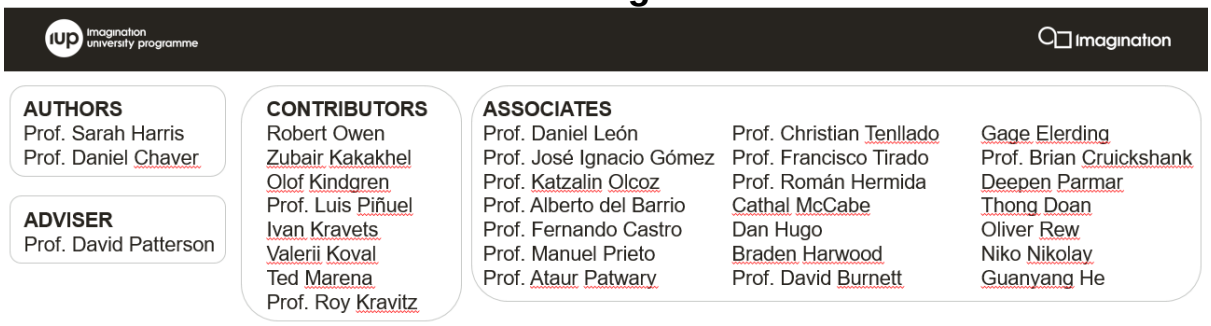
THE IMAGINATION UNIVERSITY PROGRAMME

RVfpga Lab 0
Overview of RVfpga Labs

Acknowledgements



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RVfpga Labs Overview

These RVfpga Labs provide hands-on understanding of RISC-V hardware and software. Before starting RVfpga Labs, you must have already completed the RVfpga Getting Started Guide provided by the Imagination University Programme (https://university.imgtec.com/). For example, if you have not already, install Xilinx's Vivado, PlatformIO and Verilator following the instructions in that guide. Also, make sure that you have copied the ***RVfpga*** folder that you downloaded from Imagination's University Programme to your machine. We will refer to the absolute path of the directory where you place folder RVfpga as [*RVfpgaPath*]. The RVfpga/src folder contains the Verilog and SystemVerilog sources for RVfpga, the RISC-V SoC that we will use and modify throughout the labs. The RVfpga/Labs folder contains resources you will use during Labs 1 to 10. The following labs are provided:

- Lab 0: Overview of RVfpga Labs
- Lab 1: Creating a Vivado Project
- Lab 2: C Programming
- Lab 3: RISC-V Assembly Language
- Lab 4: Function Calls
- Lab 5: Image Processing: C & Assembly
- Lab 6: Introduction to I/O
- Lab 7: 7-Segment Displays
- Lab 8: Timers
- Lab 9: Interrupt-driven I/O
- Lab 10: Serial Buses

These labs show how to view the RVfpga source code and target it to an FPGA (Lab 1), how to run programs on RVfpga (Labs 2-5), and how to modify RVfpga to add peripherals (Labs 6-10). See Table 1 in the RVfpga Getting Started Guide for the required software and hardware needed to use these labs.

If you do not have access to a Nexys A7 FPGA board (or the Nexys 4 DDR board), you can still complete these labs using Whisper (Western Digital's Instruction Set Simulator) and Verilator (an open-source HDL simulator).

The organization of the RVfpga/Labs/ folder is as follows:

- **LabInstructions:** Instructions for each lab, including exercises.
- **Lab1, Lab2,…:** Resources to be used while completing the labs
- **RVfpgaLabsSolutions:** Exercise solutions for each of the labs. **Instructors should remove this folder before distributing RVfpga to students**.
  - **Programs_Solutions:** software solutions for lab exercises
  - **RVfpga_Solutions:** Modified RVfpga source code (Verilog and SystemVerilog) extended as guided by the lab exercises (Labs 6-10). The source code is in folder [RVfpgaPath]/RVfpga/Labs/RVfpgaLabsSolutions/RVfpga_Solutions/src, where the bitstream (rvfpga.bit) is also provided. Document RVfpgaModifications.docx (also in that folder) describes the modifications performed to RVfpga in the Exercises of Labs 6-10.

RVfpga Labs 1-10 are well-suited for a one semester course for undergraduates. Prior to completing this RVfpga course, students should understand the fundamentals of logic design, processor design, and programming. This material is covered in the textbook *Digital Design & Computer Architecture: RISC-V Edition*, Harris & Harris, © Elsevier (expected publication: summer 2021).