swerv_wrapper_verilog_0 ifu axi ifu_axi_arid[2:0] ifu_axi_araddr[31:0] ifu_axi_arlen[7:0]▶ ifu_axi_arsize[2:0]> ifu_axi_arburst[1:0]> ifu_axi_arlock ifu_axi_arcache[3:0] ifu_axi_arprot[2:0]> ifu_axi_arregion[3:0]▶ ifu_axi_arqos[3:0]▶ ifu_axi_arready < ifu_axi_rid[2:0]◀ ifu_axi_rdata[63:0]◀ ifu_axi_rresp[1:0] < ifu_axi_rlast ifu_axi_rvalid◀ ifu_axi_rready lsu_axi_awid[3:0] Isu_axi_awaddr[31:0]> Isu_axi_awlen[7:0]> lsu_axi_awsize[2:0]▶ Isu_axi_awburst[1:0]> Isu_axi_awlock Isu_axi_awcache[3:0] Isu_axi_awprot[2:0] Isu_axi_awregion[3:0]▶ lsu_axi_awqos[3:0]> lsu_axi_awvalid Isu_axi_awready◀ Isu_axi_wdata[63:0]> lsu_axi_wstrb[7:0] lsu_axi_wlast lsu_axi_wvalid Isu_axi_wready < lsu_axi_bid[3:0]◀ lsu_axi_bresp[1:0]◀ lsu_axi_bvalid Isu_axi_bready> Isu_axi_arid[3:0] lsu_axi_araddr[31:0]> Isu_axi_arlen[7:0] Isu_axi_arsize[2:0]> ctk
nmi_int
nmi_vec[31:0]
ttmer_int
dmi_reg_en
dmi_reg_anddr[6:0]
dmi_reg_wdata[31:0] Isu_axi_arburst[1:0]> lsu_axi_arlock> lsu_axi_arcache[3:0]▶ Isu_axi_arprot[2:0]> lsu_axi_arregion[3:0] > lsu_axi_arqos[3:0] > lsu_axi_arready◀ Isu_axi_rid[3:0]◀ •Odmi_hard_reset lsu_axi_rdata[63:0]◀ lsu_axi_rresp[1:0]◀ lsu_axi_rlast< lsu_axi_rvalid◀ Isu_axi_rready> sb_axi= sb_axi_awid[0:0] sb_axi_awaddr[31:0]> sb_axi_awlen[7:0]> sb_axi_awsize[2:0] sb_axi_awburst[1:0]> sb_axi_awlock sb_axi_awcache[3:0]> sb_axi_awprot[2:0]> sb_axi_awregion[3:0] sb_axi_awqos[3:0]> sb_axi_awvalid sb_axi_awready ◀
sb_axi_wdata[63:0]▶ sb_axi_wstrb[7:0] sb_axi_wlast sb_axi_wready sb_axi_bid[0:0] sb_axi_bresp[1:0] < sb_axi_bvalid sb_axi_bready sb_axi_arid[0:0]> sb_axi_araddr[31:0] sb_axi_arlen[7:0] sb_axi_arsize[2:0]> sb_axi_arburst[1:0]> sb_axi_arlock> sb_axi_arcache[3:0] sb_axi_arprot[2:0]> sb_axi_arregion[3:0] > sb_axi_arqos[3:0] > sb_axi_arready < sb_axi_rid[0:0] sb_axi_rdata[63:0] sb_axi_rresp[1:0] < sb_axi_rlast sb_axi_rvalid sb axi rreadv dmi_reg_rdata[31:0]

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