swerv_wrapper_verilog_0

ifu_axi_...
ifu_axi_arid[2:0]
ifu_axi_araddr[31:0]
ifu_axi_arlen[7:0]
ifu_axi_arsize[2:0]
ifu_axi_arburst[1:0]
ifu_axi_arlock
ifu_axi_arcache[3:0]
ifu_axi_arprot[2:0]
ifu_axi_arregion[3:0]
ifu_axi_arqos[3:0]
ifu_axi_arvalid
ifu_axi_arready
ifu_axi_rid[2:0]
ifu_axi_rdata[63:0]
ifu_axi_rresp[1:0]
ifu_axi_rlast
ifu_axi_rvalid
ifu_axi_rready
lsu_axi_...
lsu_axi_awid[3:0]
lsu_axi_awaddr[31:0]
lsu_axi_awlen[7:0]
lsu_axi_awsize[2:0]
lsu_axi_awburst[1:0]
lsu_axi_awlock
lsu_axi_awcache[3:0]
lsu_axi_awprot[2:0]
lsu_axi_awregion[3:0]
lsu_axi_awqos[3:0]
lsu_axi_awvalid
lsu_axi_wdata[63:0]
lsu_axi_wstrb[7:0]
lsu_axi_wlast
lsu_axi_wvalid
lsu_axi_wready
lsu_axi_bid[3:0]
lsu_axi_bresp[1:0]
lsu_axi_bvalid
lsu_axi_bready
lsu_axi_arid[3:0]
lsu_axi_araddr[31:0]
lsu_axi_arlen[7:0]
lsu_axi_arsize[2:0]
lsu_axi_arburst[1:0]
lsu_axi_arlock
lsu_axi_arcache[3:0]
lsu_axi_arprot[2:0]
lsu_axi_arregion[3:0]
lsu_axi_arqos[3:0]
lsu_axi_arvalid
lsu_axi_arready
lsu_axi_rid[3:0]
lsu_axi_rdata[63:0]
lsu_axi_rresp[1:0]
lsu_axi_rlast
lsu_axi_rvalid
lsu_axi_rready
sb_axi_...
sb_axi_awid[0:0]
sb_axi_awaddr[31:0]
sb_axi_awlen[7:0]
sb_axi_awsize[2:0]
sb_axi_awburst[1:0]
sb_axi_awlock
sb_axi_awcache[3:0]
sb_axi_awprot[2:0]
sb_axi_awregion[3:0]
sb_axi_awqos[3:0]
sb_axi_awvalid
sb_axi_awready
sb_axi_wdata[63:0]
sb_axi_wstrb[7:0]
sb_axi_wlast
sb_axi_wvalid
sb_axi_wready
sb_axi_bid[0:0]
sb_axi_bresp[1:0]
sb_axi_bvalid
sb_axi_bready
sb_axi_arid[0:0]
sb_axi_araddr[31:0]
sb_axi_arlen[7:0]
sb_axi_arsize[2:0]
sb_axi_arburst[1:0]
sb_axi_arlock
sb_axi_arcache[3:0]
sb_axi_arprot[2:0]
sb_axi_arregion[3:0]
sb_axi_arqos[3:0]
sb_axi_arvalid
sb_axi_arready
sb_axi_rid[0:0]
sb_axi_rdata[63:0]
sb_axi_rresp[1:0]
sb_axi_rlast
sb_axi_rvalid
sb_axi_rready
dmi_reg_rdata[31:0]

clk
rst
nmi_int
nmi_vec[31:0]
timer_int
dmi_reg_en
dmi_reg_addr[6:0]
dmi_reg_wr_en
dmi_reg_wdata[31:0]
dmi_hard_reset

swerv_wrapper_verilog_v1_0

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intcon_wrapper_bd_0

clk_i_wrapper
rst_ni_wrapper
ifu_arid[2:0]
ifu_araddr[31:0]
ifu_arlen[7:0]
ifu_arsize[2:0]
ifu_arburst[1:0]
ifu_arlock
ifu_arcache[3:0]
ifu_arprot[2:0]
ifu_arregion[3:0]
ifu_arqos[3:0]
ifu_arvalid
ifu_rready
lsu_awid[3:0]
lsu_awaddr[31:0]
lsu_awlen[7:0]
lsu_awsize[2:0]
lsu_awburst[1:0]
lsu_awlock
lsu_awcache[3:0]
lsu_awprot[2:0]
lsu_awregion[3:0]
lsu_awqos[3:0]
lsu_awvalid
lsu_wdata[63:0]
lsu_wstrb[7:0]
lsu_wlast
lsu_wvalid
lsu_arid[3:0]
lsu_araddr[31:0]
lsu_arlen[7:0]
lsu_arsize[2:0]
lsu_arburst[1:0]
lsu_arlock
lsu_arcache[3:0]
lsu_arprot[2:0]
lsu_arregion[3:0]
lsu_arqos[3:0]
lsu_arvalid
lsu_bready
lsu_rready
sb_awid[0:0]
sb_awaddr[31:0]
sb_awlen[7:0]
sb_awsize[2:0]
sb_awburst[1:0]
sb_awlock
sb_awcache[3:0]
sb_awprot[2:0]
sb_awregion[3:0]
sb_awqos[3:0]
sb_awvalid
sb_wdata[63:0]
sb_wstrb[7:0]
sb_wlast
sb_wvalid
sb_bready
sb_arid[0:0]
sb_araddr[31:0]
sb_arlen[7:0]
sb_arsize[2:0]
sb_arburst[1:0]
sb_arlock
sb_arcache[3:0]
sb_arprot[2:0]
sb_arregion[3:0]
sb_arqos[3:0]
sb_arvalid
sb_rready
ram_awready
ram_arready
ram_wready
ram_bid[5:0]
ram_bresp[1:0]
ram_bvalid
ram_rid[5:0]
ram_rdata[63:0]
ram_rresp[1:0]
ram_rlast
ram_rvalid
wb_rom_dat_i[31:0]
wb_rom_ack_i
wb_spi_flash_dat_i[31:0]
wb_spi_flash_ack_i
wb_spi_flash_err_i
wb_spi_flash_rty_i
wb_sys_dat_i[31:0]
wb_sys_ack_i
wb_sys_err_i
wb_sys_rty_i
wb_uart_dat_i[31:0]
wb_uart_ack_i
wb_uart_err_i
wb_uart_rty_i
wb_gpio_dat_i[31:0]
wb_gpio_ack_i
wb_gpio_err_i
wb_ptc_dat_i[31:0]
wb_ptc_ack_i
wb_ptc_err_i
wb_ptc_rty_i
wb_spi_accel_dat_i[31:0]
wb_spi_accel_ack_i
wb_spi_accel_err_i
wb_spi_accel_rty_i

o_ifu_arready
o_ifu_rid[2:0]
o_ifu_rdata[63:0]
o_ifu_rresp[1:0]
o_ifu_rlast
o_ifu_rvalid
o_lsu_awready
o_lsu_arready
o_lsu_wready
o_lsu_bid[3:0]
o_lsu_bresp[1:0]
o_lsu_bvalid
o_lsu_rid[3:0]
o_lsu_rdata[63:0]
o_lsu_rresp[1:0]
o_lsu_rlast
o_lsu_rvalid
o_sb_awready
o_sb_arready
o_sb_wready
o_sb_bid[0:0]
o_sb_bresp[1:0]
o_sb_bvalid
o_sb_rid[0:0]
o_sb_rdata[63:0]
o_sb_rresp[1:0]
o_sb_rlast
o_sb_rvalid
o_ram_awid[5:0]
o_ram_awaddr[31:0]
o_ram_awlen[7:0]
o_ram_awsize[2:0]
o_ram_awburst[1:0]
o_ram_awlock
o_ram_awcache[3:0]
o_ram_awprot[2:0]
o_ram_awregion[3:0]
o_ram_awqos[3:0]
o_ram_awvalid
o_ram_awid[5:0]
o_ram_araddr[31:0]
o_ram_arlen[7:0]
o_ram_arsize[2:0]
o_ram_arburst[1:0]
o_ram_arlock
o_ram_arcache[3:0]
o_ram_arprot[2:0]
o_ram_arregion[3:0]
o_ram_arqos[3:0]
o_ram_arvalid
o_ram_wdata[63:0]
o_ram_wstrb[7:0]
o_ram_wlast
o_ram_wvalid
o_ram_bready
o_ram_rready
wb_rom_adr_o[31:0]
wb_rom_dat_o[31:0]
wb_rom_sel_o[3:0]
wb_rom_we_o
wb_rom_cyc_o
wb_rom_stb_o
wb_spi_flash_adr_o[31:0]
wb_spi_flash_dat_o[31:0]
wb_spi_flash_sel_o[3:0]
wb_spi_flash_we_o
wb_spi_flash_cyc_o
wb_spi_flash_stb_o
wb_spi_flash_ctl_o[2:0]
wb_spi_flash_bte_o[1:0]
wb_sys_adr_o[31:0]
wb_sys_dat_o[31:0]
wb_sys_sel_o[3:0]
wb_sys_we_o
wb_sys_cyc_o
wb_sys_stb_o
wb_sys_ctl_o[2:0]
wb_sys_bte_o[1:0]
wb_uart_adr_o[31:0]
wb_uart_dat_o[31:0]
wb_uart_sel_o[3:0]
wb_uart_we_o
wb_uart_cyc_o
wb_uart_stb_o
wb_uart_ctl_o[2:0]
wb_uart_bte_o[1:0]
wb_gpio_adr_o[7:0]
wb_gpio_dat_o[31:0]
wb_gpio_sel_o[3:0]
wb_gpio_we_o
wb_gpio_cyc_o
wb_gpio_stb_o
wb_ptc_adr_o[31:0]
wb_ptc_dat_o[31:0]
wb_ptc_sel_o[3:0]
wb_ptc_we_o
wb_ptc_cyc_o
wb_ptc_stb_o
wb_ptc_ctl_o[2:0]
wb_ptc_bte_o[1:0]
wb_spi_accel_adr_o[31:0]
wb_spi_accel_dat_o[31:0]
wb_spi_accel_sel_o[3:0]
wb_spi_accel_we_o
wb_spi_accel_cyc_o
wb_spi_accel_stb_o
wb_spi_accel_ctl_o[2:0]
wb_spi_accel_bte_o[1:0]

intcon_wrapper_bd_v1_0

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bootrom_wrapper_0

clk
rst
wb_adr[31:0]
wb_dat[31:0]
wb_sel[3:0]
wb_we
wb_cyc
wb_stb

o_wb_ack
o_wb_rdt[31:0]

bootrom_wrapper_v1_0

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syscon_wrapper_0

clk
rst
gpio_irq
ptc_irq
ram_init_done
ram_init_error
wb_adr[31:0]
wb_dat[31:0]
wb_sel[3:0]
wb_we
wb_cyc
wb_stb

o_timer_irq
o_nmi_vec[31:0]
o_nmi_int
o_wb_rdt[31:0]
o_wb_ack
AN[7:0]
Digits_Bits[6:0]

syscon_wrapper_v1_0