ECE 581 Homework 3

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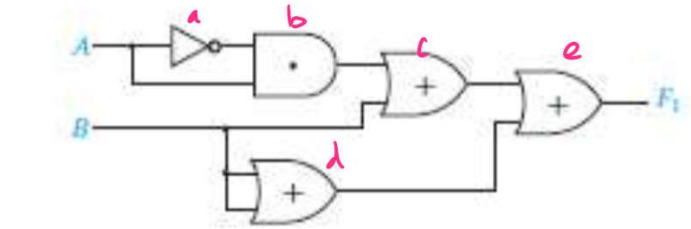
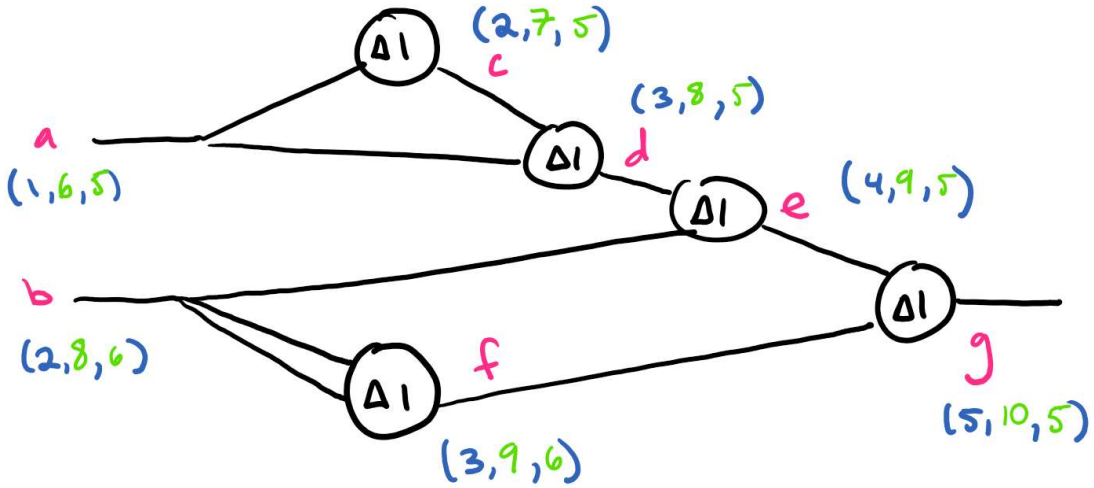
Problem 1. Consider the following circuit where the delay of each gate is one-time unit. Use the topological analysis method to estimate the timing parameters.



(5)

1) Assume that A arrives at time 1, B arrives at time 2, calculate the latest time when F1 is produced.

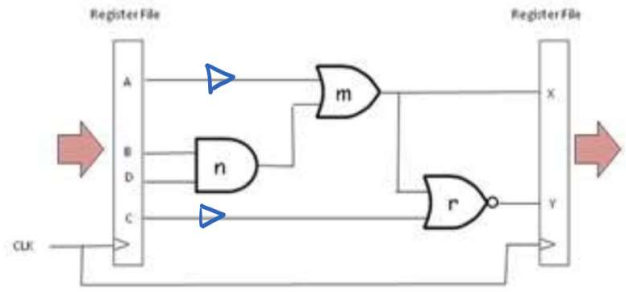
2) Assume that F1 should be expected to be available before time 10 (similar to the setup time), calculate the expected times for A and B, respectively? (6, 8)



P1.1 The latest time when F1 is produced is time 5.

P1.2 The expected time for A is time 6 and the expected time for B is time 8.

Problem 2. Determine the maximum clock frequency and whether any hold time violations could occur. Discuss the possible solution to avoid the hold time violation. Each gate has the same delay specification. T_{cd} is the contamination delay (the minimum delay) and T_{pd} is the propagation delay (the maximum delay).



FF	T_{ccq}=31ps	T_{pcq}=81ps	T_{setup}=51ps	T_{hold}=61ps
Gate	T_{cd}=26ps	T_{pd}=41ps		

Maximum Clock Frequency

$$T_c \geq t_{pcq} + t_{Pd} + t_{setup}$$

$$= 81ps + 3(41ps) + 51ps$$

$$= 255ps$$

$$f_{max} = 1/255ps = 3.92GHz$$

Possible Hold Time Violation? (Yes)

Short path if B = 0 or D = 0 and A rises after a clock cycle. X and Y will both change if C = 1.

$$t_{ccq} + t_{cd} = 31ps + 26ps = 57ps$$

$$t_{hold} = 61ps$$

* Possible hold time Violation

Hold Time Solution

We can add buffers to A & C to increase propagation delay keeping X and Y stable past hold time.

Add buffers after the A and C outputs.