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AN-5081

High Gain Step-up Converter with Coupled Inductor for Piezoelectric Element Drive

Introduction

Recently, the piezoelectric actuator is widely used in many applications especially the mobile devices such as digital cameras and smart phone camera modules due to its compact size and high resolution of the displacement. While the available power source is low-voltage battery in the mobile devices, the high driving voltage is required to drive piezoelectric actuators for high performances. Therefore, a step-up converter is necessary which has high voltage conversion ratio from several volts to several decades or more than one hundred volts.

Conventional step-up dc-dc converters or boost converters are not suitable for high voltage conversion ratio since the effective series resistor (ESR) of the boost inductor prohibits the output voltage from increasing more than 10 times of the input voltage. In this article, a high step-up dc-dc converter with tapped inductor or coupled inductor is introduced and its operational principle and design procedure will be described as well.

For a 1.5 W system with 3 V of the input and 60 V of the output as an example, the experimental results and schematic are given with simple explanation of the full-bridge driver stage of the FAN8831, an optimized control IC including dc-dc step-up converter and full-bridge driver for driving piezoelectric actuators by Fairchild.

Characteristics of Piezoelectric Actuators

Unlike electric motors, piezoelectric actuators convert the electrical energy to the mechanical energy directly with no generation of magnetic field. High resolution of the displacement in sub-nanometer range, excellent dynamic responses, and low power consumption are the advantages of the piezoelectric actuator also [1]. Thus, piezoelectric actuators are used in various applications nowadays.

The piezoelectric actuators are mainly characterized by a non-linear capacitive behavior. Figure 1 shows the impedance curve of a piezoelectric actuator near resonance frequencies. Figure 2 shows the equivalent electrical circuit of a piezoelectric actuator, Van Dyke's Model [2]. At low frequencies, since the left leg (R_m-L_m-C_m in series) looks C_m only due to its high impedance compared to L_m and R_m, the total impedance is the sum of C_m and C_o. At the series resonance frequency fr, the magnitudes of the impedance of L_m and C_m are same and their polarities are opposite each other so that the total impedance of the left leg is R_m. Thus, the total impedance of the piezoelectric actuator and the series resonance frequency are as follows:

$$Z_{f_r} = R_m \parallel Z_{C_o @ f_r} = \frac{R_m Z_{C_o @ f_r}}{R_m + Z_{C_o @ f_r}}$$
$$f_r = \frac{1}{2\pi\sqrt{L_m C_m}} \quad (1)$$

Ignoring the damping resistor R_m the locally maximum total impedance occurs at the parallel resonance frequency f_a as follows:

$$f_a = \frac{1}{2\pi\sqrt{L_m C_{eq}}} \quad where \quad C_{eq} = \frac{C_o C_m}{C_o + C_m} \quad (2)$$

At high frequencies, the total impedance will be almost C_o because the left leg looks L_m only and the impedance of C_o is generally lower than that of L_m.

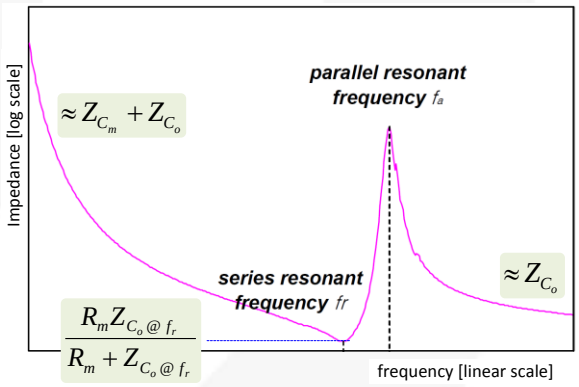


Figure 1. Impedance of Piezoelectric Actuator Near Resonance Frequencies

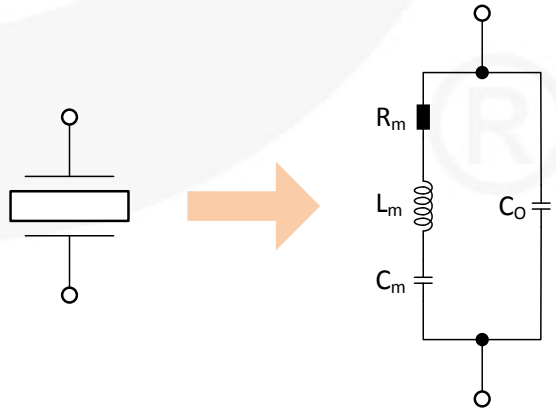


Figure 2. Equivalent Electrical Circuit of a Piezoelectric Actuator

The capacitance C_o depends on the area and thickness of the ceramic, as well as on its material properties. It also depends on the number of layers when considering the stacked actuators assembled with thin and laminar wafers of electro-active ceramic material electrically connected in parallel. To get mechanical movement, C_o should be charged and discharged repeatedly by a driver with an appropriate frequency. Meanwhile, the impedance curve is divided into three regions: capacitive regions for $f < f_r$ and $f > f_a$ and inductive region for $f_r < f < f_a$. For Zero Voltage Switching (ZVS) operation, it is usually recommended to operate in the inductive region since the operating current lags behind the applied voltage to the load. In the piezoelectric actuator, however, the energy in L_m is not enough to discharge C_o fully in general so that it is hard to achieve ZVS operation even though the piezoelectric actuator operates in the inductive region. Thus the charging and discharging currents show a large sharp shape in a hard switching manner in any operating frequencies.

The maximum mechanical movement is obtained when operating at the series resonance frequency f_r, since the total impedance of the piezoelectric actuator is the lowest at f_r. Thus it is effective to operate at f_r and it is required to consider how to improve the hard switching conditions to increase the efficiency by reducing switching losses. It is out of scope of this article but interesting topic.

Driving Piezoelectric Actuator

To drive piezoelectric actuators from a low-voltage battery in portable devices, a multi-stage converter is needed: a boost stage to get high driving voltage and a bridge stage to drive the piezoelectric actuators effectively, as shown in Figure 3.

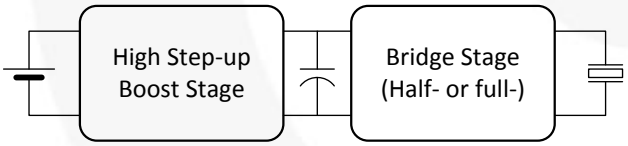


Figure 3. Power Stages to Drive Piezoelectric Actuators from Low-Voltage Battery

Ideally, the voltage conversion ratio of a conventional boost converter becomes infinity as the duty cycle increases to unity. In practical, however, it is limited due to the boost inductor copper loss. According to [3], the voltage conversion ratio of continuous conduction mode (CCM) operation with the ESR of the boost inductor is as follows:

$$\frac{V}{V_g} = \frac{1}{1-D}\frac{1}{\left(1+\frac{R_L}{(1-D)^2 R}\right)} \quad (3)$$

where V is the output voltage, V_g is the input voltage, D is the duty cycle, R is the load resistor, and R_L is the ESR of the boost inductor. The conversion ratio will be decreased as the ratio of R_L to R increases. Figure 4 shows the effect of the ESR in a graphical way. It is noticeable that the voltage conversion ratio does not exceed 5 when R_L is 1% of the load resistor R.

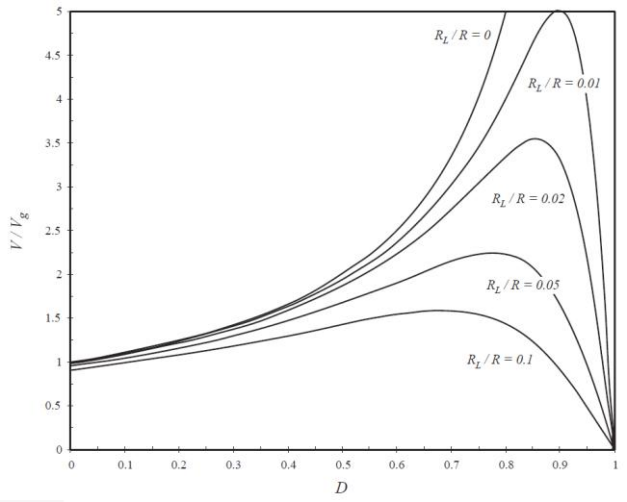


Figure 4. Voltage Conversion Ratio of a Boost Converter with Inductor Copper Loss (from reference [3])

There are two kinds of piezoelectric actuators in view point of construction: one is a single-layer, and the other is a multi-layer one. The single-layer one is relatively cheap and easily available but its driving voltage is so high up to several hundred voltages in peak-to-peak manner. Meanwhile, the multi-layer piezoelectric actuator has low driving voltage about 20 to 60 V in peak-to-peak manner, but it's expensive compared to the single-layer one. To make the total system cost low, it is favorable to use a single-layer one. It is required to provide a high driving voltage enough to drive the single-layer piezoelectric actuators even though the available power source is low-voltage battery in the mobile devices. As mentioned ahead, a conventional boost converter is not suitable for driving the single-layer piezoelectric actuators due to its low voltage conversion ratio. Therefore, a step-up converter is necessary which has high voltage conversion ratio from several volts to several decades or more than one hundred volts.

The voltage across the piezoelectric actuators changes its polarity to get the mechanical movement in the bridge stage with the high driving voltage which comes from the output of the high step-up boost stage. While the piezoelectric actuator shows either expansion or contraction with a half-bridge topology, it can be expanded and contracted with positive and negative applied voltage when a full-bridge is used. Therefore, full-bridge topologies as a secondary stage are more favorable to lighten the burden of the boost stage in its voltage conversion ratio point of view.

The FAN8831 is a suitable control IC for driving piezoelectric actuators manufactured by Fairchild. It contains both of two stages depicted in Figure 3. The Critical Conduction Mode (CRM) operated boost controller is integrated with a power MOSFET which has 36 V of the voltage rating. Many protection functions such as Over-Voltage Protection (OVP), Over-Current Protection (OCP), and Thermal Shutdown (TSD) are included in the boost controller as well. As a full-bridge stage, four high-voltage (75 V) rated MOSFETs are integrated: two are low-side driven and the others are high-side driven with high-side gate drivers. The shoot-

through prevention function is also included in the full-bridge stage. All of them are realized in QFN package sized 4 mm by 4 mm with 0.9 mm of the height.

In the next chapter, a high step-up dc-dc converter with tapped inductor or coupled inductor, a well-known topology is introduced. Its operational principle and design procedure is described as well.

High-Voltage Conversion Ratio Boost Converter with Coupled Inductor

Operational Principles

As described in the previous chapter, a conventional boost converter provides limited output voltage due to the copper loss of the inductor. Moreover, the duty cycle should be increased near to unity to get a large voltage conversion ratio. It requires a smaller inductance, resulting in the high current stress on the main switch and high conduction losses. Since the output voltage is imposed on the main switch when turned off, the voltage stress is also high and so does the switching losses. Figure 5 shows the disadvantages of the conventional boost converter.

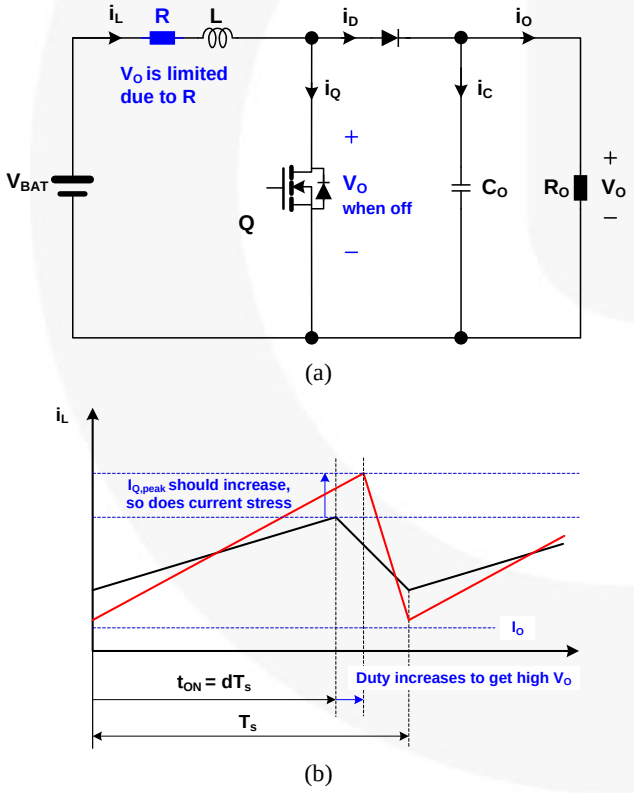


Figure 5. (a) Conventional Boost Converter and (b) its Inductor Current Waveforms when Duty Cycles Increases for Higher V_O

To overcome these shortcomings, lots of topologies have been proposed. Among them the coupled inductor boost converter has attracted a lot of attention due to the high voltage conversion ratio, no additional components, the simple winding structure in the inductor, and low voltage stress on the main switch. [4]-[7].

Figure 6 shows the schematic of the coupled inductor boost converter and its key waveforms in CRM operation. If the turn's ratio n is zero, i.e. N_2 is zero, it is identical to the conventional boost converter. Figure 7 shows the equivalent circuit for each mode. When the main switch (Q) turns on, $i_Q(t)$ increases with the slope of V_{BAT} over L_1, resulting in the built-up of energy in L_1. Since the voltage across the secondary turns N_2 is nV_{BAT}, the diode voltage $V_D(t)$ is V_O+nV_{BAT}, as shown in Figure 6 (b). After Q turns off, the voltage across the total inductor L_{eq} becomes V_O-V_{BAT}, so that the diode current $i_D(t)$ decreases with the slope of V_O-V_{BAT} over L_{eq}. Since the voltage across the primary turns N_1 is $N_1(V_O-V_{BAT})$ over N_1+N_2, the switch voltage $V_Q(t)$ is $(N_1V_O+N_2V_{BAT})$ over N_1+N_2, lower than V_O when N_2 is greater than N_1 for high voltage conversion ratio.

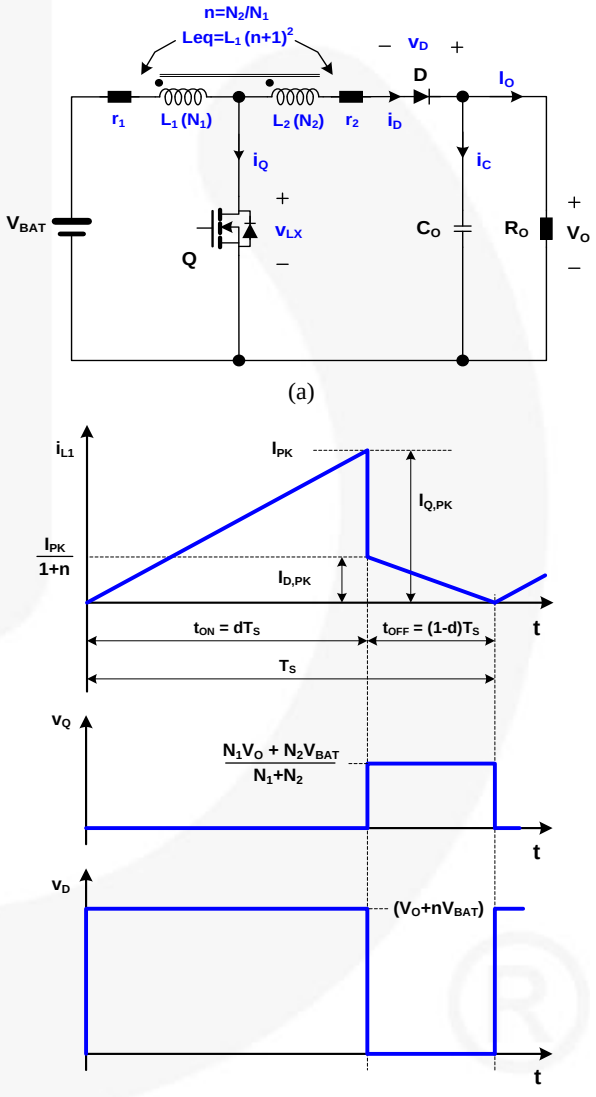


Figure 6. (a) Coupled Inductor Boost Converter and (b) its Key Waveforms: Inductor Current, Switch and Diode Voltages during CRM Operation

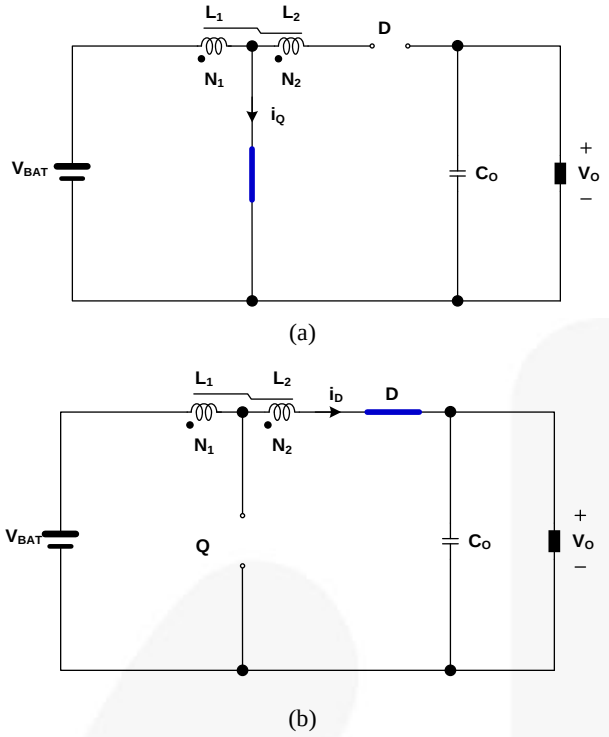


Figure 7. (a) Mode 1, Main Switch Turn-On (dTS) and (b) Mode 2, Main Switch Turn-Off ((1-d)TS) in CRM Operation

Since the inductors are coupled in one magnetic core, the total inductance is calculated as follows:

$$L_1 + L_2 : L_1 = (N_1 + N_2)^2 : N_1^2 \tag{4}$$

Therefore,

$$L_{eq} = L_1 + L_2 = (1+n)^2 L_1 \tag{5}$$

To obtain the voltage conversion ratio in CCM or CRM operations, the volt-sec balance is required either for L_1 or for L_2. Let's use L_2. The voltage across L_2 for each mode is as follows:

$$\begin{aligned} V_{L2} &= nV_{BAT} && during\ dT_S, \\ V_{L2} &= (V_{BAT} - V_O)\frac{N_2}{N_1 + N_2} && during\ (1-d)T_S \end{aligned} \tag{6}$$

The voltage conversion ratio can be obtained by letting the sum of the applied voltage on L_2 times its duration over one switching cycle be zero, as follows:

$$\begin{aligned} & nV_{BAT} \cdot dT_S + (V_{BAT} - V_O)\frac{N_2}{N_1 + N_2} \cdot (1-d)T_S = 0 \\ \Rightarrow\ & nV_{BAT} \cdot d \cdot \left(\frac{1}{n} + 1\right) = (1-d) \cdot (V_O - V_{BAT}) \\ \Rightarrow\ & dV_{BAT} + ndV_{BAT} = V_O - V_{BAT} - dV_O + dV_{BAT} \\ \Rightarrow\ & (1+nd)V_{BAT} = (1-d)V_O \\ \Rightarrow\ & \frac{V_O}{V_{BAT}} = \frac{1+nd}{1-d} \equiv G \end{aligned} \tag{7}$$

The peak current of the switch ($I_{Q,PK}$ or I_{PK}) is obtained as follows:

$$I_{PK} = \frac{V_{BAT}}{L_1} dT_S \tag{8}$$

Due to the CRM operation, the peak current of the diode ($I_{D,PK}$) is obtained as follows:

$$I_{D,PK} = \frac{V_O - V_{BAT}}{L_{eq}}(1-d)T_S = \frac{V_O - V_{BAT}}{(1+n)^2 L_1}(1-d)T_S \tag{9}$$

Since the output voltage is obtained as Equation (7), $I_{D,PK}$ can be expressed with I_{PK} as follows:

$$\begin{aligned} I_{D,PK} &= \frac{\frac{1+nd}{1-d}V_{BAT} - V_{BAT}}{(1+n)^2 L_1}(1-d)T_S \\ &= \frac{(1+nd-1+d)V_{BAT}}{(1+n)^2 L_1} T_S \\ &= \frac{(1+n)V_{BAT}}{(1+n)^2 L_1} dT_S = \frac{I_{PK}}{1+n} \end{aligned} \tag{10}$$

According to Equation (7), the voltage conversion ratio depends on the turn's ratio of the coupled inductor. If the turn's ratio is 3, the voltage gain becomes more than 10 for 0.7 of the duty cycle. It will be also decreased when the copper loss of the inductor is considered. Nevertheless, it is large compared to the conventional boost converter. Thus, it is possible to make a sufficient output voltage from a low-voltage battery to drive the piezoelectric actuator by tuning the turn's ratio. As can be seen in Figure 6, the voltage stress on the main switch is much lower than the conventional one. Therefore, the switching losses especially capacitive discharging losses can be reduced. However, the peak current of the main switch is 1+n times larger than the conventional one, which is one of the disadvantages of this topology. In addition, the voltage stress of the diode is increased as well.

Design Procedure

In this section, a design procedure for the coupled inductor boost converter using FAN8831 is presented with the specifications as follows:

- Nominal Input Voltage: 3.0 V_{DC} (Battery)
- Input Voltage Range: 2.7 ~ 3.3 V_{DC}
- Switching Frequency: 350 kHz at Full Load
- Output: 60 V_{DC} / 25 mA (1.5 W)

The FAN8831 provides Zero Current Detection (ZCD) function allowing the next switching at the moment the inductor current becomes zero. Thus the desired operation mode is CRM.

[STEP-1] Determine Turns Ratio and Duty Cycle

For prevent absolute maximum voltage in operating condition, the switching voltage V_{LX} should be lower than 35 V, as can be seen in Figure 8.

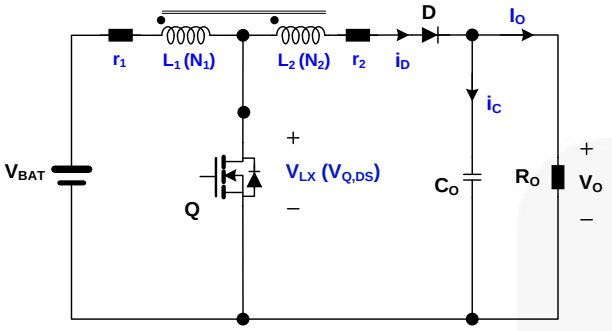


Figure 8. Schematic of coupled inductor boost converter

V_{LX} is almost determined by the drain voltage of the main switch clamped to the sum of the input voltage and the primary side magnetizing inductance voltage as follows:

$$V_{LX} = V_{Q,DS} = V_{BAT} + \frac{V_O - V_{BAT}}{n+1} = \frac{V_O + nV_{BAT}}{n+1} \quad (11)$$

Therefore, the turn's ratio can be calculated as follows:

$$n = \frac{V_O - V_{LX}}{V_{LX} - V_{BAT}} \quad (12)$$

To determine the turn's ratio, the input voltage variation has to be considered as well.

After getting the turn's ratio of the coupled inductor, the duty cycle can be determined using Equation (7) as follows:

$$d = \frac{G-1}{G+n} \quad (13)$$

(Design Example) To get V_{LX} of 16 V using Equation (12), the turns ratio is calculated as follows:

$$n_{max} = \frac{V_O - V_{LX}}{V_{LX} - V_{BAT,max}} = \frac{60-16}{16-3.3} = 3.46$$

$$n_{min} = \frac{V_O - V_{LX}}{V_{LX} - V_{BAT,min}} = \frac{60-16}{16-2.7} = 3.3$$

Thus the turn's ratio is selected as 4. Then the duty cycle is obtained using Equation (13).

$$d_{max} = \frac{\frac{V_O}{V_{BAT,min}} - 1}{\frac{V_O}{V_{BAT,min}} + n} = \frac{\frac{60}{2.7} - 1}{\frac{60}{2.7} + 4} = 0.81$$

$$d_{min} = \frac{\frac{V_O}{V_{BAT,max}} - 1}{\frac{V_O}{V_{BAT,max}} + n} = \frac{\frac{60}{3.3} - 1}{\frac{60}{3.3} + 4} = 0.77$$

Nominal 0.79 is the duty cycle of the converter when the input voltage is 3 V.

Like the conventional boost converter, the voltage conversion ratio or voltage gain of the coupled inductor boost converter is also limited due to the conduction losses in the used inductors. It is more considerable since the ESR of the coupled inductor is larger than the conventional one due to more turns. The voltage conversion ratio of CCM or CRM operation with the ESR of the boost inductor is obtained as follows:

$$\frac{V_O}{V_{BAT}} = \frac{1+nd}{1-d} \frac{1}{\left(1 + \frac{r_L}{R(1-d)} + \frac{r_1 d(1+n)^2}{R(1-d)^2}\right)} \quad (14)$$

where R is the load resistance, r_1 is the primary side ESR and r_L is the sum of r_1 and the secondary side ESR, r_2, as depicted in Figure 8. As can be seen in Equation (14), the decreasing factor becomes significant as the turns ratio of the coupled inductor increases to obtain the high voltage conversion ratio. Figure 9 shows Equation (14) in a graphical way with n=7, R=5,500 Ω, and r_L=1.5 Ω, 3.0 Ω, and 5.0 Ω as examples.

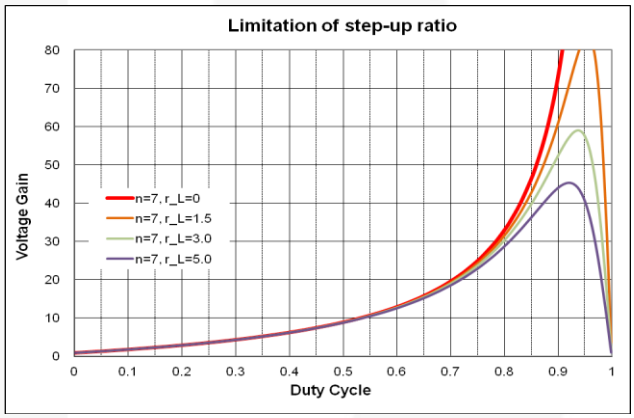


Figure 9. Voltage Conversion Ratio of the Coupled Inductor Boost Converter with ESRs of the Inductors

Compared to the ideal case in red curve (r_L=0 Ω), the practical cases with ESR show lower voltage gain as duty cycle increases. The voltage gain at duty cycle of 0.9, for example, could be reduced from more than 70 to around 60 with r_L=1.5 Ω. Even at duty cycle of 0.8, the voltage gain decreases by about 2 or 3 with r_L=1.5 Ω. Thus, it is needed to check whether the voltage gain with the measured ESR after making the coupled inductor is enough to meet the output voltage specification at the predetermined duty cycle. If not, the designer should reduce the ESR by increasing the wire thickness of the coupled inductor or determine the turn's ratio and the duty cycle again with more margins in STEP-1.

[STEP-2] Find Magnetizing Inductances

In CRM operation, the magnetizing inductance of the coupled inductor can be obtained from the slope of the inductor current, as shown in Figure 10. During t_{OFF}, the inductor current flows through the diode and its average over one switching period is equivalent to the load current, I_{OUT} which is given as a specification. The average of the diode current is calculated as follows:

$$I_{OUT} = \frac{I_{D,PK} \times (1-d)}{2} \quad (15)$$

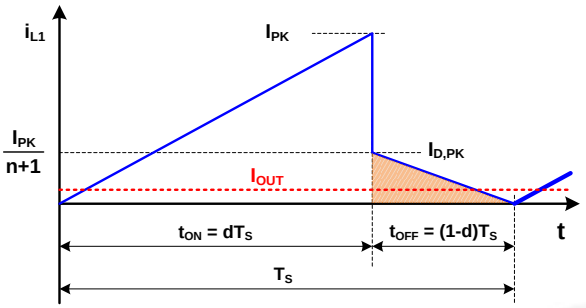


Figure 10. Current Waveform of the Coupled Inductor

Therefore, the diode peak current is expressed as follows:

$$I_{D,PK} = \frac{2I_{OUT}}{1-d} \tag{16}$$

According to Equation (10), the peak current of the main switch is obtained as follows:

$$I_{PK} = \frac{2I_{OUT}(1+n)}{1-d} \tag{17}$$

Combining Equations (17) and (8) yields

$$L_1 = \frac{V_{BAT}\,dT_S}{I_{PK}} = \frac{V_{BAT}\,d(1-d)T_S}{2I_{OUT}(1+n)} \tag{18}$$

To get more exact equation for the inductance, the system efficiency has to be considered. There are lots of loss factors in the converter such as the ESR of the inductor, MOSFET's turn-on resistance, diode's forward drop, the non-ideal coupling of transformer, and so on. For all kinds of the loss terms, it could be divided into two categories. The first is the losses after transformer in view point of the power flowing like diode's forward drop and including the transformer loss itself. In this case, the peak current required in Equation (17) should be increased to carry not only the output power but also the loss terms. On the other hand, the diode peak current calculated in Equation (16) is not changed since the output load current is kept constant regardless of the loss terms. Therefore, this loss factors related transformer and diode on the turn's ratio so that I_{PK} and L_1 in Equations (17) and (18)should be modified as follows:

$$I_{PK} = \frac{2I_{OUT}\left(1+\frac{n}{\eta}\right)}{1-d} \tag{19}$$

$$L_1 = \frac{V_{BAT}\,dT_S}{I_{PK}} = \frac{V_{BAT}\,d(1-d)T_S}{2I_{OUT}\left(1+\frac{n}{\eta}\right)} \tag{20}$$

where η is the expected efficiency of the system, generally 0.7~0.8.

The second category is the losses before transformer like the ESR of the inductor and $R_{DS(on)}$ of the MOSFET. Due to these losses the practical peak current of the switch is lower than the expected. As the inductor current increases, the voltage drops on the ESR and $R_{DS(on)}$ increases as well. The voltage applied on L_1 is reduced as time goes during t_{ON} so that the slope of the switch current decreases more and more, shown in Figure 11.

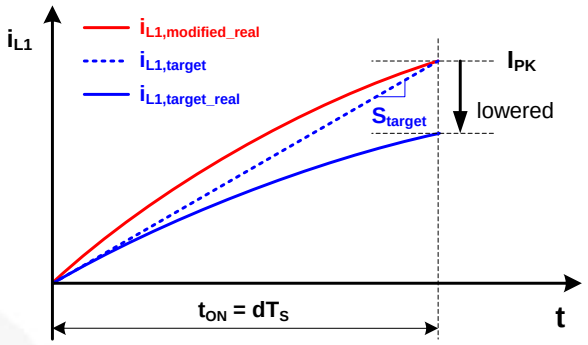


Figure 11. Current Waveform of the Coupled Inductor Considering ESR and $R_{DS(on)}$

Using the inductance L_1 calculated with Equation (20) is expected to make the peak switch current reach to I_{PK} during t_{ON}, as plotted in dotted line in Figure 11. The peak switch current I_{PK} is obtained from Equation (19), which allows the specified load current to be supplied during t_{OFF}. Due to the ESR and $R_{DS(on)}$, however, the slope of the inductor current decreases as the inductor current increases so that the real peak current of the inductor is lower than I_{PK} originally targeted, as depicted in a blue solid curve in Figure 11. The real trajectory of the inductor current with ESR, r_1 and $R_{DS(on)}$ can be expressed as follows:

$$i_{L_1}(t) = \frac{V_{IN}}{r_1 + R_{DS(on)}}\left(1 - e^{-\frac{r_1+R_{DS(on)}}{L_1}t}\right) \tag{21}$$

To make the red solid curve in Figure 11 to get required I_{PK} at $t = t_{ON}$, the following equation is obtained.

$$I_{PK} = \frac{V_{IN}}{r_1 + R_{DS(on)}}\left(1 - e^{-\frac{r_1+R_{DS(on)}}{L_1}t_{ON}}\right) \tag{22}$$

Therefore, the inductance is calculated to guarantee the required I_{PK} as follows:

$$L_1 = -\frac{(r_1 + R_{DS(on)})\cdot t_{ON}}{\ln\left(1 - \frac{I_{PK}(r_1 + R_{DS(on)})}{V_{IN}}\right)} \tag{23}$$

To conclude, if all loss terms are taken into account, calculate the required I_{PK} using Equation (19) first, then calculate the inductance L_1 using Equation (23). On the other hand, it is enough to use Equations (17) and (18) when all losses are negligible.

(Design Example) Assuming the expected efficiency is 80%, the required peak current of the main switch is obtained as follows:

$$I_{PK} = \frac{2I_{OUT}\left(1+\frac{n}{\eta}\right)}{1-d} = \frac{2\cdot 25m\cdot\left(1+\frac{4}{0.8}\right)}{1-0.79} = 1.52\,[A]$$

According to the datasheet of the FAN8831, the $R_{DS(on)}$ of the MOSFET is 600 mΩ. Assuming the ESR of the inductor r_1 is 300 mΩ, the inductance is calculated as follows:

$$L_1 = -\frac{(r_1 + R_{DS(on)}) \cdot t_{ON}}{\ln\left(1 - \frac{I_{PK}(r_1 + R_{DS(on)})}{V_{IN}}\right)}$$

$$= -\frac{(0.3+0.6) \cdot \frac{0.79}{350k}}{\ln\left(1 - \frac{1.52 \cdot (0.3+0.6)}{3}\right)} = 3.34\,[\mu H]$$

Let's select 3.3 µH. Therefore, L_2 is obtained as follows:

$$L_2 = n^2 L_1 = 4^2 \cdot 3.3 = 52.8\,[\mu H]$$

[STEP-3] Voltage and Current Stresses on the Main Switch and the Diode

As mentioned in STEP-1, the voltage stress on the main switch equals to V_{LX}. V_{LX} voltage obtained from Equation (11), as can be seen in Figure 12.

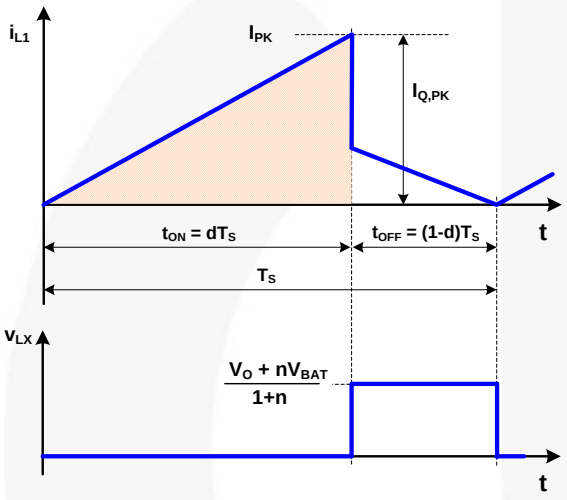


Figure 12. Inductor Current and Main Switch's Drain Voltage

The current stress on the main switch is the rms (root-mean-square) value of the dark area in Figure 12 as follows:

$$L_1 = -\frac{(r_1 + R_{DS(on)}) \cdot t_{ON}}{\ln\left(1 - \frac{I_{PK}(r_1 + R_{DS(on)})}{V_{IN}}\right)} \quad (24)$$

Compared to the conventional boost converter, the voltage stress is reduced approximately by 1+n and the current stress is increased by 1+n, which is a kind of trade-off.

The voltage and current stresses on the diode are obtained simply as follows:

$$V_{D,PK} = V_O + nV_{BAT}$$
$$I_{D,ave} = I_{OUT} \quad (25)$$

(Design Example) The V_{LX} value calculated using Equation (11) as follows:

$$V_{LX} = V_{Q,DS} = \frac{V_O + nV_{IN,\max}}{n+1} = \frac{60 + 4 \cdot 3.3}{4+1} = 14.64\,[V]$$

The current stress of the main switch is as follows:

$$I_{Q,rms} = I_{PK}\sqrt{\frac{d}{3}} = 1.52\sqrt{\frac{0.79}{3}} = 0.78\,[A]$$

The integrated MOSFET in FAN8831 has the absolute voltage rating of 36 V which is enough to cover the voltage stress of 24 V with consideration of the derating of 80%. In addition, $R_{DS(on)}$ of the integrated MOSFET is maximally 500 mΩ, so that the expected conduction loss on it is around 0.4 W which is acceptable.

The voltage stress of the diode is as follows:

$$V_{D,PK} = V_O + nV_{IN} = 60 + 4 \cdot 3.3 = 73.2\,[V]$$

The average current of the diode is as follows:

$$I_{D,ave} = I_{OUT} = 25\,[mA]$$

A diode with more than 100 V of the voltage rating for the output diode should be selected.

[STEP-4] Determine Output Capacitance

The value of the output capacitor can be selected based on the output voltage ripple requirements. Without consideration of the effect of Effective Series Resistance (ESR) of the electrolytic capacitors as output capacitors, the output voltage ripple in a peak-to-peak manner is obtained as follows:

$$V_{ripple,pp} = \frac{\left(2d + \frac{(1-d)^2}{2}\right) \cdot I_{OUT} \cdot T_S}{2C_O} \quad (26)$$

where $V_{ripple,pp}$ is the output voltage ripple in peak-to-peak manner. Therefore, the output capacitance can be selected with the given output voltages ripple specification as follows:

$$C_O \geq \frac{\left(2d + \frac{(1-d)^2}{2}\right) \cdot I_{OUT} \cdot T_S}{2V_{ripple,pp}} \quad (27)$$

On the other hand, it needs to check the required ESR, depending on the output voltage ripple specification, as calculated in Equation (29).

$$ESR \leq \frac{V_{ripple,pp}(1-d)}{2I_{OUT}} \quad (28)$$

After finding an appropriate capacitor with the calculated ESR; compare its capacitance with the result from Equation (27) and select larger one.

(Design Example) If the output voltage ripple is required to be less than 5% of the rated value, i.e. 3 V, then the output capacitance should be greater than:

$$C_O \geq \frac{\left(2d + \frac{(1-d)^2}{2}\right) \cdot I_{OUT} \cdot T_S}{2V_{ripple,pp}}$$

$$= \frac{\left(2 \cdot 0.79 + \frac{(1-0.79)^2}{2}\right) \cdot \frac{25m}{350k}}{2 \times 3} = 18.7\,[nF]$$

Meanwhile, the ESR of the output capacitor should be less than 13.5 Ω:

$$ESR \le \frac{V_{ripple,pp}(1-d)}{2I_{OUT}} = \frac{3\cdot(1-0.79)}{2\times 25m} = 13.5[\Omega]$$

The electrolytic capacitor cases as a rule of thumb, the required capacitance is about 3.6 µF. Therefore, 3.6 µF is selected (at least). To get an optimal capacitance value, refer to the electrolytic capacitor datasheet that provides the allowable rms current.

On the other hand, if a ceramic capacitor is used as the output capacitor due to the limited space, it is no need to take its ESR into account. Select the capacitance to achieve a sufficient output voltage ripple according to Equation (27) only. In this example, 2.2 µF of a ceramic capacitor is selected as the output capacitor.

[STEP-5] ZCD Circuit Design

The Zero Current Detect (ZCD) pin of FAN8831 is to detect the instant when the boost inductor current runs dry for Zero Voltage Switching (ZVS) operation of the main switch. Once the boost inductor current becomes zero, the output capacitor of the main MOSFET (C_{OSS}) and the magnetizing inductor of the coupled inductor (L_1) resonate together, and the drain voltage of the main switch decreases, as shown in Figure 13.

Since the ZCD pin can be connected to the drain pin of the main switch due to its low voltage stress, FAN8831 can notice when the drain voltage reaches its minimum value directly. The threshold voltage to detect the drain voltage inside the ZCD pin is 1.83 V typically. Therefore, the next switching begins after the drain voltage of the main switch reaches 1.83 V. It also has 200 ns maximum delay time to the next gate turn-on, guaranteeing the almost ZVS operation of the main switch.

The internal clamping circuit allows the voltage on ZCD pin to limit between 3.5 V and 0.12 V, typically. To limit the current in the clamping circuit, a resistor should be connected between the drain pin of the main switch and the ZCD pin. The resistor limits the negative current when the ZCD pin is clamped to 3.5 V (V_{CLAMPH}) with the maximum drain voltage. It limits the positive current also when the ZCD pin is clamped to 0.12 V (V_{CLAMPL}) with the minimum drain voltage in resonant manner.

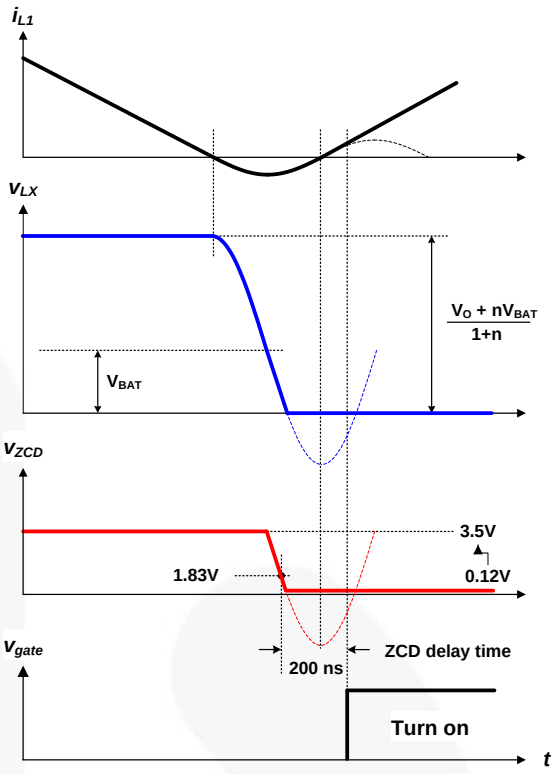


Figure 13. Waveforms for ZVS Detection

The resistor R_{ZCD} is obtained as follows:

$$R_{ZCD} \ge \frac{\left(\frac{V_O + nV_{BAT,\max}}{1+n} - V_{CLAMPH}\right)}{I_{ZCD,SR}} \quad (29)$$

$$R_{ZCD} \ge \frac{\left(\frac{V_O - (2+n)V_{BAT,\max}}{1+n} - V_{CLAMPL}\right)}{I_{ZCD,SK}} \quad (30)$$

where V_{CLAMPH} is the input high clamp voltage, V_{CLAMPL} is the input low clamp voltage, $I_{ZCD,SR}$ is the source current capability, and $I_{ZCD,SK}$ is the sink current capability, described in the datasheet of FAN8831. R_{ZCD} should be selected the larger one from Equations (29) and (30).

(Design Example) The minimum R_{ZCD} is determined as:

$$R_{ZCD} \ge \frac{\left(\frac{60+4\cdot 3.3}{1+4} - 3.5\right)}{2.3m} = 4.84\,[k\Omega]$$

$$R_{ZCD} \ge \frac{\left(\frac{60-(2+4)\cdot 3.3}{1+4} - 0.12\right)}{2.3m} = 3.44\,[k\Omega]$$

Therefore, R_{ZCD} should be selected as 4.7 kΩ at the ZCD received from V_{LX}, not to exceed the current capability of FAN8831.

On the other hand, if ZCD signal received from anode terminal of the switching diode, R_{ZCD} is determined as:

$$R_{ZCD} \ge \frac{(V_{DRV} + 0.7) - V_{CLAMPH}}{I_{ZCD}}$$

[STEP-6] Compensation Network Design

[Current Mode Control]

The duty cycle of the main switch is produced by comparing a control signal reflecting the system output voltage with an internal sawtooth waveform in voltage-mode control, while the inductor current or main switch current is sensed and directly compared to the control signal in current-mode control.

Current-mode control has two feedback loops: the output voltage is compared to a reference voltage and its error signal is applied to the input of a compensator in outer loop. The output of the compensator is compared to the current of the main switch and produces an appropriate duty cycle of the main switch in inner loop. There are usually three types of current-mode control methods: peak, average, and hysteresis current-mode control.

One of the advantages of current-mode control is a good line regulation. The change of the input line voltage is reflected to the slope of the main switch directly so the duty cycle of the main switch is changed directly as well.

Moreover, when operating in CRM or DCM, since there are no sub-harmonic oscillation problem in duty ratio D>0.5 and a simple single-pole transfer function without the right half-plane zero, it is easier to control the converter system.

[Feedback Loop Compensation Design]

The compensation network to stabilize the system could be either Type-I configuration (a simple integrator) or Type-II (an integrator with additional pole-zero pair). The type of the compensation circuit is selected according to the gain and the phase of the transfer function of the power plant at the crossover frequency.

Figure 14 shows the internal block diagram and the vicinity of the FAN8831 with Type-II compensator for regulating the output voltage of a coupled-inductor boost converter.

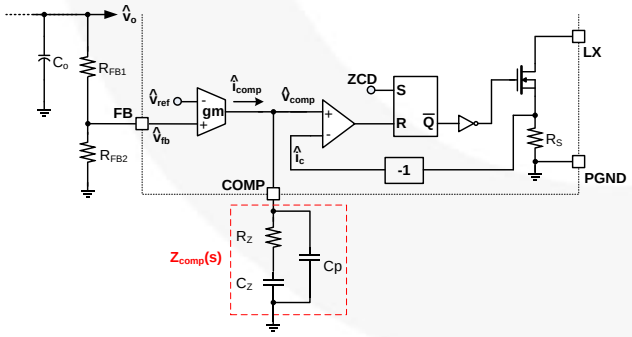


Figure 14. Internal Block Diagram and Compensation Gain for Regulating the Output Voltage for FAN8820

Equations (31) ~ (33) are obtained from Figure 14.

$$\hat{v}_{comp}(s) = -\hat{i}_c(s) \times R_S \tag{31}$$

$$\hat{v}_{comp}(s) = \hat{i}_{comp}(s) \times Z_{comp}(s) \tag{32}$$

$$\hat{i}_{comp}(s) = \hat{v}_{fb}(s) \times g_m = (\hat{v}_o(s) \times \frac{R_{FB2}}{R_{FB1} + R_{FB2}}) \times g_m \tag{33}$$

Combining the above equations gives the following:

$$\frac{\hat{i}_c(s)}{\hat{v}_o(s)} = -\frac{1}{R_S} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot g_m \cdot Z_{comp}(s) \tag{34}$$

where:

$$Z_{comp}(s) \cong \frac{1}{sC_Z} \cdot \frac{1 + sR_ZC_Z}{1 + sR_ZC_P},$$

$$R_S = \frac{Internal\ \ sensing\ \ resistor}{Sense\ \ Ratio} = \frac{V_{RAMP\_PP}}{I_{OCP}} \cong \frac{1.7\,[V]}{1.52\,[A]} \cong 1.12\,[\Omega], \tag{35}$$

and $C_Z >> C_P$.

FAN8831 uses internal SenseFET so that the sensing resistor R_S is calculated as Equation (35). When an external MOSFET and a sensing resistor are used, the value of the sensing resistor should be applied.

When the coupled-inductor boost converter is operating in CRM, the simplified small-signal model is obtained by letting the input inductor zero, as depicted in Figure 15.

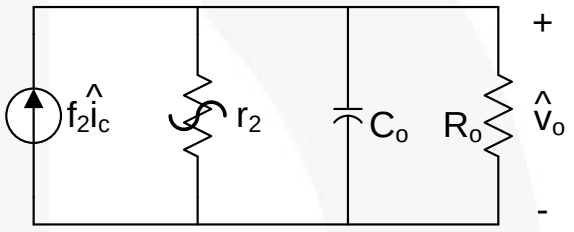


Figure 15. Small-Signal Model for CRM Coupled-Inductor Boost Converter

The control-to-output transfer function $G_{vc}(s)$, ignoring the effective-series-resistor ESR of the output capacitor, is:

$$G_{vc}(s) = \left.\frac{\hat{v}_o(s)}{\hat{i}_c(s)}\right|_{\hat{v}_{in}(s)=0} = f_2 \cdot \left(r_2 \,//\, R_O \,//\, \frac{1}{sC_O}\right) = \frac{G_{vc0}}{1 + \frac{s}{\omega_p}} \tag{36}$$

where:

$$f_2 = \frac{1}{2}\frac{1}{G+n}, \quad r_2 = R_O\left(\frac{G+n}{G}\right),$$

$$G_{vc0} = \frac{R_O}{2}\left(\frac{1}{2G+n}\right), \quad \omega_p = \frac{1}{R_OC_O}\left(\frac{2G+n}{G+n}\right), \tag{37}$$

$$G = \frac{V_O}{V_{IN}}, \quad n = \frac{N_2}{N_1}, \quad and \quad R_O = \frac{V_O}{I_{OUT}}.$$

The procedure to design the feedback loop is as follows:

(1) Obtain the control-to-output transfer function of the power stage using Equation (36). It is one-pole system whose pole frequency is ω_p with the DC gain of G_{vc0}.

(2) Determine the crossover frequency (f_c) around more than 10 times the pole frequency. Since the closed loop gain has -40 dB/dec slope and -180° of phase shift at the crossover frequency, as shown in Figure 16, it is required to place a zero of the compensation network (f_{cz}) around the crossover frequency in order

to maximize the bandwidth of the closed loop gain function so that 45° of phase margin is obtained.

(3) Place a pole of the compensation network (f_{cp}) at least a decade higher than f_c to ensure that it does not affect the phase margin of the compensated system. It should also be sufficiently lower than the switching frequency of the system so the switching noise can be attenuated.

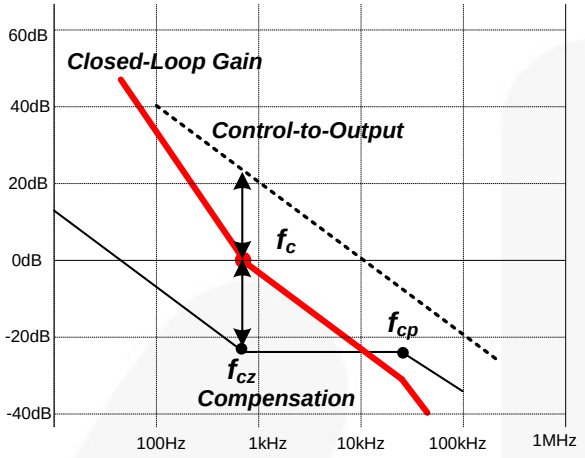


Figure 16. Compensation Network Design

The voltage divider network of R_{FB1} and R_{FB2} should be designed for the output voltage to meet the internal reference voltage V_{REF} (=1 V) as follows:

$$V_O = V_{REF}\left(1+\frac{R_{FB1}}{R_{FB2}}\right) \quad (38)$$

(Design Example) Find the control-to-output transfer function of the power stage. The parameters in the previous examples are summarized in the table below.

Parameters	Value
V_{IN}	3 V
V_O	60 V
I_{OUT}	25 mA
C_O	0.33 µF
N	4
R_S	1.12 Ω
g_m	800 µmho
f_S	350 kHz

If R_{FB1} is 560 kΩ, then R_{FB2} is:

$$R_{FB2} = \frac{V_{REF}\times R_{F1}}{(V_O - V_{REF})} = \frac{1\times 560\times 10^3}{(60-1)} = 9.5\,[k\Omega]$$

G, R_O, f_2, and r_2 are calculated as follows:

$$G = \frac{V_O}{V_{IN}} = \frac{60}{3} \cong 20,$$

$$R_O = \frac{V_O}{I_{OUT}} = \frac{60}{0.025} = 2.4\,[k\Omega],$$

$$f_2 = \frac{1}{2}\left(\frac{1}{G+n}\right) = \frac{1}{2}\left(\frac{1}{20+4}\right) \cong 0.0208,$$

$$r_2 = R_O\left(\frac{G+n}{G}\right) = 2400\left(\frac{20+4}{20}\right) \cong 2.88\,[k\Omega].$$

The DC gain G_{vc0} and frequency of the pole are calculated as follows:

$$G_{vc0} = \frac{R_O}{2}\left(\frac{1}{2G+n}\right) = \frac{2400}{2}\left(\frac{1}{2\times 20+4}\right) \cong 27.3 = 28.71\,[dB],$$

$$f_p = \frac{1}{2\pi R_O C_O}\left(\frac{2G+n}{G+n}\right) = \frac{1}{2\pi\cdot 2.4k\cdot 0.33\mu}\left(\frac{2\times 20+4}{20+4}\right) \cong 55.3\,[Hz]$$

Next, design the compensation network. Place the crossover frequency of the compensated system at 800 Hz, about more than 10 times the pole frequency of the coupled-inductor boost converter. The gain of the uncompensated power stage at 800 Hz is calculated as follows:

$$G_{vc@800Hz} = 28.71 - 20\times(\log(800) - \log(55.3)) = 5.5\,[dB]$$

Since the DC gain of the compensator should be -5.5 dB at 800 Hz, R_Z can be obtained as follows:

$$R_Z = \frac{R_S}{g_m}\cdot\frac{R_{FB1}+R_{FB2}}{R_{FB2}}\cdot 10^{\left(\frac{-5.5}{20}\right)} = \frac{1.12}{800\mu}\cdot\frac{569.5k}{9.5k}\cdot 10^{\left(\frac{-5.5}{20}\right)} \cong 44.5\,[k\Omega].$$

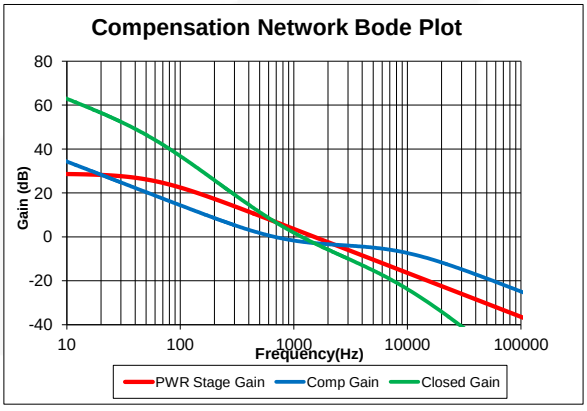
If choose the R_Z is 47 KΩ. C_Z is obtained as follows:

$$C_Z = \frac{1}{2\pi R_Z\times f_{cz}} = \frac{1}{2\pi\times 47k\times 800} \cong 4.2\,[nF]$$

Let the frequency of the pole of the compensator placed at 8 kHz be a decade higher than the zero. C_P is obtained as follows:

$$C_P = \frac{1}{2\pi R_Z\times f_{cp}} = \frac{1}{2\pi\times 47k\times 8k} \cong 423\,[pF]$$

The below shows the result of the compensation network design.



[STEP-7] Input Signal Frequency Setting

The FAN8831 is needed the INPUT pulse signal for the sinusoidal waveform drive of the Piezoelectric actuator as shown in Figure 17. The outputs are stops immediately when the input signal is not applied. Its valid input signal frequency range is from 20 Hz to 1000 Hz.

The frequency of sine wave can be determined using Equation (39) as follows:

$$f_{PIEZO} = \frac{f_{INPUT}}{2} \quad (39)$$

A test point connected to INPUT of the SIGNAL connector is located next to TP11. The internal sine reference signal is generate by 6-bit DACs were used which were frequency controlled by external pulse input signal (INPUT).

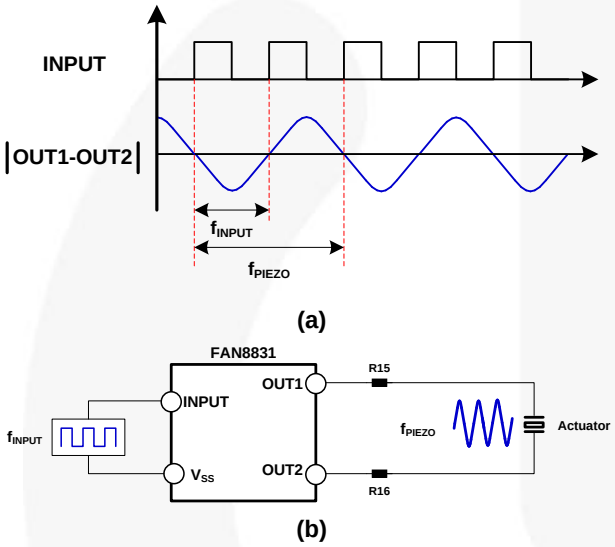


Figure 17. (a) Timing Chart, (b) Schematic of using External PWM Input

(Design Example) Assumed frequency of Piezoelectric driving voltage is 100 Hz when used the external pulse input, the required frequency of the input signal is obtained as follows:

$$f_{INPUT} = 2 \times f_{PIEZO} = 2 \times 100 = 200[Hz]$$

If when using the timer IC like as LM555, The frequency of oscillation can be determined using equation as follows:

$$f_{INPUT} = \frac{1}{(1.4 \times R17 \times C12)}$$

If choose the timing capacitor C12 is 100 nF, the timing resistor R17 is obtained as follows;

$$R17 = \frac{1}{(1.4 \times 200 \times 100nF)} \cong 35.7[kHz]$$

Where R17= R20 + R21

[STEP-8] Programmable OCP Trip Level Setting

The peak current level (I_{OVP}) of boost switch is programmed via external resistor (R8) and the maximum value is limited typically 1.8 A. The programmed current limit should be less than the rated saturation limit of the inductor selected by the user to avoid damage to both the inductor and the FAN8831. The peak current limit level is according to the R_{OCP} (R8) values as show the Figure 18.

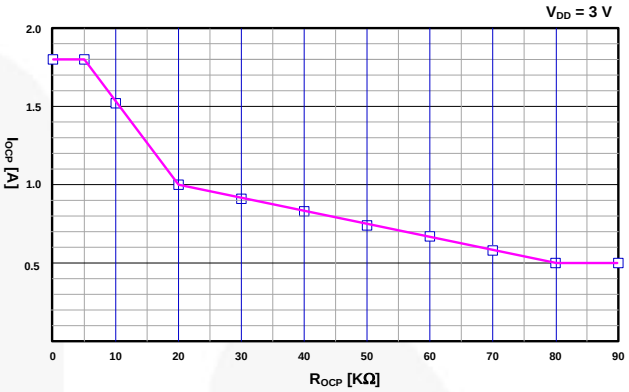


Figure 18. Characteristic Graph of I_{OCP} vs. R_{OCP}

[STEP-9] Over-Voltage Protection Setting

The FAN8831 features unique V_{DRV} monitoring to maximize safety when the feedback voltage is higher than the specified threshold voltages as shown in Figure 18. The OVP comparator shuts down the output drive block when the voltage of FB pin is higher than 1.1 V and there is 0.1 V for hysteresis. If output voltage exceeds its rated output, the output capacitor (C3 and C4) may be damaged. To prevent this, an additional OVP pin is assigned to double-check output voltage when FB pin is shorted ground or open conditions. The additional OVP is called "second" OVP, while FB pin OVP is called "first" OVP. The second OVP level (V_{OVP}) is programmed via three external resistors as shown in Figure 19. If the second OVP function is not used, the OVP pin must be connected to the FB pin or to the ground.

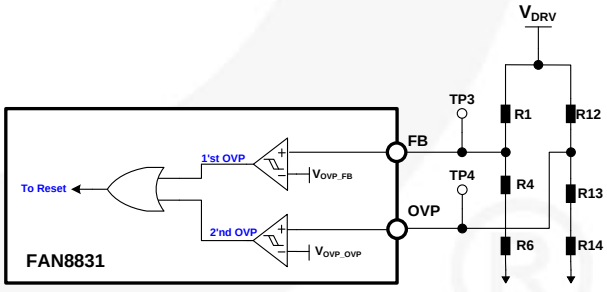


Figure 19. Boost Converter Over Voltage Setting

The boost output voltage can be determined using Equation (41) as follows:

$$V_{OVP} = V_{OVP\_OVP}\left(1 + \frac{R12}{R13 + R14}\right) \quad (40)$$

where V_{OVP_OVP}=1.15 V.

(Design Example) Choose the over-voltage trip level is 70 V. If R12 is 560 kΩ, then R13+R14 is:

$$R13 + R14 = \frac{V_{OVP\_OVP} \times R12}{(V_{OVP} - V_{OVP\_OVP})} = \frac{1.15 \times 560 \times 10^3}{(70 - 1.15)} = 9.35[k\Omega]$$

[STEP-10] PWM Switching Frequency Setting

The frequency of sine PWM modulator can be controlled by RT (R11) values and the switching frequency is according to the RT (R11) values as show the Figure 20.

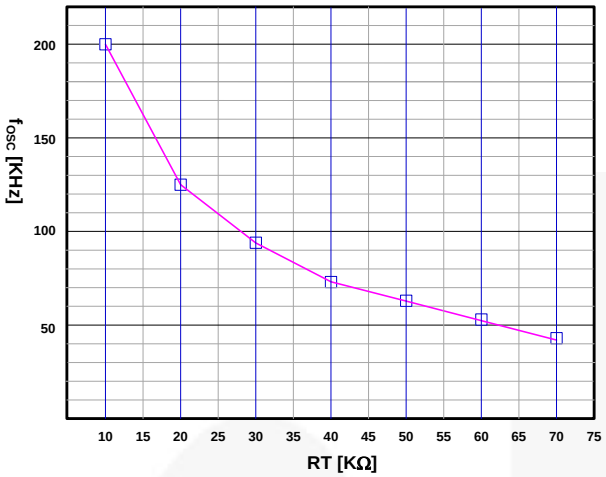


Figure 20. Characteristic Graph of PWM Frequency vs. RT Values

[STEP-11] Sine Wave Amplitude Setting

The amplitude of sine wave can be controlled by R_{ADJ} (R9) values and the sine wave amplitude is according to the R_{ADJ} (R9) values as show the Figure 21.

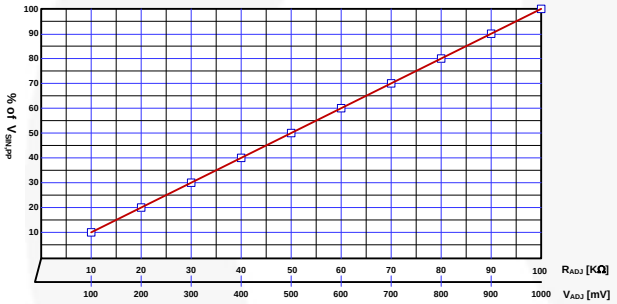


Figure 21. Characteristic Graph of Sine Amplitude vs. R_{ADJ} and V_{ADJ}

Experimental Verification

To show the validity of the design procedure presented in this application note, a prototype of the design example was implemented and tested. All the circuit components are used as designed in the design example.

Startup Characteristics

Measure the startup time interval between Enable and stable output at output peak to peak voltage 60 V with capacitive load as shown in Figure 22. Sine wave comes from 3rd rising edge of input pulse signal after when step-up DC-DC converter output voltage reaches the specified target level.

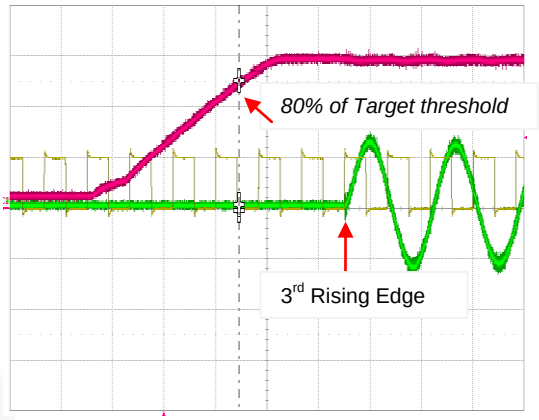
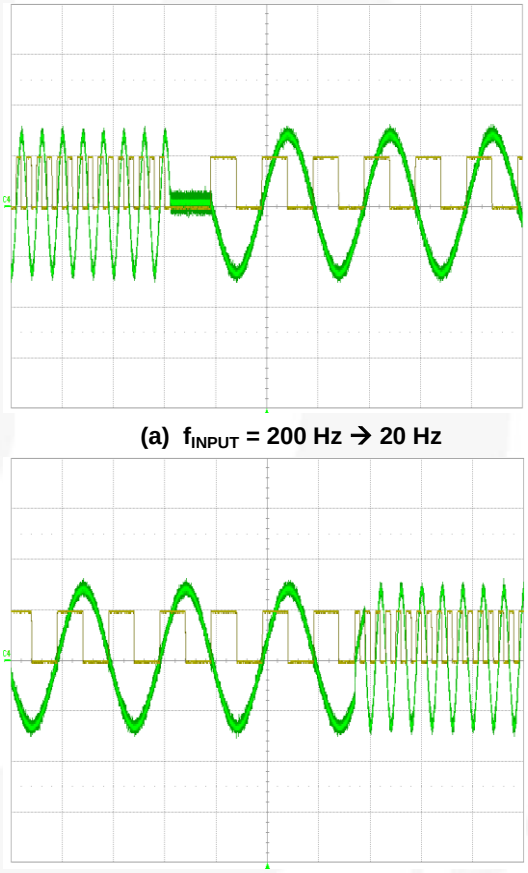


Figure 22. Operation Waveforms during Startup Green(V_{PIEZO}), Red (V_{DRV}), Yellow (INPUT), Blue (ENABLE)

INPUT Signal Characteristics

Measure the operating waveforms when frequency change of input pulse as shown in Figure 23.



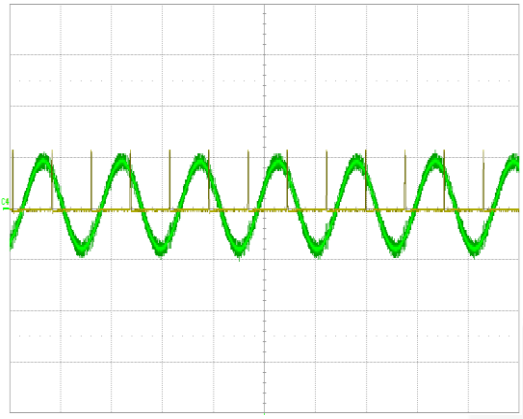
(a) f_{INPUT} = 200 Hz → 20 Hz

(b) f_{INPUT} = 20 Hz → 200 Hz

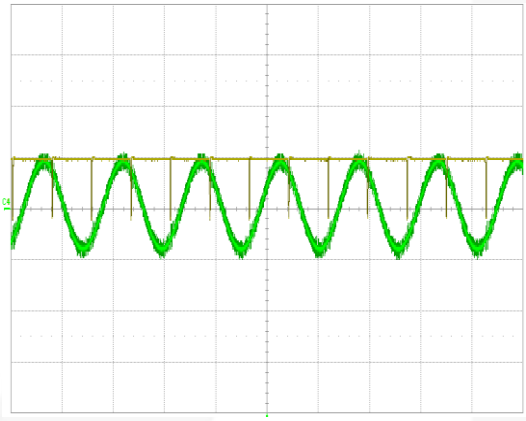
Figure 23. Operation Waveforms when the INPUT Signal Frequency Change

The FAN8831 feature have frequency of output voltage does not change even if change the duty cycle of the input signal as shown in Figure 24.

Measure the operating waveforms when duty cycle changes of the input signal as shown in Figure 24.



(a) f_{INPUT} = 1.3 kHz with 2% Duty Cycle



(b) f_{INPUT} = 1.3 kHz with 98% Duty Xycle

Figure 24. Operation Waveforms when the INPUT Signal Frequency Change

Consideration of Output Filter

The class-D amplifier outputs are driven by heavy-duty in an H-bridge configuration. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the internal sine reference signal. The output may be directly applied to the piezoelectric load. So, EMI is a consideration when used the class-D amplifier because of the piezoelectric is capacitive load. The main goal of the output filter is attenuation of the high frequency switching noise of the class-D amplifier while preserving the signals in the sine wave driving as shown in Figure 25.

The switching frequency (f_S) of the class-D amplifier can influence the choice of the filter order — the higher the f_S, the lower the order required to achieve a given attenuation within a specified pass band. This would seem to dictate the use of the highest switching frequency possible. The tradeoff is that increasing f_S increases the switching losses and the EMI, and decreases the efficiency of the amplifier.

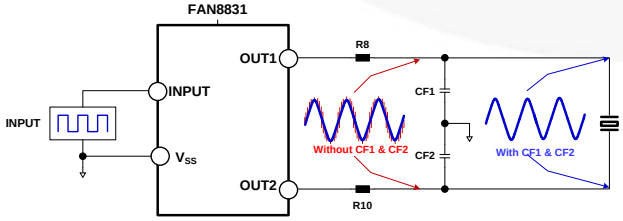


Figure 25. Schematic of Output Filter

The Piezo driving frequency is limited by the RC low-pass filter configuration of the load as follows:

$$f_{PIEZO,MAX} = \frac{1}{2 \times \pi \times R \times C_{PIEZO}} \quad (41)$$

where, R is R8+R10

C_{PIEZO} is equivalent capacitance of Piezoelectric.

$f_{PIEZO,MAX}$ = 500 Hz in FAN8831

Peak output current from the Class-D Amplifier should therefore be limited to the maximum Piezo driving frequency:

$$I_{PEAK,DRIVER} = \frac{V_{DRVPEAK}}{\sqrt{R^2 + XC^2}} \quad (42)$$

where, XC is:

$$XC = \frac{1}{2 \times \pi \times f_{PIEZO} \times C_{PIEZO}} \quad (43)$$

The output filter capacitors and resistors form a low-pass filter with the corner frequency, $f_{C,\ FILTER}$, determined in equation (44).

$$f_{C,FILTER} = \frac{1}{2 \times \pi \times R_F \times C_F} \quad (44)$$

$$C_F = \frac{1}{2 \times \pi \times R_F \times f_{C,FILTER}} \quad (45)$$

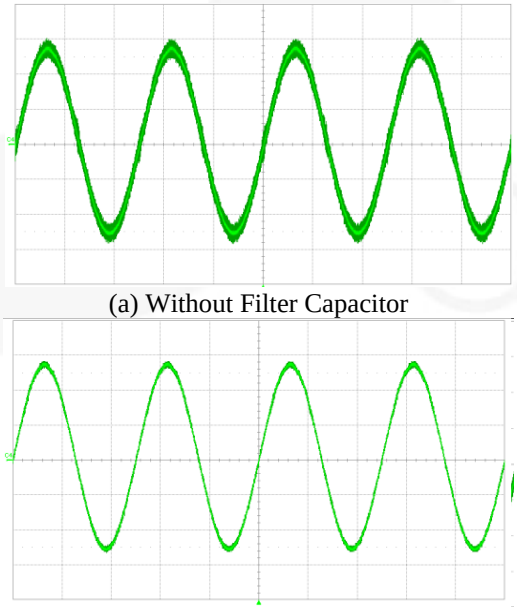
where, R_F =R15=R16

The filter capacitors should be ceramic capacitors with X7R characteristics for stability over voltage and temperature.

The corner frequency of output filter, $f_{C,FILTER}$, should be choose between larger than at least 10 times of sine wave frequency and less than 1/10 of PWM switching frequency in equation (46).

$$(10 \times f_{SINE}) \le f_{C,FILTER} \le \frac{f_S}{10} \quad (46)$$

Measure the voltage waveforms of piezoelectric actuator when not using an output filter capacitor (CF1 and CF2) or using an output filter capacitor to reduce the switching noise as shown in Figure 26.



(a) Without Filter Capacitor

(b) With Filter Capacitor (CF1=6.8 nF)

Figure 26. Waveforms of Piezoelectric Driving Voltage

Application Circuit Diagram and BOM List

Typical Application Circuit

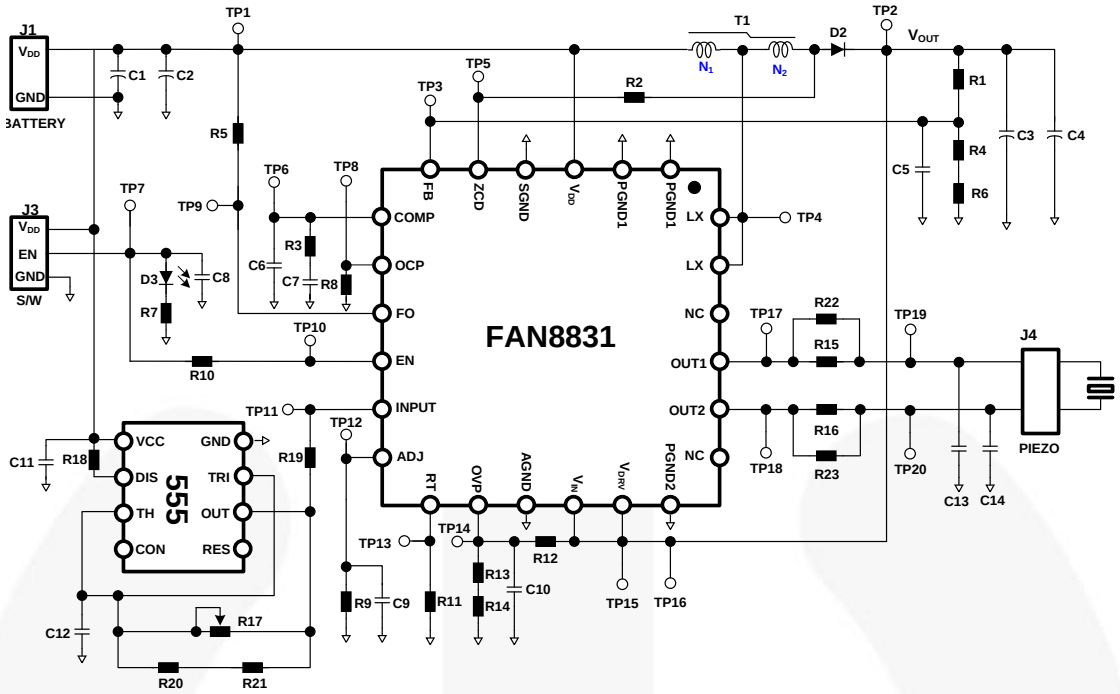


Figure 27. Typical Application Circuit for Piezoelectric Driving

List of Test Point

Table 1 shows the list of test point on evaluation board.

Table 1. List of Test Point of Evaluation Board

TP	Reference	Description
TP1	V_{DD}	Power supply of step-up DC-DC converter.
TP2	V_{DRV}	Power supply of full-bridge driver, (TP15, TP16)
TP3	FB	Step-up DC-DC converter output voltage feedback input.
TP4	LX	Switch node. This pin is connected to the inductor.
TP5	ZCD	The input of the zero current detection
TP6	COMP	Compensation network. Connected to the output of the voltage error amplifier.
TP7	EN	Enable pin to turn on and off the step-up DC-DC converter, (TP10)
TP8	OCP	Sets Step-up DC-DC converter current limit
TP9	FO	Fault output. An open drain fault-out (FO) signal indicates if an over-voltage of dc-dc converter or thermal-shutdown has occurred
TP11	INPUT	PWM input signal for internal sine wave generation
TP12	ADJ	Output voltage adjust control pin. Connect to internal current source to change output voltage using an external resistor.
TP13	RT	Oscillator frequency control pin
TP14	OVP	Voltage sense input of Step-up DC-DC converter for Over-Voltage Protection
TP17	OUT1	Output 1 for full-bridge driver
TP18	OUT2	Output 2 for full-bridge driver

Bill of Materials

Item No.	Part Reference	Part Number	Qty.	Description	Manufacturer
1	U1	FAN8831	1	Controller	Fairchild
2	U2	LMC555	1	Timer IC	
3	D2	ES1B	1	1 A/100 V Diode	Fairchild
4	D3	HSML-C197	1	LED	DIALIGHT
5	T1	NA-5880AE	1	3.3 µH Coupled-Inductor	Coil Craft
6	R1, R12	MCR01YRTF5603	2	560 kΩ /±1% Chip Resistor	Rohm or Equivalent
7	R2	MCR01YRTF2002	1	20 kΩ /±1% Chip Resistor	Rohm or Equivalent
8	R3	MCR01YRTF4702	1	47 kΩ /±1% Chip Resistor	Rohm or Equivalent
9	R4	MCR01YRTF8201	1	8.2 kΩ /±1% Chip Resistor	Rohm or Equivalent
10	R5	MCR01YRTF5102	1	51 kΩ /±1% Chip Resistor	Rohm or Equivalent
11	R6	MCR01YRTF3001	1	3 kΩ /±1% Chip Resistor	Rohm or Equivalent
12	R7	MCR01YRTF4300	1	430 Ω /±1% Chip Resistor	Rohm or Equivalent
13	R8	MCR01YRTF1202	1	12 kΩ /±1% Chip Resistor	Rohm or Equivalent
14	R9, R11, R18	MCR01YRTF1003	3	100 kΩ /±1% Chip Resistor	Rohm or Equivalent
15	R10, R14, R19	MCR01YRTF000	3	0 Ω /±1% Chip Resistor	Rohm or Equivalent
16	R15, R16	MCR18YRTF5101	2	5.1 kΩ /±1% Chip Resistor	Rohm or Equivalent
17	R13	MCR01YRTF8201	1	9.31 kΩ /±1% Chip Resistor	Rohm or Equivalent
18	R17	3296X-1-104	1	Variable Resistor	Boarns
19	R20, R21, R22, R23	OPEN	4	OPEN	OPEN
20	C1	C2012X5R0J226K125AB	1	6.3 V/22 µF Chip Capacitor	TDK or Equivalent
21	C3	C3225JB2A225K230AB	1	100 V/2.2 µF Chip Capacitor	TDK or Equivalent
22	C5	CGJ4C2C0G1H151J060AA	1	50 V/150 pF Chip Capacitor	TDK or Equivalent
23	C6	CGJ4C2C0G1H181J060AA	1	50 V/390 pF Chip Capacitor	TDK or Equivalent
24	C7	C2012C0G1H222J060AA	1	50 V/3.9 nF Chip Capacitor	TDK or Equivalent
25	C8	C2012C0G1H222J060AA	1	50 V/2.2 nF Chip Capacitor	TDK or Equivalent
26	C9	C2012C0G1H102J060AA	1	50 V/1 nF Chip Capacitor	TDK or Equivalent
27	C10	CGJ4C2C0G1H101J060AA	1	50 V/100 pF Chip Capacitor	TDK or Equivalent
28	C11	C2012JB1C105K085AA	1	16 V/1 µF Chip Capacitor	TDK or Equivalent
29	C12	CGJ4J2X7R1C104K125AA	1	16 V/100 nF Chip Capacitor	TDK or Equivalent
30	C2, C4, C13, C14	OPEN	4	OPEN	OPEN
31	J1, J4	5268-02	2	Connector	Molex
32	J3	SS1290	1	Switch	Samyoung High Tech

Coupled-Inductor and Winding Specifications

- Turn ratio = Np: Ns = 1: 4

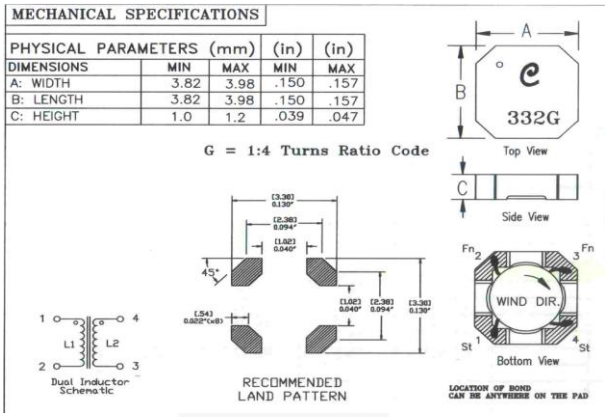


Figure 28. Coupled-Inductor Specifications and Construction

Table 2. Winding Specifications

No.	Winding	Pin (S → F)	Values [µH]		DCRMAX [Ω]
			Min.	Max.	
1	Np	1 → 2	2.64	3.96	0.306
2	Ns	4 → 3	38.8	59.2	2.30
3	Turn-Ratio	Np: Ns	1: 4		
4	Leakage Inductance		Values [nH]		Condition
			Typ.	Max.	
		1 → 2	270	356	Short Pins 4 - 3
	Measured by 100 KHz, 0.1 V_{RMS} 0 Adc				
	Recommended Inductor: CoilCraft NA5880-AE				

References

[1] Physik Instrumente (PI). Web page http://www.physikinstrumente.com.

[2] T.L. Jordan and Z. Ounaies, “Piezoelectric Ceramics Characterization” NASA/CR-2001-211225 and ICASE Report No. 2001-28.

[3] R.W.Erickson and D.Maksimovic, “Fundamentals of Power Electronics (2nd edition)”

[4] Rong-Jong Wai and Rou-Youg Duan, “High Step-Up Converter with Coupled-Inductor”, IEEE Trans. on Power Electronics, 2005, Vol.20 (5), pp. 1025-1035.

[5] P.D. Evans, W.M. Chew, “Reduction of proximity losses in coupled inductors”, *IEE Proceedings-B*, 1991, Vol. 138(2), pp 51-58.

[6] Suman Dwari, Saurabh Jayawant, Troy Beechner, Stephanie K. Miller,Anu Mathew, Min Chen, Jonathan Riehl, and Jian Sun, “DynamicCharacterization of Coupled-Inductor Boost DC-DC Converters”, IEEE Proceedings on COMPEL, 2006, pp 264-269.

[7] N. Vazquez, L. Estrada, C. Hernadez, E. Rodriguz, “The Tapped-Inductor Boost Converter”

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FAN8831 Product Folder

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