Part 5 – BASIC DIFFERENTIAL SIGNALLING

References

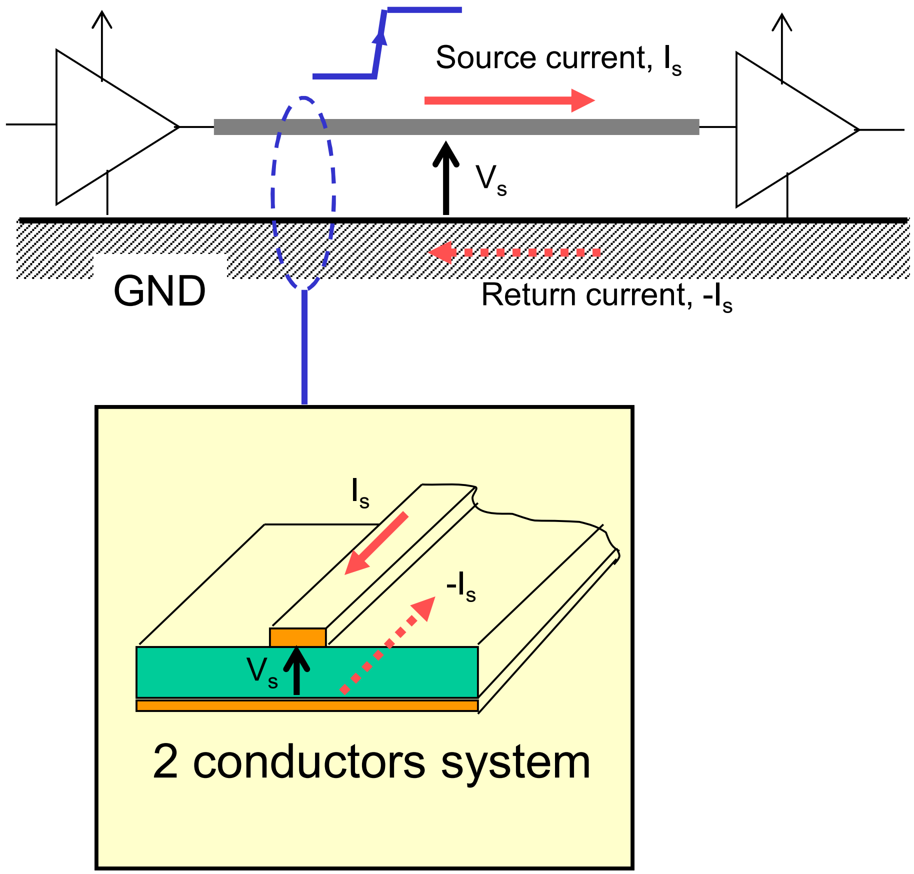
- [1] H. Johnson, M. Graham, "High-speed signal propagation - Advanced black magic", Prentice-Hall, 2002.
- [2] C.R. Paul, "Introduction to electromagnetic compatibility", Wiley Interscience, 1992.
- [3] T. C. Edwards, "Foundations of interconnect and microstrip design", 3rd edition, 2000, John-Wiley & Sons.
- [4] D.M. Pozar, "Microwave engineering", 2nd edition, 1998 John-Wiley & Sons.
- [5] Application notes from National Semiconductor (on LVDS specifications). National Semiconductor also has a good archive of online seminars on this topic.
- [6] T. Grandberg, "Handbook of digital techniques for high-speed design", Prentice-Hall, 2004.

5.1 – Single-Ended Versus Differential Signaling Configurations

Introduction

- Thus far all our discussion on electrical signaling use one signal trace, which we call single-ended signaling.
- When transmitting high-speed electrical signal, the EM fields for the signal trace and the return current on the ground plane have the potential to cause electrical interference on adjacent circuits.
- Furthermore with digital system going for lower operating voltage, logic signal swing and noise margin also decrease, this undermines the noise immunity of the digital system.
- This prompts the introduction of differential signaling, which uses two signal traces in close coupling to transmit electric signals.
- Differential signaling promises better immunity for the same operating voltage level, much lower return current on ground plane, lower EM fields emission.

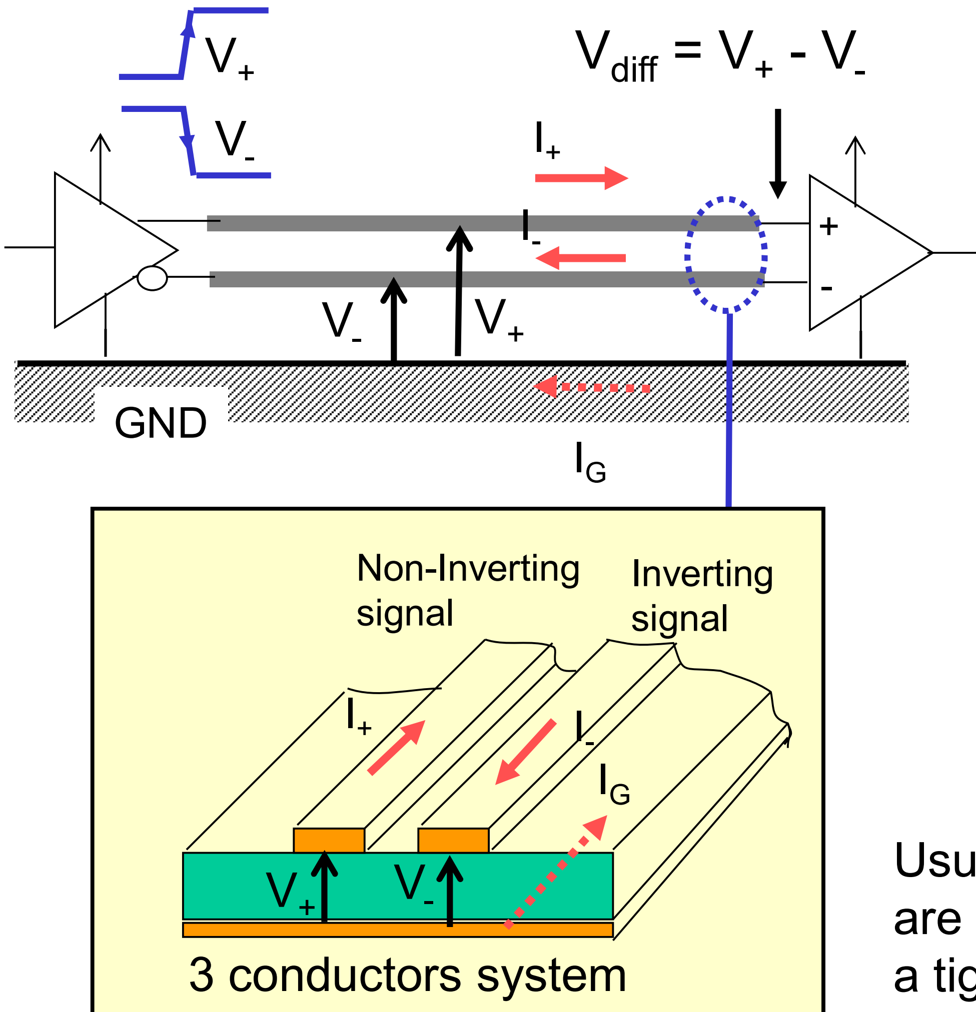
Single-Ended Signaling



A single-ended signaling system:

- 2 conductors.
- 1 driver.
- 1 receiver.
- Source current = Return current.
- Signal is the voltage between signal conductor and GND.

Differential Signaling (1)



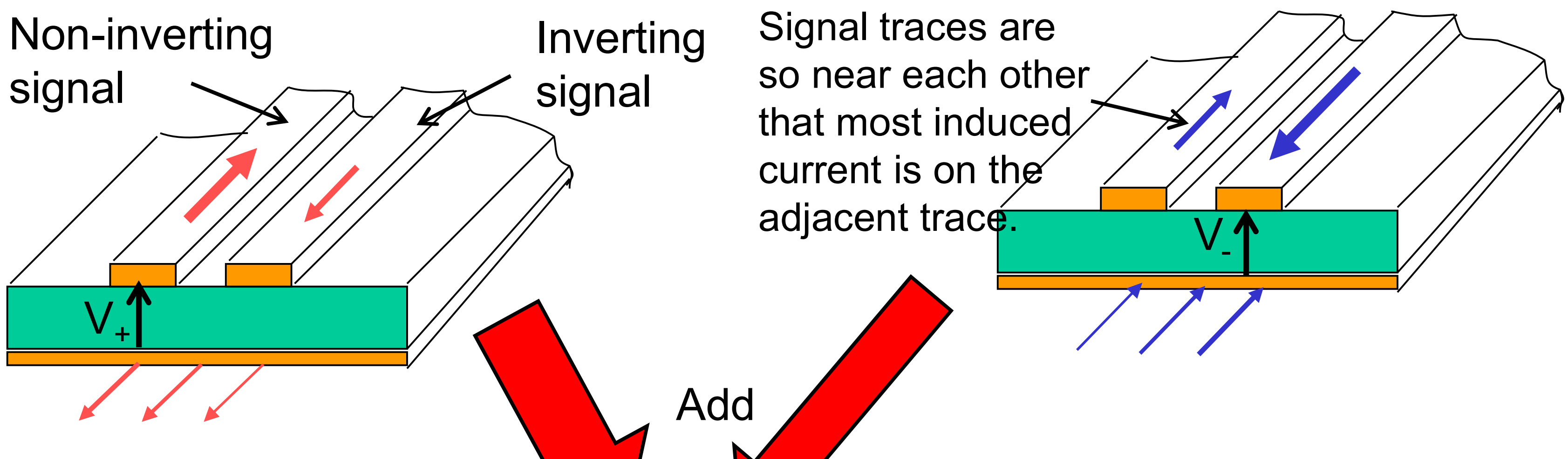
A differential-signaling system:

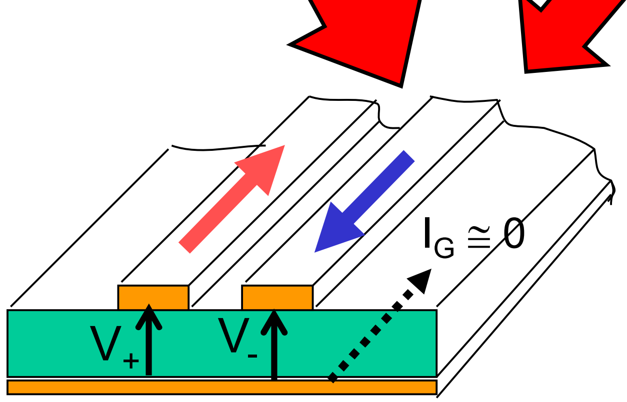
- 3 conductors system.
- 2 drivers – inverting and non-inverting.
- 1 differential receiver.
- $V_+ = -V_-$
- Usually $|I_+| = |I_-|$ by design (we call this **balanced signal**).
- $I_G = I_+ + I_- \cong 0$ by design.
- Signal is the voltage difference between V_+ and V_-.

Usually the signal conductors are close together, forming a tightly coupled system, resulting in $I_G \cong 0$ (balanced condition).

Differential Signaling (2)

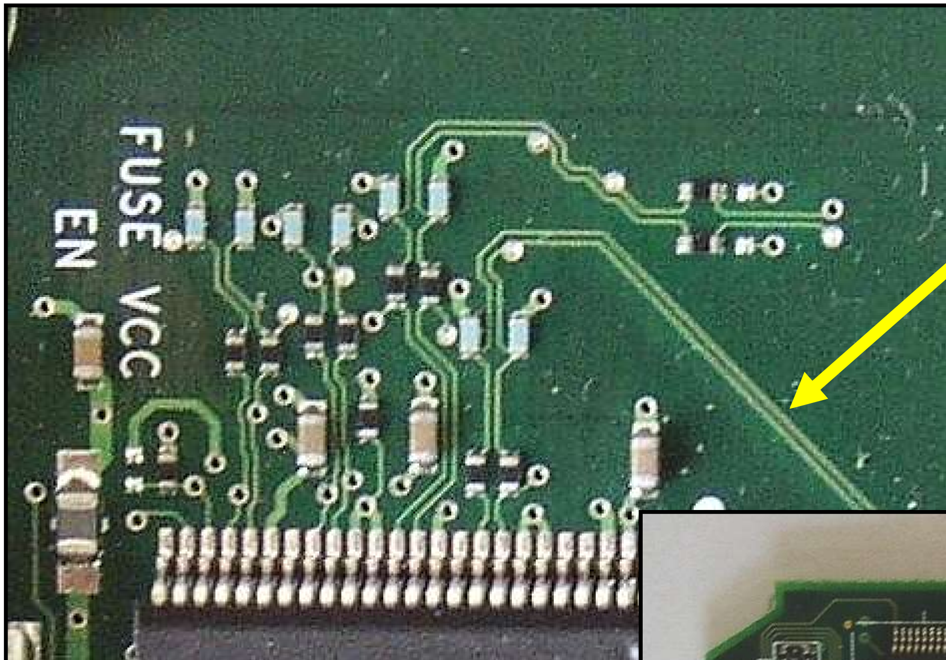
- Why very small ground current in ideal differential signaling.





- When we add both inverting and non-inverting signaling together, the total GND plane current is small compare to the currents on the signal traces.
- Effectively the inverting and non-inverting signal conductors act as a pair.

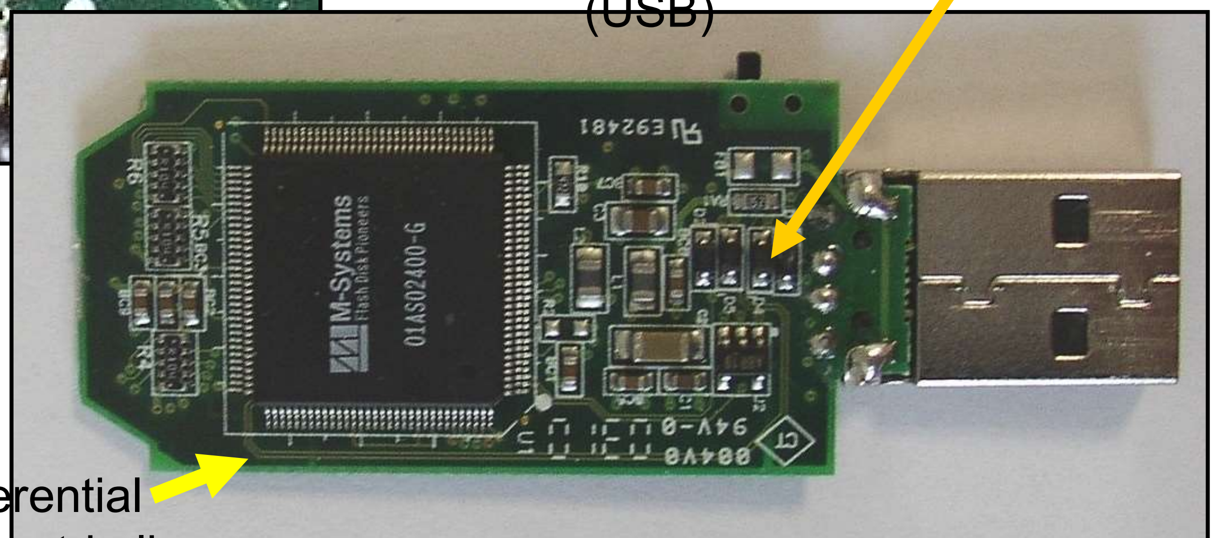
Example 1.1 – Differential Signaling Example



Differential microstrip lines, ground plane on the underside.

Portion of DDR2 DRAM module

Overvoltage protection diodes for V_D^+ and V_D^- lines (USB)

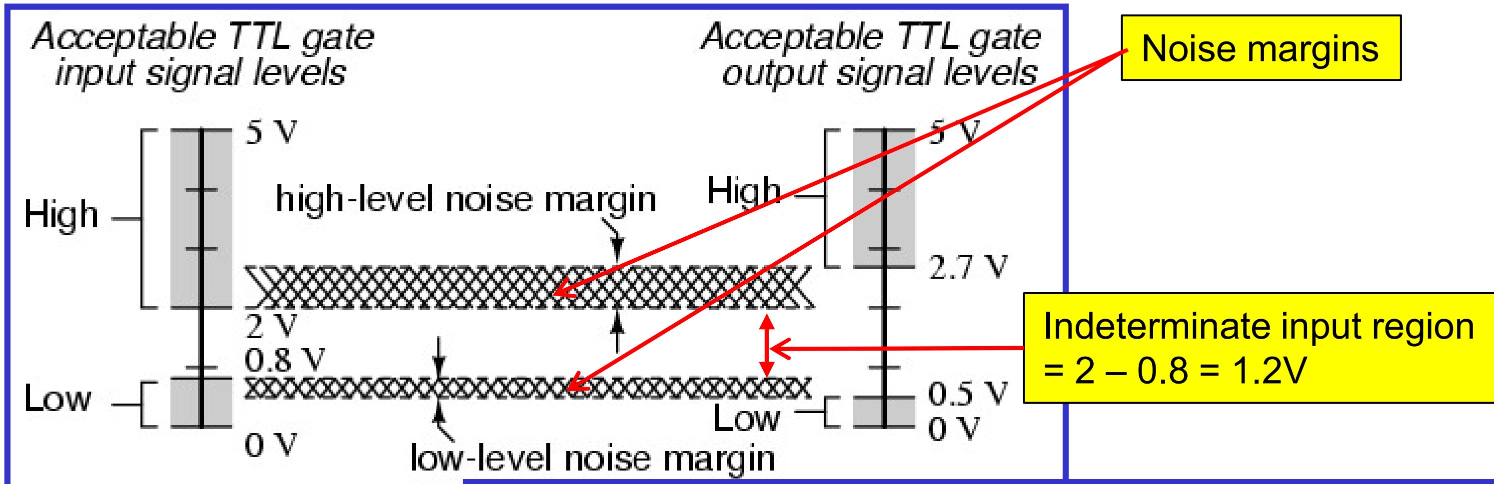


Differential microstrip lines

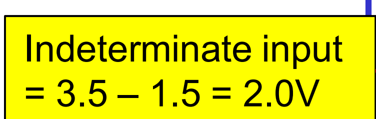
5.2 – Motivation for Differential Signaling (DS)

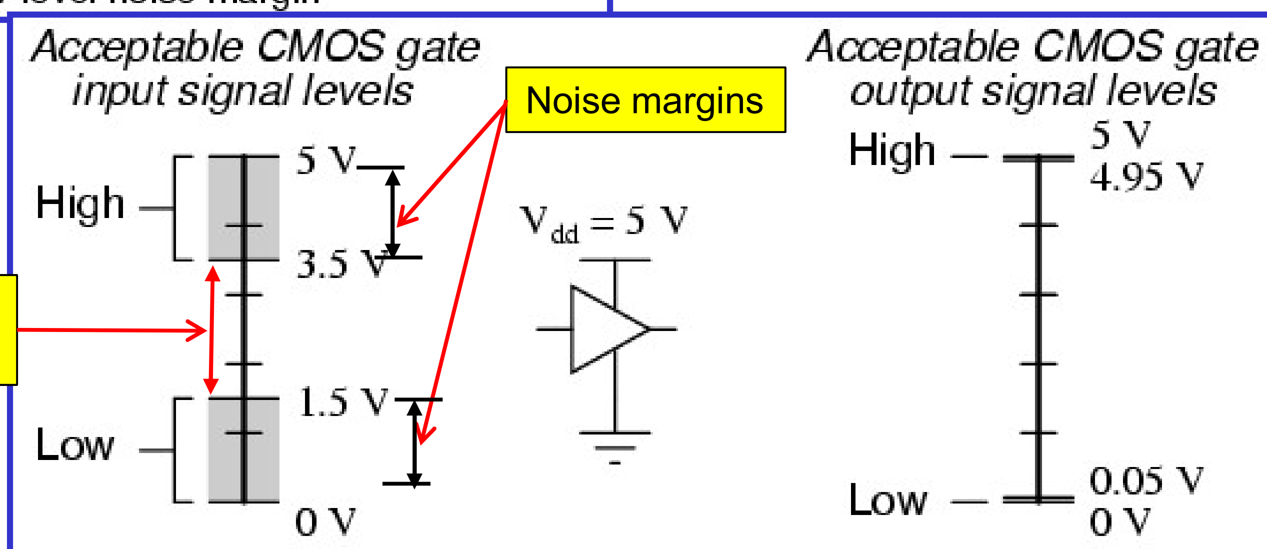
Noise Margin in Digital Level – TTL and CMOS

- Typical noise margin (NM) for 5V TTL and CMOS logic:



- CMOS at 5.0V supply:



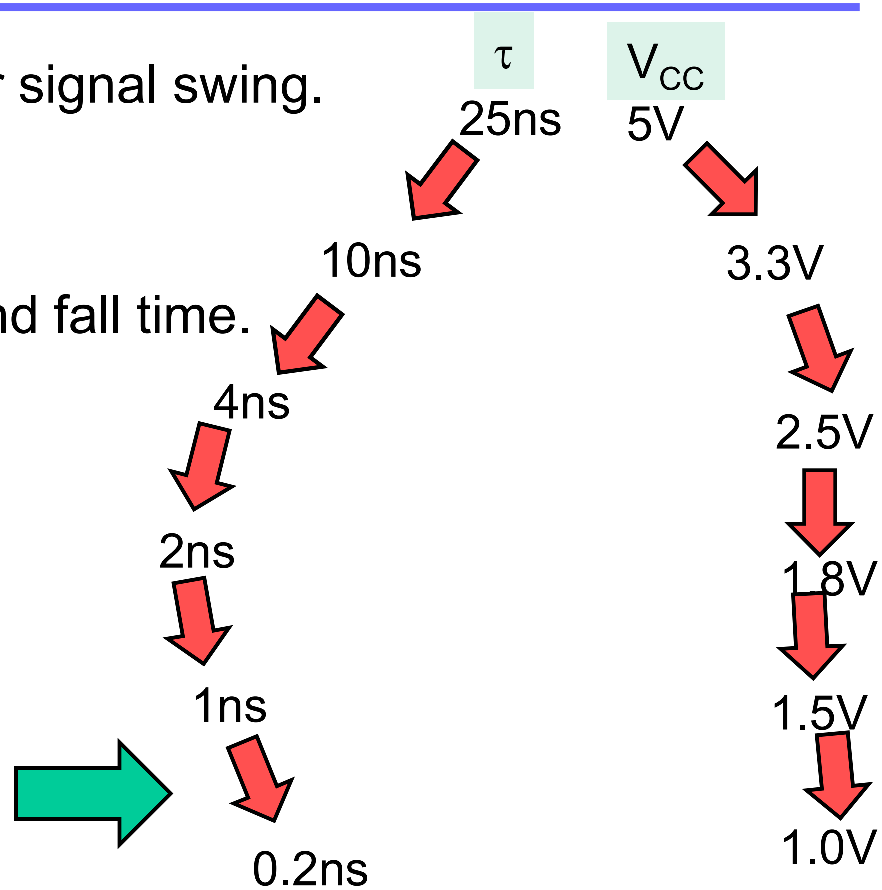


Trend in Digital Signals

- Lower power supply, e.g. smaller signal swing.

- Faster signal, e.g. smaller rise and fall time.

For high data rate Communication.



- Smaller signal swing
  → smaller noise margin.
  → lower power consumption.
- More EMI.

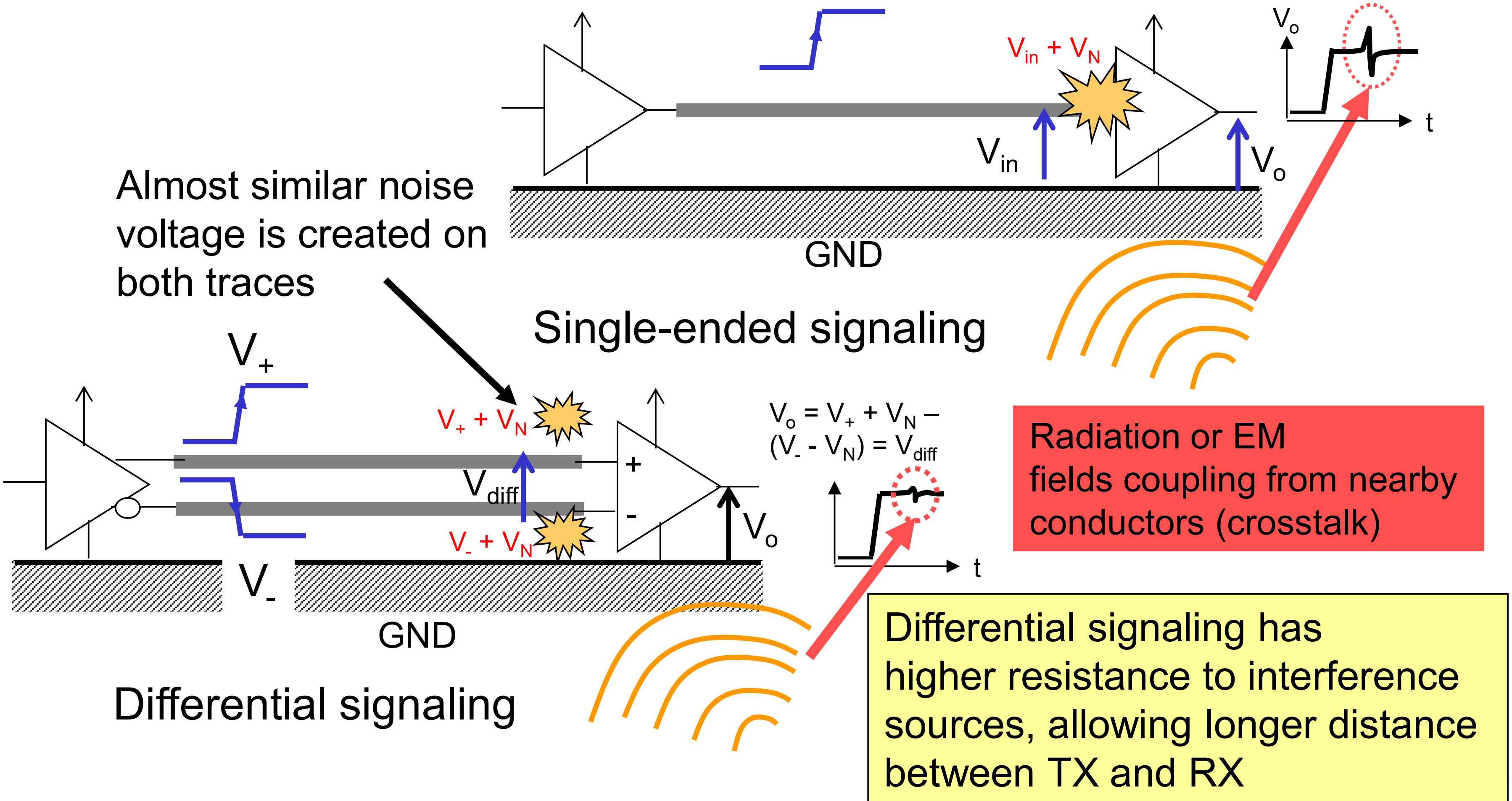
The Case for Differential Signaling

- Thus there is a need for an electrical signaling scheme with the following properties:
  - (1) Low voltage swing.
  - (2) Robust, small noise margin.
  - (3) Does not cause substantial EMI to adjacent circuits.
  - (4) Allow very high data rate.

An electrical signaling scheme that fulfills the above is the **Differential Signaling** (DS)

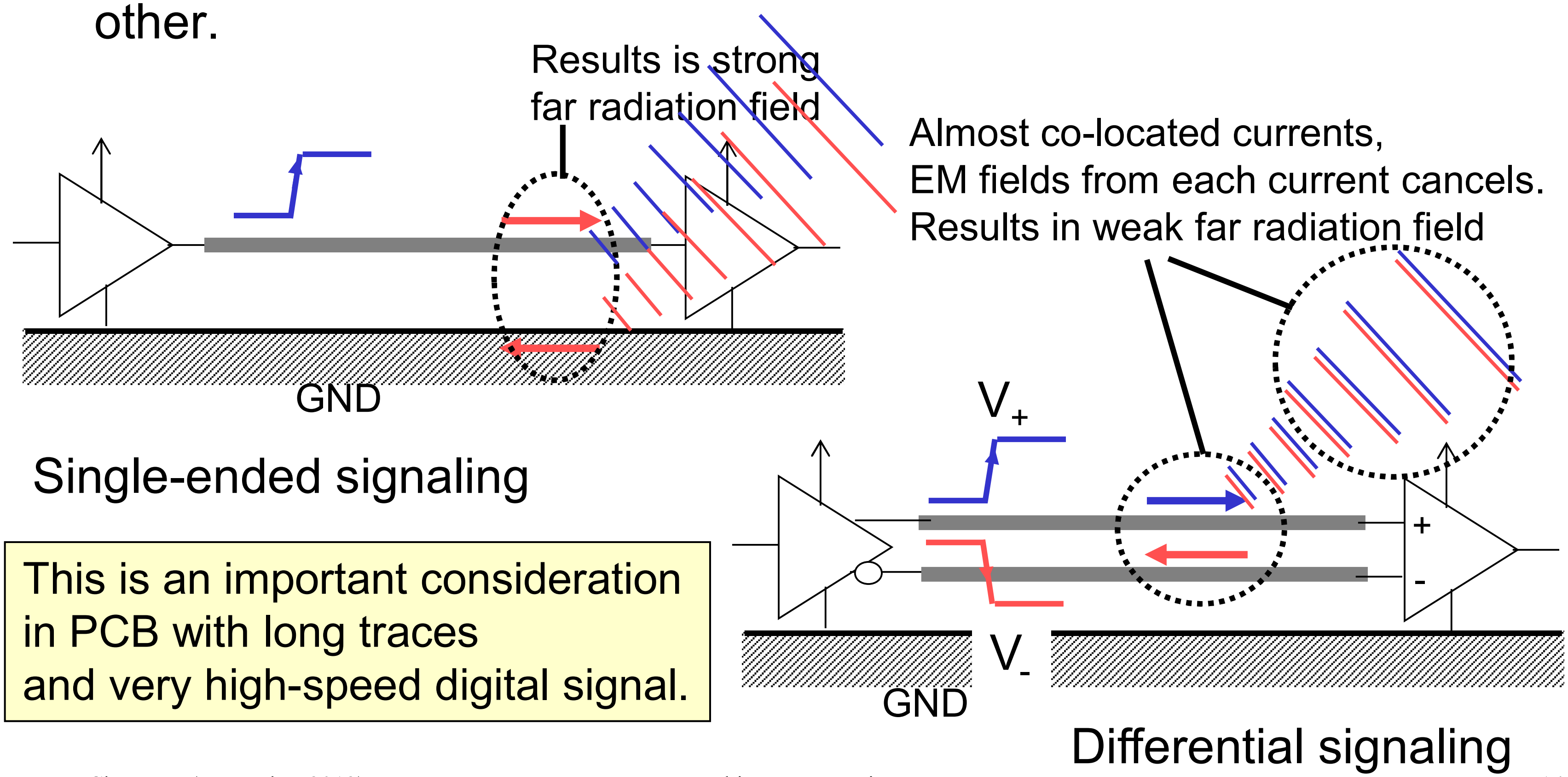
Benefit of DS - Immunity to EMI

- Interference from external sources causes changes to input voltage level at the receiver, differential signaling suppresses this effect.



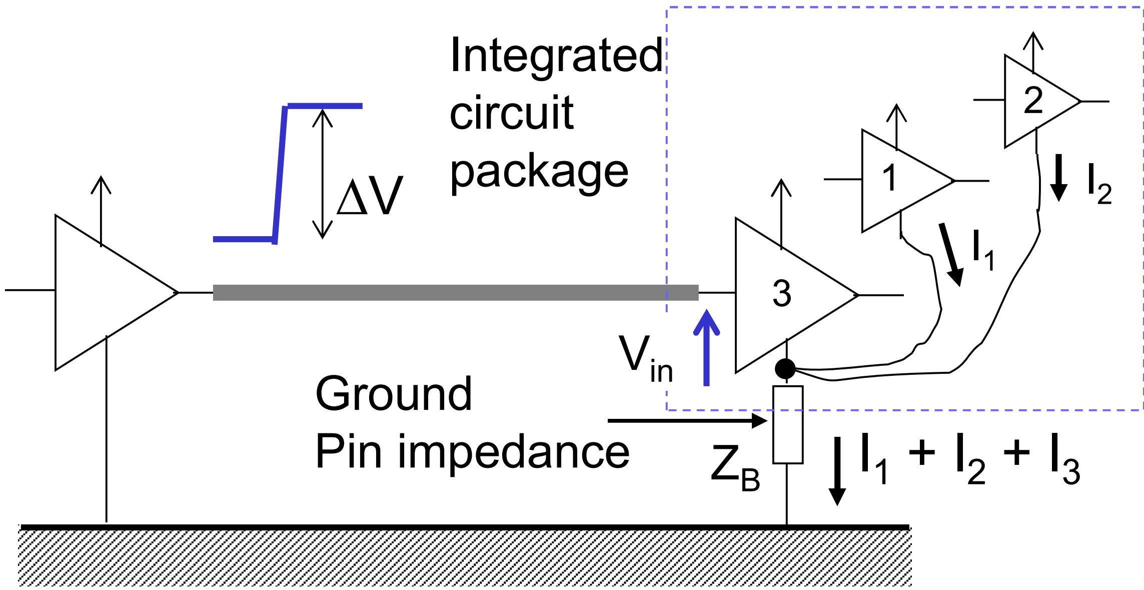
Benefit of DS - Lower Spurious Radiation

- Differential lines tends to radiate less, especially for very high-speed digital pulse.
- This is because the incident and return current are closer to each other than single-ended transmission, the net far EM fields cancel each other.



This is an important consideration in PCB with long traces and very high-speed digital signal.

Benefit of DS - Immunity to Common Impedance Coupling (1)



Single-ended signaling

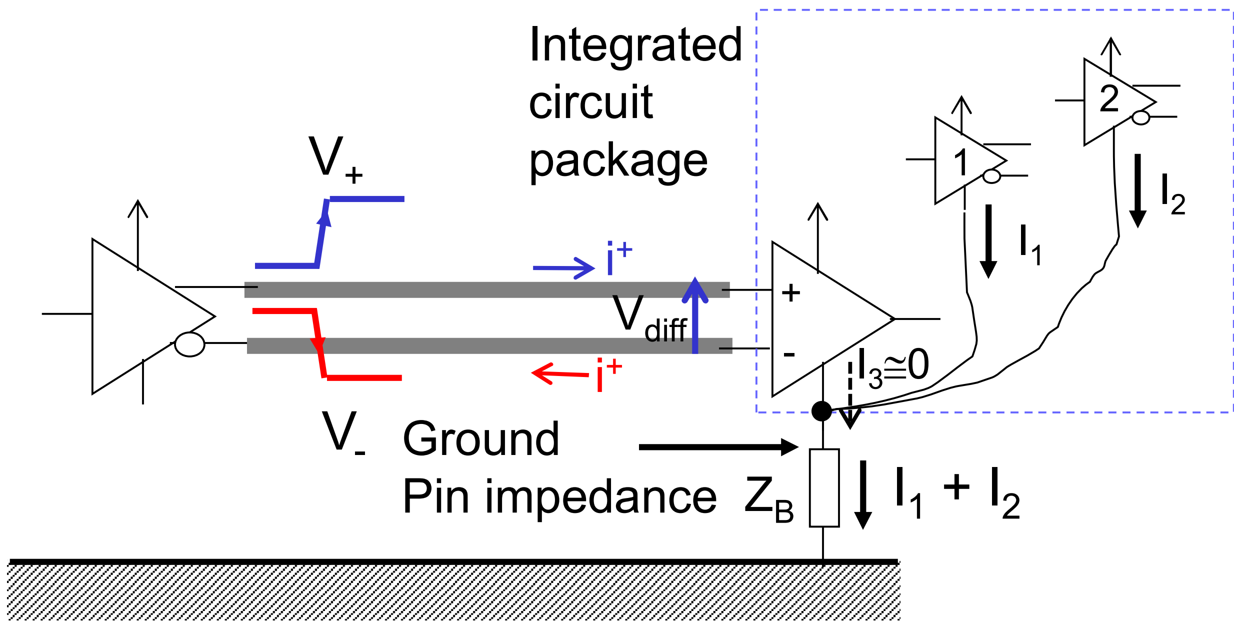
Reference voltage at receiver is disturbed due to non-zero ground pin impedance

$$V_{in} = \Delta V - Z_B\left(I_1 + I_2 + I_3\right)$$

Potential difference seen at the receiver fluctuates due to voltage drop cause by current from other gates or modules.

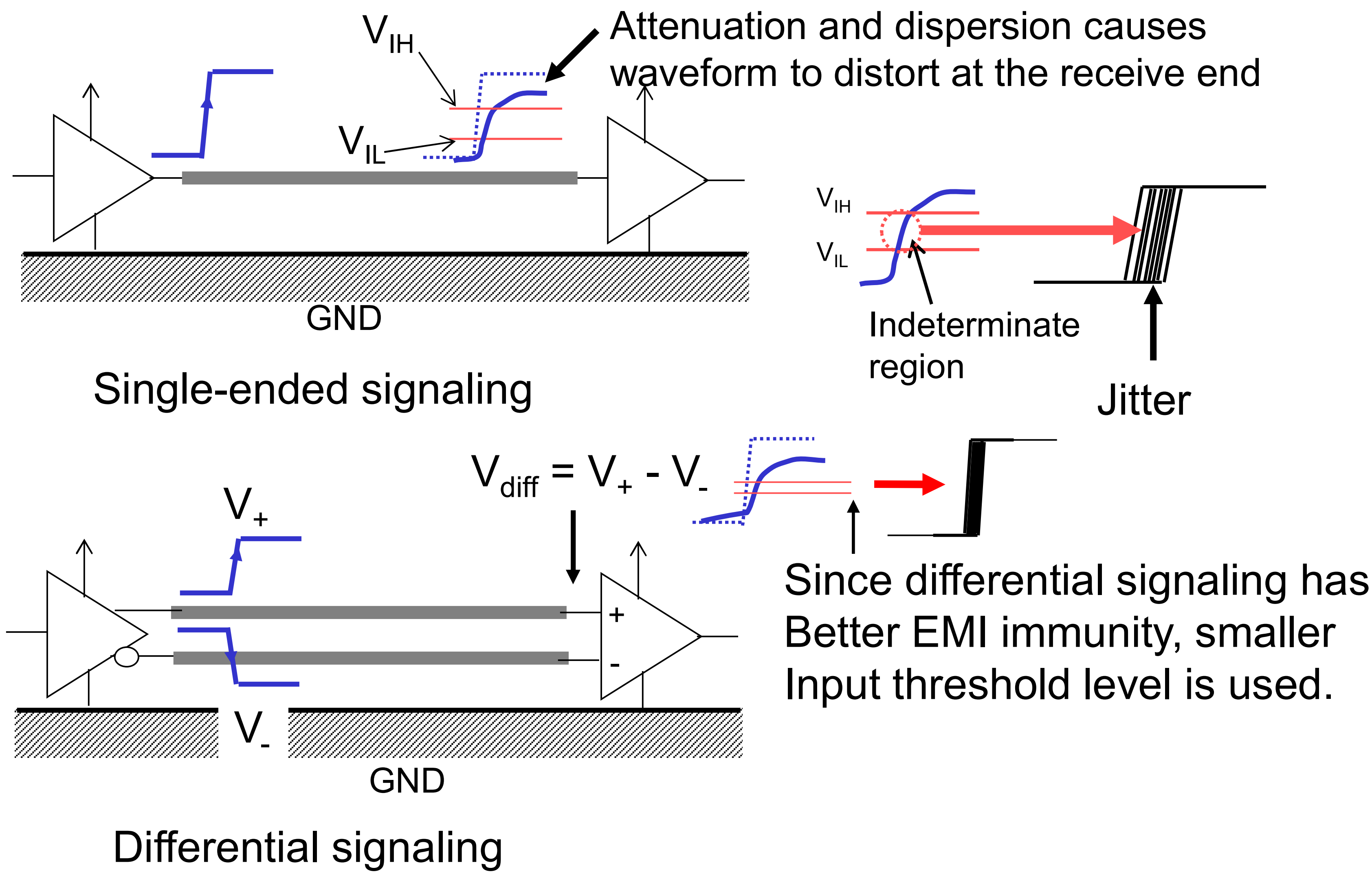
Benefit of DS - Immunity to Common Impedance Coupling (2)

- No problem with differential signaling.



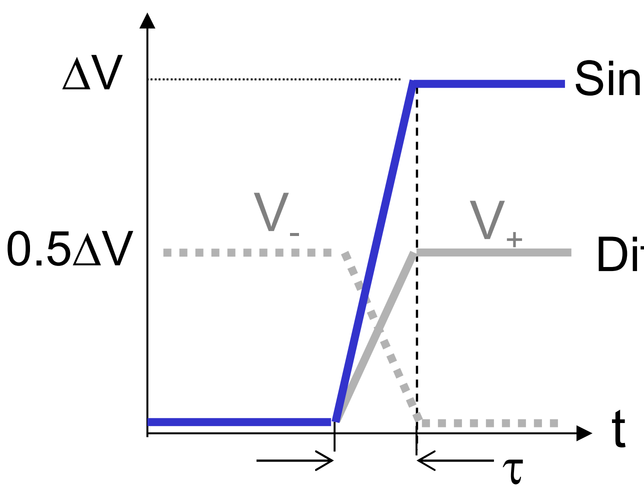
$$V_{din} = \left[V_+ - Z_B\left(I_1 + I_2 + I_3\right)\right] - \left[V_- - Z_B\left(I_1 + I_2 + I_3\right)\right]$$
$$= V_+ - V_-$$

Better Resistance to Line Attenuation, Distortion and Jitter



Lower Logic Voltage Swing and Higher Speed

- For the same amount of logic swing, differential signaling requires half the voltage swing per output pin.
- This translate into lower switching current (dV/dt current needed to charge up parasitic capacitance at the logic gate input).
- It also implies differential signaling is able to operate up to twice as fast as single-ended signaling…



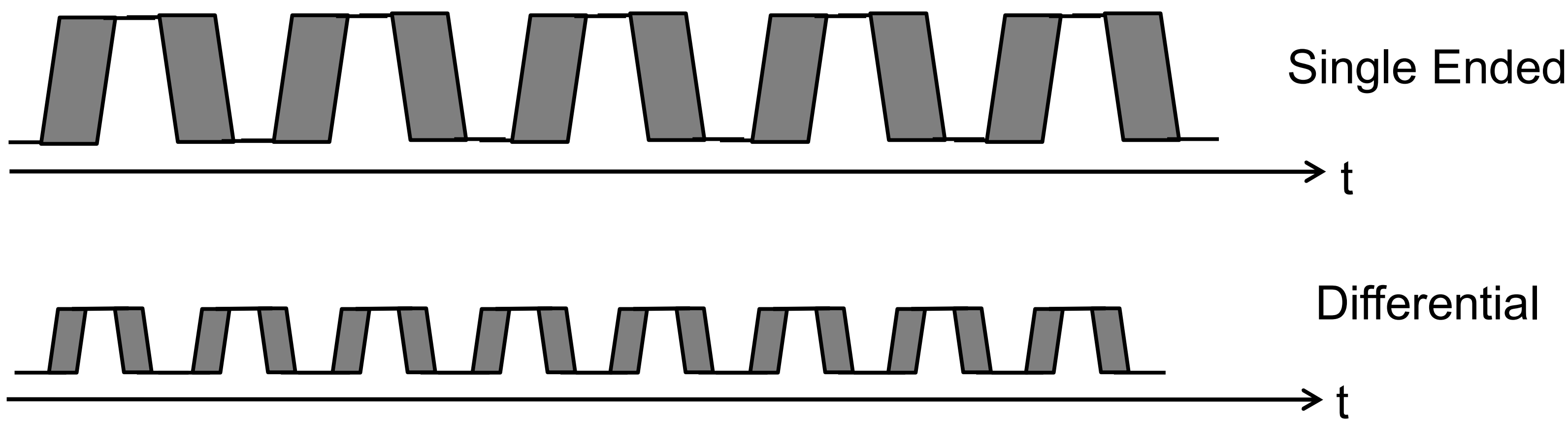
Single-ended $\frac{dV}{dt} = \frac{\Delta V}{\tau}$

Differential $\frac{dV}{dt} = \frac{\Delta V}{2\tau}$

Differential signaling can operate at lower supply voltage. For instance LVDS system can operate with $V_{CC} \cong 1.4$ to 2.0V.

High Data Rate

- The combine effect of lower voltage swing and smaller jitter allows high data rate transmission.



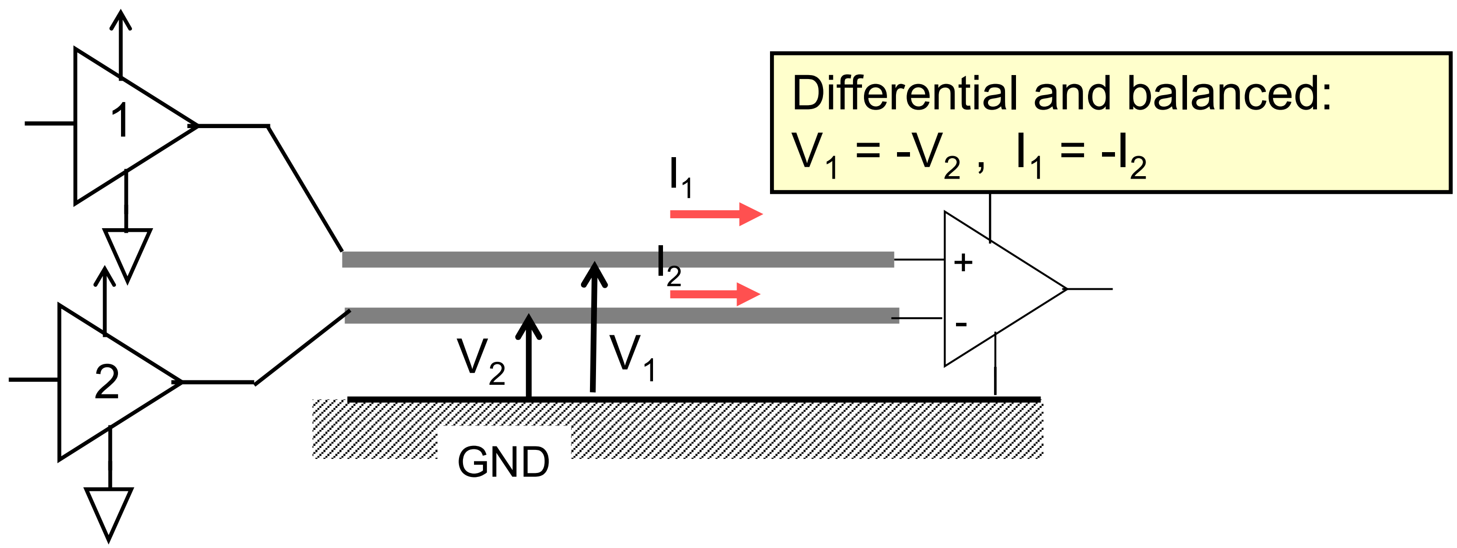
Some Drawbacks of DS

- Differential signaling is more difficult to implement.
- Higher cost, because of higher complexity in interconnection, transmit buffer and differential receiver.
- Extra conducting trace needed.
- Also both traces have to be tightly coupled, with sufficient isolation from other metallic structures. Else this would cause induction of common-mode signals on the differential traces.
- Differential signaling is usually restricted to interface that requires to support very high-speed digital pulse, for instance clock signal, or gigabit serial data in high performance SERDES (serializer/deserializer).

5.3 – Differential Signaling Theory

Differential and Balanced

- Merely injecting two equal amplitude and opposite polarity voltage signals onto two parallel traces does not make a pair of signal balanced.
- We may loosely say the pair of voltage signals is differential.
- The differential signal is truly balanced when the electric current induced in each signal trace is also equal in magnitude and opposite in polarity, with almost zero GND current.



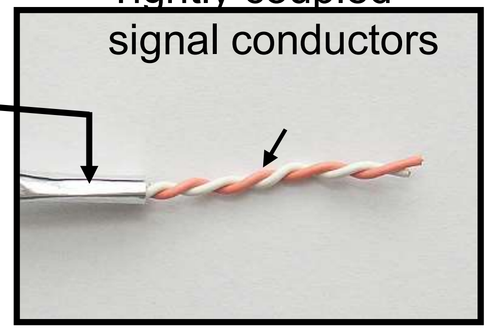
- Thus to achieve balanced condition, the electrical signal in each trace must encounter the same 'scene' when the other trace is deactivated.

Achieving Balanced Differential Signal (1)

- 3 criteria for balanced differential signal:
- **1**: Use tightly coupled transmission system, e.g. signal conductors very near each other compare to GND. Common in differential signaling on cables, for instance unshielded twisted-pair (UTP) cables, coupling coefficient, $0.6 < k < 1$.

The makes the signal conductors less susceptible to effect of other nearby conductors, ensuring the same 'scene' for both signals.

The shield forms the 3rd conductor



- **2**: Use perfectly balanced physical transmission system. Typically implemented on PCB, as it is difficult to achieve coupling coefficient of > 0.5 in adjacent traces on PCB.
- **3**: Two equal and opposite polarity driving

Coupling coefficient usually refers to inductive coupling, which is defined as:

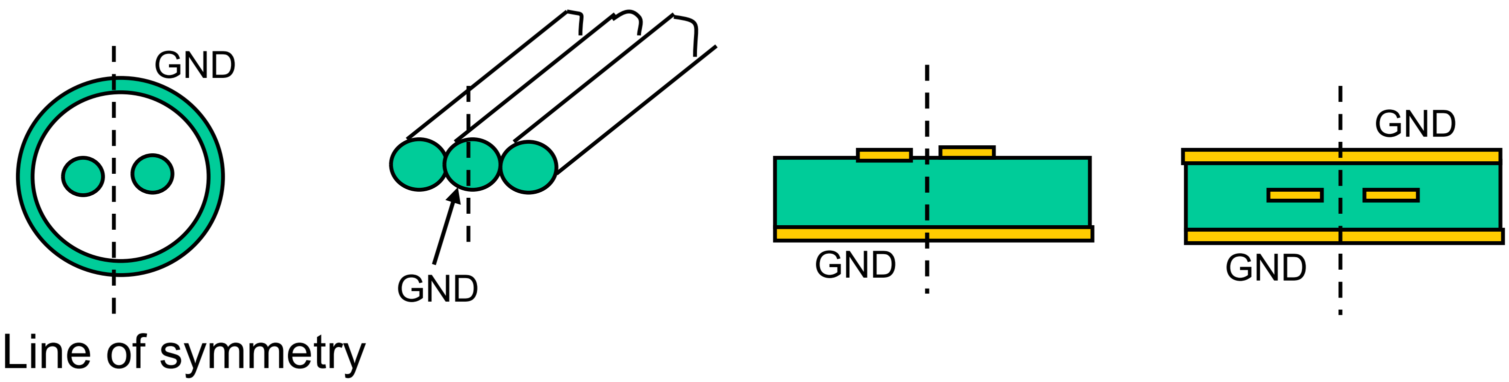
$$k = \frac{L_{12}}{\sqrt{L_1 L_2}}$$

Achieving Balanced Differential Signal (2)

- 3 Conductors – 2 signals and 1 GND.
- Signals conductors tightly coupled.
- Symmetry (this is to ensure similar current flows when each signal conductor is energized with a voltage signal).

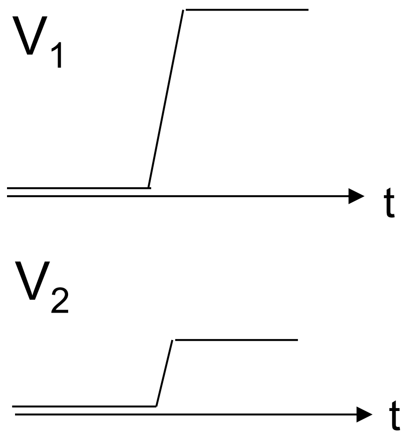
Coupled interconnection or transmission line (if interconnection is long)

Some examples (cross section)…

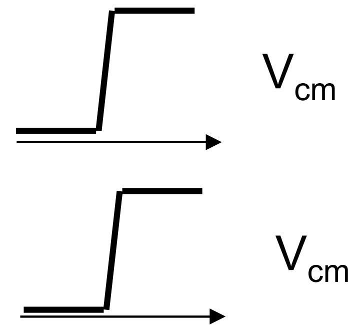


Differential and Common-Mode Voltage Signals

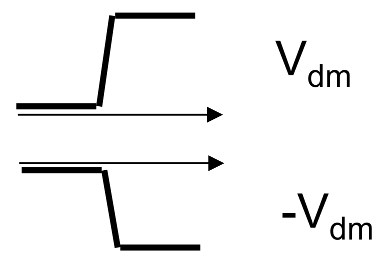
- Every pair of signals can be decomposed into similar and opposite components.
- In analog and digital world this is called common-mode (CM) and differential-mode (DM) components, and is defined as follows:



$$V_{cm} = \tfrac{1}{2}\left(V_1 + V_2\right) \qquad \textbf{(3.1a)}$$
$$V_{dm} = V_1 - V_2$$



Common-Mode Signal

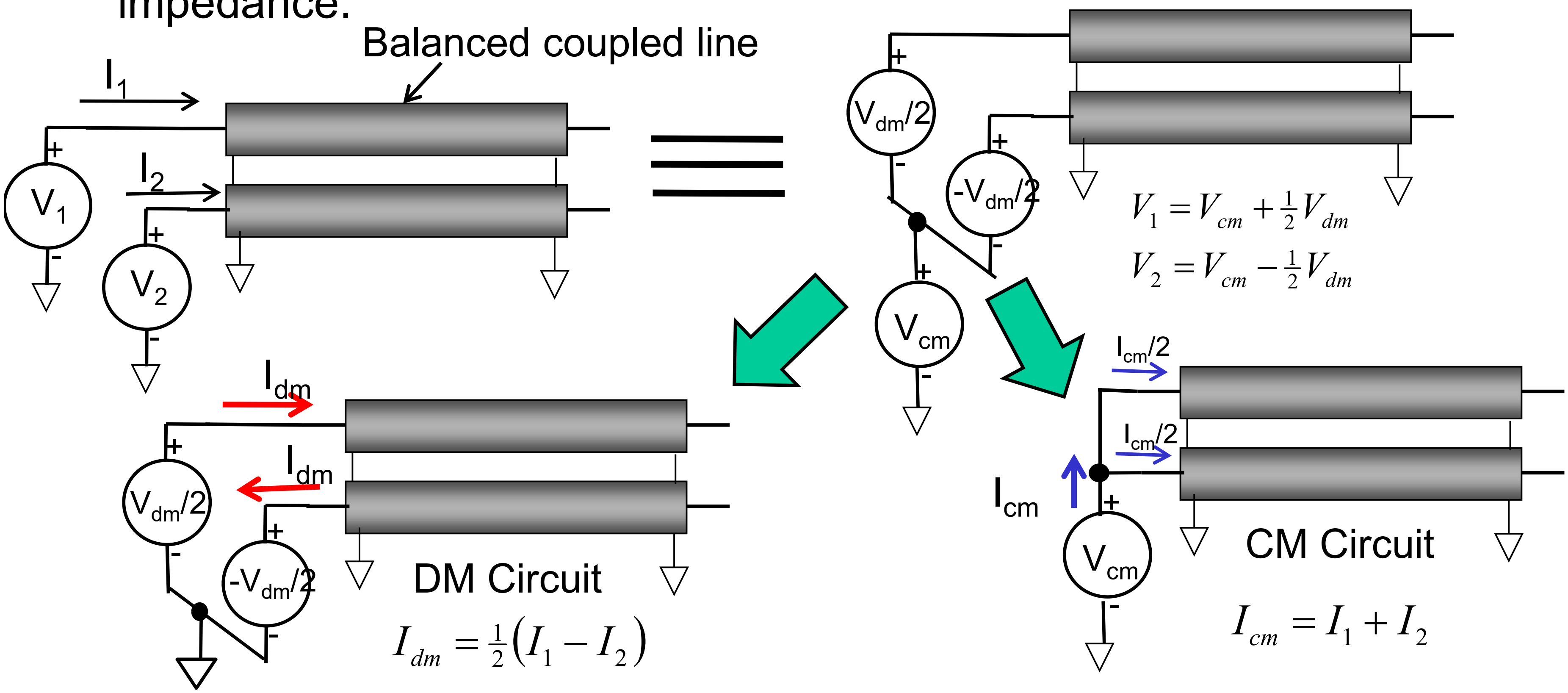


$$V_1 = V_{cm} + \tfrac{1}{2}V_{dm} \qquad \textbf{(3.1b)}$$
$$V_2 = V_{cm} - \tfrac{1}{2}V_{dm}$$

Differential-Mode Signal

Differential and Common-Mode Currents and Characteristic Impedance

- Thus the coupled transmission line circuit can be decomposed into DM and CM circuits, from which we define differential and common mode impedance.



$$Z_{dm} = \frac{V_{dm}}{I_{dm}} \quad \textbf{(3.2a)}$$

$$Z_{cm} = \frac{V_{cm}}{I_{cm}} \quad \textbf{(3.2b)}$$

Extra Even and Odd-Mode Signals (1)

- In RF/microwave engineering, a similar concept to the CM and DM signals is used, these are called even and odd mode signals.
- The even mode signal is similar to CM signal, while the odd mode signal is similar to DM signal (except different amplitude).
- Below is the definition of even and odd signals from a pair of voltage inputs V_1 and V_2, and the relationship between even-CM, and odd-DM signals.

$$V_{even} = \tfrac{1}{2}\left(V_1 + V_2\right) = V_{cm} \quad \textbf{(3.3a)}$$

$$V_{odd} = \tfrac{1}{2}\left(V_1 - V_2\right) = \tfrac{1}{2} V_{dm} \quad \textbf{(3.3b)}$$

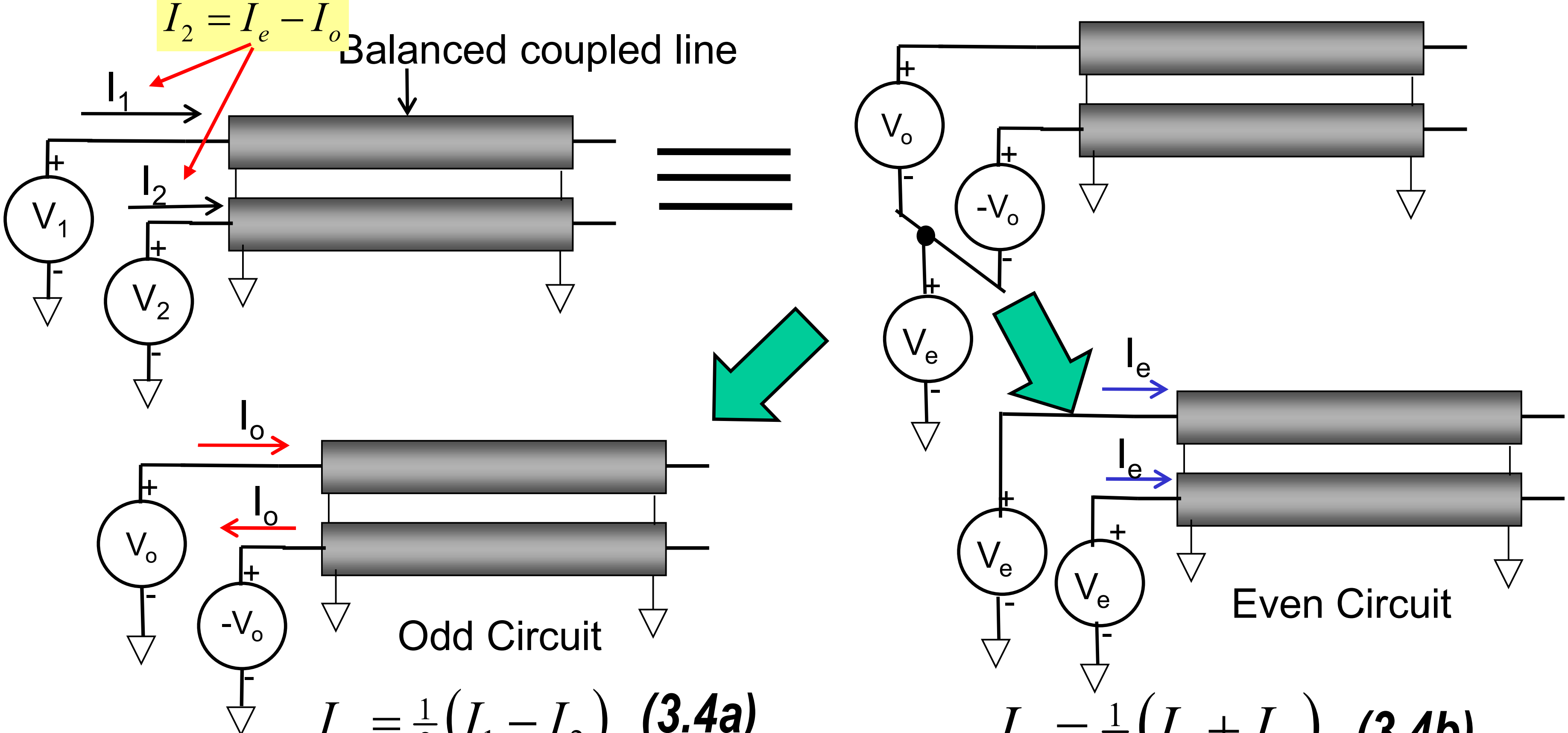
Notice that the definitions of V_{even} and V_{odd} is symmetry, whereas V_{cm} and V_{dm} definitions are not.

- The reason we want to introduce concepts in RF/microwave is there is already a lot of investigation into using balanced transmission and systems in RF/microwave domain since 1940s. And much of the results used in digital system design stems from the pioneering works in RF/microwave.

Extra Even and Odd-Mode Signals (2)

- Thus the following circuits are equivalent.

$$I_1 = I_e + I_o$$
$$I_2 = I_e - I_o$$



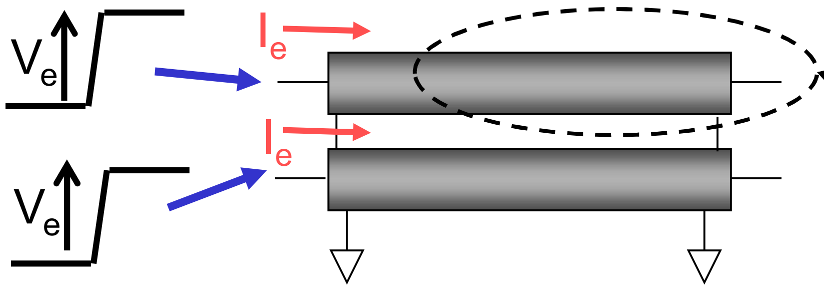
$$I_o = \tfrac{1}{2}\left(I_1 - I_2\right) \quad \textbf{(3.4a)}$$

$$I_e = \tfrac{1}{2}\left(I_1 + I_2\right) \quad \textbf{(3.4b)}$$

Even and Odd Mode Characteristic Impedance

Extra

- The definition of even and odd characteristic impedance is illustrated below, with the impedance being the ratio of the propagating voltage wave over the propagating current wave on ONE transmission line.

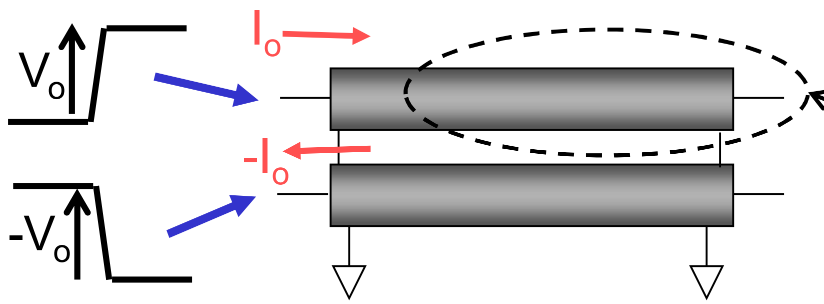


Even mode impedance

Defined for individual transmission line

$$Z_e = \frac{V_e}{I_e} \quad \textbf{(3.5a)}$$

These are usually provided in the form of charts or design equations in articles/books

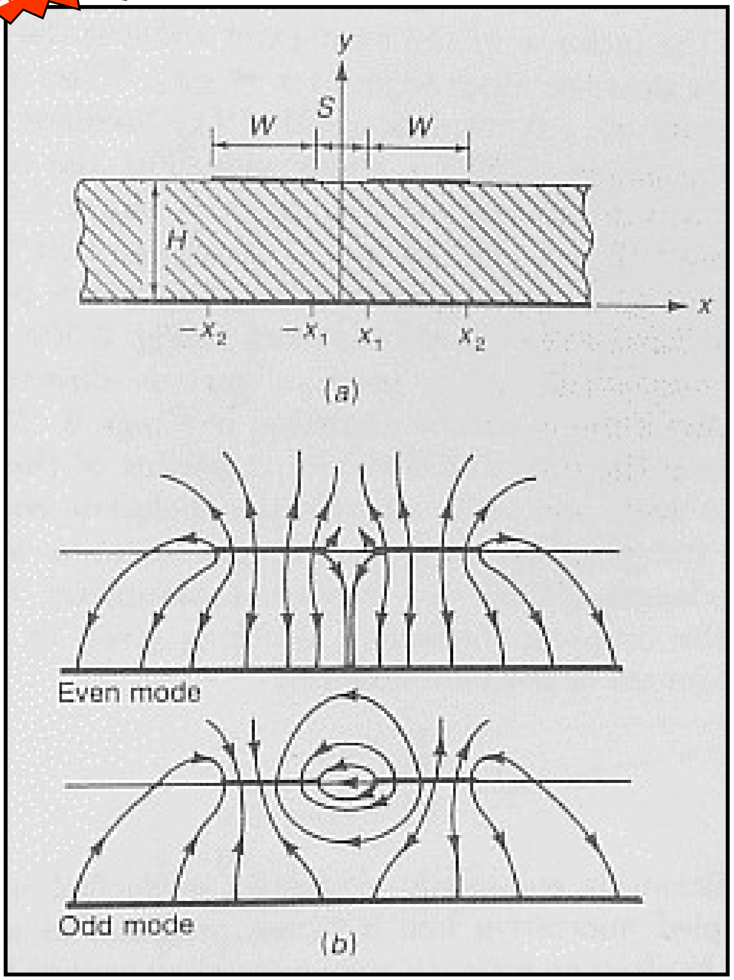


$$Z_o = \frac{V_o}{I_o} \quad \textbf{(3.5b)}$$

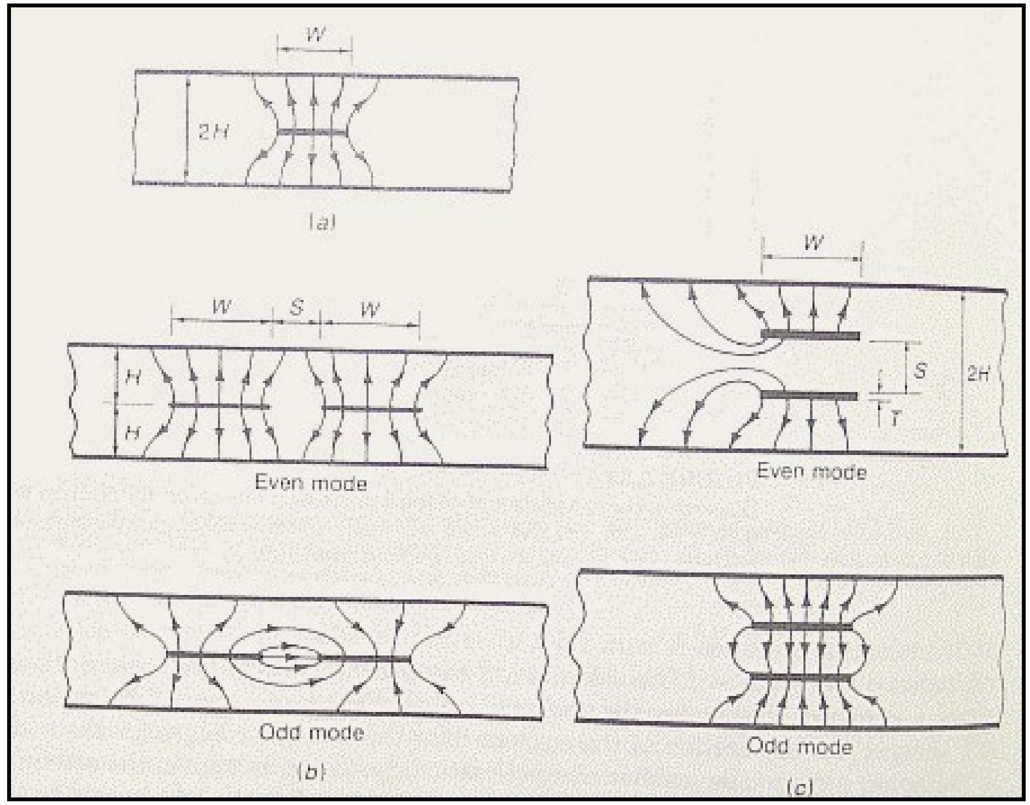
Odd mode impedance

EM Fields Under Even and Odd Mode

Extra



E-field for coupled microstripline
– Even and Odd mode



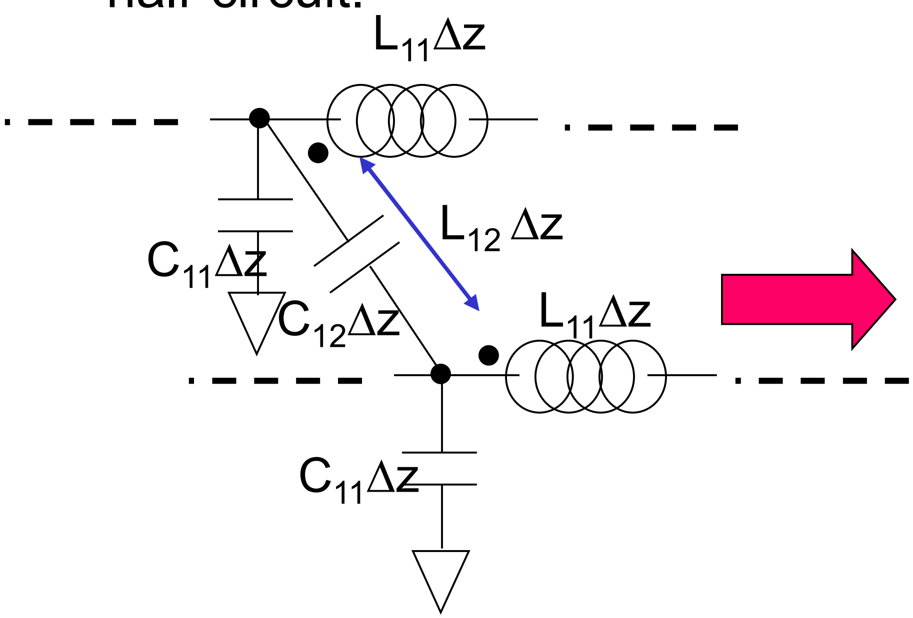
E-field for coupled stripline
– Even and Odd mode

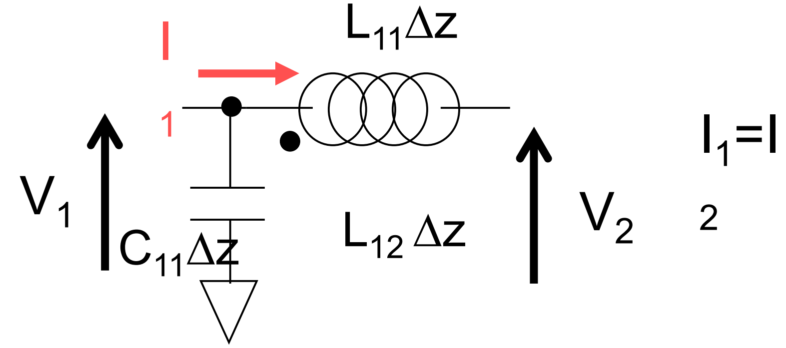
From Chapter 3, "Foundations for microwave engineering", R.E. Collin, 2nd Edition, 1992, McGraw-Hill.

Even Mode Impedance (Lossless Case) in Distributed RLCG Parameters

Extra

- Even-mode impedance is always larger than odd-mode impedance. To see why, consider the lossless case. Half-circuit concept can be used to analyze the two conditions.
- For even mode, no current flows through C_{12}, we have the following half-circuit.





$$V_1 = V_2 + j\omega L_{11}\Delta z I_1 + j\omega L_{12}\Delta z I_2$$
$$\Rightarrow V_1 = V_2 + j\omega\left(L_{11} + L_{12}\right)\Delta z I_1 \qquad (3.6)$$

$$I_1 - j\omega C_{11}\Delta z V_1 = I_2 \qquad (3.7)$$

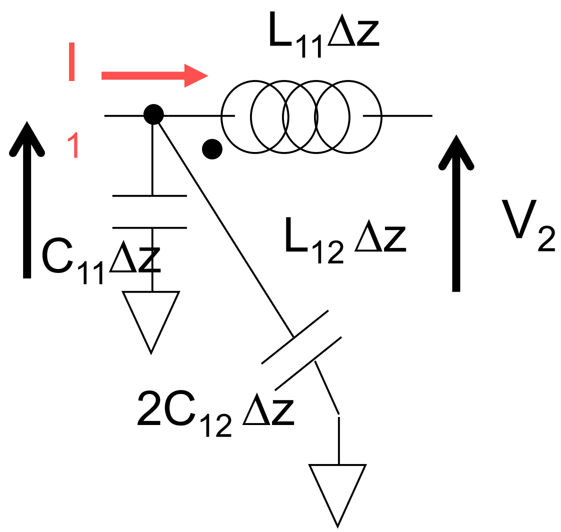
Compare (3.6) and (3.7) with the equations for single tline:

$$Z_e = \sqrt{\frac{L_{11}+L_{12}}{C_{11}}} \qquad (3.8)$$

Odd Mode Impedance (Lossless Case) in Distributed RLCG Parameters

Extra

- For odd mode, C_{12} can be divided into half, we have the following half-circuit.



$I_1 = -I_2$

$$V_1 = V_2 + j\omega L_{11}\Delta z I_1 + j\omega L_{12}\Delta z I_2$$
$$\Rightarrow V_1 = V_2 + j\omega(L_{11} - L_{12})\Delta z I_1 \qquad \textbf{(3.9)}$$

$$I_1 - j\omega(C_{11} + 2C_{12})\Delta z V_1 = I_2 \qquad \textbf{(3.10)}$$

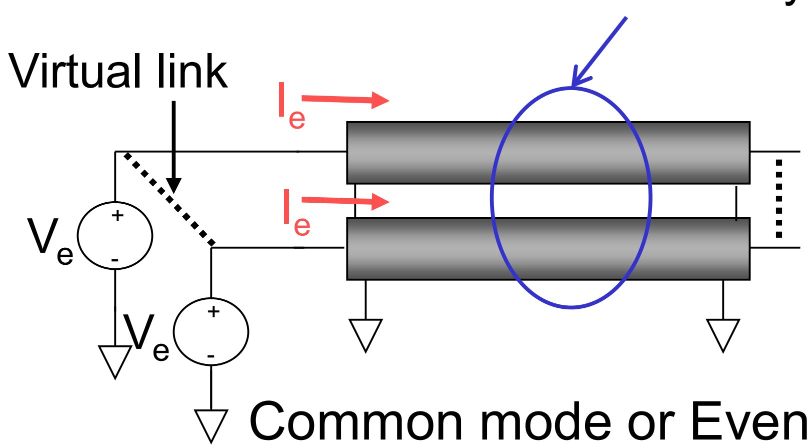
Compare (3.9) and (3.10) with the equations for single tline:

$$Z_o = \sqrt{\frac{L_{11} - L_{12}}{C_{11} + 2C_{12}}} \qquad \textbf{(3.11)}$$

Link between Z_{cm}, Z_{dm} and Z_o, Z_e (1)

Extra

- In the digital domain, the coupled pair of transmission lines are treated as a single system.
- Thus in the case of Common mode or Even excitation, we treat the system as being driven by a voltage source of V_e (or V_{cm}) with total current of $2 \times I_e$.
- This leads to the following definition for Common Mode Impedance.



$$Z_{cm} = \frac{V_{cm}}{I_{cm}} = \frac{V_e}{2I_e} = \frac{1}{2} Z_e$$

$$\Rightarrow Z_{cm} = \frac{1}{2} Z_e \quad \textbf{(3.12a)}$$

$$\boxed{Z_{cm} = \frac{1}{2}\sqrt{\frac{L_{11}+L_{12}}{C_{11}}}} \quad \textbf{(3.12b)}$$

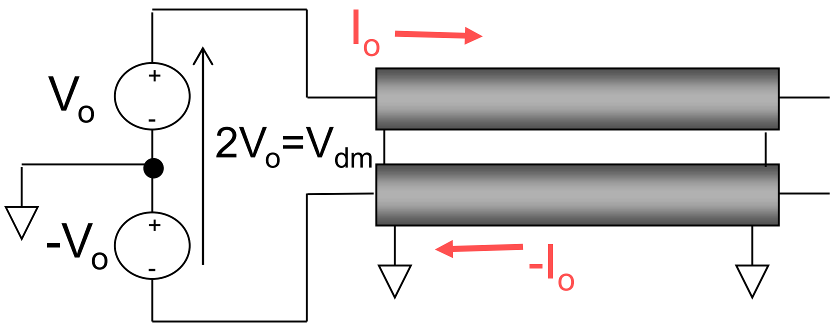
Link between Z_{cm} , Z_{dm} and Z_o , Z_e (2)

Extra

- Similarly for Differential Mode or Odd excitation, it is treated as one system in digital domain, with the following definition for Differential Impedance.

$$Z_{dm} = \frac{V_{dm}}{I_{dm}} = \frac{2V_o}{I_o} = 2Z_o$$

$$\Rightarrow Z_{dm} = 2Z_o \qquad \textbf{(3.13a)}$$



Differential mode or Odd mode
(we assume no current flows
in the GND conductor)

$$Z_{dm} = 2\sqrt{\frac{L_{11}-L_{12}}{C_{11}+2C_{12}}} \qquad \textbf{(3.13b)}$$

In general:

$$Z_o \le Z_e$$

$$\Rightarrow \frac{1}{2} Z_{DM} \le 2Z_{CM}$$

$$\Rightarrow \boxed{Z_{DM} \le 4Z_{CM}}$$

Important relation, equals when both lines are balanced and uncoupled.

Link Between I_{cm}, I_{dm} and I_e, I_o

- From the discussion, it is easy to see that:

$$I_{dm} = I_o \quad \textit{(3.14a)}$$

$$I_{cm} = 2I_e \quad \textit{(3.14b)}$$

$$I_{dm} = \tfrac{1}{2}\left(I_1 - I_2\right) \quad \textit{(3.15a)}$$

$$I_{cm} = I_1 + I_2 \quad \textit{(3.15b)}$$

Designing Coupled Transmission Line for Differential Signaling

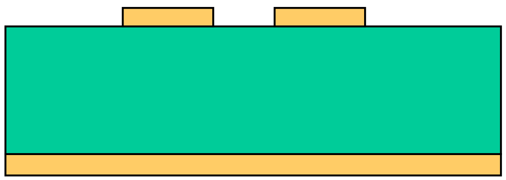
- Thus we see that there is a link between Common and Differential mode impedance with Even and Odd mode impedance.
- There are already vast literatures dealing with the design procedures of coupled transmission line in RF/microwave domain.
- These are usually in the form of tables or design equations linking the physical parameters with Z_e and Z_o.
- Thus most of the time, when given a specification of Z_{dm} and Z_{cm} for differential signaling, we can convert these into the odd and even mode impedance, then use the tools in RF/microwave domain to perform the synthesis.
- Of course nowadays this is automated in the form of software, nevertheless the underlying procedures are unchanged.

Procedures for Designing Traces for Specific Z_{DM} and Z_{CM}

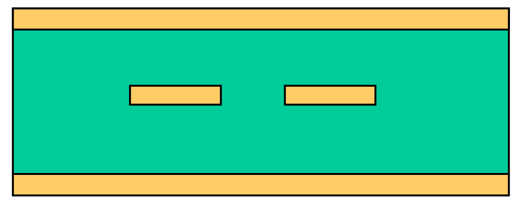
- Similar iterative procedure for designing single transmission line trace is used to design differential traces.
- **Step 1** – Draw cross section of differential trace.
- **Step 2** - The most accurate way to compute differential and common-mode impedance, is to used a 2D electromagnetic field solver software as shown in Part 2 and Part 3 to solve for the TEM mode E and H fields.
- **Step 3** - Assuming low loss condition, from the fields calculate C_{11}, C_{12}, L_{11} and L_{12}. Most commercial field solver software can perform this automatically.
- **(Optional) Step 4** - Use relations (3.8) and (3.11) to find Z_e and Z_o.
- **Step 5** - Then use the relations (3.12b) and (3.13b) to find the Z_{cm} and Z_{dm}.
- **Step 6** - If the computed Z_{dm} and Z_{cm} do not meet requirement repeat Step 1 by changing the physical dimensions of the differential traces.

5.4 – Designing Differential Transmission Line in PCB

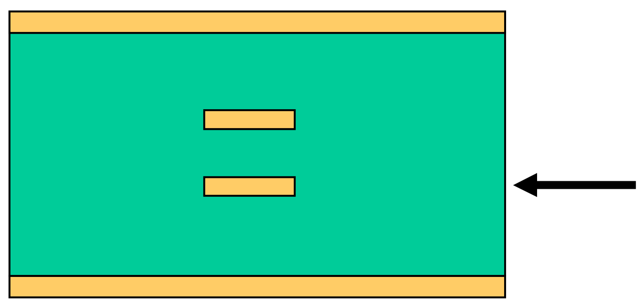
Differential Tline Implementation on PCB



Microstrip line (Edge coupled)



Strip line (Edge coupled)



For lower differential Impedance Z_{DM}

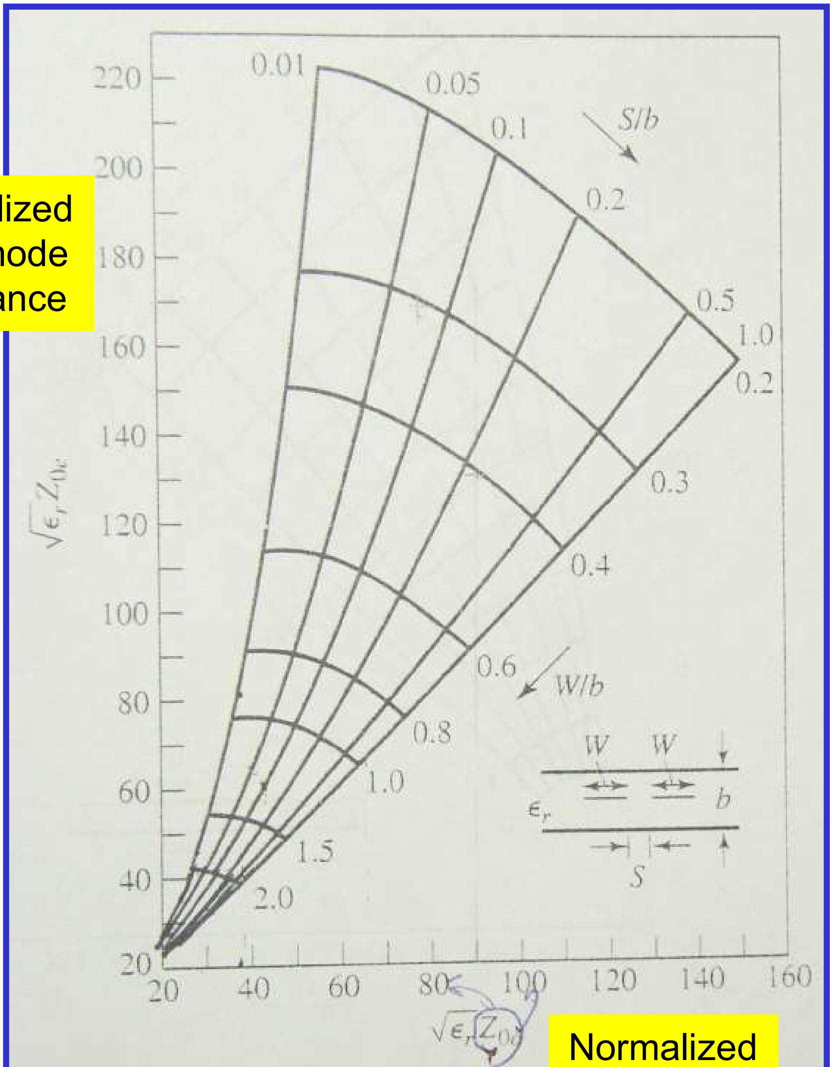
Strip line (Broadside coupled)

Coupled Transmission Lines Design Approaches

- Similar to single transmission line design, we can design a pair of coupled transmission using various approaches, such as:
  - EM field solver program.
  - Design equations or charts from curve-fitted results from EM field solver program.
  - Commercial and non-commercial software which incorporate the design equations into a unified graphical user interface.

Example of Design Chart for Coupled Stripline

Normalized even mode impedance

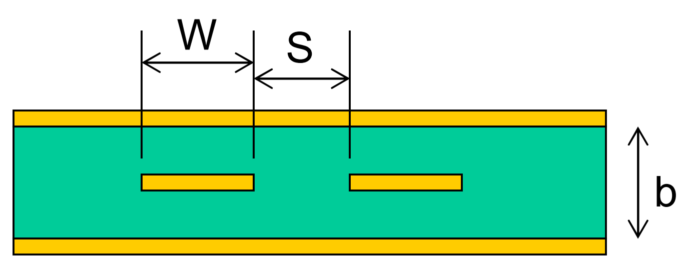


Normalized odd mode impedance

Diagram taken from Pozar [5], chapter 8.

See the book by T.C. Edwards, for in-depth coupled microstripline design equations.

By choosing a suitable b, the W and S can be computed.



Example 4.1 - Differential Transmission Line Design using Chart

- Design a differential stripline for with Z_{DM}=90Ω differential impedance and Z_{CM}= 45Ω common mode impedance. Dielectric constant ε_r = 4.4, and thickness b = 1.0mm

$$Z_e = 2Z_{CM} = 90$$

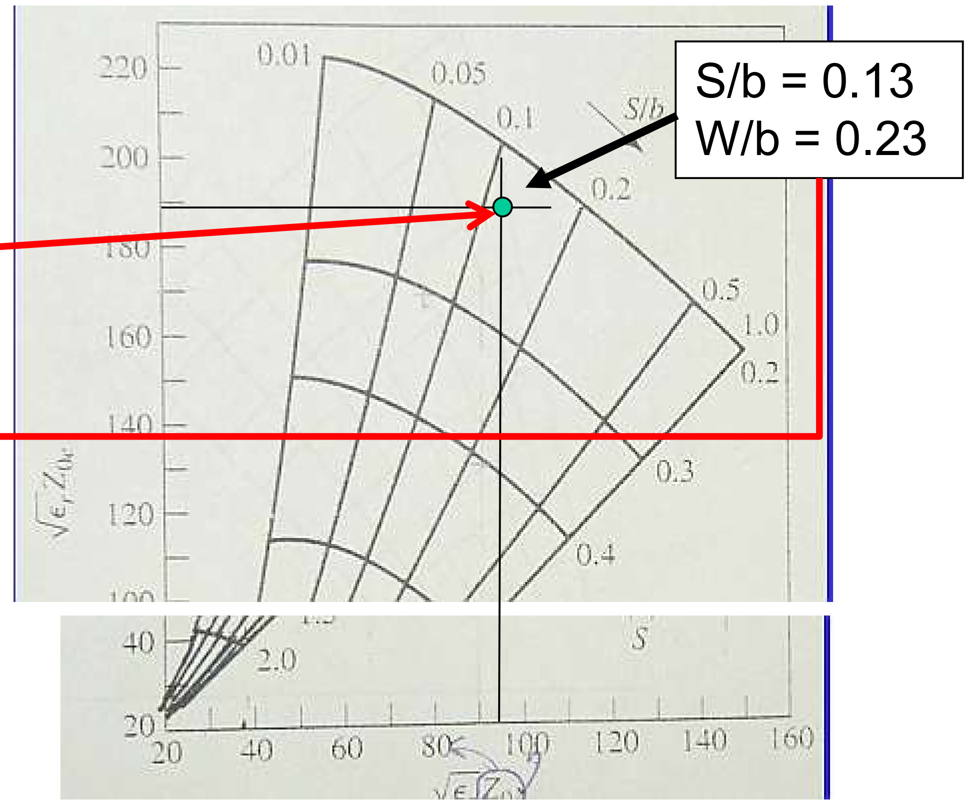
$$Z_o = \frac{1}{2}Z_{DM} = 45$$

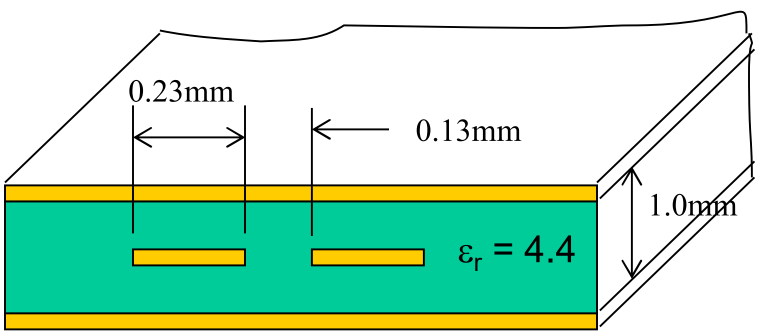
$$\sqrt{\varepsilon_r}Z_e = \boxed{188.79\Omega}$$

$$\sqrt{\varepsilon_r}Z_o = \boxed{94.40\Omega}$$

$$S = 0.13b = 0.13 \text{ mm}$$

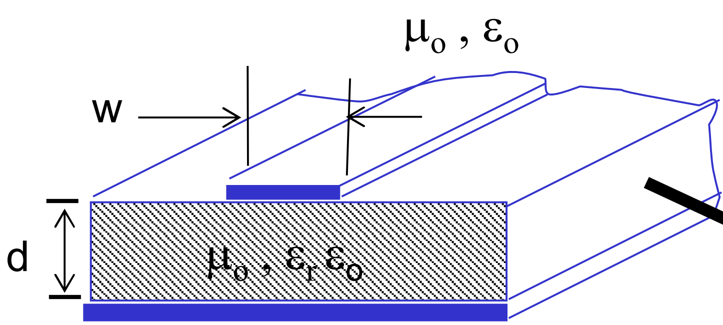
$$W = 0.23b = 0.23 \text{ mm}$$



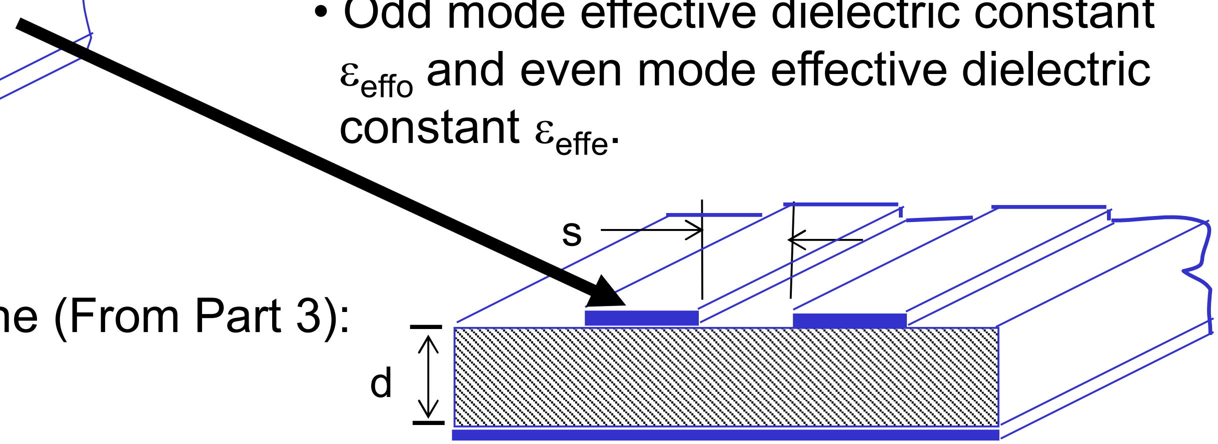


Coupled Microstrip Design Equation (1)

- Taken from Chapter 6 of [3], accuracy of around 3%.



Parameters for coupled Tline:
- Odd mode impedance Z_{oo}.
- Even mode impedance Z_{oe}.
- Odd mode effective dielectric constant ε_{effo} and even mode effective dielectric constant ε_{effe}.



Consider a single microstrip line (From Part 3):

$$\varepsilon_{eff} = 1 + \frac{\varepsilon_r - 1}{2}\left[1 + \frac{1}{\sqrt{1 + \frac{10d}{w}}}\right]$$

$$Z_c = \frac{377}{\sqrt{\varepsilon_{eff}}}\left[\frac{w}{d} + 1.98\left(\frac{w}{d}\right)^{0.172}\right]^{-1}$$

Speed of light in vacumn

$$c = \frac{1}{\sqrt{\mu_o \varepsilon_o}}$$

Key assumptions:
- Low loss.
- Ignore conductor thickness.
- Quasi-static or quasi-TEM.
- Non-magnetic dielectric, $\mu = \mu_o$.

Coupled Microstrip Design Equation (2)

- From the parameters of single microstrip Z_c and ε_{eff} and *w*, *s* and *h*, we can find the even mode capacitance C_e of coupled microstrip line as follows:

$$C_e = C_p + C_{f1} + C_{f2} \qquad \textbf{(4.1a)}$$

$$C_p = \varepsilon_o \varepsilon_r \tfrac{w}{d} \qquad \textbf{(4.1b)}$$

$$C_{f1} = \tfrac{1}{2}\left(\frac{\sqrt{\varepsilon_{eff}}}{cZ_c} - C_p\right) \qquad \textbf{(4.1c)}$$

$$C_{f2} = \frac{C_{f1}}{1 + \left(e^{-0.1e^{\left(2.33-2.53\frac{w}{d}\right)}}\right)\left(\frac{d}{s}\right)\tanh\left(8\frac{s}{d}\right)}\sqrt{\frac{\varepsilon_r}{\varepsilon_{eff}}} \qquad \textbf{(4.1d)}$$

Note that when $\varepsilon_r = 1$

$$\varepsilon_{eff} = 1$$

$$Z_c = 377\left[\frac{w}{d} + 1.98\left(\frac{w}{d}\right)^{0.172}\right]^{-1}$$

$$C_p = \varepsilon_o \frac{w}{h}$$

$$C_{f1} = \frac{1}{2}\left(\frac{1}{cZ_c} - C_p\right)$$

$$C_{f2} = \frac{C_{f1}}{1 + \left(e^{-0.1e^{\left(2.33-2.53\frac{w}{h}\right)}}\right)\frac{h}{s}\tanh\left(8\frac{s}{h}\right)}$$

The resulting even mode capacitance is called C_{e1}.

Coupled Microstrip Design Equation (3)

- From C_e and C_{e1}, we then find Z_{oe} and ε_{effe}:

$$Z_{oe} = \frac{1}{c\sqrt{C_e C_{e1}}} \qquad \textbf{\textit{(4.2a)}}$$

$$\varepsilon_{effe} = \frac{C_e}{C_{e1}} \qquad \textbf{\textit{(4.2b)}}$$

Coupled Microstrip Design Equation (4)

- In a similar manner we find the odd mode capacitance C_o as follows:

$$C_o = C_p + C_{f1} + C_{ga} + C_{gd} \qquad \textbf{(4.3a)}$$

$$k = \frac{\left(\frac{s}{d}\right)}{\left(\frac{s}{d}\right) + 2\left(\frac{w}{d}\right)} \qquad \textbf{(4.3b)}$$

$$C_{ga} = \begin{cases} \frac{\varepsilon_o}{\pi} \ln\left[2\frac{1+\left(1-k^2\right)^{\frac{1}{4}}}{1-\left(1-k^2\right)^{\frac{1}{4}}}\right] & \text{for } 0 \le \mathrm{k}^2 \le 0.5 \\ \frac{\varepsilon_o \pi}{\ln\left[2\left(\frac{1+\sqrt{k}}{1-\sqrt{k}}\right)\right]} & \text{for } 0.5 < \mathrm{k}^2 \le 1.0 \end{cases} \qquad \textbf{(4.3c)}$$

$$C_{gd} = \frac{\varepsilon_o \varepsilon_r}{\pi} \ln\left[\coth\left(\frac{\pi}{4} \cdot \frac{s}{d}\right)\right] + 0.65 C_{f1}\left[\frac{0.02}{\frac{s}{d}}\sqrt{\varepsilon_r} + 1 - \varepsilon_r^{-2}\right] \qquad \textbf{(4.3d)}$$

We also need to compute The corresponding C_o when $\varepsilon_r = 1$, known as C_{o1}.

Coupled Microstrip Design Equation (5)

- And finally obtain Z_{oe} and ε_{effo}:

$$Z_{oo} = \frac{1}{c\sqrt{C_o C_{o1}}} \quad \textbf{(4.4a)}$$

$$\varepsilon_{effo} = \frac{C_o}{C_{o1}} \quad \textbf{(4.4b)}$$

- The phase velocity of both even and odd modes propagation are given by:

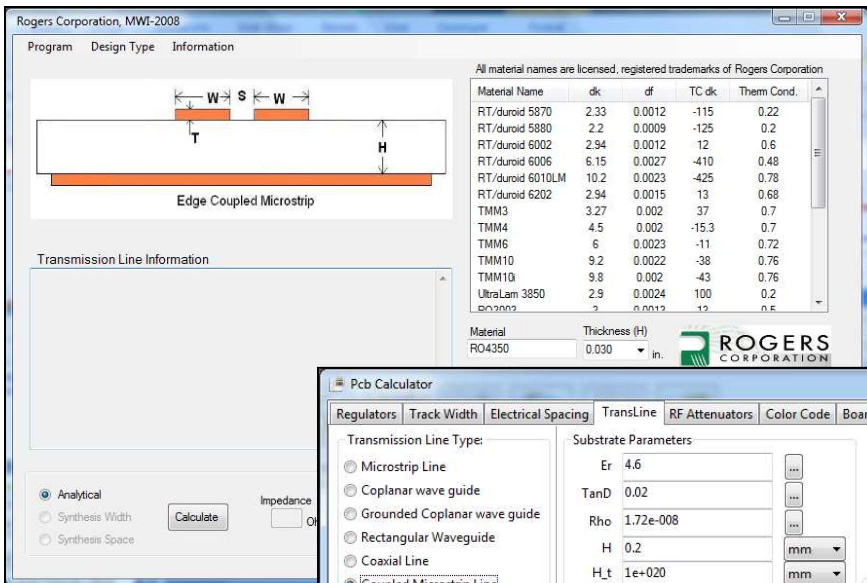
$$v_{pe} = \frac{1}{\sqrt{\mu_o \varepsilon_o \varepsilon_{effe}}} \quad \textbf{(4.5a)}$$

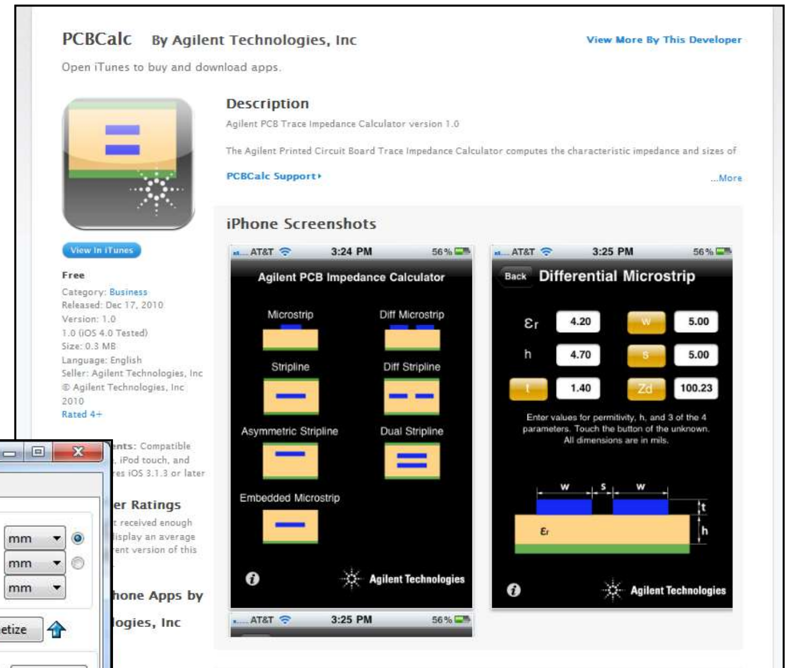
$$v_{po} = \frac{1}{\sqrt{\mu_o \varepsilon_o \varepsilon_{effo}}} \quad \textbf{(4.5b)}$$

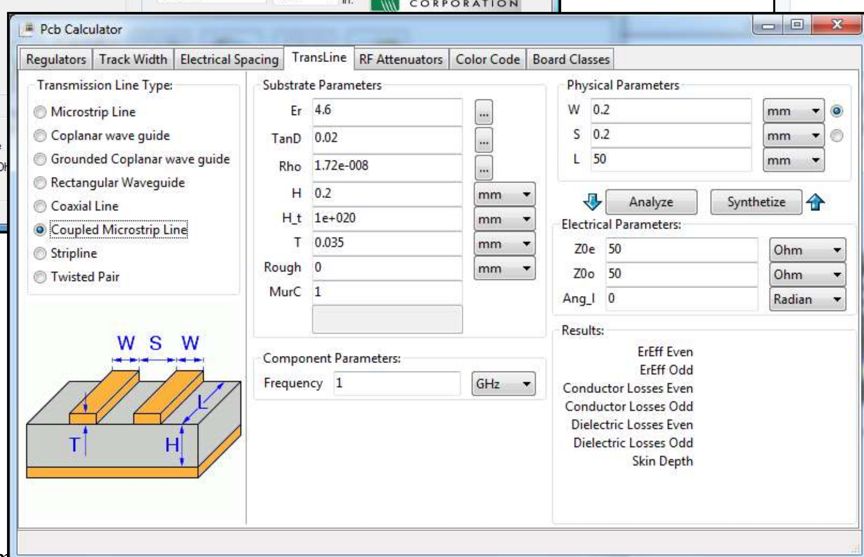
For the origin of this set of Formulae, see Garg R., Bahl I. J.,"Characteristics of coupled microstriplines", IEEE Transaction on Microwave Theory and Techniques, MTT-27, No.7, pp. 700-705, July 1979.

Free Coupled Transmission Lines Design Tools

- **Microwave Impedance Calculator** from Rogers Corporation, KiCAD (for Windows PC) and **PCB Trace Impedance Calculator** from Agilent Technologies (Apple iPhone, iPad).







5.5 – Some Layout Considerations for Differential Signaling

Suppressing Common-Mode Component

- We have seen in the first section that CM component cause the most interference, and it presence indicates physical imbalance in the system (hence more susceptible to EMI).
- Thus in driving a differential interconnections, we try to suppress the CM component as much as possible.
- This is done by ensuring that the two voltage and current signals in differential interconnections are equal in amplitude, opposite in polarity AND similar in timing.

$$
\begin{aligned}
&\tfrac{1}{2}\left[V_1(t)+V_2(t)\right]=0\\
&\Rightarrow V_1(t)+V_2(t)=0\\
&\Rightarrow V_1(t)=-V_2(t)
\end{aligned}
$$

When CM component is 0, a pair of signal is naturally equal amplitude, opposite polarity and similar in timing

- When the above is not true, common mode components will occur.

Potential Issues

- The major concern with differential signaling is non-zero common-mode signals.

$$\frac{1}{2}\left(V_1 + V_2\right) \neq 0$$
$$\Rightarrow V_1 \neq -V_2$$

$V_{CM} \neq 0$
$I_{CM} \neq 0$ (of $I_G \neq 0$)

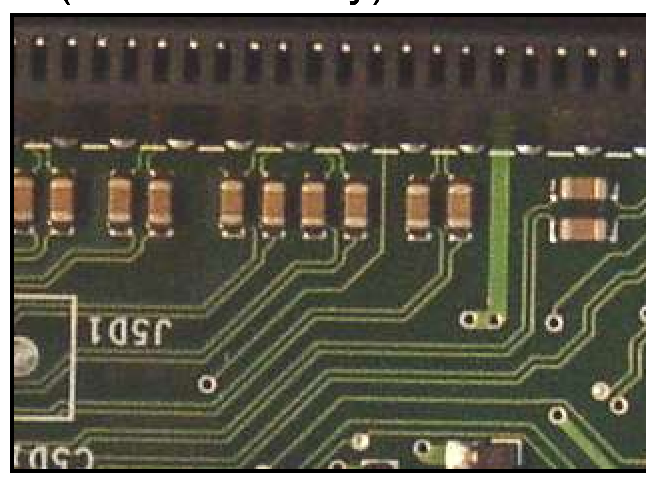
- This is mainly due to unbalanced condition, which is caused by…
  – Insufficient isolation from nearby metallic structures. Coupling to other metallic objects result in physical unbalance condition.
  – Unwanted timing difference (skew).
  – Unbalance physical interconnections can result in common-mode to differential-mode signal conversion.

Issues from Common-Mode Signals

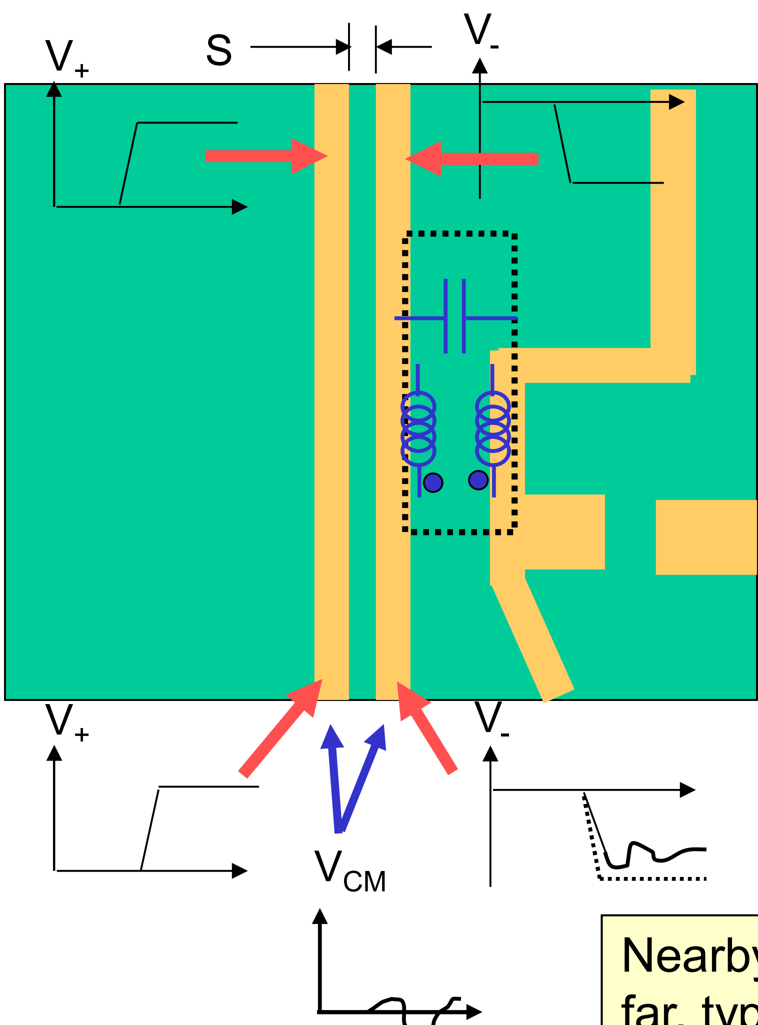
- Common-mode current contribute to high spurious radiation.
- Common-mode EM fields can interfere with nearby signal traces.
- If termination scheme for differential signaling does not cater for common-mode signal, large reflection of common-mode signal might occur.

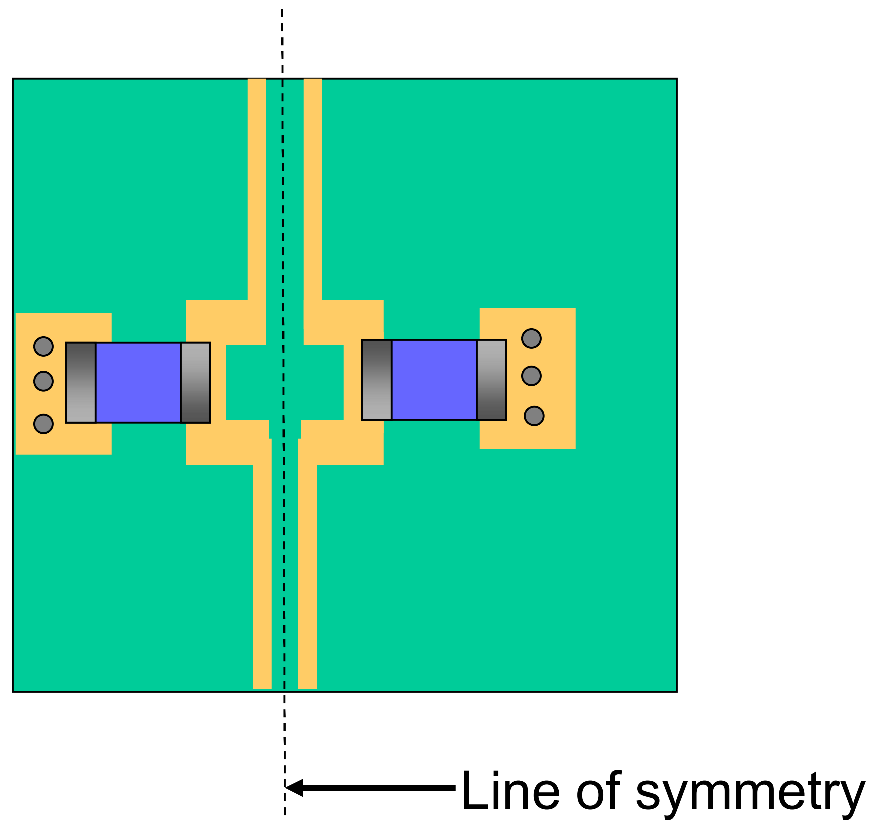
Maintaining Balance

- One of the key requirement to suppress Common-Mode component in a differential signaling system is to maintain balanced – both physical and electrical (timing, slew rate and amplitude of the driving voltage).
- Thus each trace has to have similar geometrical structure, ‘see’ similar ‘scenery’, and be of the same length from the differential buffer to the differential amplifier at the receiver.   This has to be kept in mind by the PCB layout engineer.
  - Same trace cross section.
  - Same length.
  - Sufficiently far from other metallic strucutre (same scenery).



Maintaining Balance – Isolation and Termination

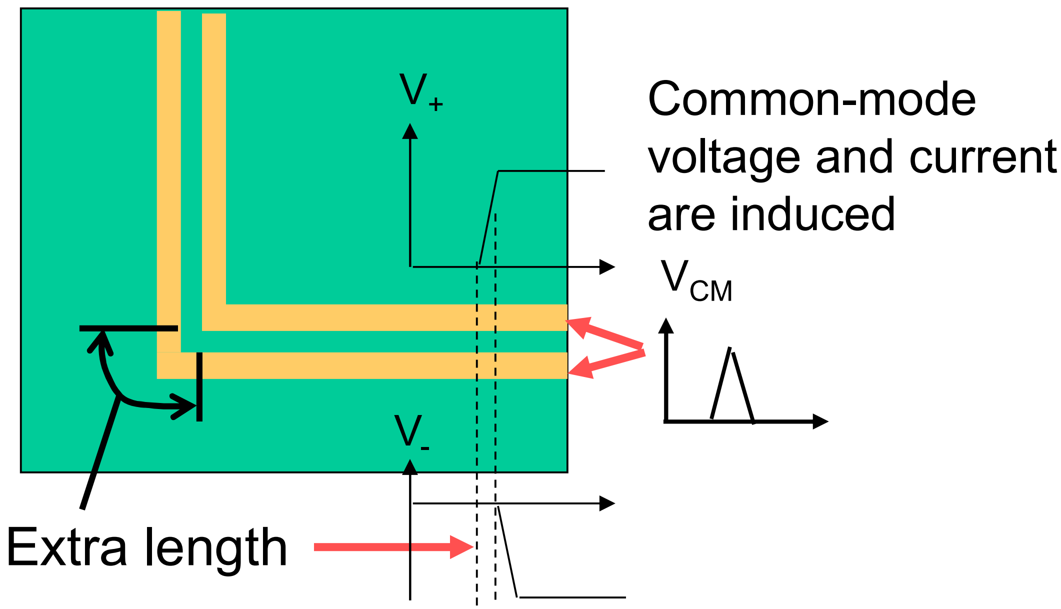


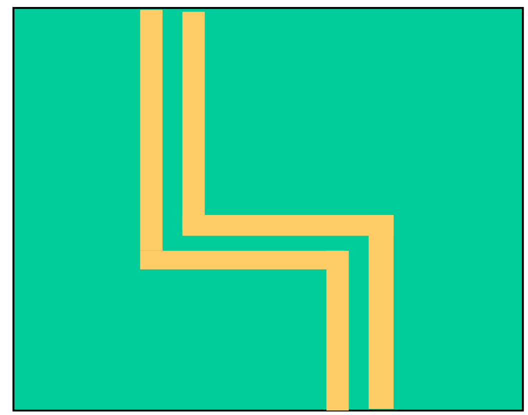


Nearby metallic object should be sufficiently far, typically 3S from either traces.

Maintaining Balance - Unwanted Delay (1)

- A bend on differential trace introduces extra delay (skew).
- This can be countered by adding another skew in the opposite line.
- The bend will also introduce differential reflection as in single-ended case.



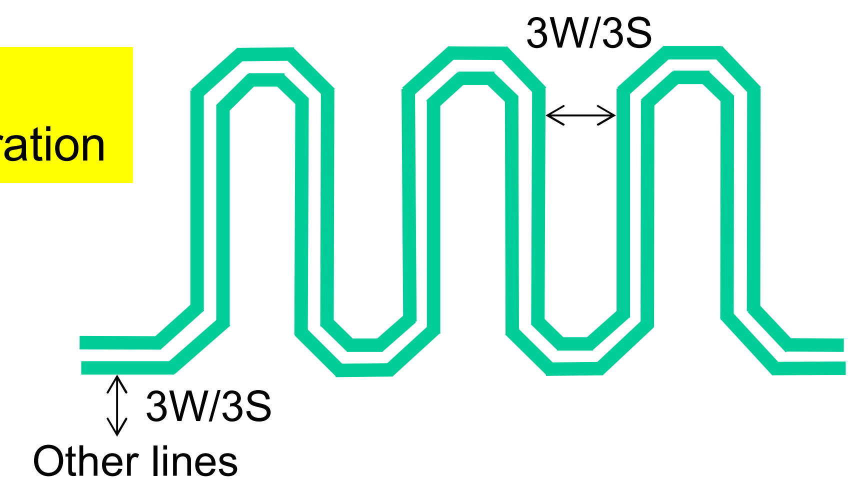


Adding another bend to balance off the skewing. Shape of the bend will affect differen -tial reflection.

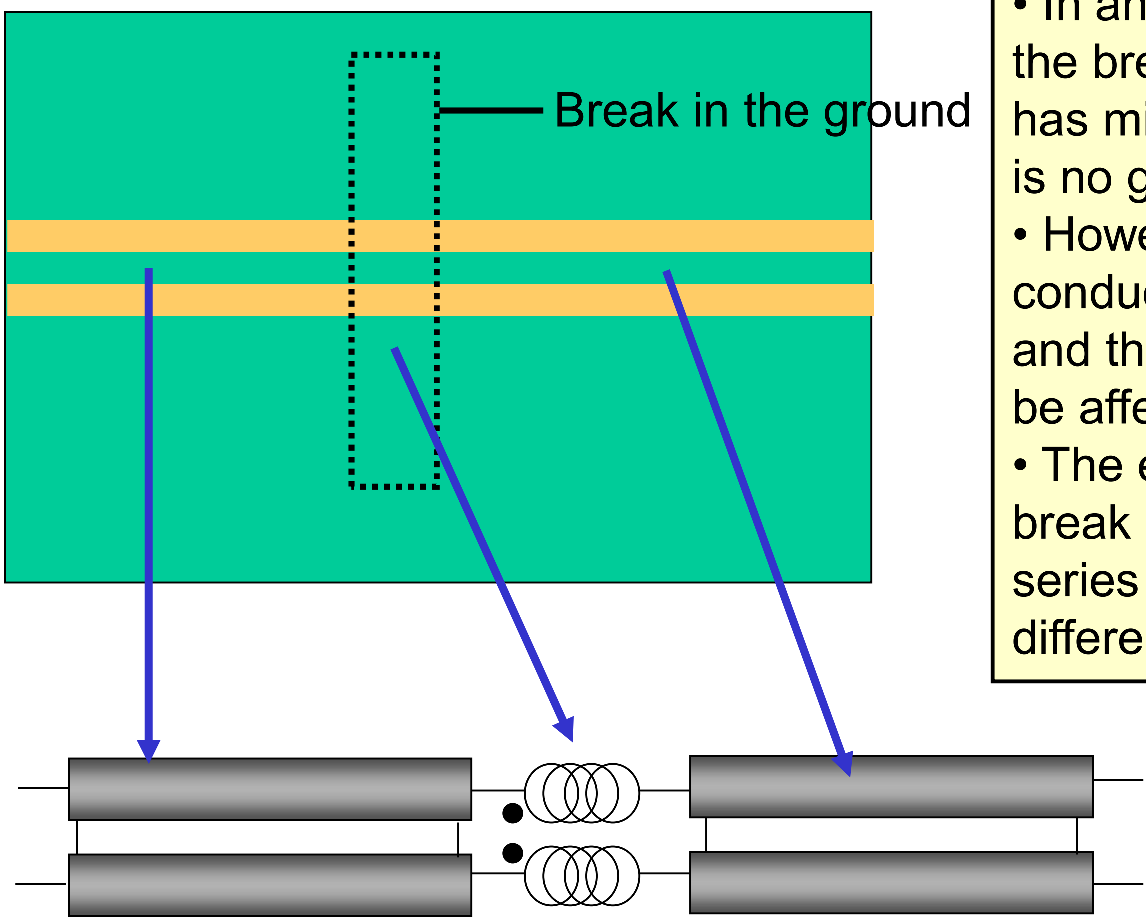
Serpentine Routing

- Timing skew control is usually accomplished by introducing extra "turning" or "serpentine" routing to the traces.
- For single-end lines (W), keep at least 3W separation between serpentine traces.
- For differential pairs (W/S), keep at least 3W/3S (whichever larger) separation between serpentine traces.

W = trace width
S = Edge-to-edge separation



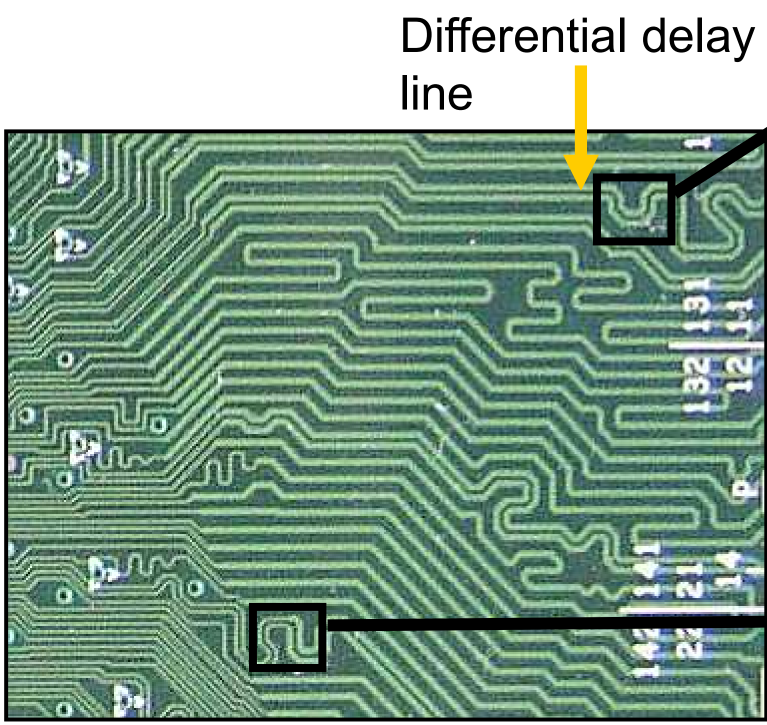
Effect of Ground Break on Differential Traces

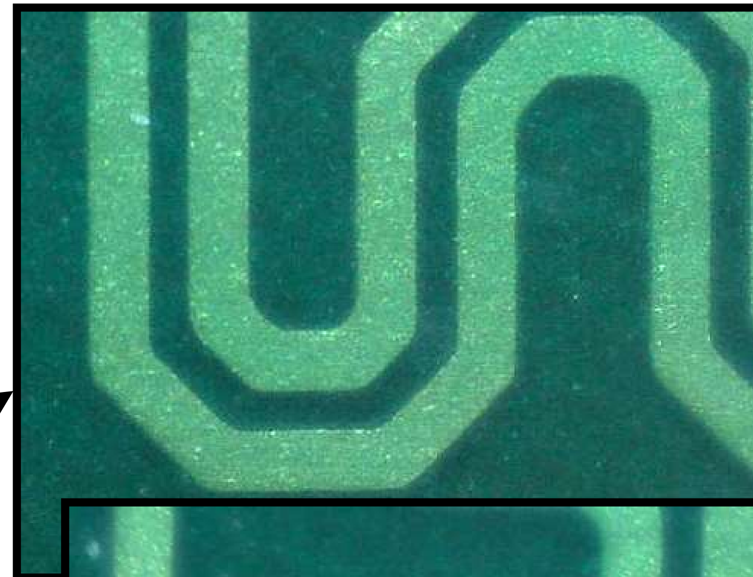


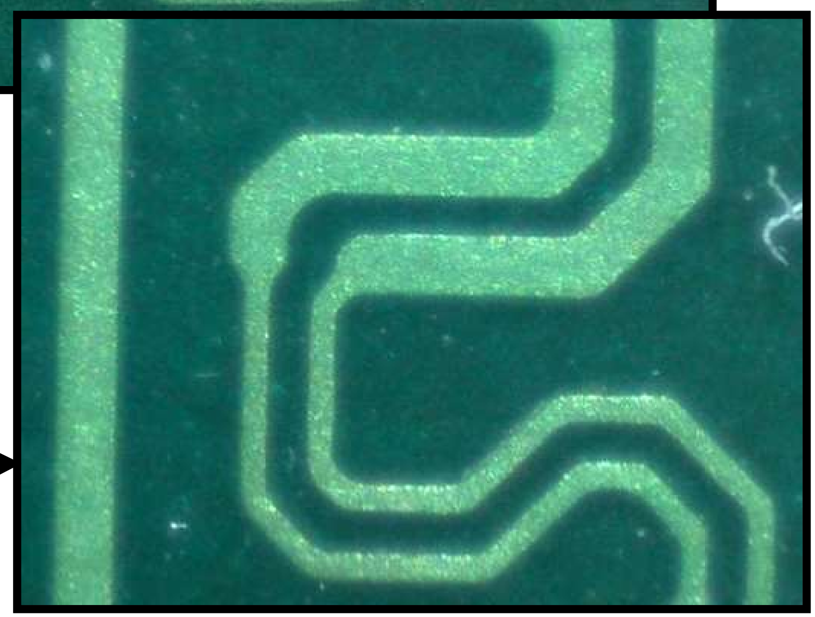
- In an ideal differential line, the break in ground plane has minimal effect since there is no ground current.
- However the absence of ground conductor do affect the EM field and the differential impedance will be affected.
- The electrical impact of a ground break is like having coupled series inductor inserted into the differential line.

Example 5.1 – Photomicrograph of Differential or Coupled Microstrip Lines

- A snap shot of a computer motherboard is taken below, with and without optical magnification (60X).

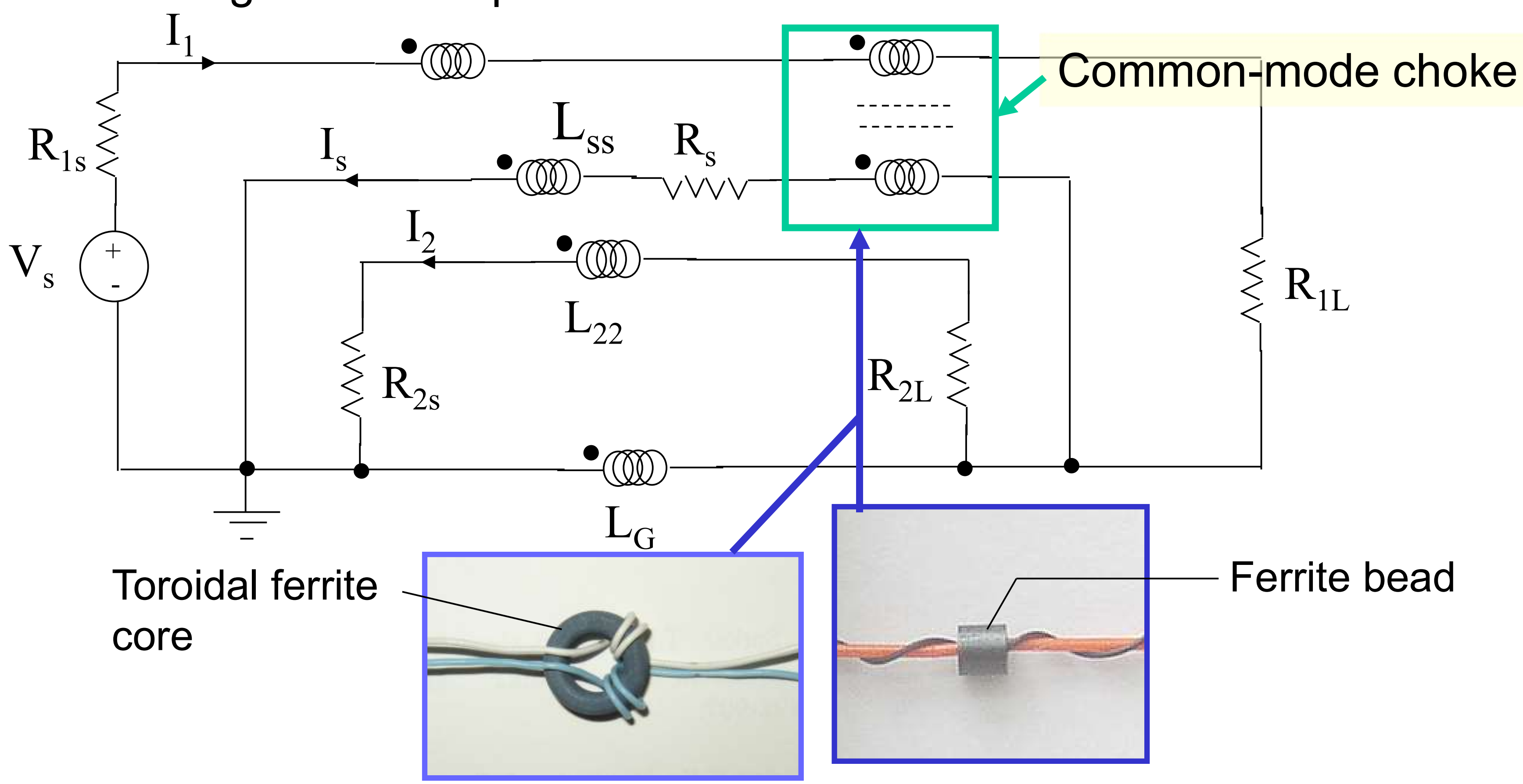






Using Common-Mode Choke to Suppress Common-Mode Signal

- A common-mode choke will present high impedance to CM currents while having minimal impact on DM current.



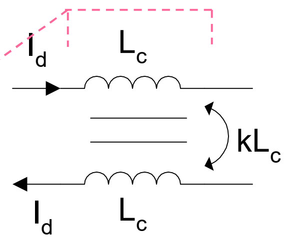
Two simple DIY common-mode chokes

Extra

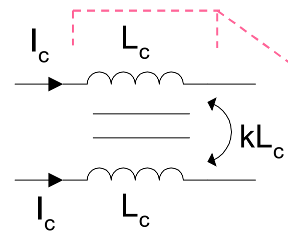
Common-Mode Choke Impedance

Differential-mode Impedance:

$$Z_{DM} = \frac{I_d \omega (L_c - M)}{I_d} = \omega (L_c - kL_c)$$



differential mode current



common mode current

Common-mode Impedance:

$$Z_{CM} = \frac{I_c \omega (L_c + M)}{I_c} = \omega (L_c + kL_c)$$

- Increases common-mode impedance without affecting the differential-mode impedance.
- The two inductors are tightly coupled (like transformer). The pair of wires is normally wound on a ferrite core for optimum frequency response.
- Coupling coefficient, k, is close to 1, thus $Z_{DM} \approx 0$ and $Z_{CM} \approx 2\omega L_c$

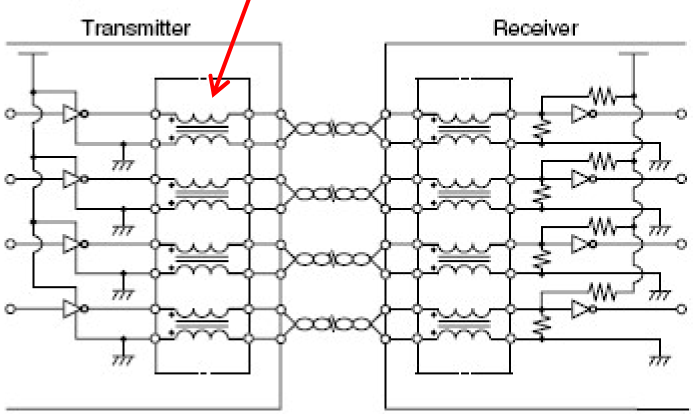
$$\boxed{Z_{CM} >> Z_{DM}}$$

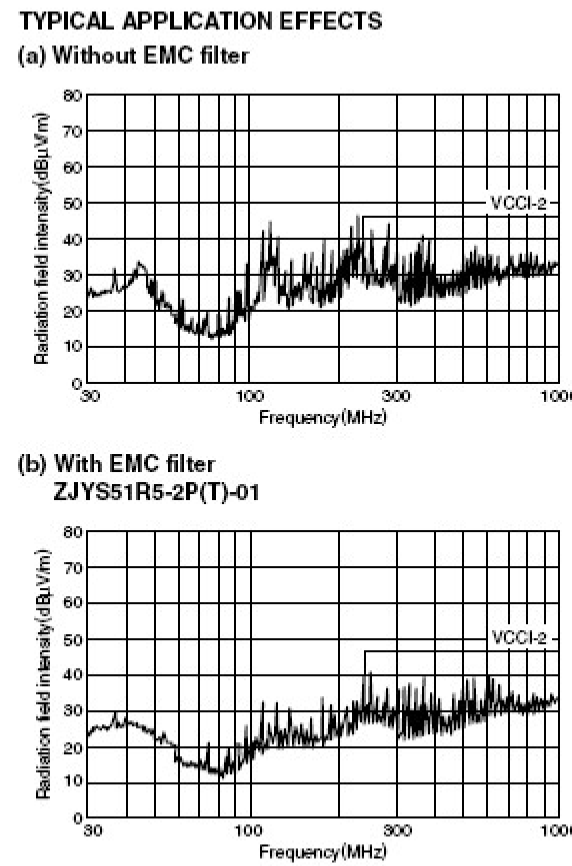
Example of Commercial Common-Mode Choke for Differential Signalling

- An example of commercial CM Choke from TDK Corp.

TYPICAL APPLICATION

An application example showing how radiation noise is prevented when transmitter and receiver are connected via twisted pair cabling.





5.6 – Signal Propagation and Termination For Differential Signaling

Introduction

- Since any arbitrary pair of electrical signals can be decomposed into CM and DM components, we can analyzed the propagation effects of electrical charge using the perspective of CM and DM circuits.
- The propagation effects of electrical charges in CM and DM circuits can be handled in the usual manner using the principles of single-ended circuit.
- Here instead of using the characteristic impedance of a single-ended transmission line, we use the common-mode and differential-mode characteristic impedance (Z_{CM} and Z_{DM}).
- All the concepts of charge propagation such as phase velocity, reflection, attenuation etc apply, except it is now for CM and DM circuits individually.
- This will be illustrated in the following slides.

Differential and Common-mode Reflection Coefficient

- The formula for reflection coefficient Γ applies equally well to differential signaling. In this case the incident and reflected voltages are considered independently for differential-mode and common-mode voltages.

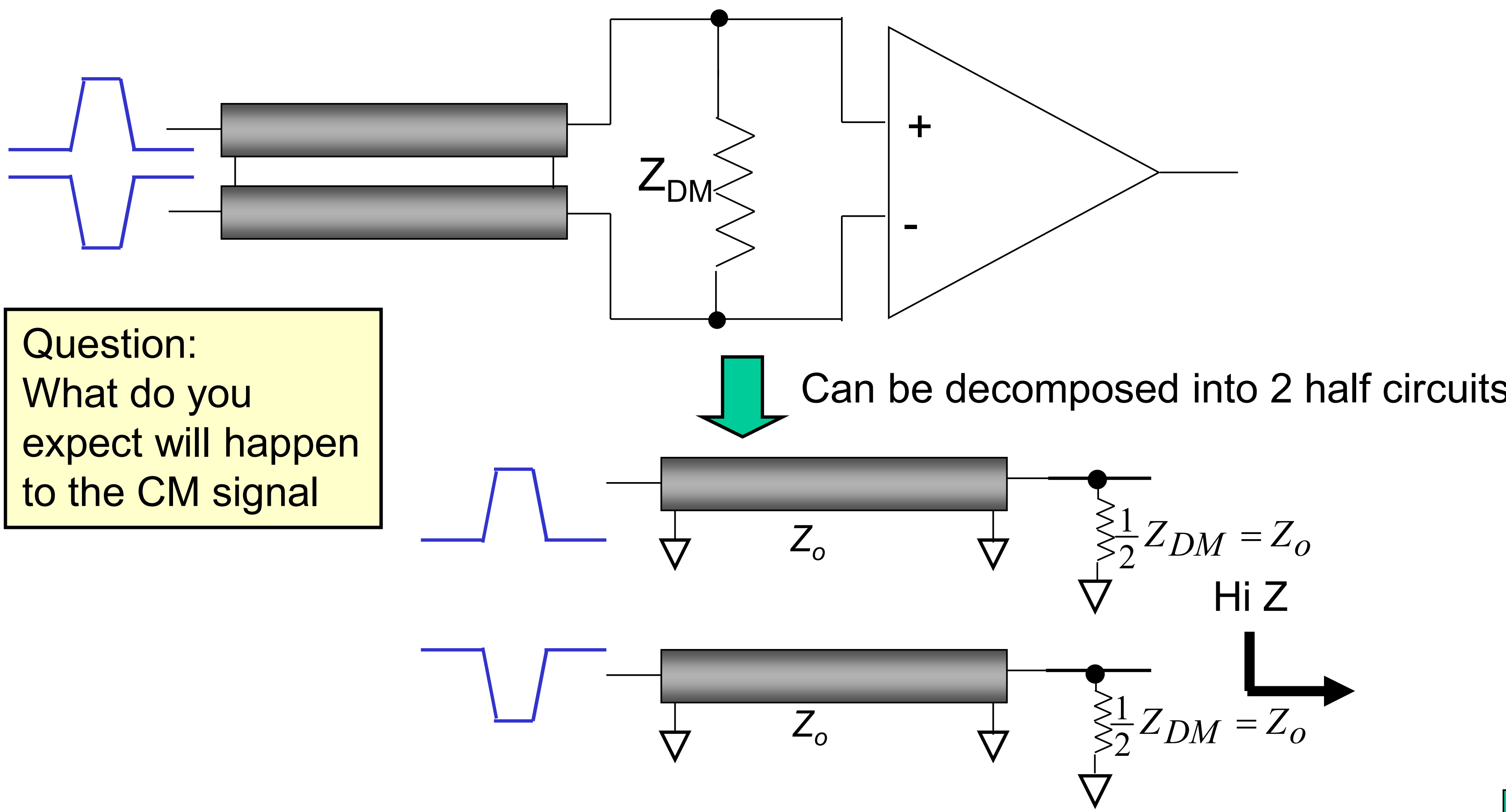
$$\Gamma_{L(diff)} = \frac{Z_{L(diff)} - Z_{DM}}{Z_{L(diff)} + Z_{DM}} = \frac{V_d^{-}}{V_d^{+}} \qquad \textbf{\textit{(6.1a)}}$$

$$\Gamma_{L(com)} = \frac{Z_{L(com)} - Z_{CM}}{Z_{L(com)} + Z_{CM}} = \frac{V_c^{-}}{V_c^{+}} \qquad \textbf{\textit{(6.1b)}}$$

- Thus rules for handling discontinuities in single transmission line also apply to differential traces.

Termination for Differential Signaling (1)

- Termination for differential signal only…



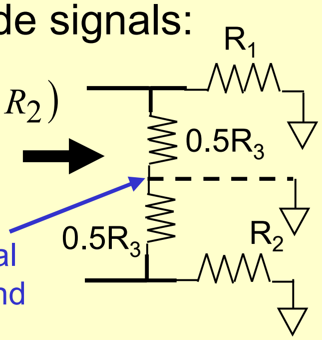
Question:
What do you expect will happen to the CM signal

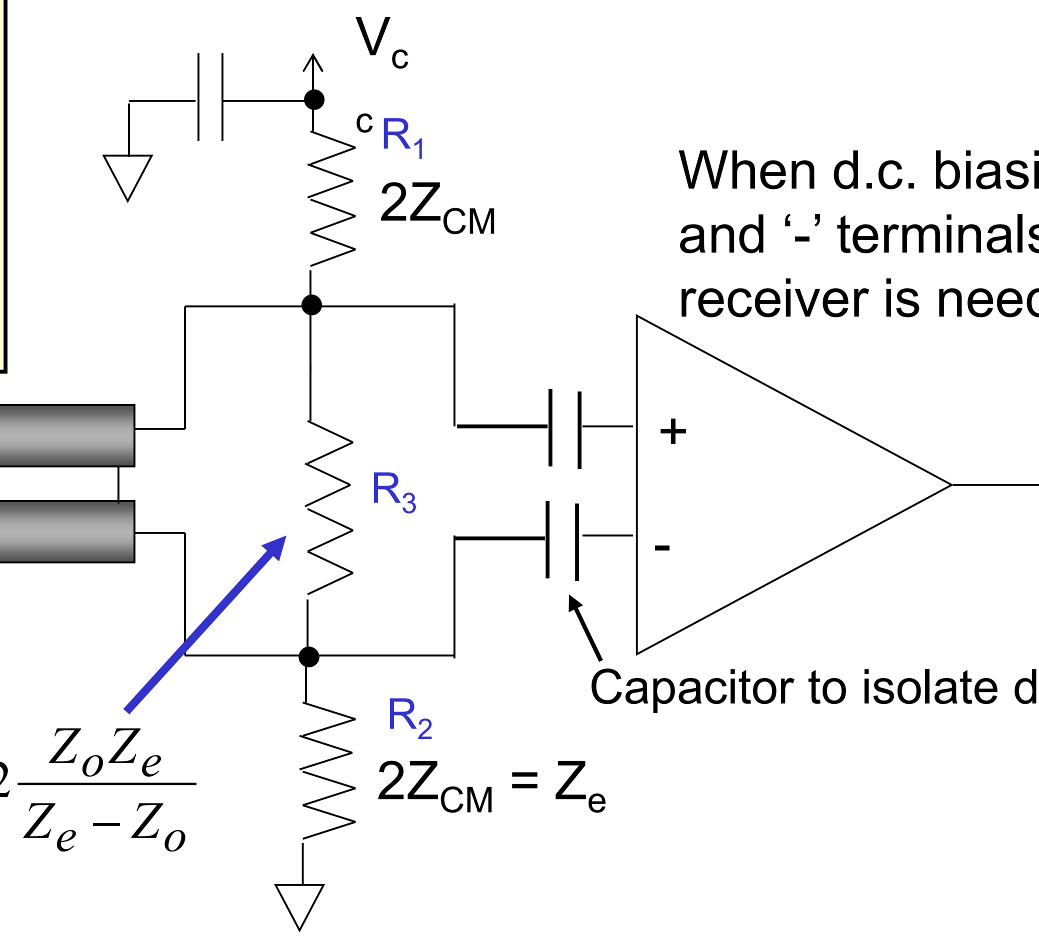
Termination for Differential Signaling (2)

- Termination for both differential and common-mode signals…

Note: From the perspective of odd mode signals:

$$R_{in} = R_3 // (R_1 + R_2) = \frac{R_3(R_1+R_2)}{R_1+R_2+R_3}$$





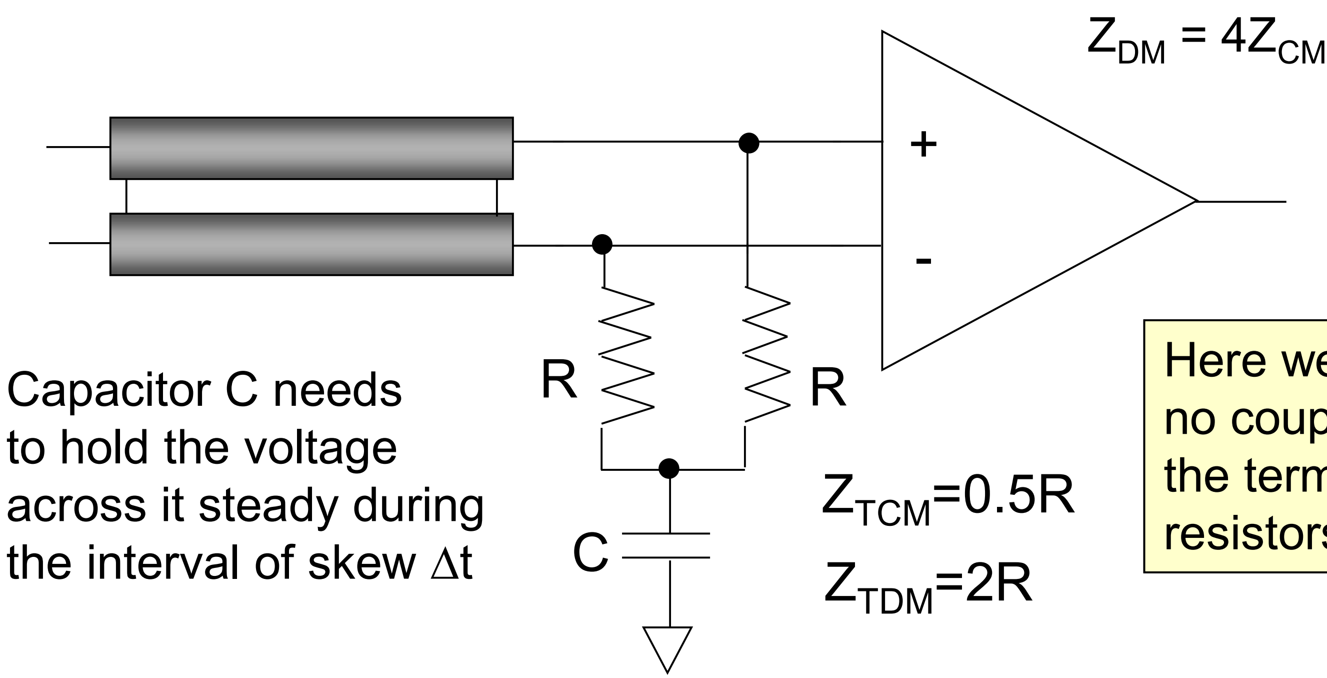
When d.c. biasing of '+' and '-' terminals at the receiver is needed.

Capacitor to isolate d.c. voltage

$$R_3 = \frac{4Z_{CM}Z_{DM}}{4Z_{CM} - Z_{DM}} = 2\frac{Z_o Z_e}{Z_e - Z_o}$$

Termination for Differential Signaling (3)

- Termination for both differential and common-mode signals…

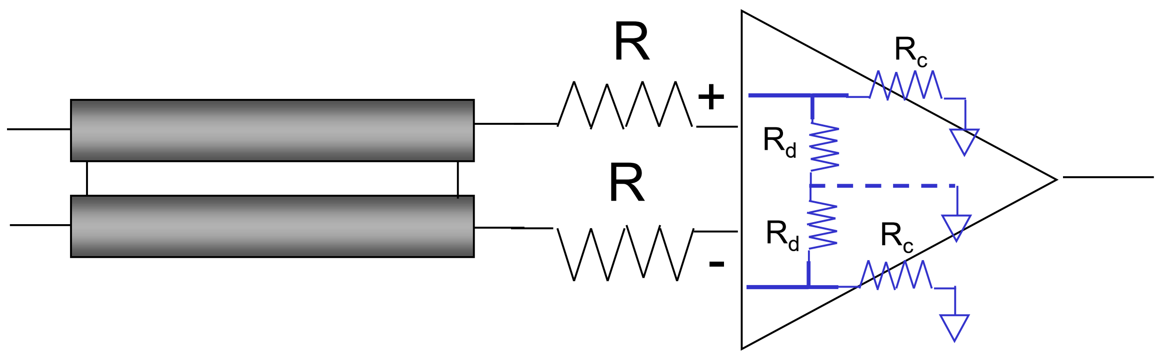


Here we are assuming no coupling between the termination resistors.

In other words make $Z_e = Z_o = R$!!!

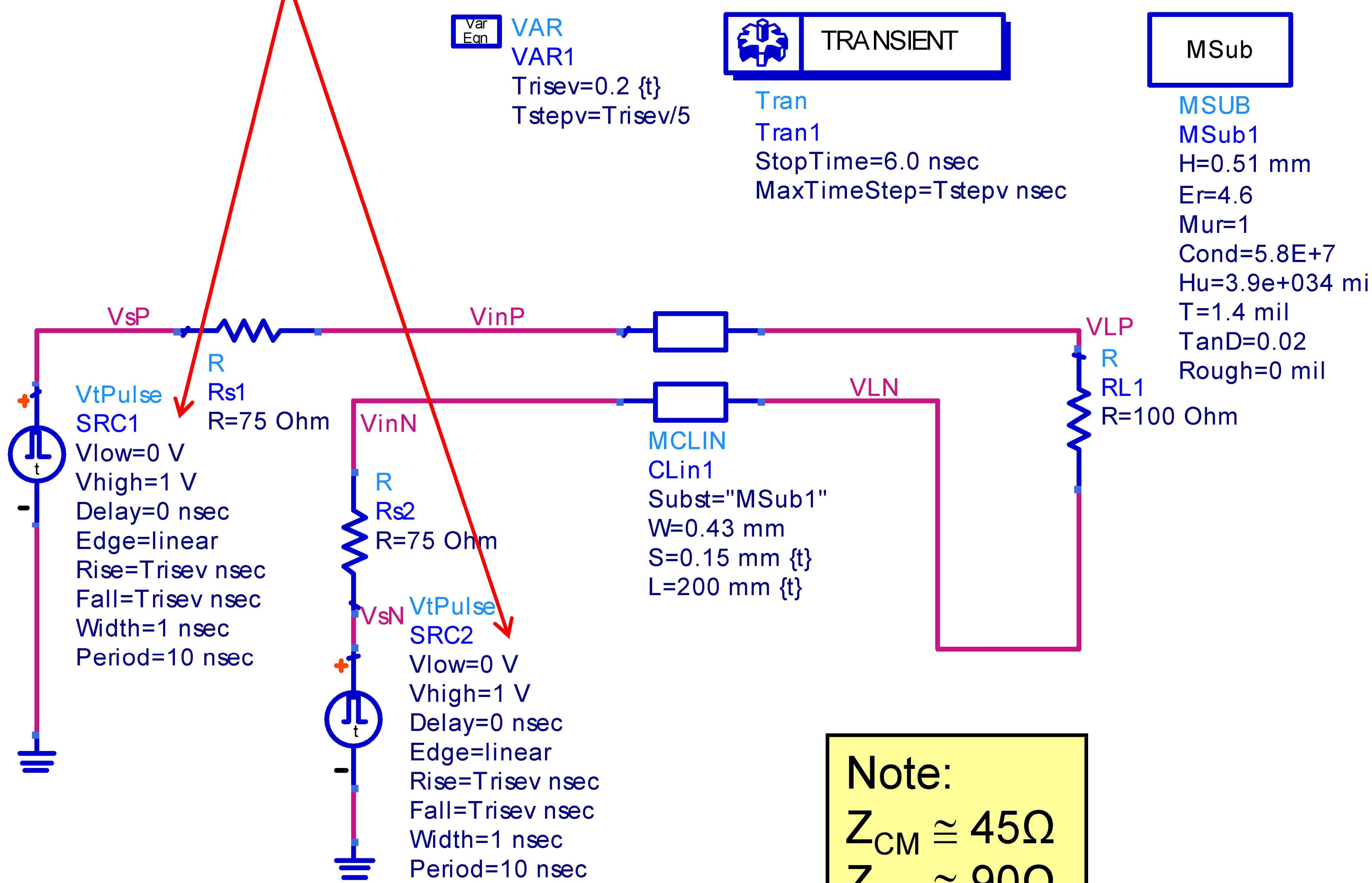
Series Termination for Differential Signaling

- Termination for both differential and common-mode signals…



Exercise 6.1 – Differential Transmission Line Simulation

- Setup for pure CM excitation:

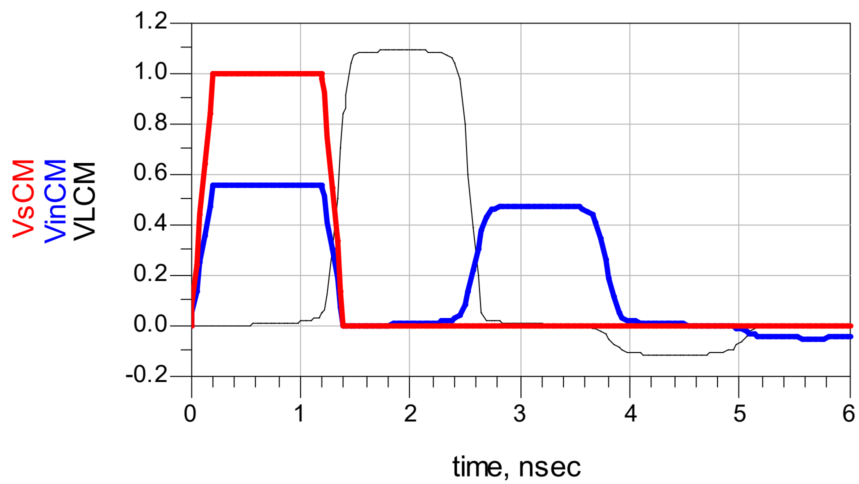


Note:
$Z_{CM} \cong 45\Omega$
$Z_{DM} \cong 90\Omega$

Exercise 6.1 Cont…

Eqn VLDM=VLP-VLN

Eqn VLCM=0.5*(VLP+VLN)

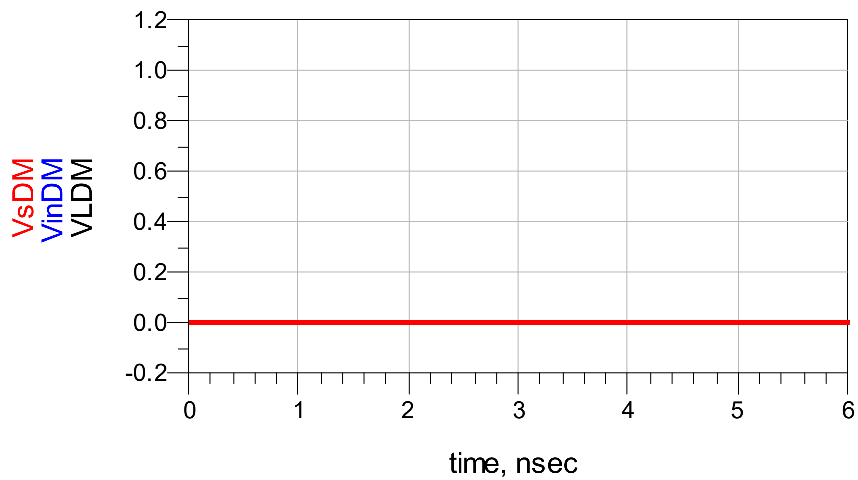


Eqn VinDM=VinP-VinN

Eqn VinCM=0.5*(VinP+VinN)

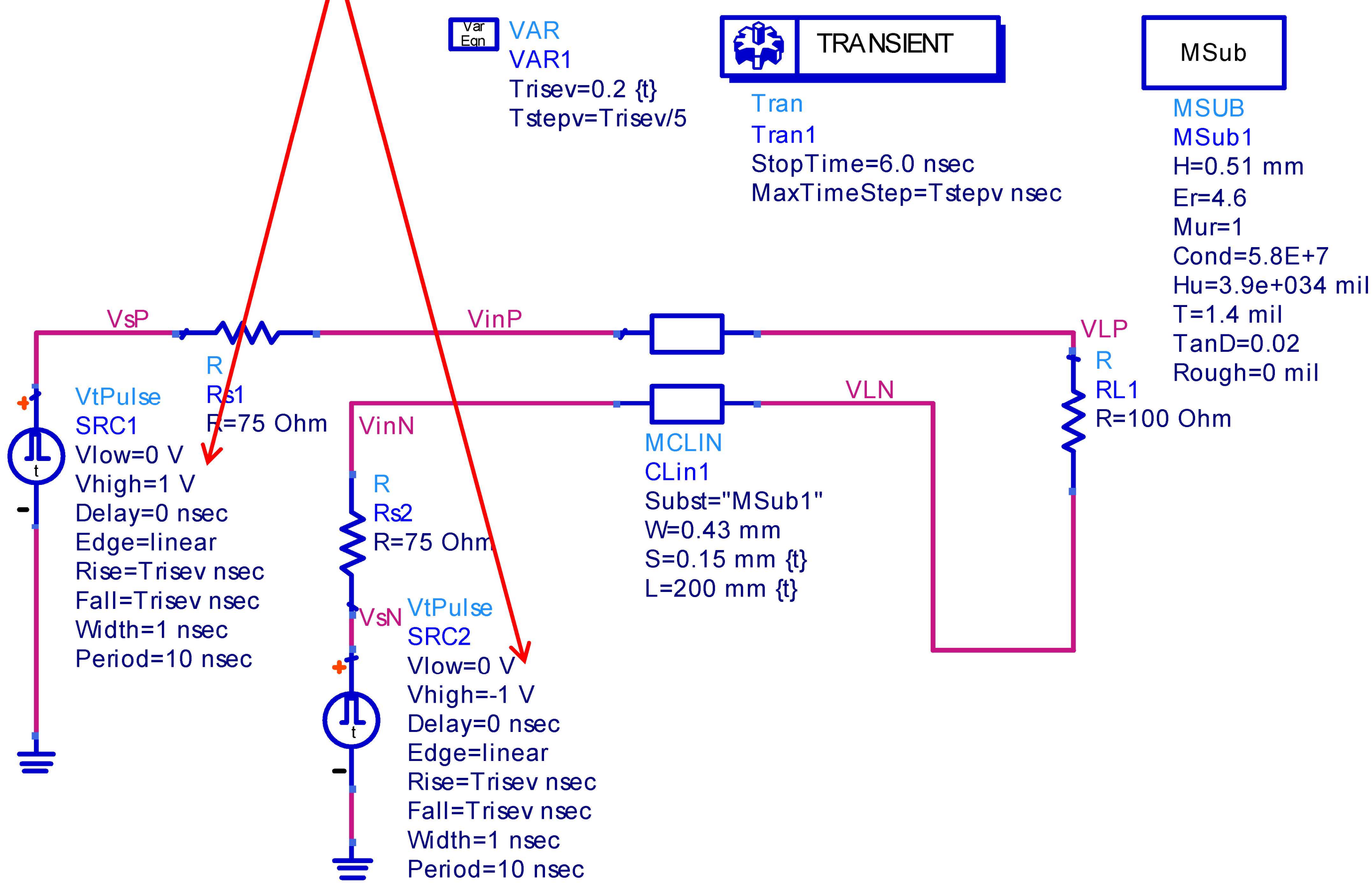
Eqn VsDM=VsP-VsN

Eqn VsCM=0.5*(VsP+VsN)



Exercise 6.1 Cont…

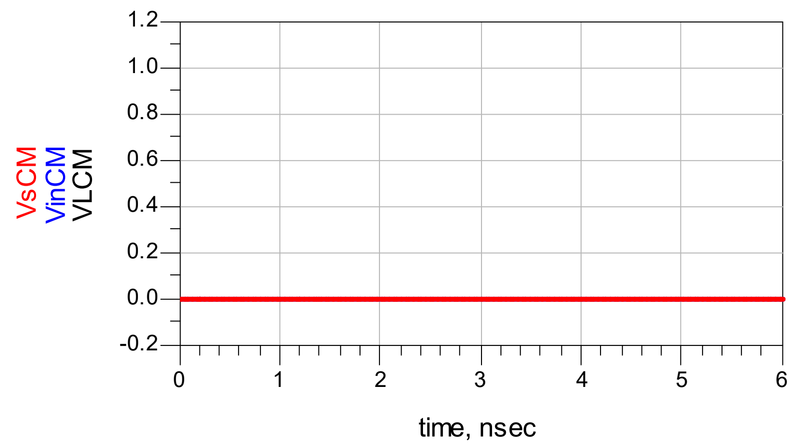
- Setup for pure DM excitation.



Exercise 6.1 Cont…

Eqn VLDM=VLP-VLN

Eqn VLCM=0.5*(VLP+VLN)

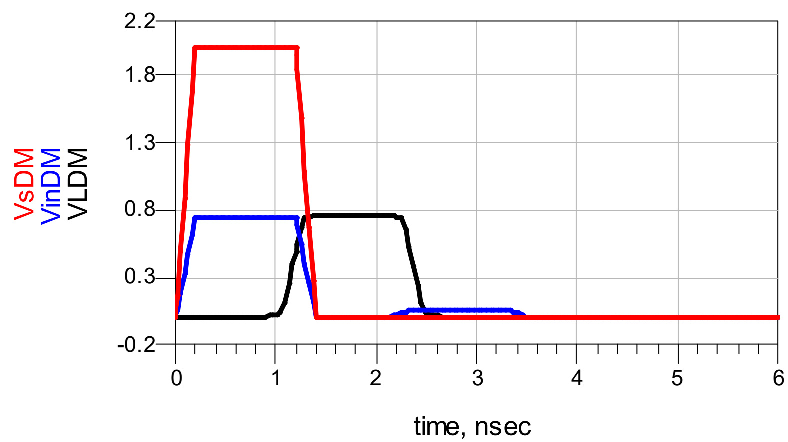


Eqn VinDM=VinP-VinN

Eqn VinCM=0.5*(VinP+VinN)

Eqn VsDM=VsP-VsN

Eqn VsCM=0.5*(VsP+VsN)



Key Learning for Part 5

- Why differential signaling is needed?
- Physical and electrical requirements for differential signaling.
- Key properties of differential signaling – minimal ground return current, less susceptible to electromagnetic interference, do not radiate as much as single-ended signaling.
- Benefits of differential signaling – able to send signal at higher rate.
- Differential impedance – V_t over I_t for differential and common mode propagating voltages & currents.
- Reflection coefficients for differential signals.
- Procedures for designing differential transmission lines.
- Termination schemes and layout rules for differential transmission line circuits.