Part 4 –PCB LAYOUT RULES FOR SIGNAL INTEGRITY

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References

- [1] H. Johnson, M. Graham, "High-speed digital design – A handbook of black magic", Prentice-Hall, 1993.
- [2] D.M. Pozar, "Microwave engineering", 2nd edition, 1998 John-Wiley & Sons.
- [3] M. I. Montrose, "EMC and printed circuit board – design theory and layout made simple", IEEE Press, 1999.
- [4] T. C. Edwards, "Foundations for microstrip circuit design", 2nd edition, 1992 John-Wiley & Sons.
- [5] T. C. Edwards, "Foundations of interconnect and microstrip design", 3rd edition, 2000, John-Wiley & Sons.
- [6] H. Howe, "Stripline circuit design", 1974, Artech House.
- [7] I. Bahl, P. Bhartia, "Microwave solid state circuit design", 2nd edition, 2003, John-Wiley & Sons.
- [8] http://pesona.mmu.edu.my/~wlkung/Master/mthesis.htm
- [9] S. H. Hall, G. W. Hall, J. A. McCall, "High-speed digital system design", 2000, John-Wiley & Sons.
- [10] T. Williams, "EMC for product designers", 2001, Butterworth-Heinemann.
- [11] H. W. Ott, "Noise reduction techniques in electronic systems", 1988, John-Wiley & Sons.
- [12] D. Brooks, "Signal integrity issues and printed circuit board design", 2003, Prentice Hall.

Introduction

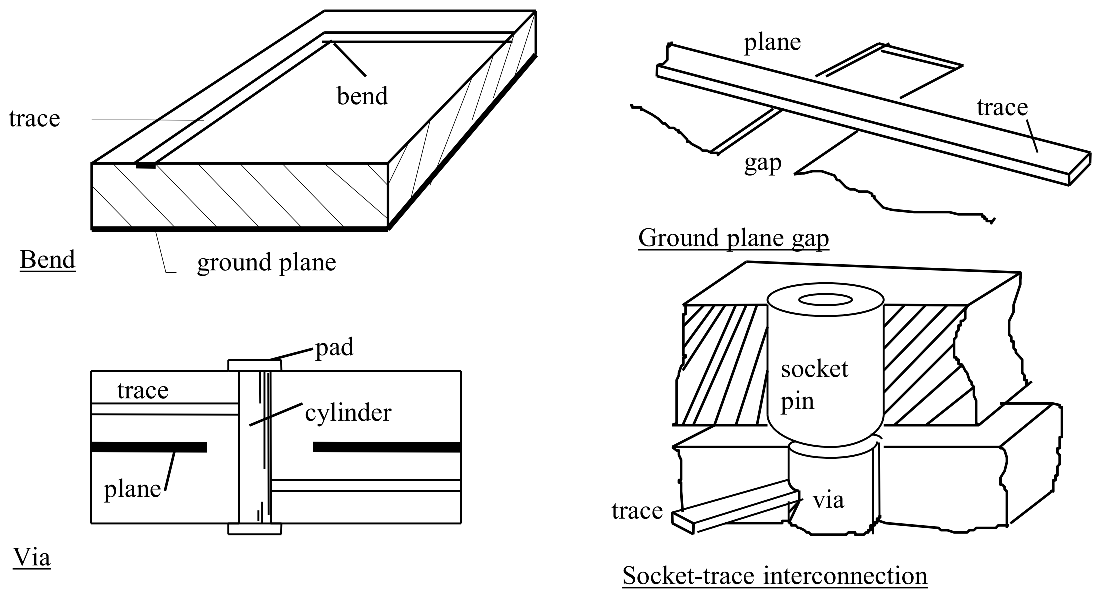
- By PCB layout we imply the designing the pattern or the shape of the conducting structures on the PCB, stacking up the various layers of the PCB, placement of components and vias.
- The purpose of a good PCB layout tends to achieve the following objectives:
  - **(A) Provide a means of sending electrical energy from one component to the other with as little 'obstacle' as possible**.
  - **(B) Provide sufficient isolation such that electrical signal in one path does not affect other, and vice versa**. This means we want to reduce electric/magnetic field coupling, and also common impedance coupling.
- We can achieve objective **A** by reducing unnecessary reflections or distortion and loading along the signal path for high-speed signal.
- We can achieve objective **B** by providing proper 'grounding', noise suppression on the power delivery system of the circuit (and also sufficient spatial separation) and shielding.

4.1 – Discontinuities in Striplines and Traces

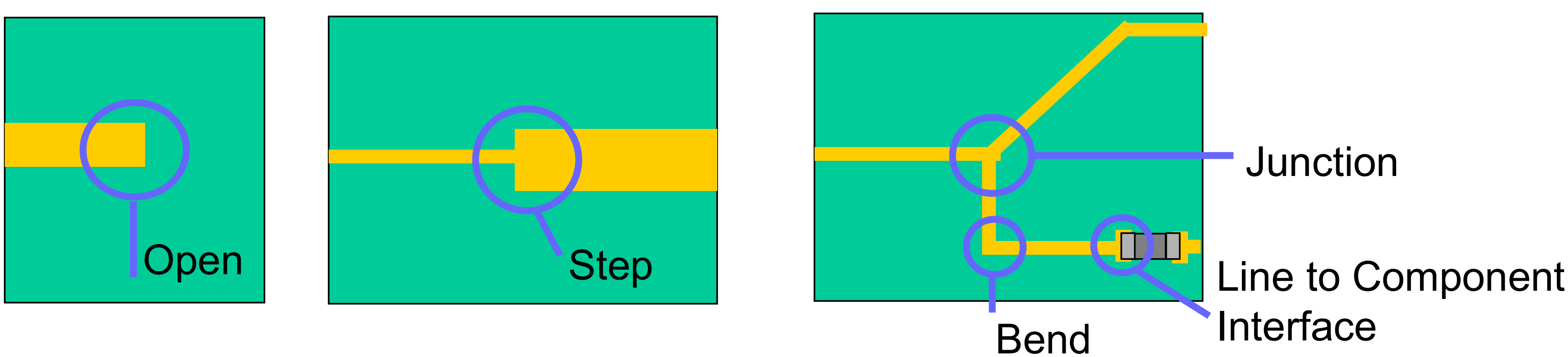
Practical Transmission Line Design and Discontinuities

- Discontinuities in Tline are changes in the Tline geometry to accommodate layout and other requirements on the printed circuit board.
- Virtually all practical distributed circuits, whether in waveguide, coaxial cables, microstrip line etc. must inherently contains discontinuities. A straight uninterrupted length of waveguide or Tline would be of little engineering use.
- The following discussion consider the effect and compensation for discontinuities in PCB layout. This discussion is restricted to TEM or quasi-TEM propagation modes.

Transmission Line Discontinuities Found in PCB (1)

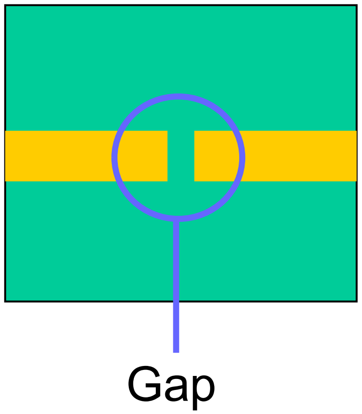


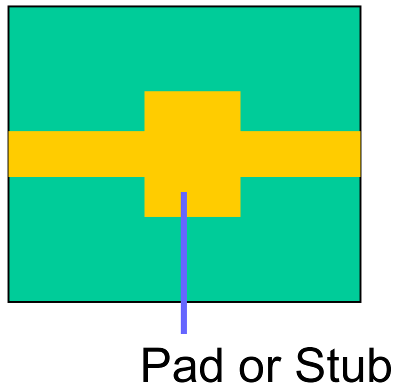
Here we illustrate the discontinuities using microstripline. Similar structures apply to other transmission line configuration as well.

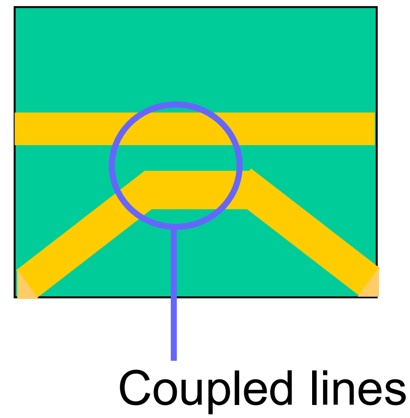


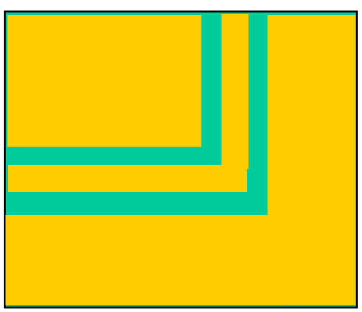
Transmission Line Discontinuities Found in PCB (2)

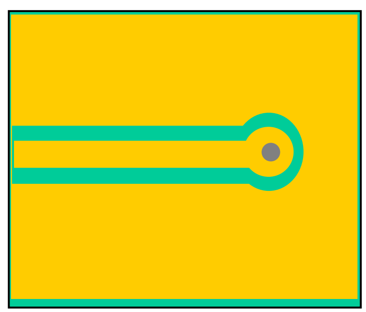
- Further examples of microstrip and co-planar line discontinuities.











Examples of bend and via on co-planar Tline.

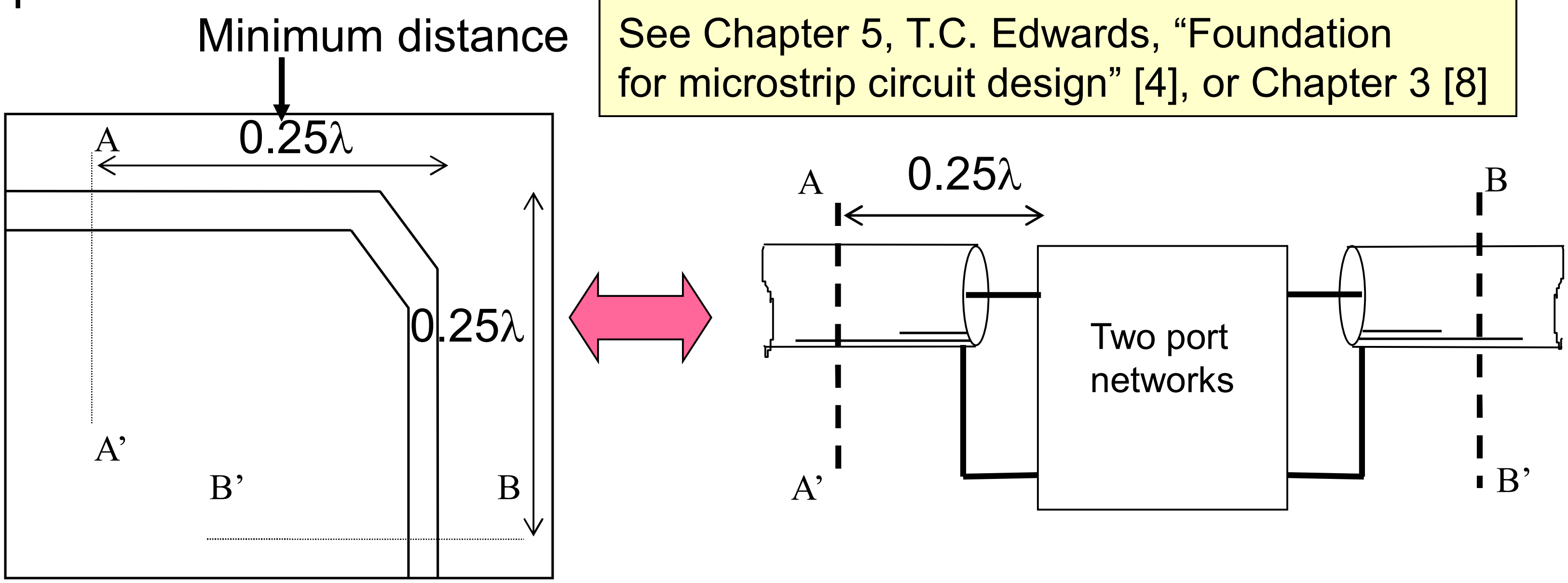
Discontinuities and EM Fields (1)

- Introduction of discontinuities will distort the uniform EM fields present in the infinite length Tline. Assuming the propagation mode is TEM or quasi-TEM, the discontinuity will create a multitude of higher modes (such as TM_{11} , TM_{12} , TE_{11} , …) in its vicinity in order to fulfill the boundary conditions (Note - there is only one type of TEM mode !!).
- Most of these induced higher order modes are evanescent or non-propagating as their cut-off frequencies are higher than the operating frequency of the circuit. Thus the fields of the higher order modes are known as local fields.
- The effect of discontinuity is usually reactive (the energy stored in the local fields is returned back to the system) since loss is negligible.
- The effect of reactive system to the voltage and current can be modeled using LC circuits (which are reactive elements).
- For TEM or quasi-TEM mode, we can consider the discontinuity as a 2-port network containing inductors and capacitors.

Discontinuities and EM Fields (2)

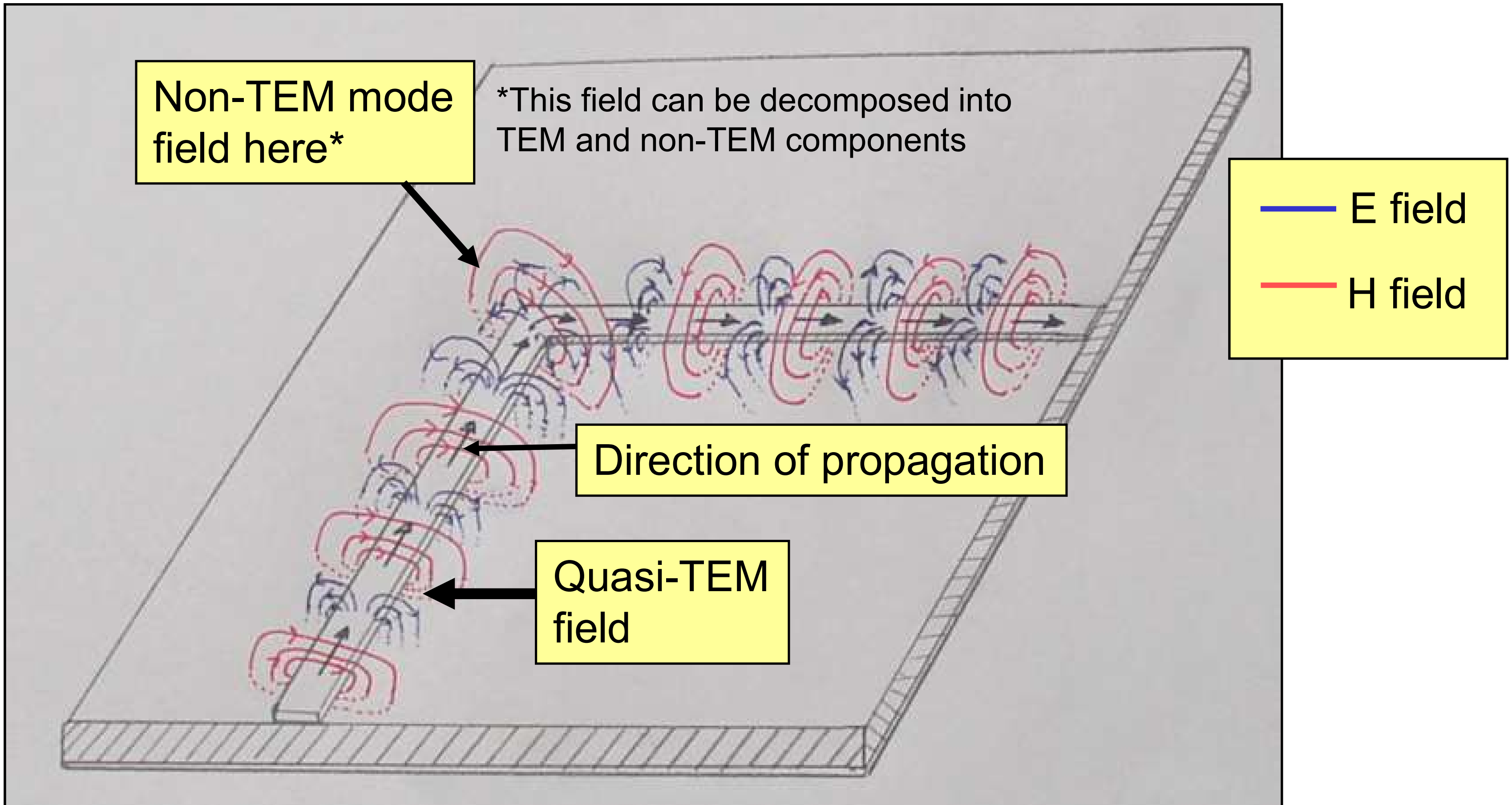
- Modeling a discontinuity using circuit theory element such as RLCG is a good approximation for operating frequency up to 6 -20 GHz. This upper limit depends on substrate thickness and size of discontinuity.
- The smaller the dimension of the discontinuity as compared to the wavelength, the higher will be the upper usable frequency.
- As a example, the 2-port model for a microstrip bend is usually accurate up to 10 GHz.

See Chapter 5, T.C. Edwards, “Foundation for microstrip circuit design” [4], or Chapter 3 [8]



Discontinuities and EM Fields (3)

- For instance for a microstrip bend, a snapshot of the EM fields at a particular instant in time:



Methods of Obtaining Equivalent Circuit Model for Discontinuities (1)

- **3 Typical approaches…**
- **Method 1**: Analytical solution - see Chapter 4, reference [3] on Modal Analysis for waveguide discontinuities.
- **Method 2**: Numerical methods, for example:
  - Method of Moments (MOM).
  - Finite Element Method (FEM).
  - Finite Difference Time Domain Method (FDTD).
  - And many others.

Agilent's Momentum

Ansoft's HFSS

•CST's Microwave Studio

•Sonnet

- Numerical methods are used to find the quasi-static EM fields of a 3D model containing the discontinuity. The EM field in the vicinity of the discontinuity is split into TEM and non-TEM fields. LC elements are then associated with the non-TEM fields using formula similar to (3.1) in Part 3.

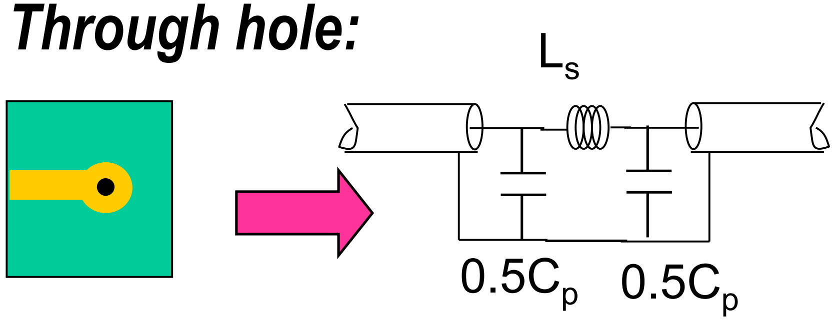
Methods of Obtaining Equivalent Circuit Model for Discontinuities (2)

- **Method 3**: Fitting measurement with circuit models. By proposing an equivalent circuit model, we can try to tune the parameters of the circuit elements in the model so that frequency/time domain response from theoretical analysis and measurement match.
- Measurement can be done in time domain using time-domain reflectometry (TDR) and frequency domain measurement using a vector network analyzer (VNA) (see Chapter 3 of Ref [4] for details).

4.2 - Practical Striplines Discontinuities and Models

Microstrip Line Discontinuity Models (1)

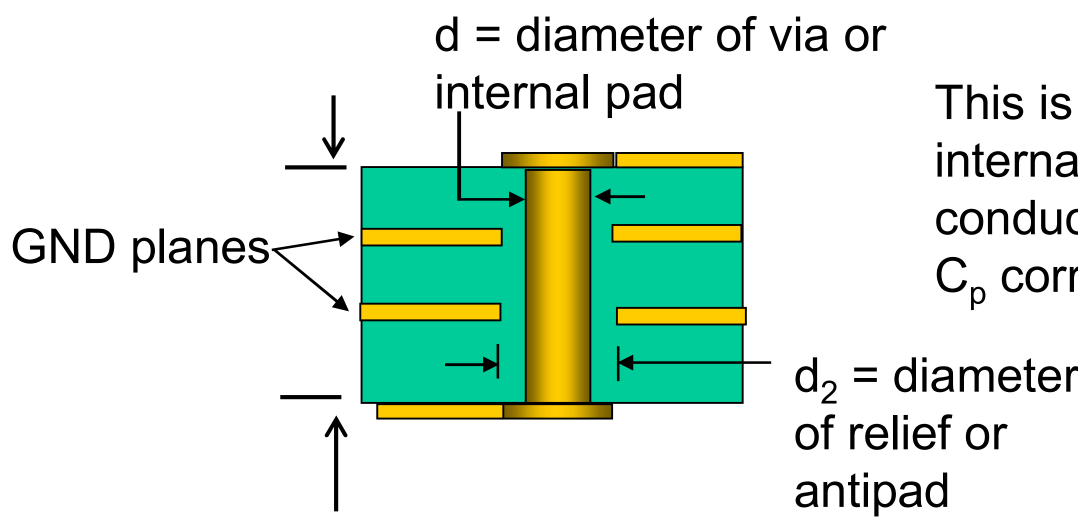
Through hole:



$$L_s \cong 0.2h\left(\ln\left(\frac{4h}{d}\right)+1\right) \qquad \textbf{\textit{(2.1a)}}$$

$$C_p \cong 0.056\frac{\varepsilon_r hd}{d_2-d}N \qquad \textbf{\textit{(2.1b)}}$$

This is the capacitance between the via and internal plane. If there are multiple internal conducting planes, then there should be one C_p corresponding to each internal plane.

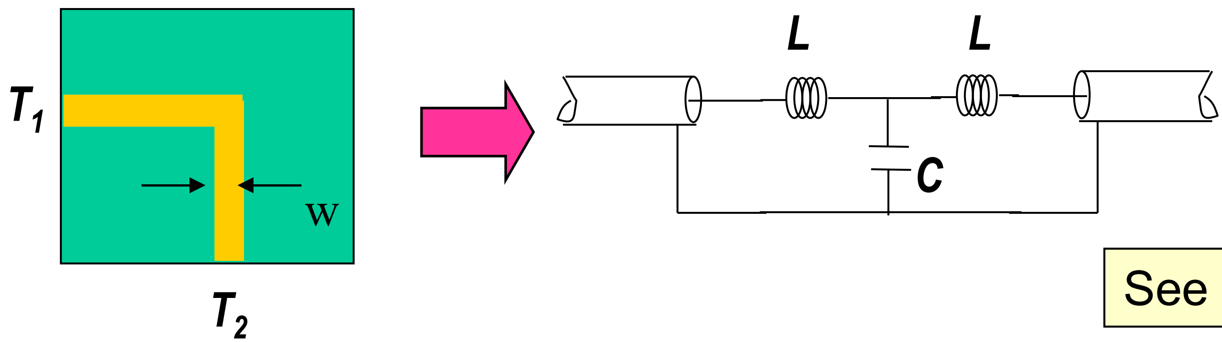


Cross section of a Via

L_s in nH
C_p in pF
h in mm
d and d_2 in mm
ε_r = dielectric constant of PCB
N = number of GND planes

Microstrip Line Discontinuity Models (2)

90^o Bend:



See Edwards [4], Chapter 5

Approximate quasi-static expressions for L_1, L_2 and C:

$$\frac{C}{w} = \frac{(14\varepsilon_r + 12.5)\frac{w}{d} - (1.83\varepsilon_r - 2.25)}{\sqrt{w/d}} \text{ pF/m} \quad \text{for} \quad \frac{w}{d} < 1$$

$$\frac{C}{w} = (9.5\varepsilon_r + 1.25)\frac{w}{d} + 5.2\varepsilon_r + 7.0 \text{ pF/m} \quad \text{for} \quad \frac{w}{d} > 1$$

(2.2a)

$$\frac{L}{d} = 100\left[4\sqrt{\frac{w}{d}} - 4.21\right] \text{ nH/m}$$

(2.2b)

ε_r = dielectric constant of substrate, assume non-magnetic.
d = thickness of dielectric in meter.

Example 2.1 - Microstrip Line Bend

- For a 90° microstrip line bend, with w = 0.92mm, d = 0.51mm, ε_r = 4.6 (non-magnetic substrate). Find the value of L and C for the bend.

$$\frac{C}{w} = (9.5\times 4.6+1.25)1.8+5.2\times 4.6+7.0$$

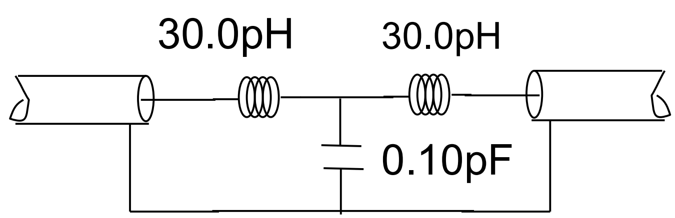
$$=111.83\ \text{pF/m}$$

$$\frac{w}{d}=1.834$$

$$\Rightarrow \text{C}=111.83\times 0.00092=0.10\text{pF}$$

$$\frac{L}{d}=100\left[4\sqrt{1.8}-4.21\right]=115.66\ \text{nH/m}$$

$$\Rightarrow \text{L}\cong 60\text{pH}$$



At 1GHz:

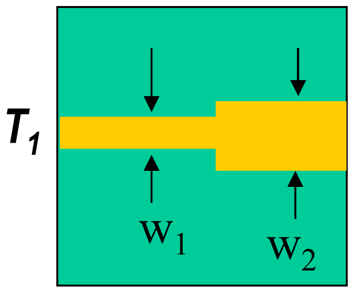
Reactance of C $\quad X_c=\frac{1}{2\pi fC}\cong 1592$

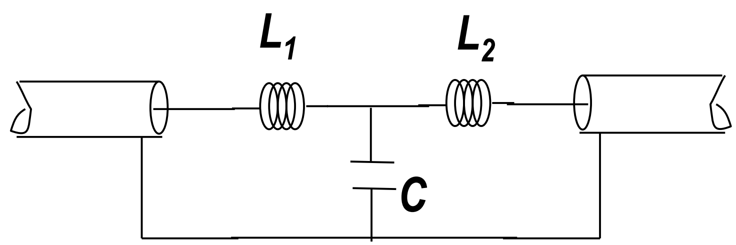
Reactance of L $\quad X_L=2\pi fL\cong 0.38$

Typically the effect of bend is not important for frequency below 1 GHz. This is also true for discontinuities like step and T-junction.

Microstrip Line Discontinuity Models (3)

Step:





See Edwards [4] Chapter 5

Approximate quasi-static expressions for L_1, L_2 and C:

$$\frac{C}{\sqrt{w_1 w_2}} = \left(10.1\log\varepsilon_r + 2.33\right)\frac{w_1}{w_2} - 12.6\log\varepsilon_r - 3.17\ \text{pF/m} \quad \text{for} \quad \varepsilon_r \le 10;\ 1.5 \le \frac{w_2}{w_1} \le 10$$

$$\frac{C}{\sqrt{w_1 w_2}} = 130\log\left(\frac{w_2}{w_1}\right) - 44\ \text{pF/m} \quad \text{for} \quad \varepsilon_r = 9.6;\ 3.5 \le \frac{w_2}{w_1} \le 10$$

(2.3a)

$$\frac{L}{d} = 40.5\left(\frac{w_1}{w_2} - 1.0\right) - 75\frac{w_1}{w_2} + 0.2\left(\frac{w_1}{w_2} - 1.0\right)^2\ \text{nH/m}$$

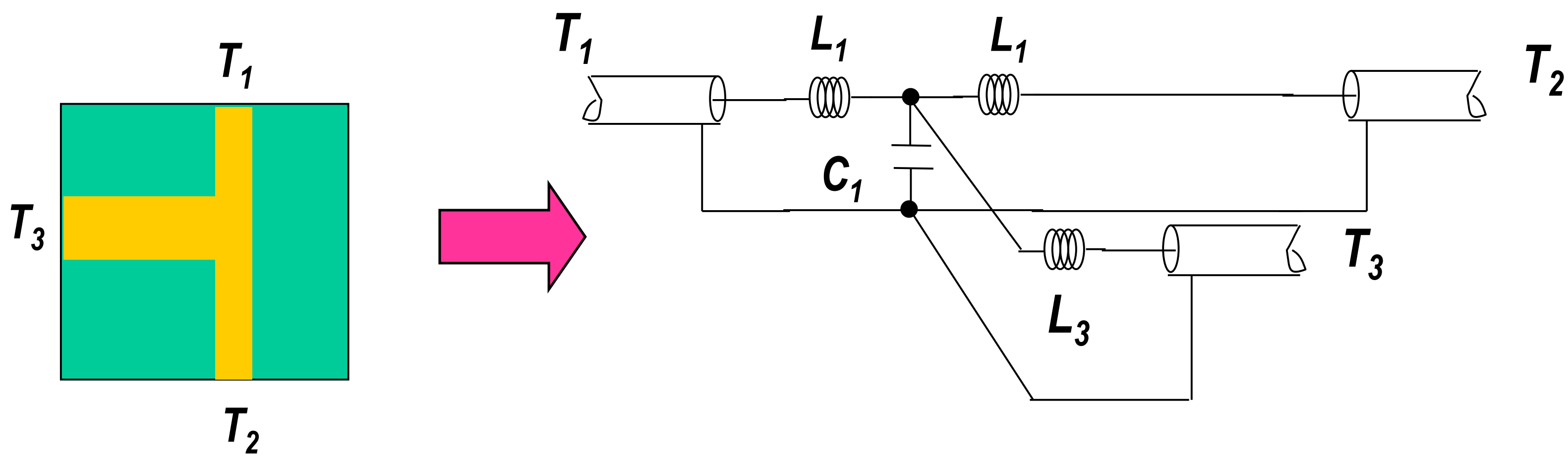
(2.3b)

$$L_1 = \frac{L_{m1}}{L_{m1} + L_{m2}}L \qquad L_2 = \frac{L_{m2}}{L_{m1} + L_{m2}}L$$

L_{m1} and L_{m2} are the per unit length inductance of T_1 and T_2 respectively.

Microstrip Line Discontinuity Models (4)

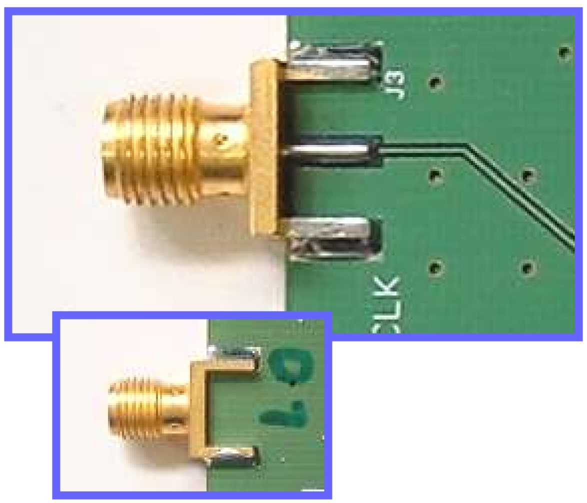
T-Junction:

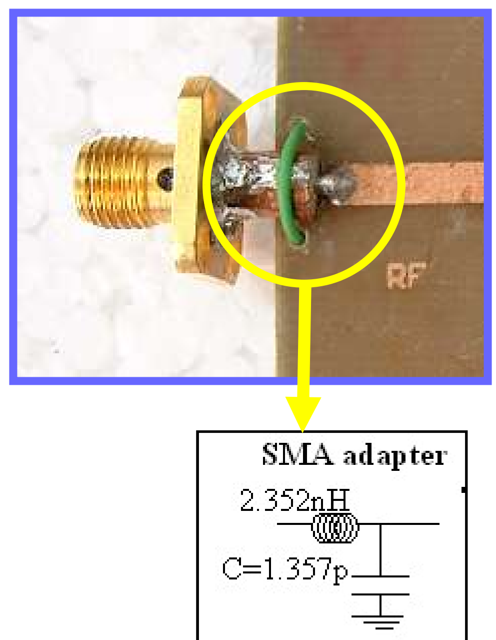


See Edwards [4], Chapter 5 for alternative model and further details.

Connector Discontinuity: Coaxial - Microstrip Line Transition (1)

- Since most microstrip line invariably leads to external connection from the printed circuit board, an interface is needed. Usually the microstrip line is connected to a co-axial cable.
- An adapter usually used for microstrip to co-axial transistion is the SMA to PCB adapter, also called the SMA End-launcher.



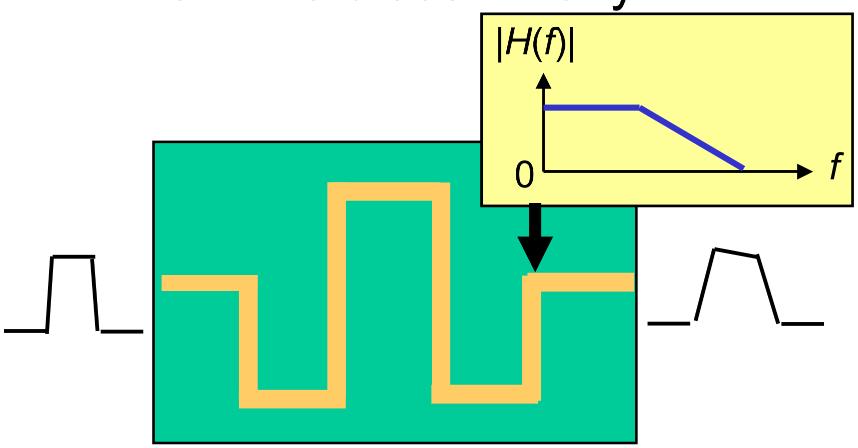


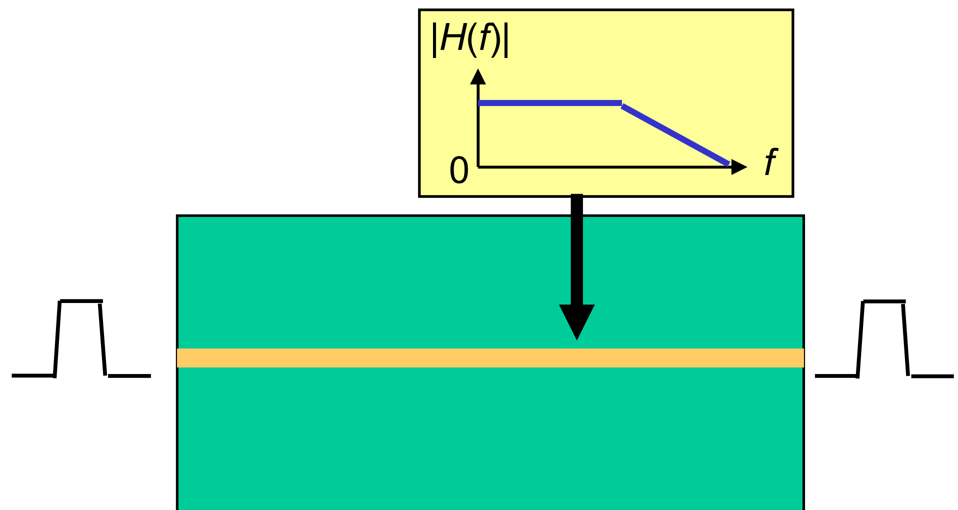
Connector Discontinuity: Coaxial - Microstrip Line Transition (2)

- Again the coaxial-to-microstrip transition is a form of discontinuity, care must be taken to reduce the abruptness of the discontinuity. For a properly designed transition such as shown in the previous slide, the operating frequency could go as high as 6 GHz for the coaxial to microstrip line transition and 9 GHz for the coaxial to co-planar line transition.

Effect of Discontinuities

- Looking at the equivalent circuit models for the microstrip discontinuities, the sharp reader will immediately notice that all these networks can be interpreted as Low-Pass Filters. The inductor attenuates the electrical signal at high frequency while the capacitor shunts electrical energy at high frequency.
- Thus the effect of having too many discontinuities in a high-frequency circuit reduces the overall bandwidth of the interconnection.
- Another consequence of discontinuities is attenuation due to radiation from the discontinuity.



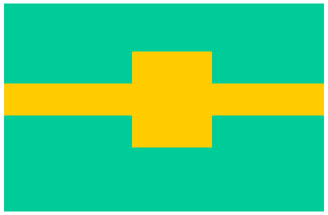


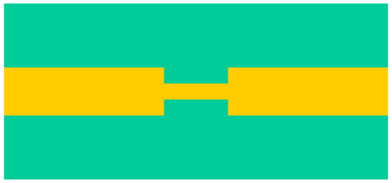
Radiation Loss from Discontinuities

- At higher frequency, say > 5 GHz, the assumption of lossless discontinuity becomes flawed. This is because the higher order mode EM fields can induce surface wave on the printed circuit board, this wave radiates out so energy is loss.
- Furthermore the acceleration or deceleration of electric charge also generates radiation.
- The losses due to radiation can be included in the equivalent circuit model for the discontinuity by adding series resistance or shunt conductance.

Exercise 2.1

- What do you expect the equivalent circuit of the following discontinuity to be ?





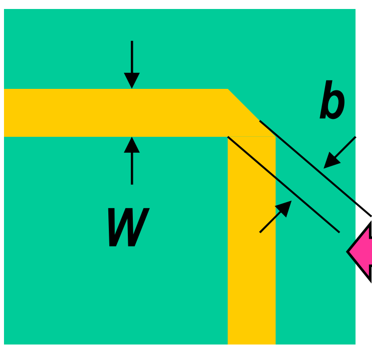
4.3 – PCB Layout Rules for Reducing the Effect of Trace Discontinuities

Reducing the Effects of Discontinuity (1)

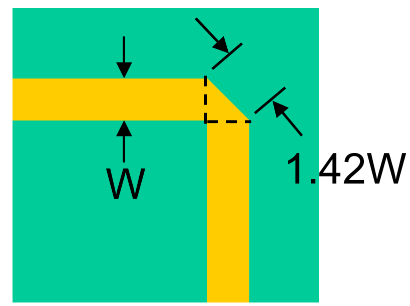
- To reduce the effect of discontinuity, we must reduce the values of the associated inductance and capacitance. This can be achieved by decreasing the abruptness of the discontinuity, so that current flow will not be disrupted and charge will not accumulate.

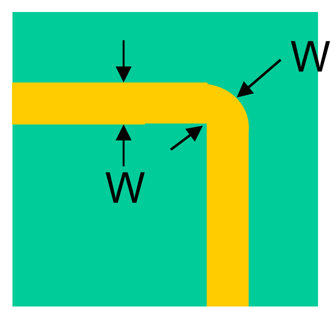
NOTE:
Generally these are not needed for frequency < 300 MHz

Chamfering of bends



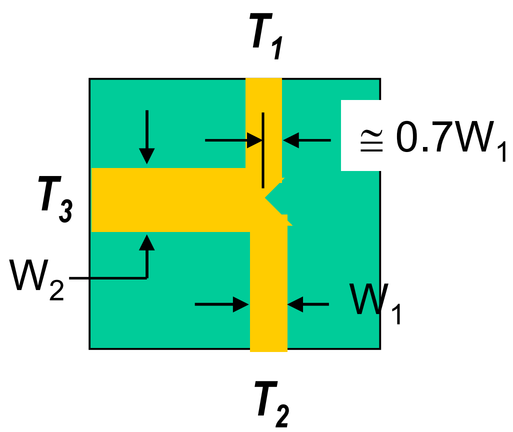
For 90^o bend:
It is seen that the optimum chamfering is b=0.57W (see Chapter 5, Edwards [4])
For further examples see Chapter 2, Bahl [7].

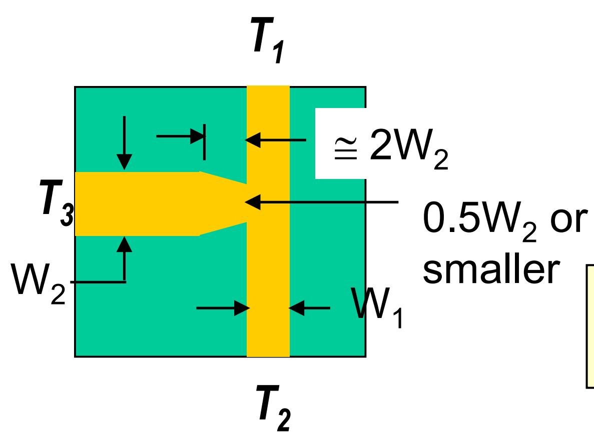




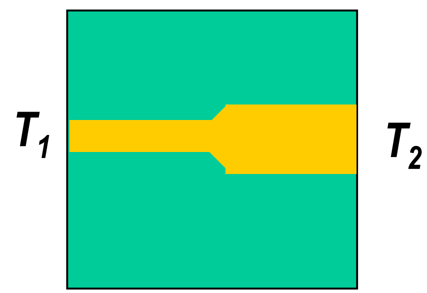
Reducing the Effects of Discontinuity (2)

Mitering of junction





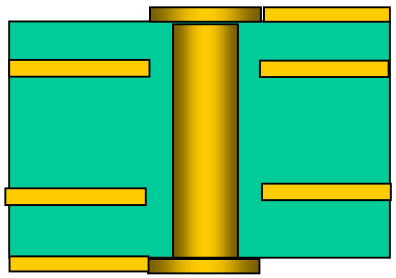
Mitering of step



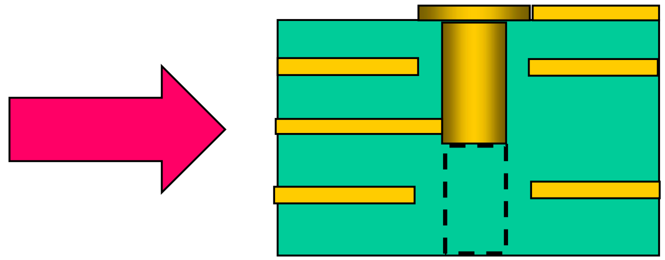
For more details of compensation for discontinuity, please refer to Chapter 5 of Edwards [4] and Chapter 2 of Bahl [7].

NOTE:
Generally these are not needed for frequency < 300 MHz

Handling Vias and Pads (1)

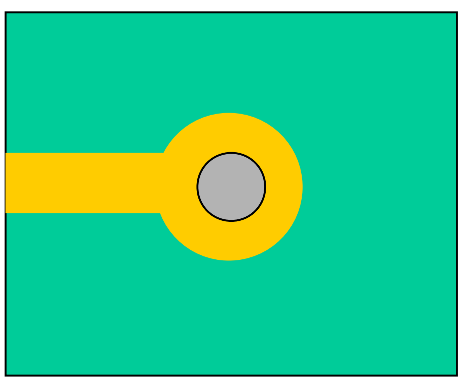


Side view of a Via

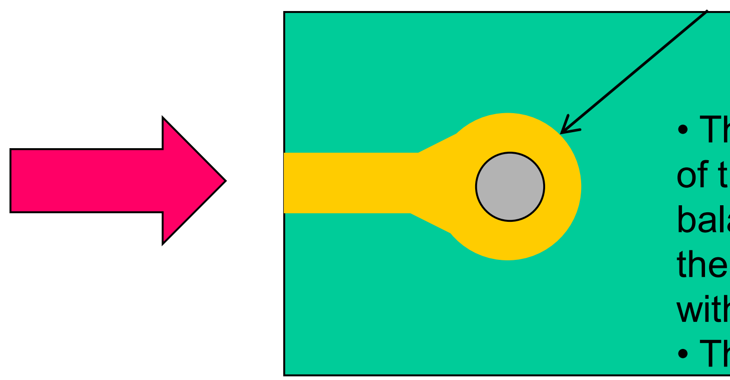


Reduce the length of the via by using inner trace layer and remove the stub (e.g. use buried or blind via).

A tear-drop shape pad (typically only recommended for frequency above 1 GHz).



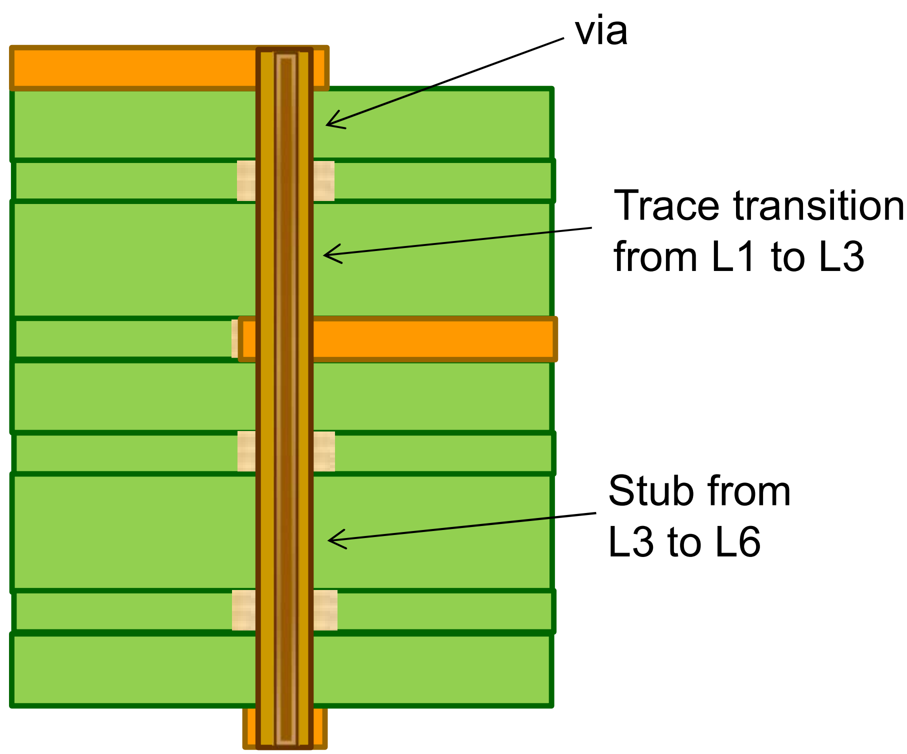
Top view of a Via



- The extra capacitance of the tear-drop shape balance the effect of the inductance associated with the via.
- The tear-drop shape also improves reliability of contact between trace and pad.

Handling Vias and Pads (2)

- Vias are used for transitioning traces to different layers.
- For a through hole via, if the trace is not transitioned from top layer to bottom layer, it does not use the whole via length and thus there exists a **stub length** to the signal.
- This problem usually happens in PCB of 6 or more layers.
- The end of the stub appears as open and it has reflection coefficient of +1.



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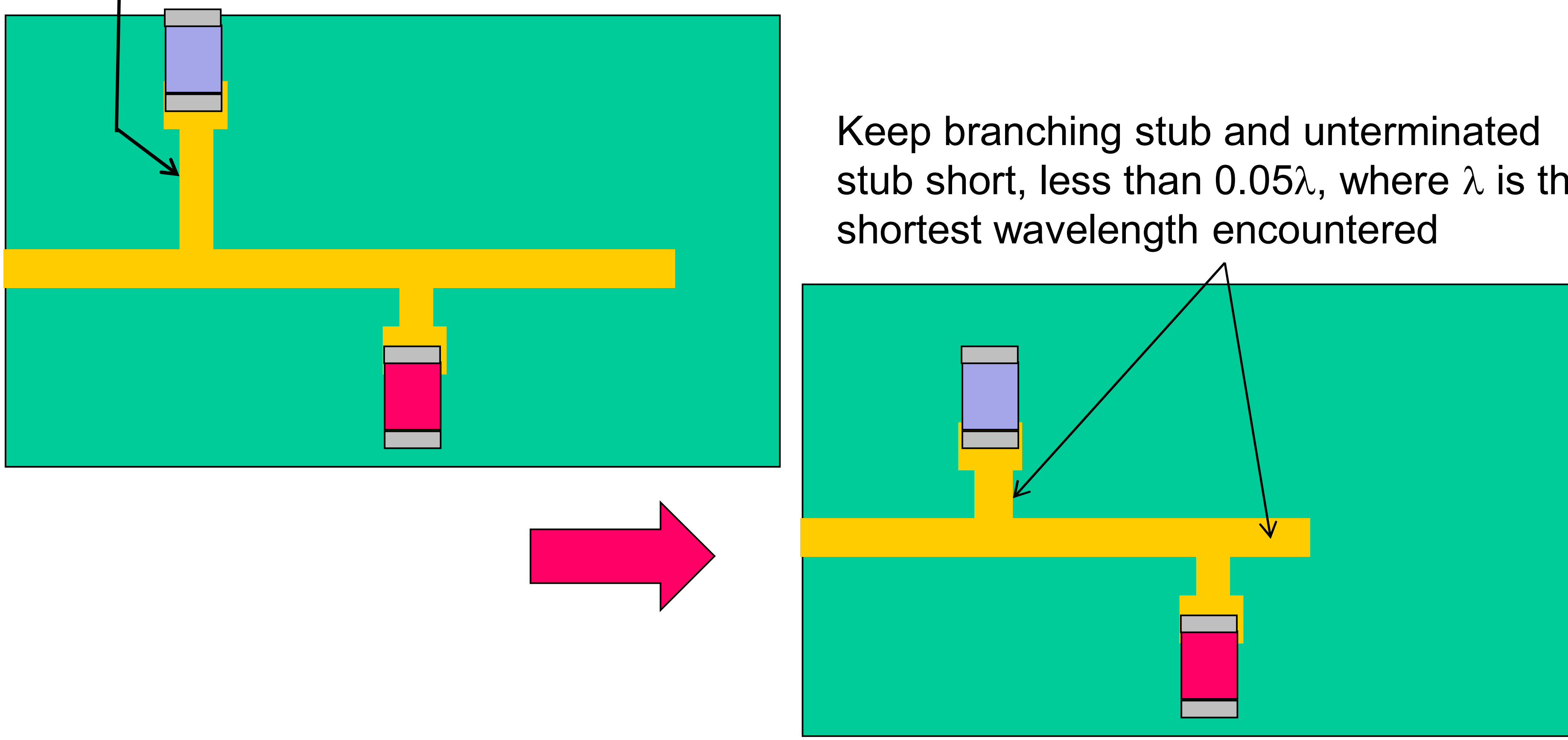
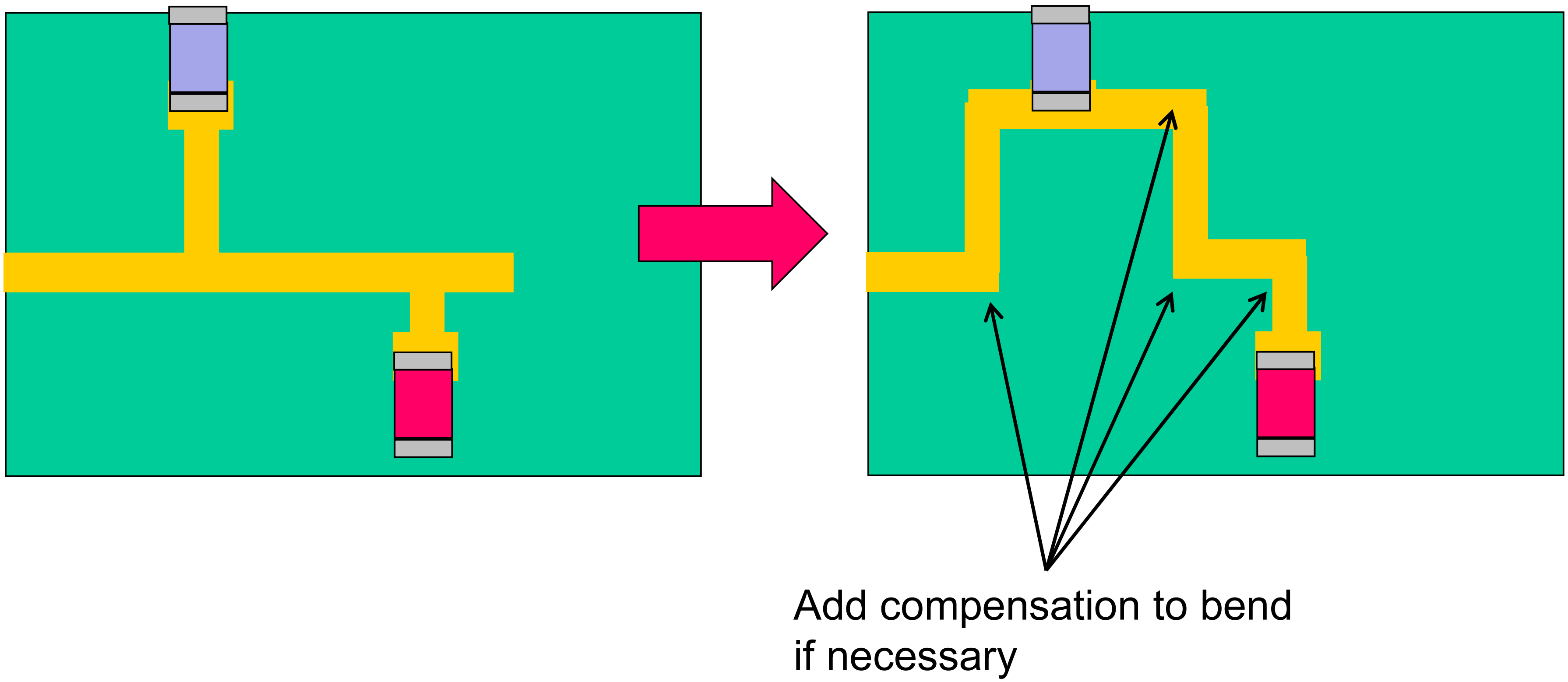
Handling Stubs (1)

- Stubs are short trace segment that extend from the main trace. Most often they connect to a solder pad and a component.

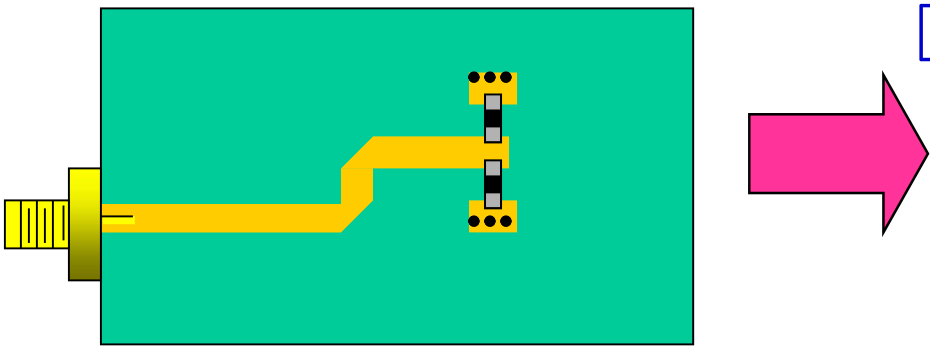


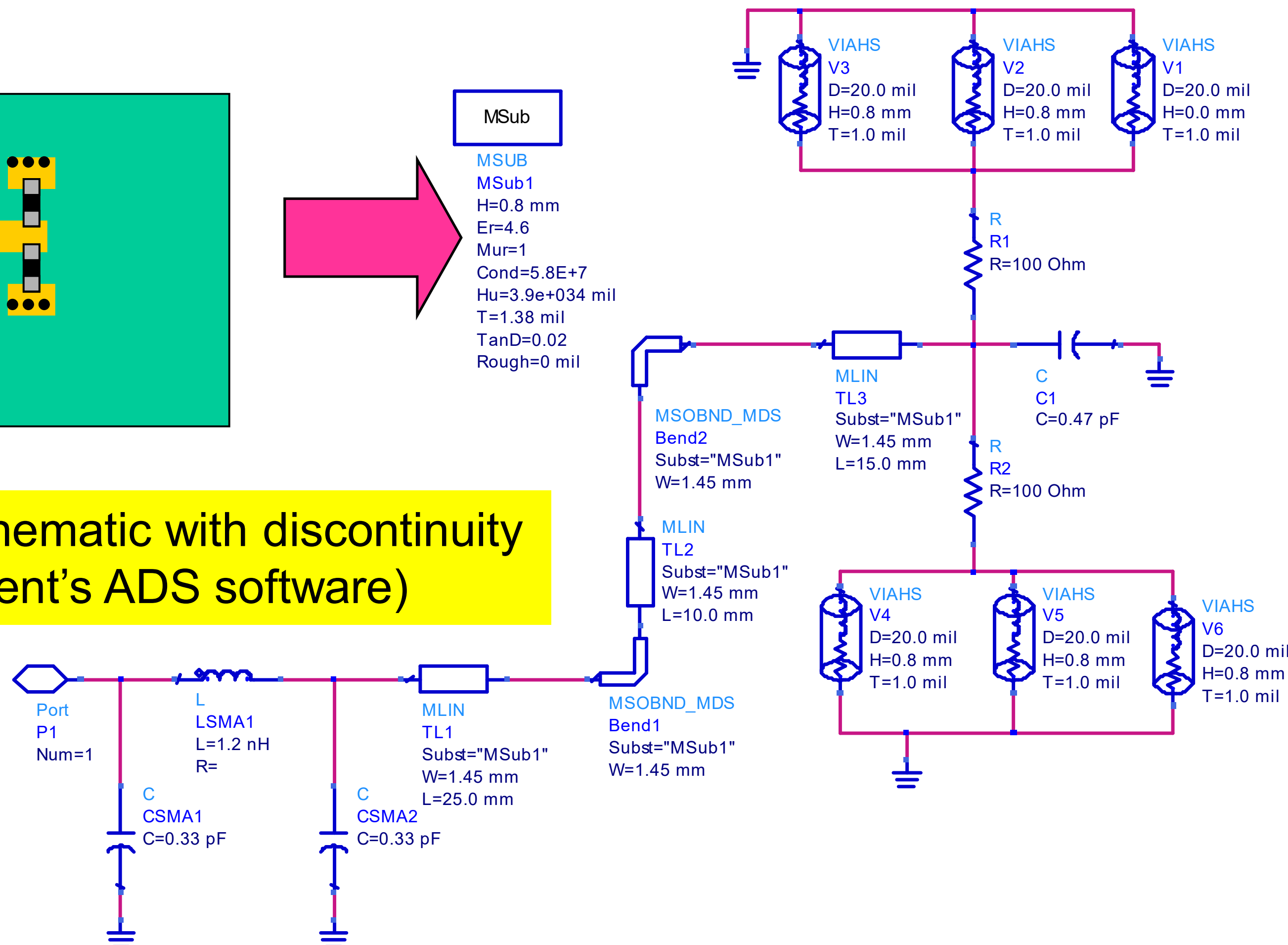
Handling Stubs (2)



Example 3.1

- A Z_c = 50Ω microstrip Tline is used to drive a resistive termination as shown.

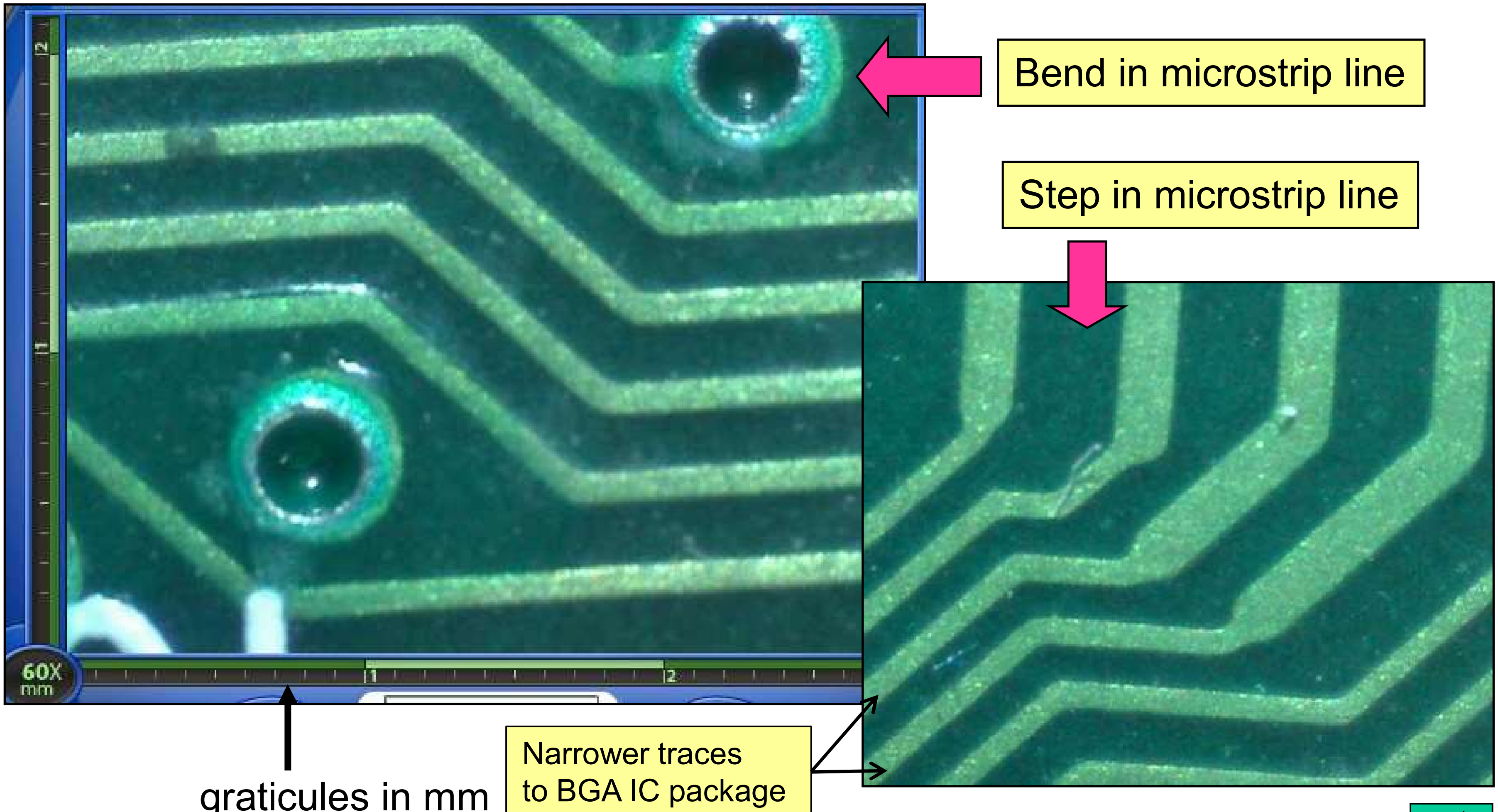




Example of schematic with discontinuity Elements (Agilent's ADS software)

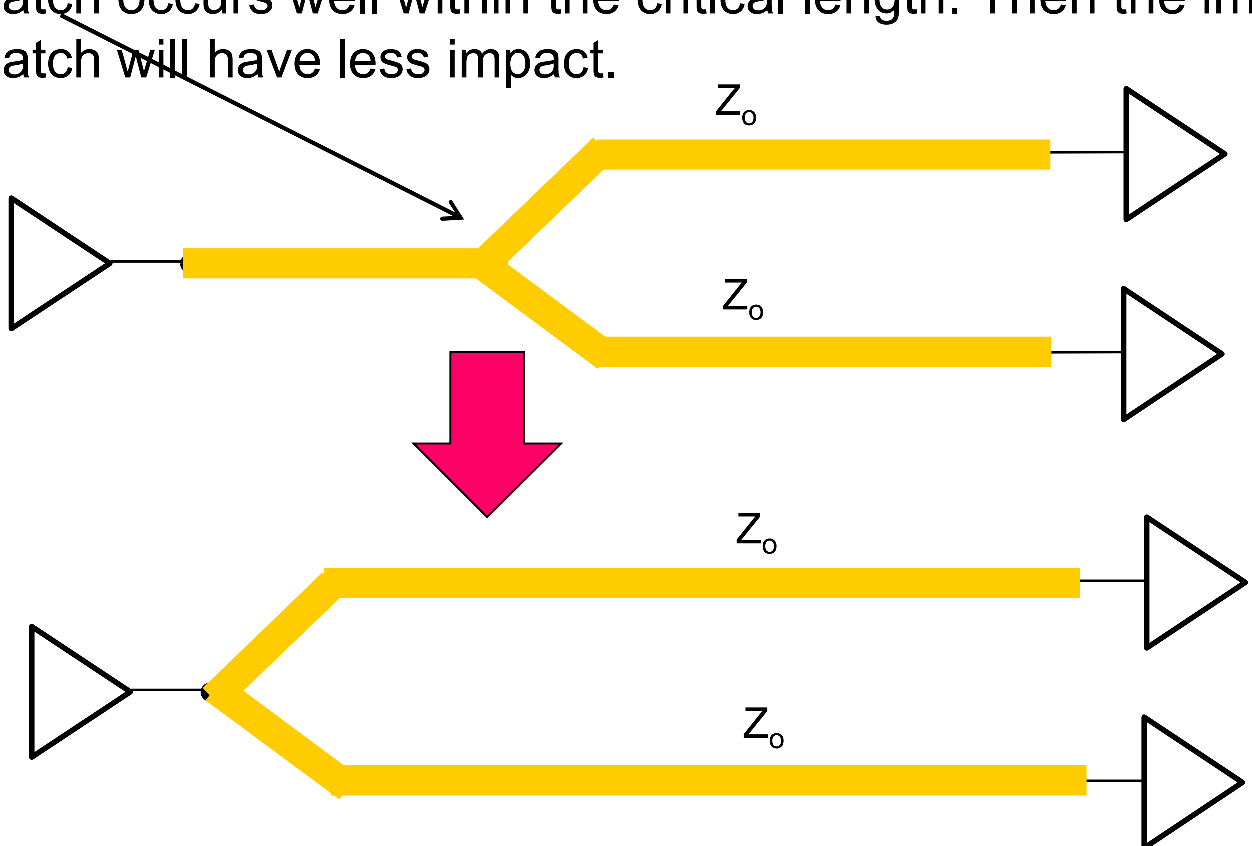
Example 3.2 – Photomicrographs of PCB

- Photomicrograph of microstrip line bend and step (60X).



Another Method of Handling Branching

- We have seen one method of handling branching in Chapter 3B, here's another useful approach.
- Locate the split point very close to the driver so that the impedance mismatch occurs well within the critical length. Then the impedance mismatch will have less impact.



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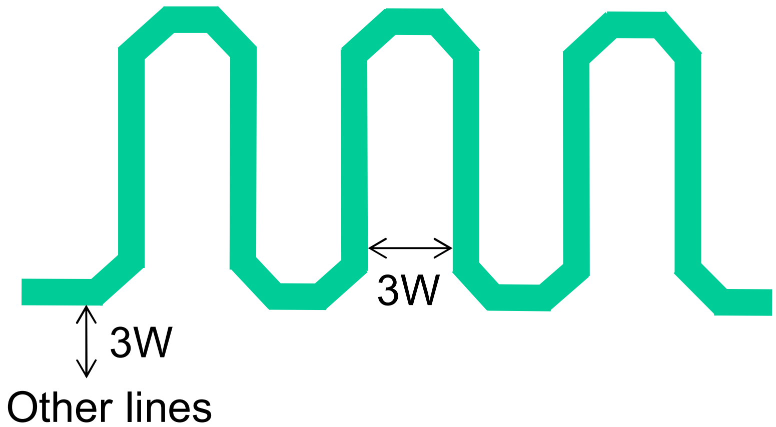
Serpentine Routing

Useful rules for serpentine routing in length control

- Timing skew control is usually accomplished by introducing extra “turning” or “serpentine” routing to the traces.
- For single-end lines (W), keep at least 3W separation between serpentine traces.



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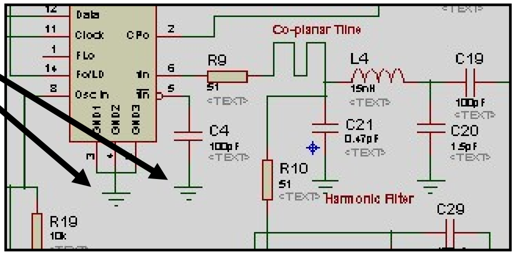
4.4 – Grounding

The Ground (GND)

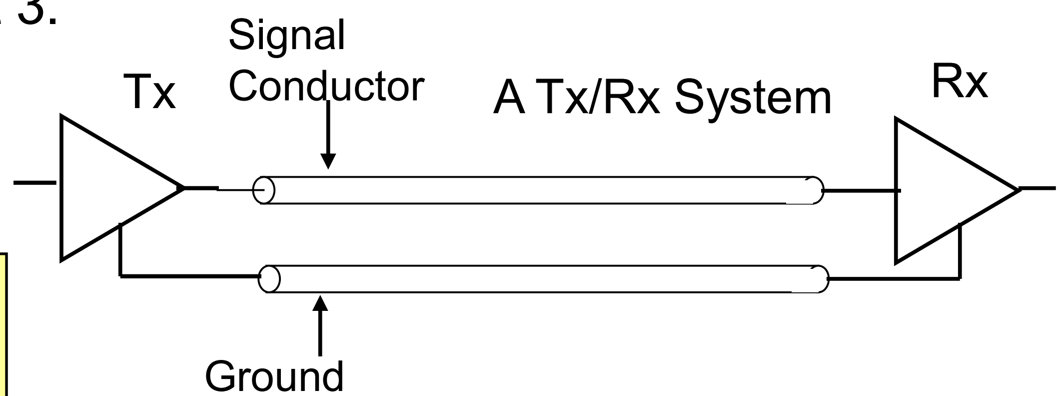
- A SINGLE conductor in the PCB or system is called the Ground (GND).
- It is assumed the GND has a stable electric potential (with respect to infinity) and this potential is uniform throughout the conductor. This can be enforced by using a good conductor (high conductivity) and limiting the GND conductor size to as small as practical.
- All electric potential in the PCB or system is measured with respect to GND, and we can arbitrarily assign a value of 0V to the GND potential.
- This 0V GND conductor is what we assumed when drawing schematics.



- The process of creating the GND conductor is called Grounding. An ideal GND is just a concept, as all real conductor has finite impedance and we cannot ensure uniform potential throughout the GND conductor for high frequency signals.

Signal Ground

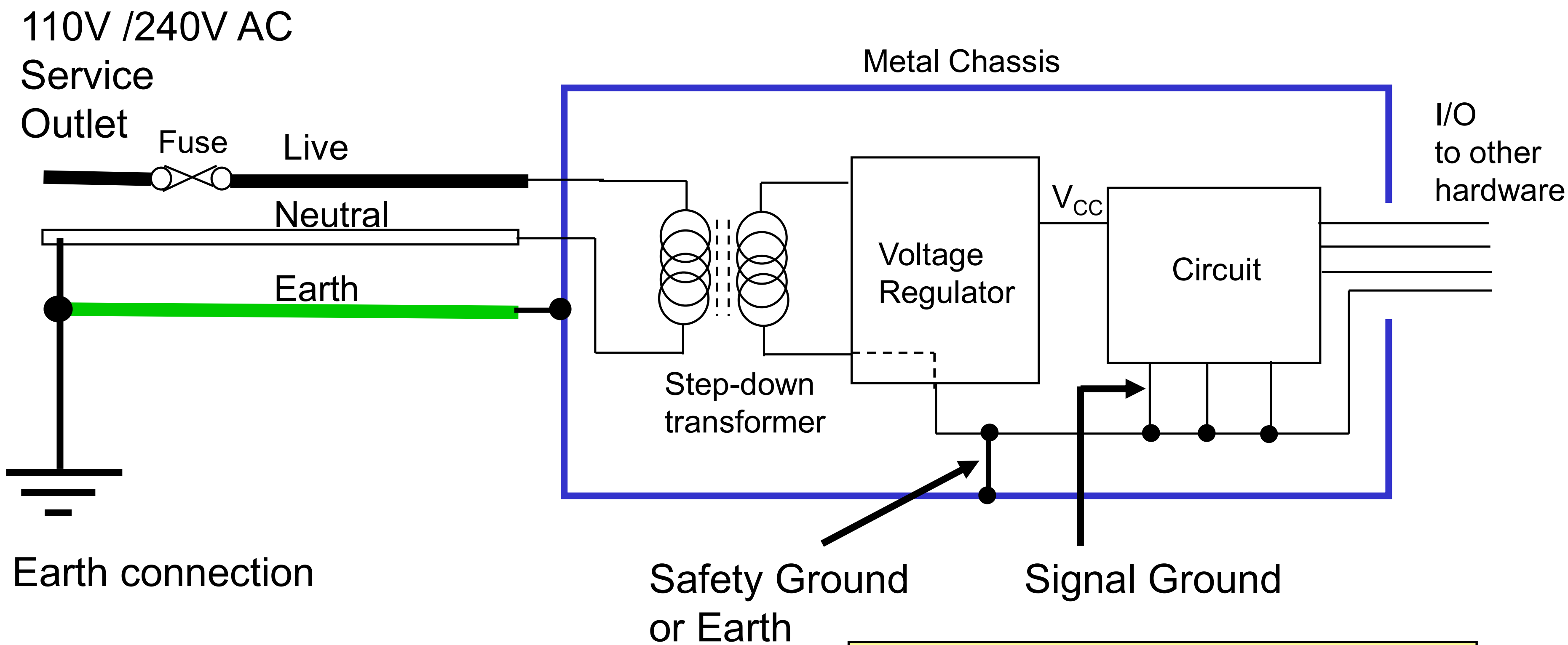
- The aims of grounding are:
  - To allow electric charge and current to flow from source to load and back to the source, i.e. provide a return path.
  - For low frequency circuit, to provide a stable reference potential (0V).
  - To control electromagnetic interference due to electric and magnetic field coupling, i.e. provide reasonable isolation. We have already seen this in action in our discussion on multiconductor transmission line and crosstalk in Part 3.



Good layout practices on the PCB are of utmost importance in ensuring the circuit works properly.

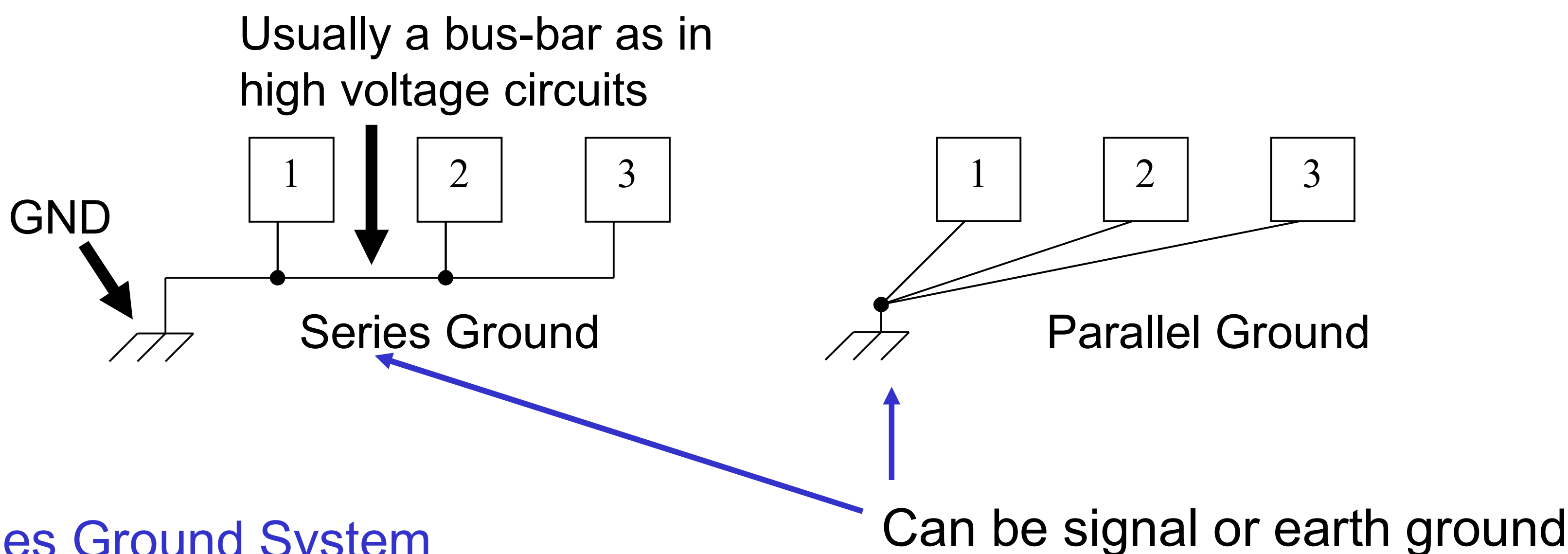
Example of Ground - Earth and Signal Ground

- A simplified view of typical instrument powered via mains supply.



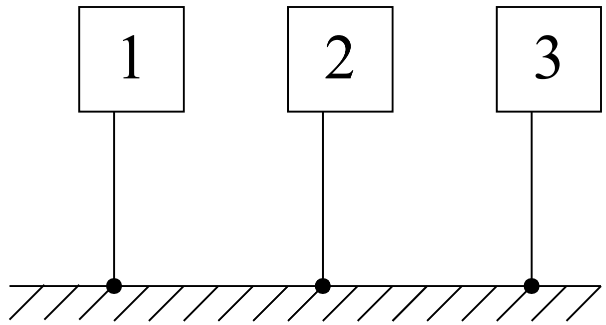
Note that only ONE point on the signal ground is connected to the chassis of the instrument

Signal Ground: Single-Point Ground



- Series Ground System
  - Easy to implement.
  - Suffers from common-impedance coupling.
- Parallel Ground System
  - Less common-impedance coupling.
  - Mutual coupling (inductive and capacitive) between ground leads should be minimised.

Signal Ground: Multi-point Ground

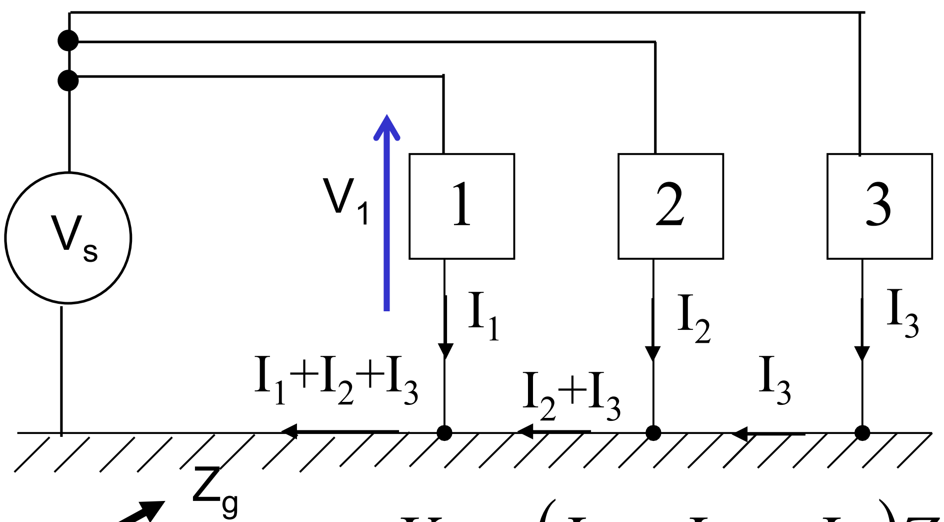


- Uses large ground plane as common ground conductor.
- Circuits that require ground connection are connected to the nearest available ground plane.
- Also suffer from common impedance coupling but it can be reduced by lowering the ground-impedance.
- Typically used in multilayer PCB.

4.4 – Grounding Considerations and Layout Rules

Grounding Consideration: Common-Impedance Coupling (1)

- The same GND impedance is seen by all modules.



Inclusive of the resistance and partial inductance of the GND

$$V_s = (I_1 + I_2 + I_3)Z_g + V_1$$

$$\Rightarrow V_1 = V_s - \boxed{(I_1 + I_2 + I_3)Z_g}$$

Voltage across module 1 is 'modulated' by the changes in other modules. This effect is also known as Ground Bounce.

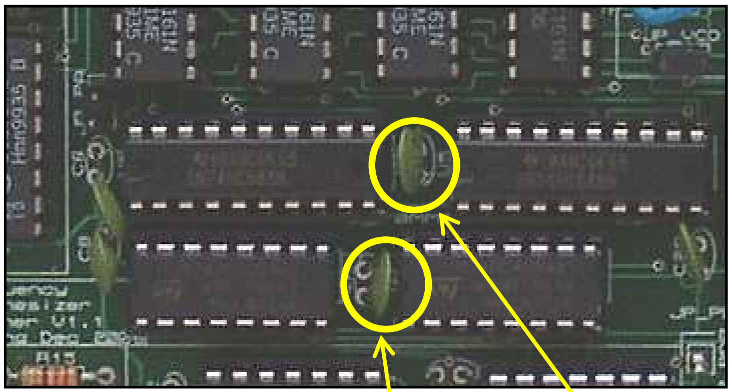
Grounding Consideration: Common-Impedance Coupling (2)

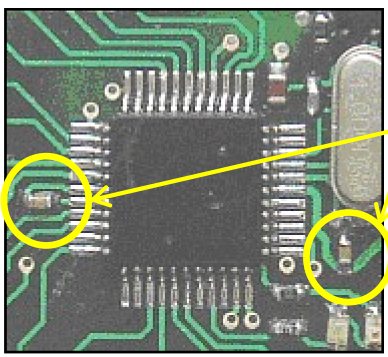
- Common-impedance coupling can occurs on both source (i.e. the V_{CC}) and return path in a PCB assembly. It is more serious in system which uses series or multi-point ground scheme.
- Common-impedance coupling can be reduced by using low impedance source and ground path, reduce Z_g and Z_p (V_{CC} path impedance), i.e. use power plane and ground plane instead of power and ground traces/buses.
- Segmentation of the circuits and ground planes reduces common-impedance coupling.
- Using decoupling capacitors and RF chokes can help filter out large voltage fluctuations seen by a component V_{CC} and GND terminals.

NOTE: Techniques of analyzing and reducing the supply voltage fluctuation on a component is generally called Power Integrity (PI), as opposed to Signal Integrity which is our concern here. The physical V_{CC} and GND paths are usually called the Power Distribution Network (PDN).

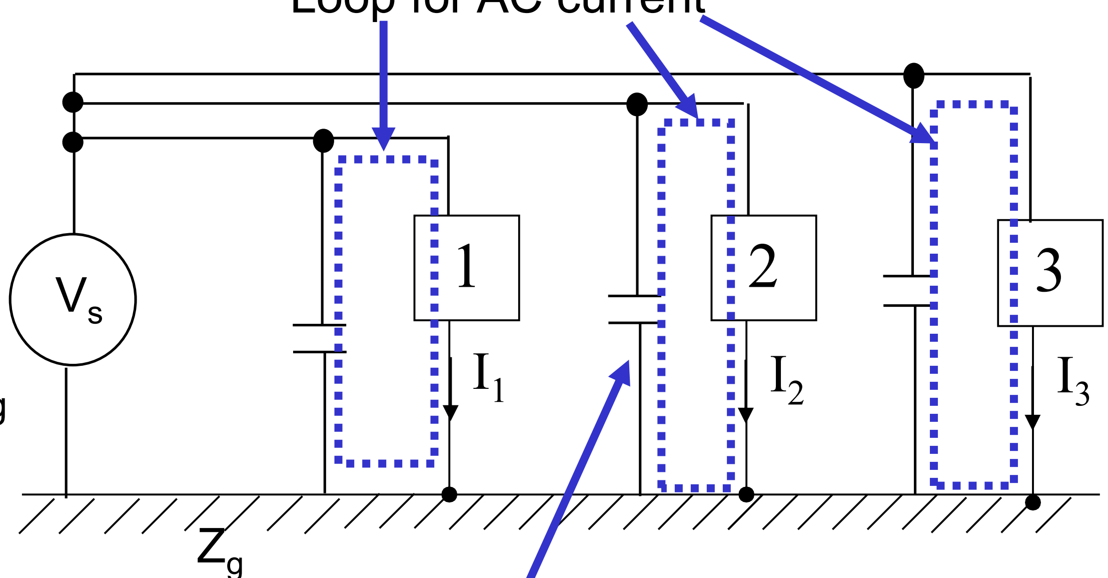
Reducing Common-Impedance Coupling with Decoupling Capacitors

- If common-impedance coupling is mainly due to large transient/AC current, adding decoupling capacitors on each block will helps.
- Block here can means a group of components or an integrated circuit.





Putting decoupling capacitors near each IC in through-hole and SMD components

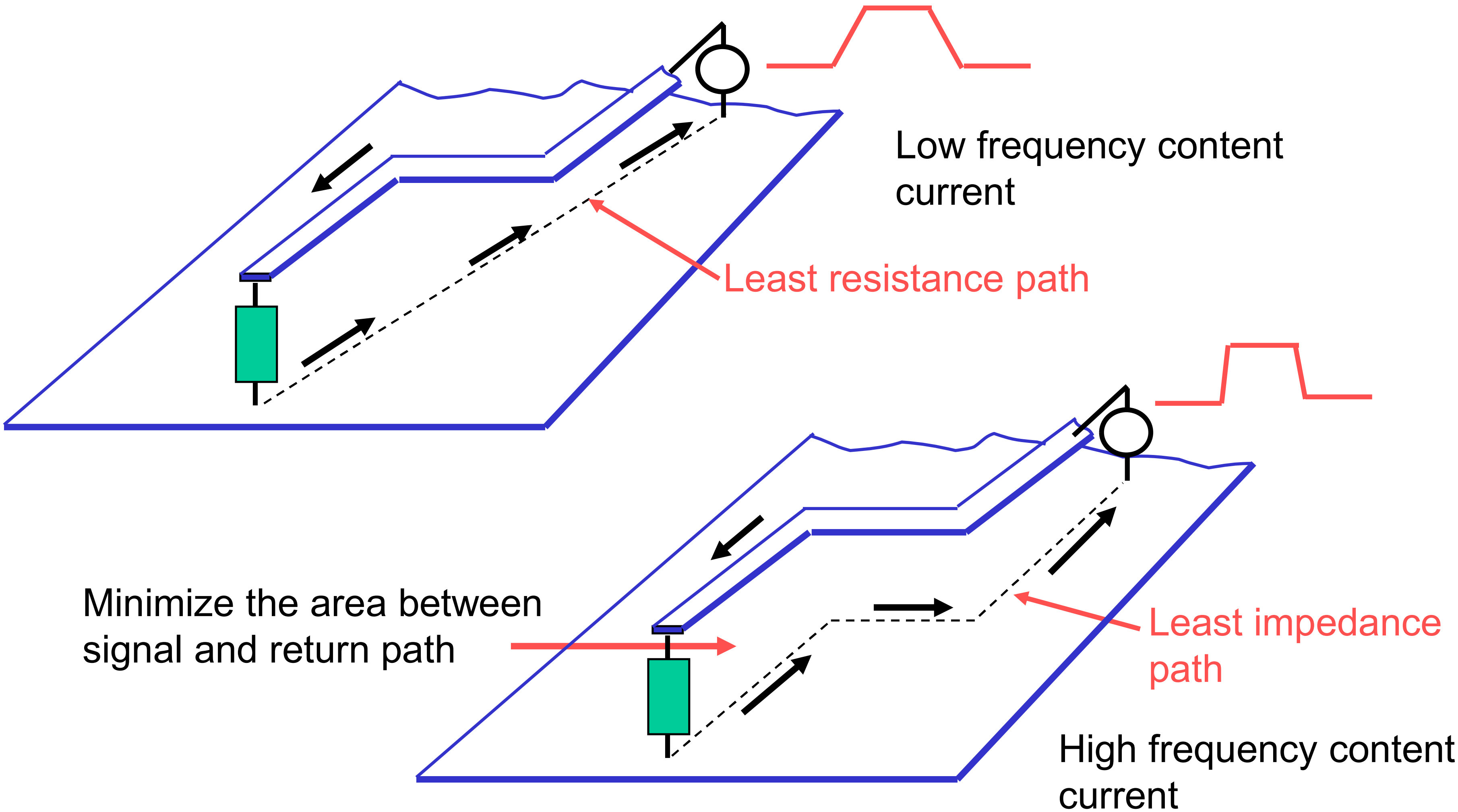


Decoupling capacitor, good quality capacitor (with low ESR, ESL) placed near the module.

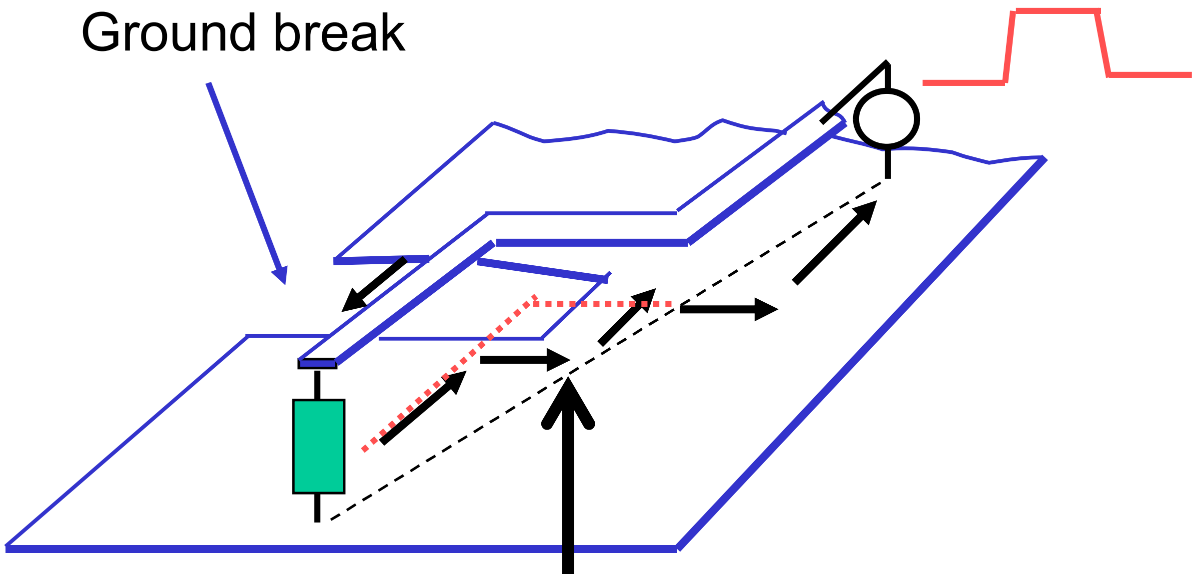
Grounding Consideration: Current Return Path (1)

- Coupling is minimised if current returns via a path as near as possible to the incident path (to reduce the effect of stray fields).
- Current will always follows the path with least impedance, this is a consequent of the law of physics where the energy of a system will tend towards lowest energy state.
- At low frequency, the resistance of a path dominates the impedance, while at high frequency, the reactance of a path dominates. This is best summarized as follows:
  - Low frequency current flows through the path with least resistance.
  - High frequency current flows through the path with least impedance.
- Current that flows on least impedance path will create less 'fringing' EM fields, thus less opportunity to interfere with other circuits.
- Least impedance path usually correspond to the signal and return path which minimizes the loop area.

Grounding Consideration: Current Return Path (2)



Grounding Consideration: Ground Break

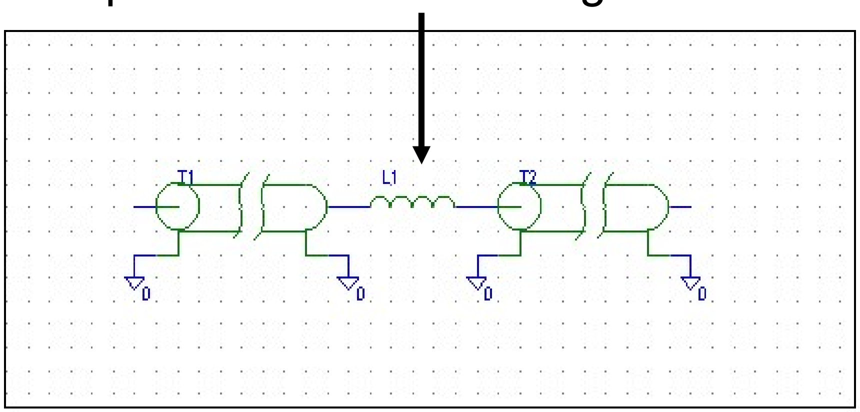


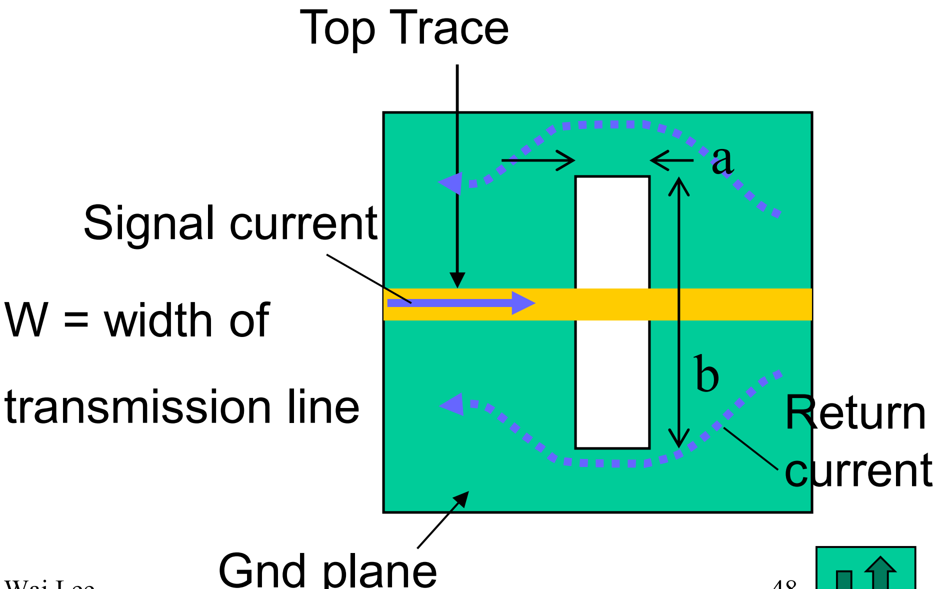
Detour for return current, more magnetic flux linkage. This will manifest as extra inductance in the interconnect circuit.
Furthermore the E and H fields will ‘extend’ further from the circuit, making it easier for this circuit to interfere and be interfered.

Effect of Ground Break (1)

- A break in ground plane for transmission line is not desirable, return current will have to flow a longer distance, this manifests as extra inductance (because of extra magnetic field generated in the vicinity of the break). However, from measurement, it is observed that this effect is only important for frequencies of 2 GHz and above if a,b > 3W.
- In system where a ground plane is not possible, then the use of ground grid is encouraged. Usage of grid provides a number of return path for the signal current, thus allowing the return current to choose the path that is of lowest impedance.

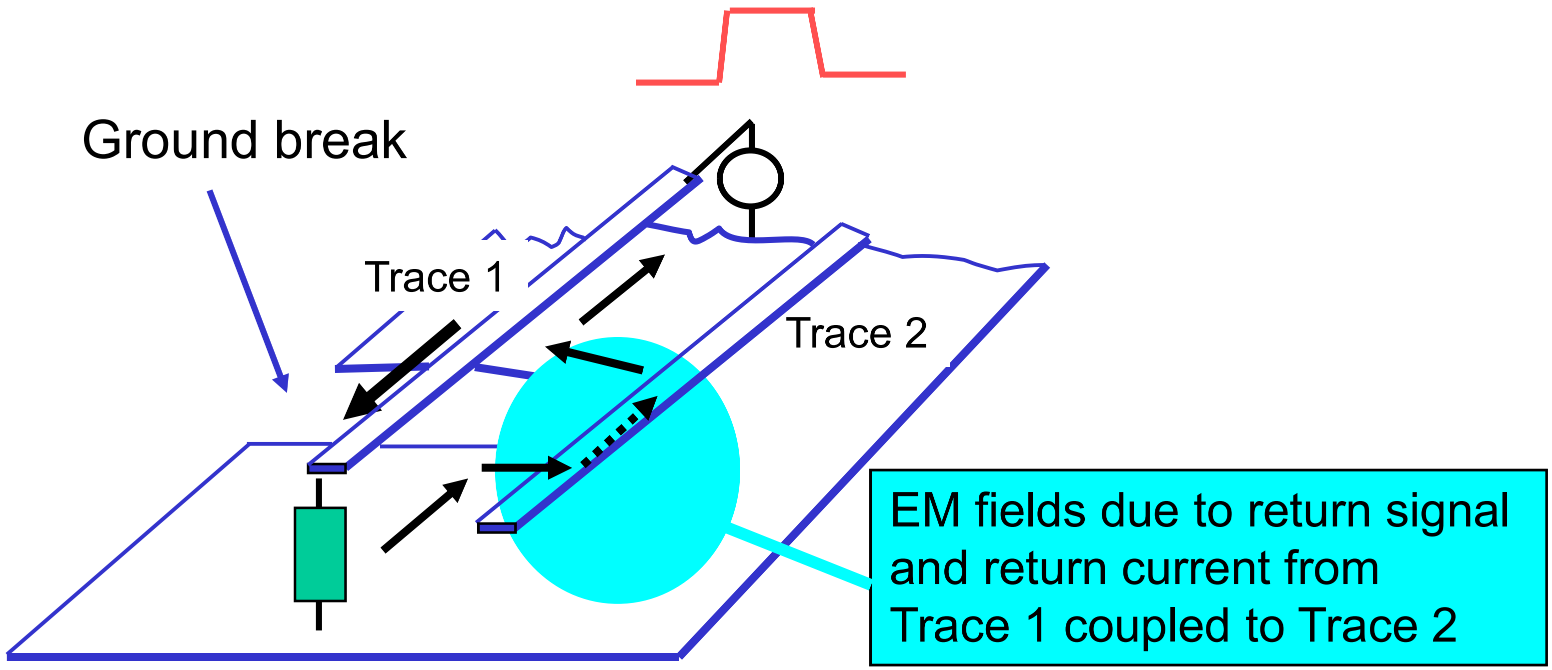
Equivalent circuit due to ground break





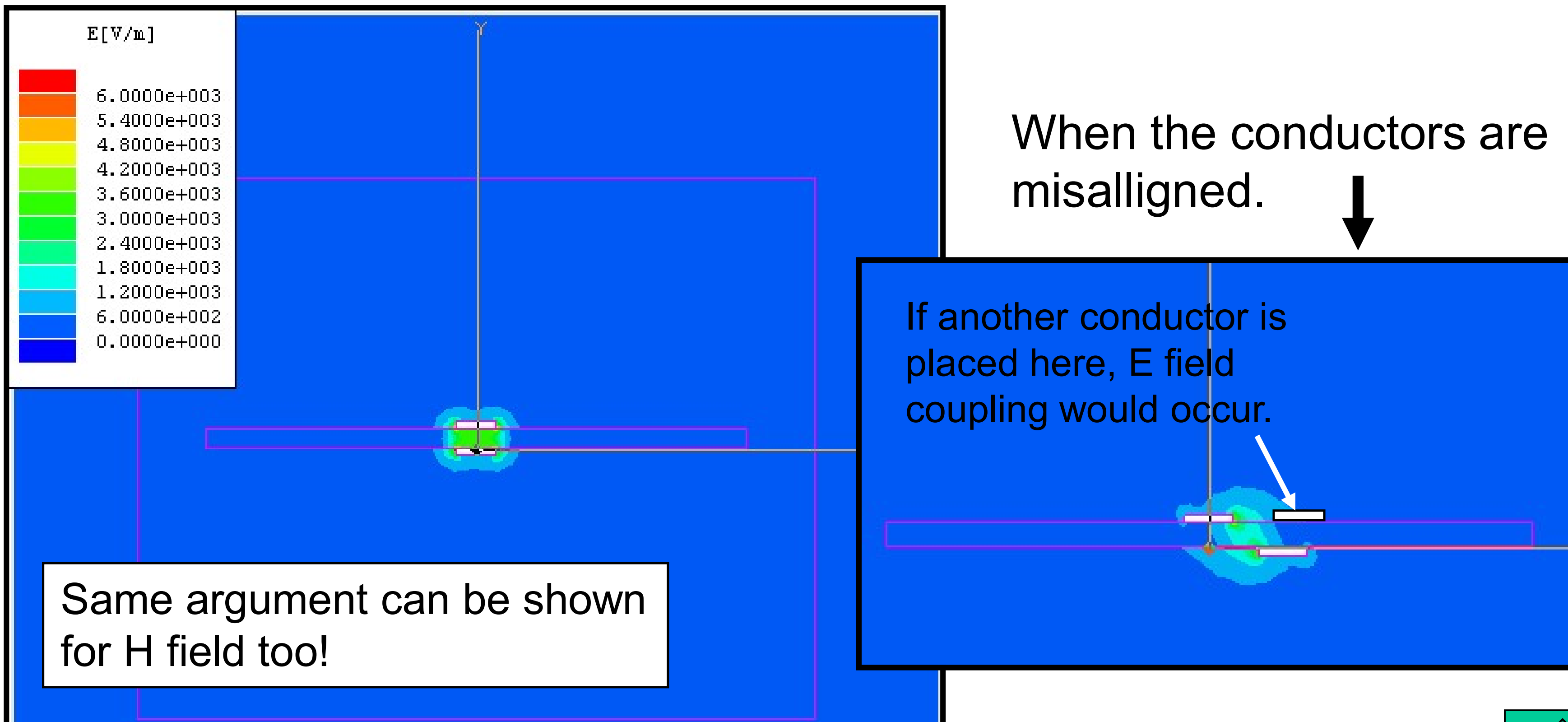
Effect of Ground Break (2)

- Ground break also increases coupling between traces.



Example 4.1

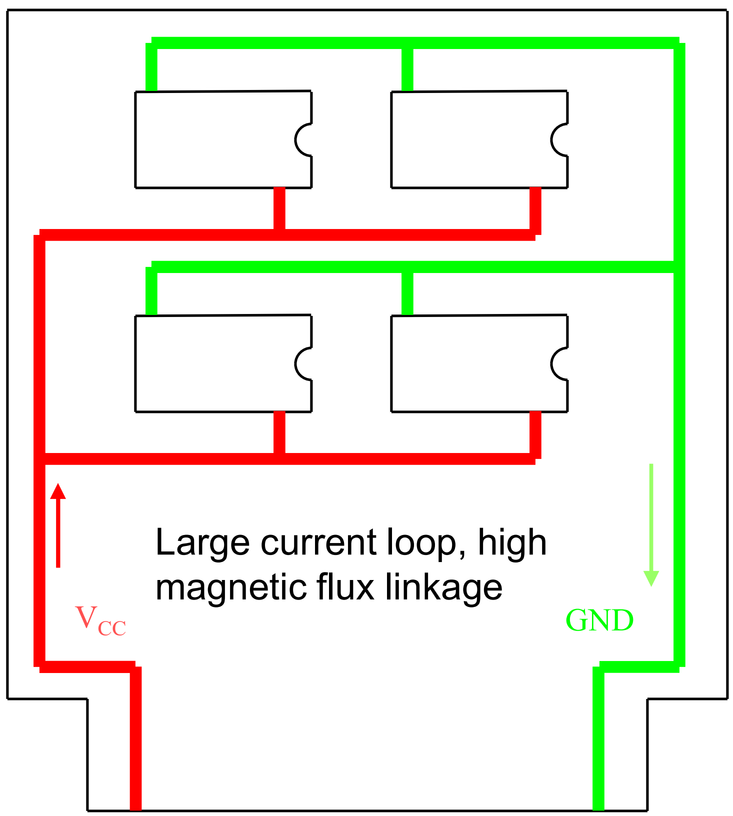
- A numerical experiment is performed using Maxwell SV software. The figure below shows the 2D plot of the E field magnitude for 2 conductors sandwiching a FR4 substrate.
- Top conductor has 1V potential while bottom is GND at 0V.



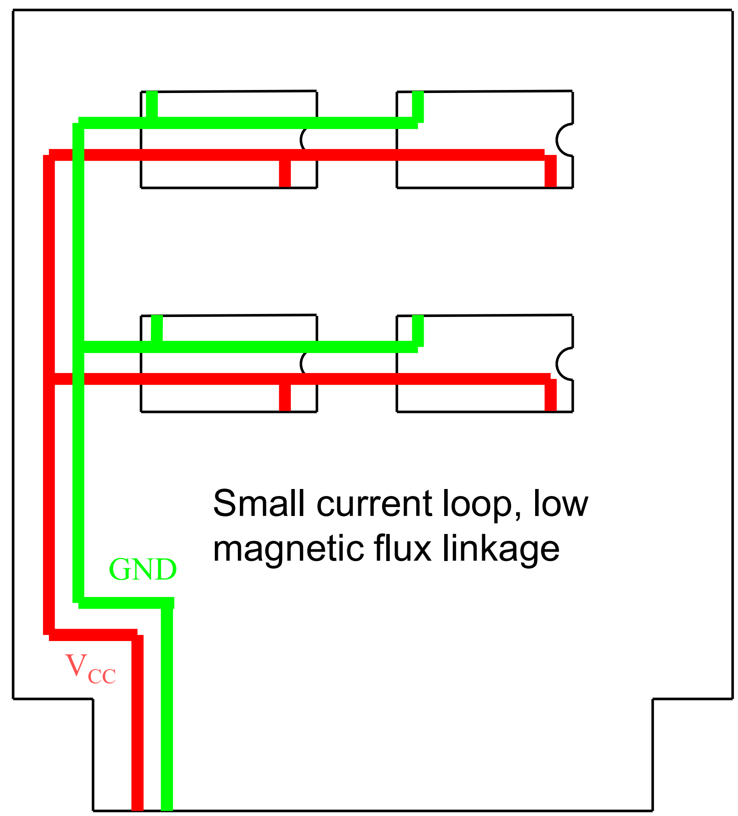
Ground Scheme 1 - Power Distribution and Ground on Same Layer

Extra

- The power and ground wires can be considered as a signal-ground combination. Therefore based on previous discussion on current return path, these must be near each other.



Not Encouraged



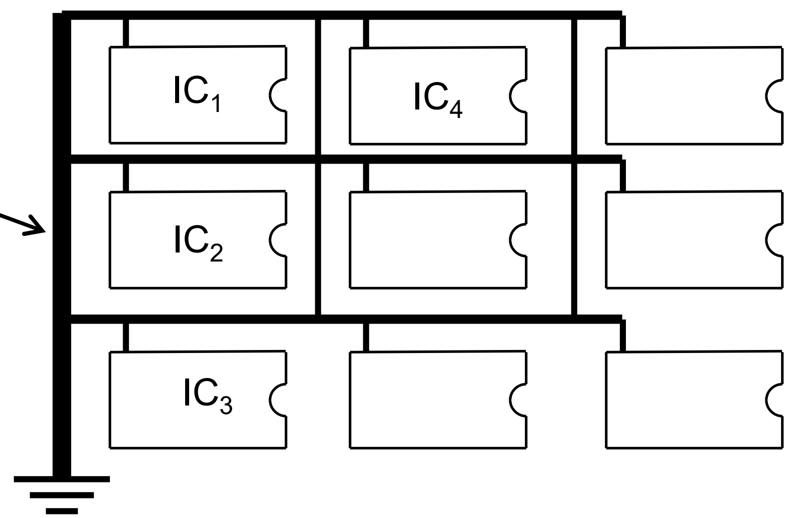
Good Practice

Ground Scheme 2 – Using Ground Grid

Extra

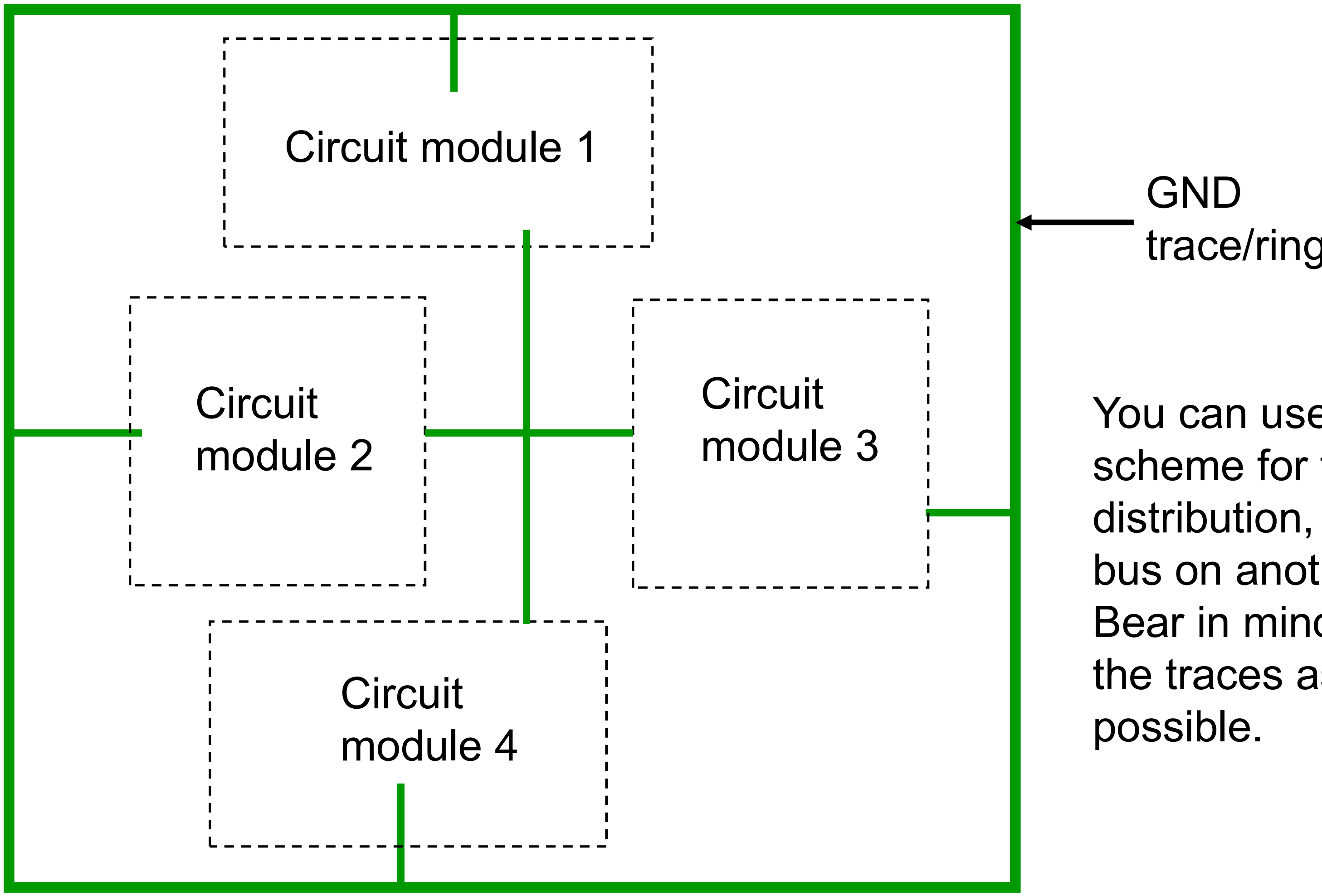
- Reduces ground path impedance.
- Reduces common impedance coupling between ICs.
- Allow shorter return path, less interference and unwanted radiations.

Use wide trace
(for instance this can be a microstrip trace with $Z_c < 5$)



Ground Scheme 3 – Using Ground Ring

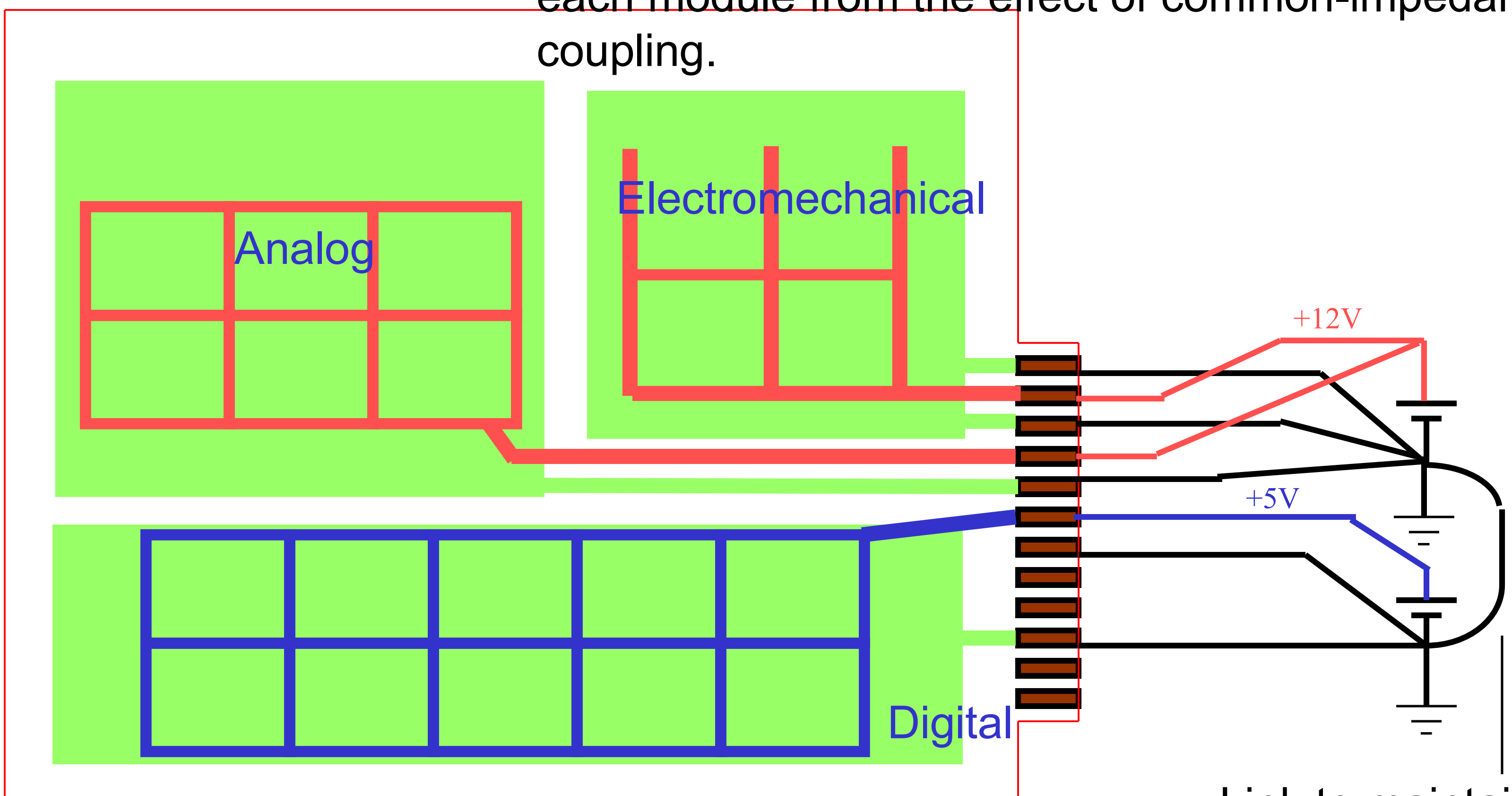
Extra



You can use similar scheme for the power distribution, the VCC bus on another layer. Bear in mind to keep the traces as close as possible.

Ground Scheme 4 - Ground Plane and Segmentation for Hybrid System

Separation of ground plane allows isolation of each module from the effect of common-impedance coupling.

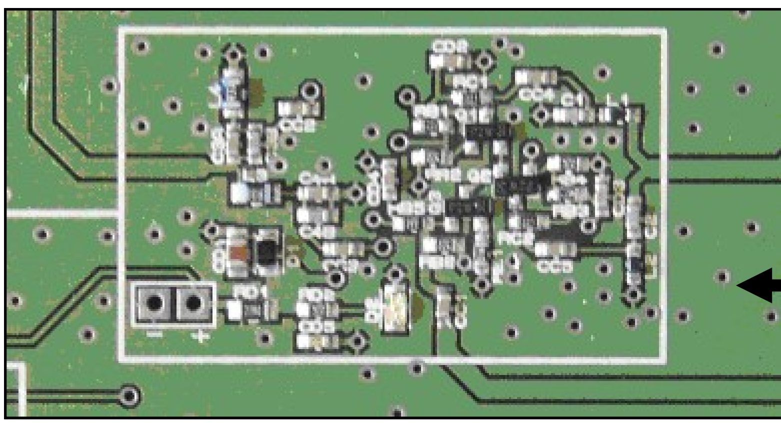


This is the best scheme as it allows return current to flow directly beneath the power lines.

Link to maintain same d.c. ground potential

Using Ground Plane

- To reduce common impedance coupling and promote return current to flow as near as source current, ground plane should be used wherever possible.
- Ground plane has much lower partial self inductance and resistance as compared to ground trace. Thus common impedance effect is vastly reduced.
- Source and return current near each other results in small loop area, this in turn reduces mutual inductance between different current loop.

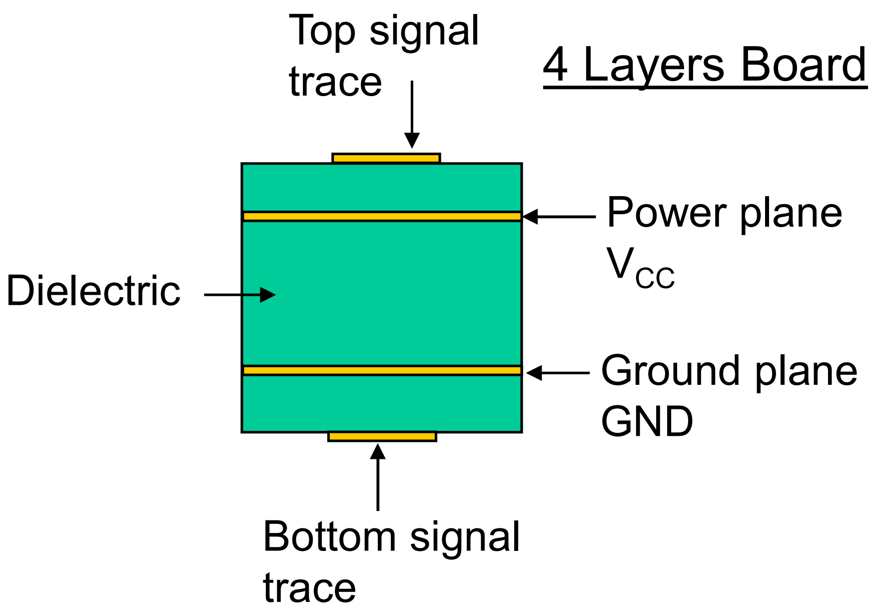


'Flooded' ground on top side and ground plane on bottom side of PCB to ensure return current follows the signal current closely. A GND plane is on the bottom to provide further isolation.

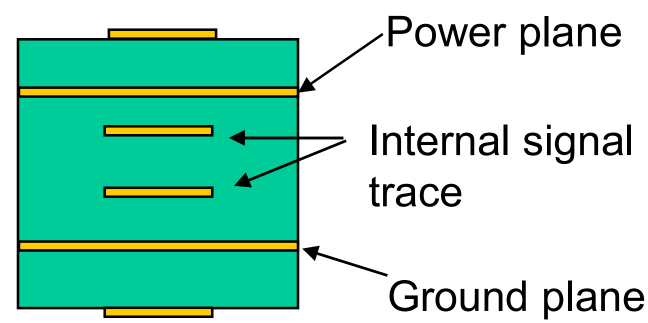
Using Multi-Layer PCB

- The advantages:
- More trace layers for routing.
- Can minimize crosstalk by having critical traces on different trace layers isolated by conducting planes, or having the critical traces perpendicular to each other.
- The GND and Power planes provide the return path, return current flows near source current.
- The planes have low self impedance.
- The planes serve to isolate traces (top and bottom trace layer).
- The planes form a good decoupling capacitor.

Some Suggestions for Layer Stacking in Multi-layer PCB



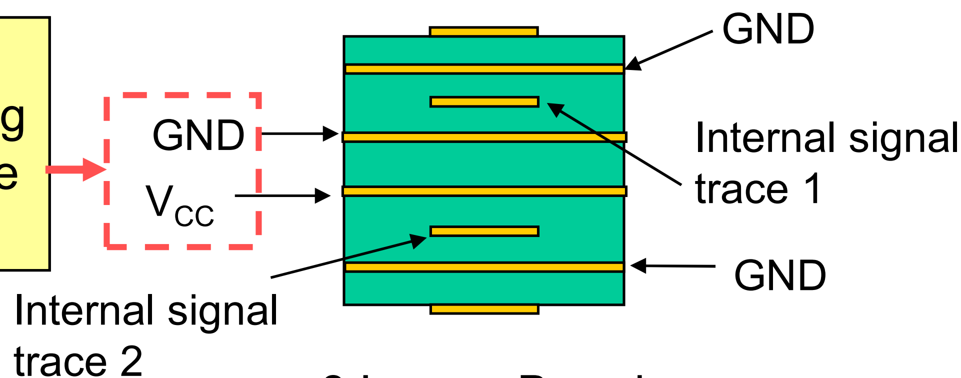
4 Layers Board



6 Layers Board

Use Top and Bottom traces for high-speed signals. The planes serve to isolate the high-speed traces.

These form a good decoupling capacitor for the power supply

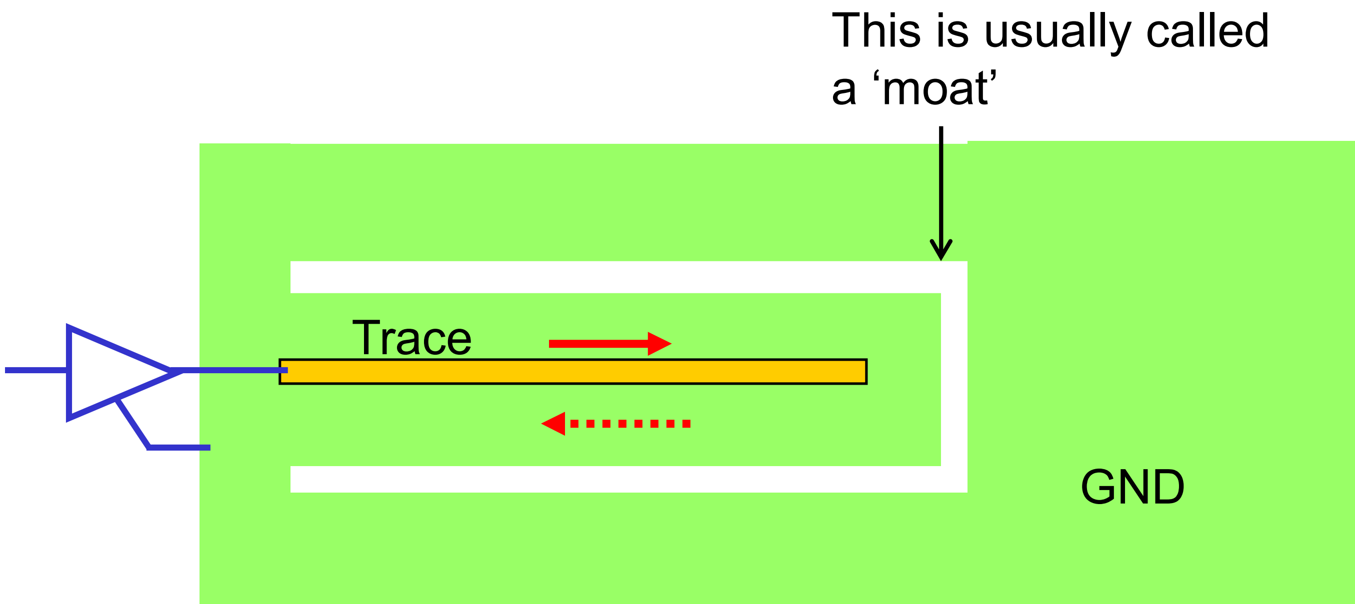


8 Layers Board

Use internal signal trace 1 for high-speed signals. These internal trace acts as striplines, with the added benefits of very low dispersion.

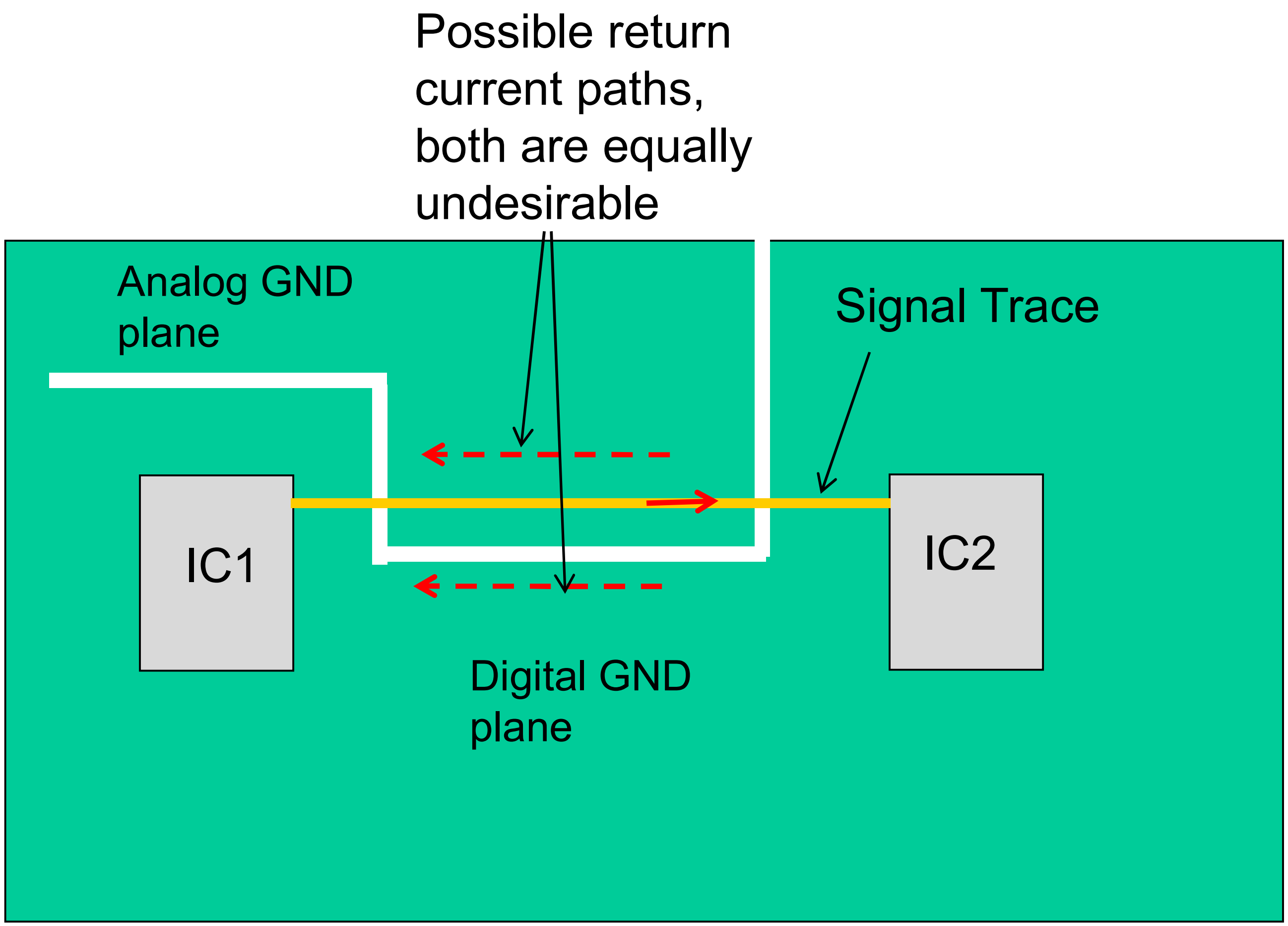
Example 4.2 - Isolating Noisy Return Current

- If there are only a few traces that carry high-speed signal, we can control the flow of the return current by removing part of the GND conductor.



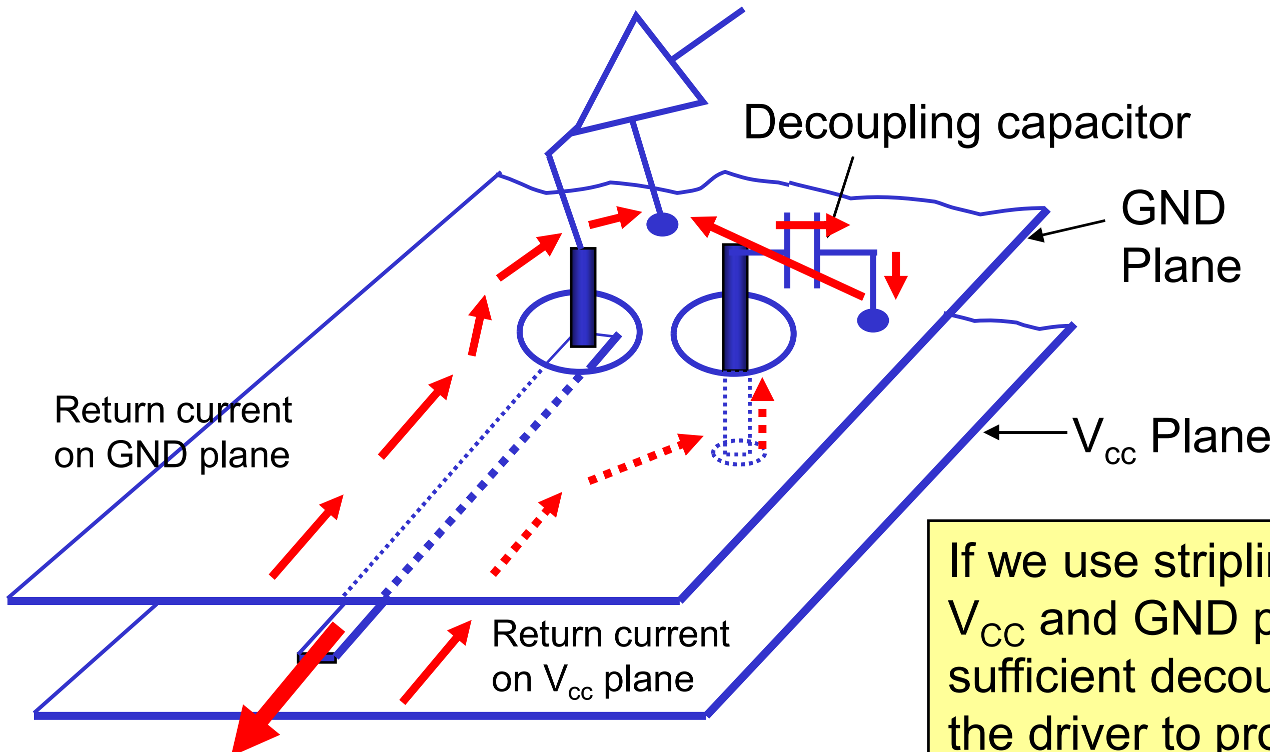
Top View

Example 4.3 – Signal Trace Crossing Unrelated GND Plane



Return Current Path for Multi-Layer PCB (1)

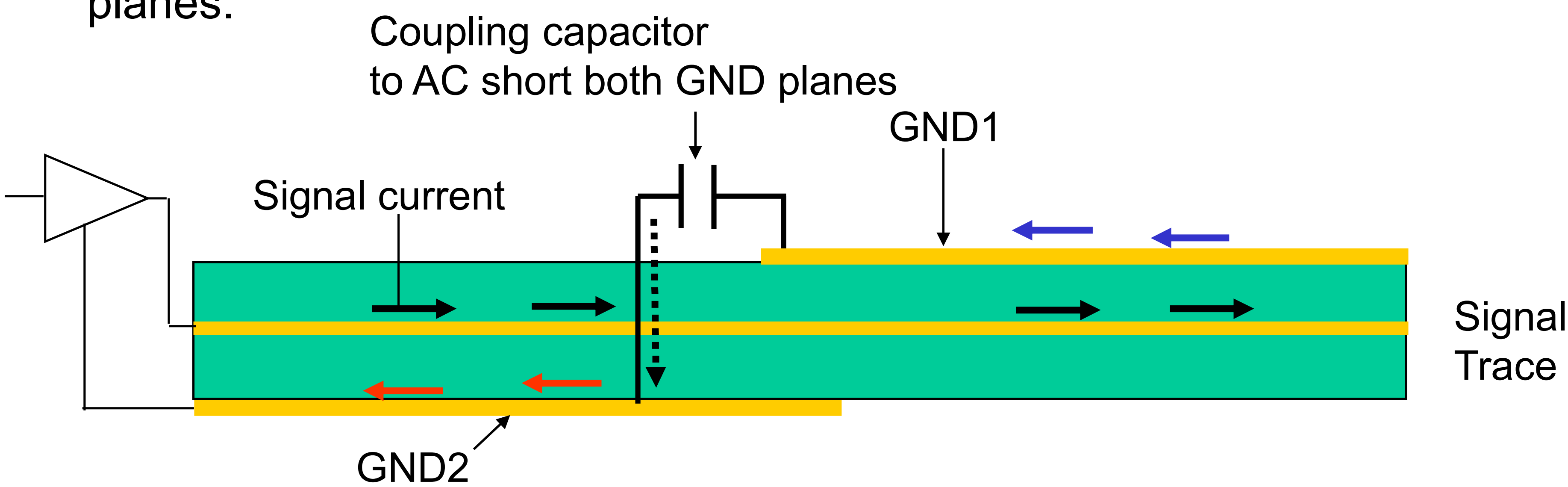
- For a signal trace which is sandwiched by two conducting planes, the return current exist on both planes.



If we use stripline configuration with V_{CC} and GND planes, always place sufficient decoupling capacitors near the driver to provide an AC short between both planes.

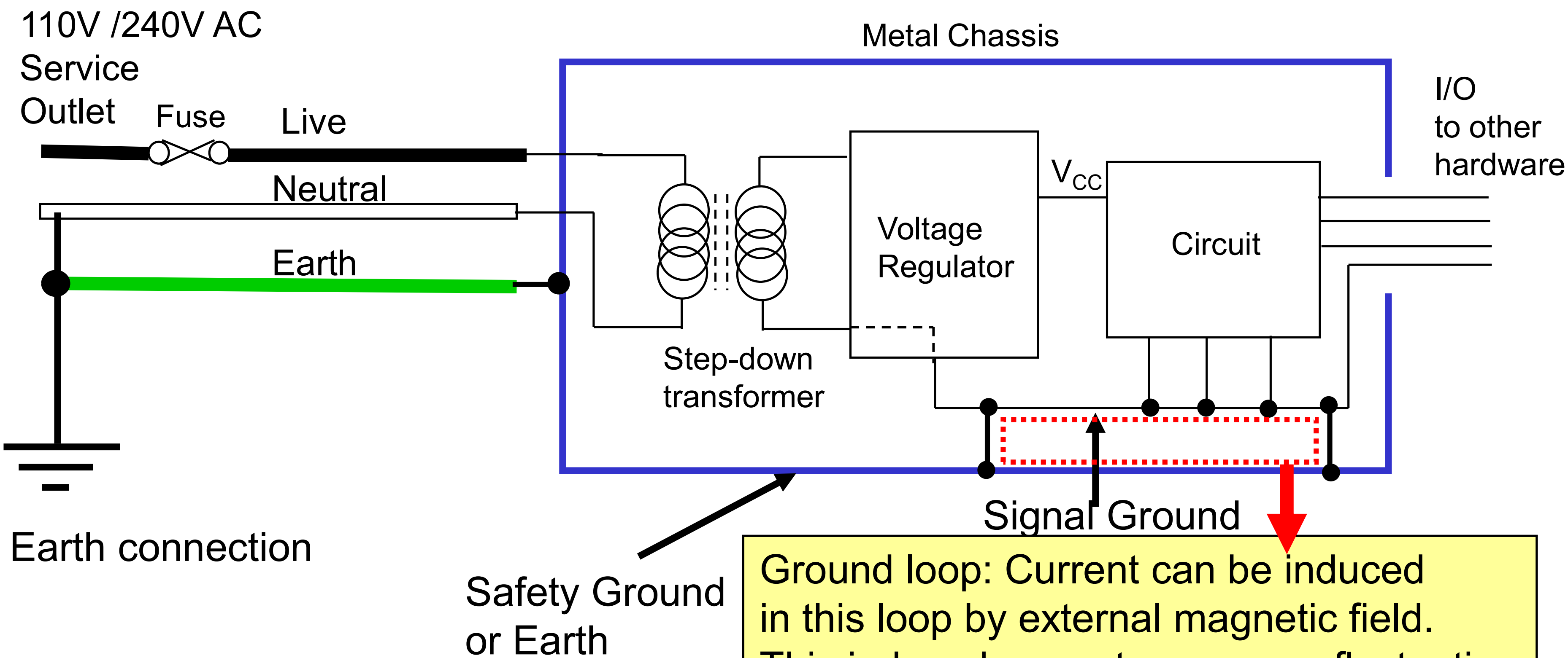
Return Current Path for Multi-Layer PCB (2)

- There are occasions when the return current has to switch GND planes.



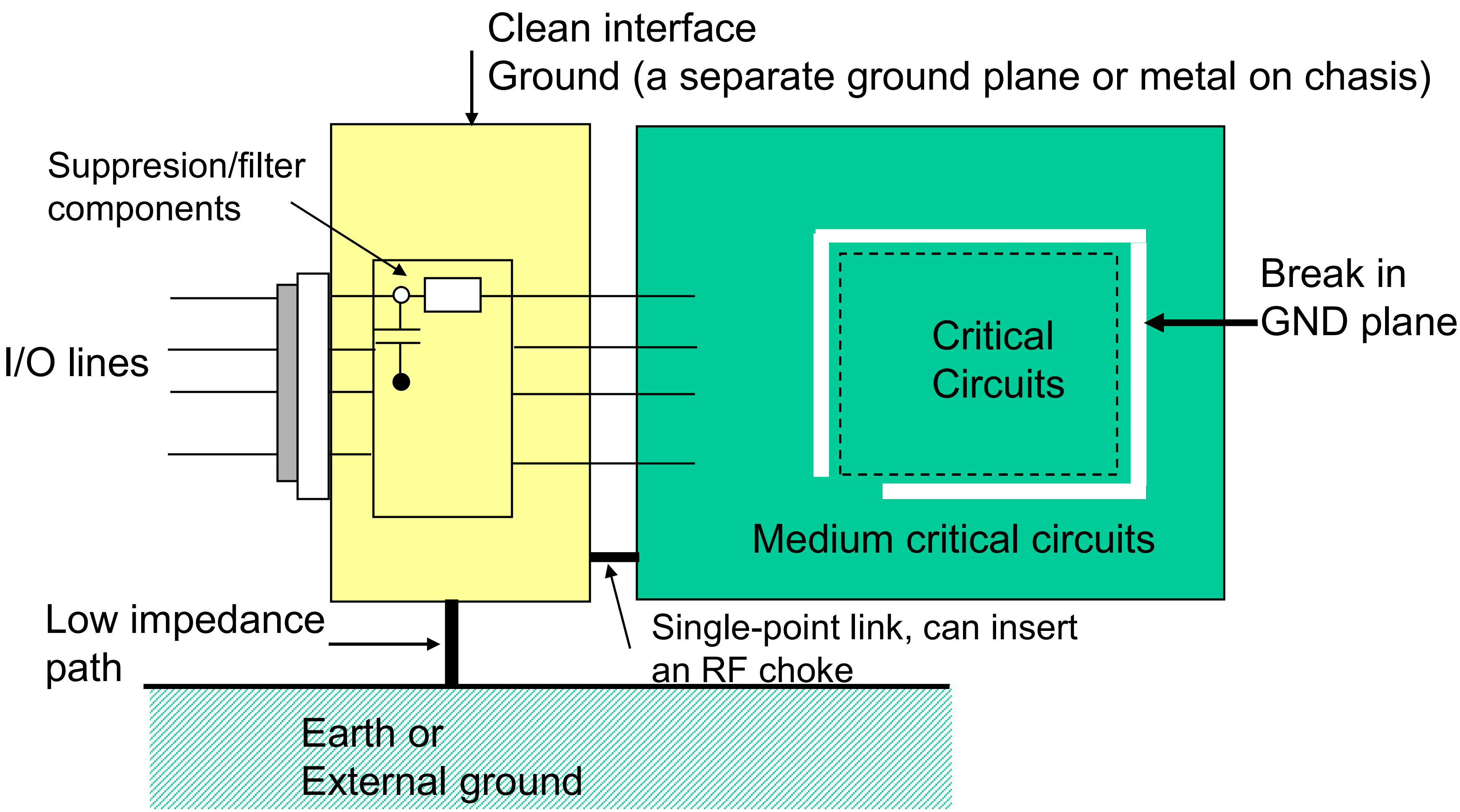
Example 4.4 - Minimizing Noise on Sensitive Circuits: Preventing Unwanted GND Current

- Be careful of accidental current loop due to multi-point ground connections.



Ground loop: Current can be induced in this loop by external magnetic field. This induced current can cause fluctuation of GND potential and stray current to flow into the circuit (common-mode current).

Example 4.5 - Minimizing Noise on Sensitive Circuits: Connecting I/O Lines to Outside World



Grounding Rules

- Identify circuits with high rate-of-change (di/dt, dv/dt, for emissions), e.g. clocks, bus buffers/drivers and high-power oscillators.
- Identify sensitive circuits (for susceptibility), e.g. low-level analog signal or high-speed digital data.
- Ensure that return current of circuits with high rate-of-change do not interfere with sensitive circuits by:
  - checking that each signal trace current has a 'convenient' return path to its source.
  - preventing return current from crossing regions.
  - minimizing current loops.
- Minimize ground impedance by 1) Keeping sensitive circuits away from the edge of the PCB, 2) Minimize loop area, 3) Use ground plane.
- Ensure that internal and external ground noise cannot couple in or out of the system, incorporate a clean interface ground.
- Segmentation of circuits and ground.
- No crossing of signal trace from one region to another.

More Resources

- **“How to Design for Power Integrity: Finding Power Delivery Noise Problems” by Keysights (Jun 2015)**
- https://www.youtube.com/watch?v=oL6qjhJH_m4&feature=youtu.be

Other Topics of Interests in this Part

- Here are some other topics that are deemed important but are not covered due to time constraint:
- Power supply noise filtering and decoupling.
- Simultaneous switching noise.
- Placement and selection of capacitors for decoupling.
- Decoupling performance analysis.
- Using active voltage regulator onboard PCB.

Key Learning of Part 4

- Concept of discontinuity in interconnection or transmission line.
- Equivalent electrical circuits of discontinuities.
- Effect of discontinuities on electrical signal propagation along interconnection.
- How to compensate for the electrical effects of discontinuities.
- Types of grounding schemes.
- Concept of current return path – high and low-frequency conditions.
- Common-impedance coupling.
- Ground break and it’s effect.
- Usage of decoupling capacitors.
- Usage of multi-layer PCBs and conductor layers stacking.