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# **INTRODUCTION TO PHASE-LOCKED LOOP AND FREQUENCY SYNTHESIZER**

## **Part 2**

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## **3 – Dynamic Behavior of the PLL in Tracking Mode**

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## Introduction (1)

- In the previous section we have examined the voltage, frequency and phase along the PLL system under phase-locked condition with input signal  $v_{in}$  remains unchanged. This is called the **static condition**.
- In most real applications, the input signal frequency changes over time, most of the time rapidly.  
Corresponds to DC analysis
- Under this condition the PLL's VCO will continuously tracks  $v_{in}$ 's frequency. Thus the voltages, frequency and phase along the PLL system changes with time, they vary corresponding to the changes in  $v_{in}$ .
- This is called **dynamic condition of the PLL**. Corresponds to AC analysis
- Apart from knowing the static behavior of the PLL, like what is the lock-range and the static phase error, we are also interested in the dynamic behavior of the PLL under dynamic condition.
- For instance if the input frequency  $f_{in}$  is suddenly changed from 10 MHz to 15 MHz, we want to know how long it takes for the PLL to lock to the new input frequency and whether there is any long-term error.

## Introduction (2)

- When the variation of  $v_{in}$  over time is sufficiently small, i.e. under **small-signal** condition, the PLL will always remain in phase-locked and its behavior can be represented by a **linear mathematical model**.
- This concept is similar to, for instance the transistor amplifier, where for small voltage and current fluctuation we can replace the amplifier with small-signal equivalent circuit.

## 3.1 – Linear Model of the PLL in Tracking Mode

### PLL Linear Model (1)

- Under tracking mode, a PLL can be modeled as a linear system assuming instantaneous variation of the phase along the system to be small.
- The direct approach is to linearize the system equations describing the PLL.

Consider the 1st order analog PLL with mixer type PD and no loop amplifier (see Example 2.4.1):  $\frac{d}{dt}\theta_e = \Delta\omega - 2\pi k_\phi k_o \sin \theta_e$

For small phase error  $\theta_e \ll 1 \text{ rad}$

$$\frac{d}{dt}\theta_e = \Delta\omega - 2\pi k_\phi k_o \sin \theta_e$$

Phase error      Frequency error  
 $\sin \theta \approx \theta$   
 $\theta \ll 1$

The nonlinear PLL system equation can be approximated by the linear form:  $\frac{d}{dt}\theta_e \cong \Delta\omega - 2\pi k_\phi k_o \theta_e$

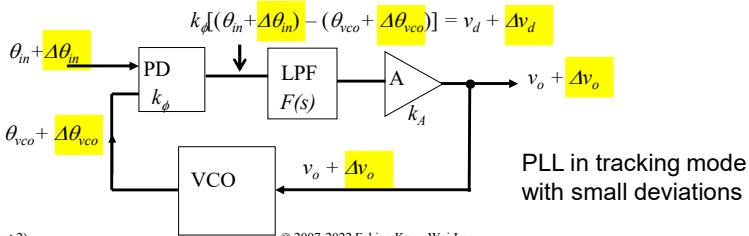
Using  $\Delta\omega_o = \frac{d\theta_o}{dt} = 2\pi k_o v_o$  and Laplace Transformation:

$$s\theta_e(s) = 2\pi k_o V_o(s) - k_\phi k_o \theta_e(s) \quad \rightarrow \quad \frac{\theta_e(s)}{V_o} = \frac{2\pi k_o}{s + k_\phi k_o} \quad (3.1.1)$$

Linear system equation (Transfer function) for zeroth order PLL 6

## PLL Linear Model (2)

- Alternatively, we can linearize each and every component of the PLL at a reference point.
- Initially assume the PLL to be in tracking mode, i.e. the PLL is locked to an input  $v_{in}(t)$  at fixed frequency  $f_{in}$ . The phase along the system would be constant.
- If  $f_{in}$  is varied from its steady-state value by a small amount  $\Delta f$ , all the parameters within the PLL will also vary by a small amount, as shown below.
- Let  $\Delta\theta_{vco}$ ,  $\Delta\theta_{in}$ ,  $\Delta v_d$ ,  $\Delta v_o$  be the deviations from steady state.



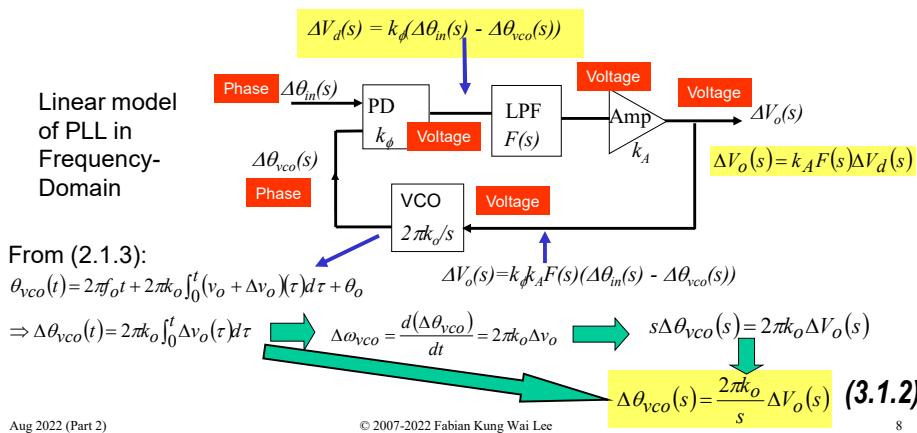
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## PLL Linear Model (3)

- Now let us focus only on the small deviations on each block.
- Applying the Laplace transformation, the following ‘small-signal’ or linear model of the PLL can be obtained.



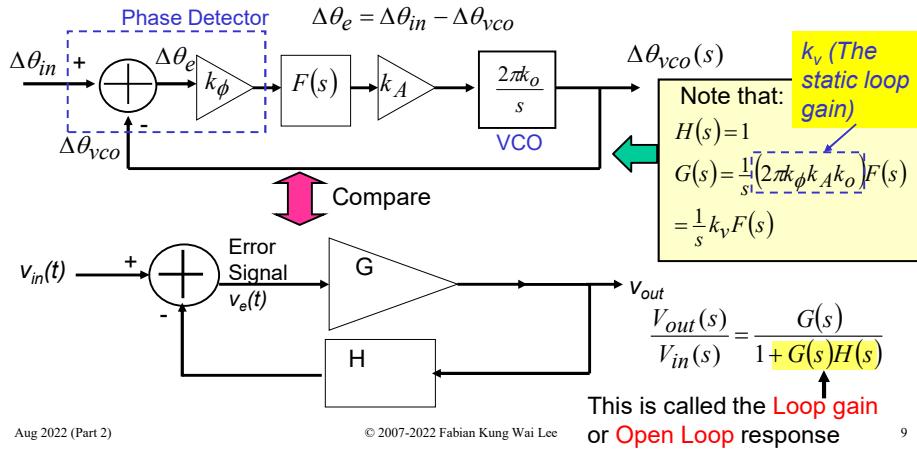
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## PLL Linear Model (4)

- The block diagram is rearranged as shown. Note the similarity to a conventional negative feedback system, which allow us to easily derive the linear transfer function.



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## PLL Linear Model (5)

- From the previous slide and using the concepts of feedback system, the Loop Gain (open loop) of the PLL is:

$$G(s)H(s) = \frac{1}{s} k_v F(s) \quad (3.1.3)$$

Open loop response

- While the Transfer Function (closed-loop) of the PLL is:

$$\frac{\Delta\theta_{vco}(s)}{\Delta\theta_{in}(s)} = \frac{G(s)}{1 + G(s)H(s)} = \frac{k_v F(s)}{s + k_v F(s)} \quad (3.1.4)$$

Close loop response

Using (3.1.2):

$$\Delta\theta_{vco}(s) = \frac{2\pi k_o}{s} \Delta V_o(s)$$

$$\text{Where } k_v = 2\pi k_o k_\phi k_A$$

Characteristic equation

Using:  $f = \frac{s\theta}{2\pi}$

$$\frac{\Delta V_o(s)}{\Delta\theta_{in}(s)} = \frac{s k_\phi k_A F(s)}{s + k_v F(s)}$$

$$(3.1.5a)$$

These are alternative forms of the close loop response for PLL which are more practical

$$\frac{\Delta V_o(s)}{\Delta f_{in}(s)} = \frac{2\pi k_\phi k_A F(s)}{s + k_v F(s)}$$

$$(3.1.5b)$$

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## Classification of PLL Response by Loop Gain - Type I and Type II PLLs

- From the previous slides we note that the Loop Gain (i.e.  $G(s)H(s)$ ) of the PLL contains at least a pole at  $s = 0$  in the complex plane (see equation (3.1.3)).
- Sometimes depending on the expression of  $F(s)$  and  $k_v$ , one or more extra poles are introduced into the Loop Gain at the origin.
- Traditionally, PLL with Loop Gain having 1 pole at the origin is called **Type I PLL**.
- Similarly PLL with Loop Gain having 2 poles at the origin is known as **Type II PLL**, and so on.
- This kind of classification is important as the poles of the Loop Gain at origin determines the steady-state error of the feedback system [9].

Type 0 response implies no zero at the origin

$$\text{Type I response } G(s)H(s) = \frac{K_1}{s(s^2 + \alpha_1^2)}$$

$$\text{Type II response } G(s)H(s) = \frac{K_2}{s^2(s^2 + \alpha_2^2)}$$

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## Classification of PLL by Transfer Function – PLL Order (1)

- At times PLL can also be classified according to the **order** of the Close-Loop Gain or Transfer Function's denominator.
- For instance if  $k_v$  is a constant, and  $F(s) = 1$ , then it is a First Order PLL.

$$\frac{\Delta\theta_{vco}(s)}{\Delta\theta_{in}(s)} = \frac{G(s)}{1 + G(s)H(s)} = \frac{k_v F(s)}{s + k_v F(s)} = \frac{k_v}{s + k_v} \quad \leftarrow \text{No. of poles} = 1$$

Nominator      Denominator

- Similarly we would have Second and Third Order PLL should  $k_v$  or  $F(s)$  depends on complex frequency  $s$ .
- We will look at some examples in the next section.

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## Classification of PLL by Transfer Function – PLL Order (2)

- For instance:

$$\frac{G(s)}{1+G(s)H(s)} = \frac{K_1}{s^2 + a_1 s + a_2}$$

2<sup>nd</sup> order response

$$\frac{G(s)}{1+G(s)H(s)} = \frac{K_2(s+b_0)}{(s+\alpha)(s^2 + a_1 s + a_0)} = \frac{K_2(s+b_0)}{s^3 + a_2 s^2 + a_1 s + a_0}$$

3<sup>rd</sup> order response

Nominator

  $K_2(s+b_0)$

Denominator

Note: Classification according to Loop Gain tells us the steady-state behaviour of the system (Type I or higher system has 0 steady-state error for step input), while classification using Transfer Function provide clues to the dynamic behaviour of the system (stable or not, got ringing or not etc). Both are useful. Next section provides a basic review.

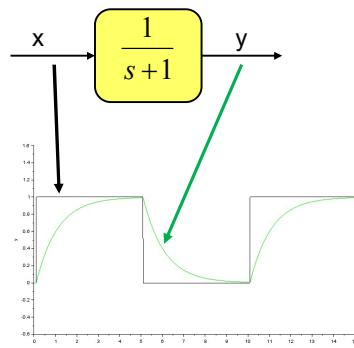
## 3.2 – Review of (Classical) Feedback Control

 Extra

**Extra**

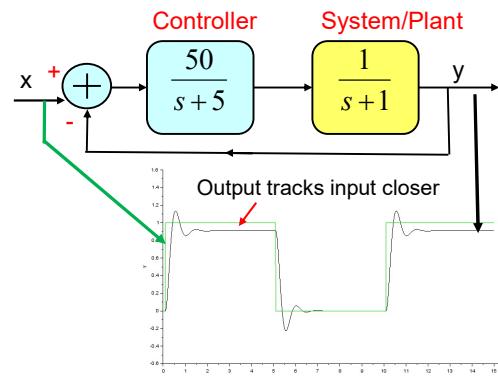
## Why Use (Negative) Feedback? (1)

An open-loop system (or plant)



For instance the plant is an electric motor,  $x$  is a voltage input,  $y$  represents the output torque of the motor.

A closed-loop system with negative feedback and controller



Adding negative feedback and controller can improve the response of the system

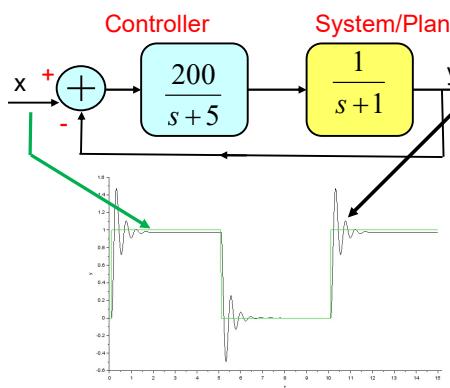
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## Why Use (Negative) Feedback? (2)

Increasing the gain of the controller, the steady-state error is decreased, but we notice a higher overshoot and undershoot



Thus including a carefully crafted controller and negative feedback into a system, we can affect:

1. Transient response (how fast, overshoot, undershoot, how long).
2. Steady-state error, and
3. The stability.

Other reasons of adding feedback control is to improve the immunity of the system to external noise and internal parameters deviation.

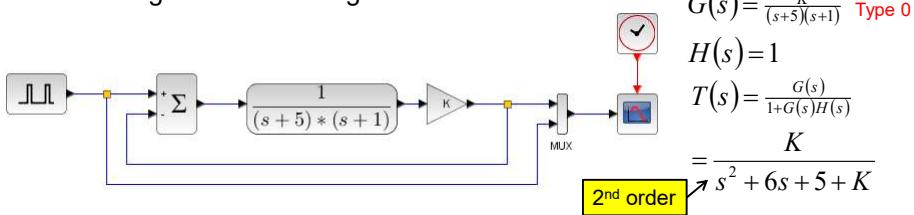
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## Feedback (FB) Control System Properties

- For a linear system the **Transfer Function** is used to relate the input and output. To simplify our discussion we will use a feedback system with 2<sup>nd</sup> order transfer function to illustrate.
- Most systems with order higher than 2 can be approximated by a 2<sup>nd</sup> order system in the frequency range of interest.
- Most of us are familiar with Simulink for MATLAB, which can be used to model a dynamical system. Here we will use the open-source equivalent, Scilab ([www.scilab.org](http://www.scilab.org)) to simulate our control system model. Below is a block diagram model using Scilab's Xcos simulator.



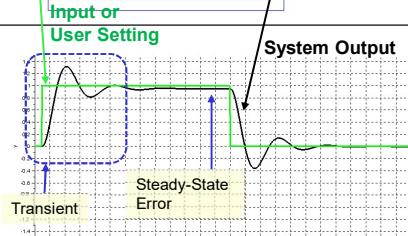
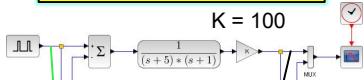
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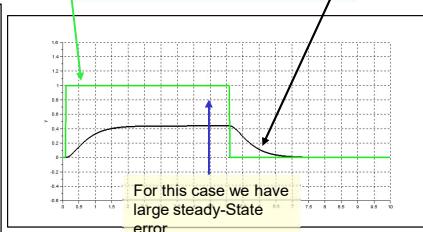
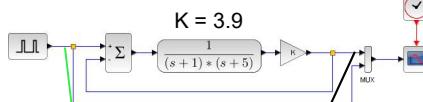
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## Time-Domain Response - Transient, Steady-State Error and Stability (1)

Typical Stable Response (Under-damped)



Typical Stable Response (Over-damped)

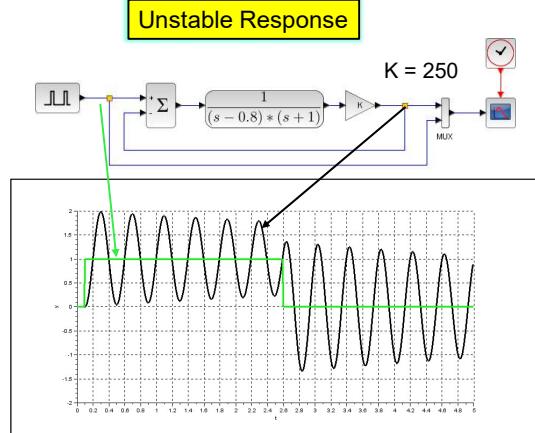


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## Time-Domain Response - Transient, Steady-State Error and Stability (2)



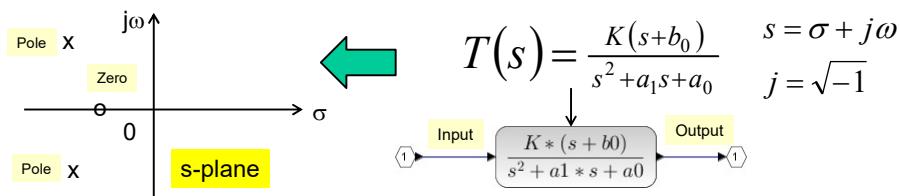
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## General Linear Second Order Feedback System (1)

- The transfer function of a linear system can be expressed as a rational polynomial in terms of  $s$  (the complex frequency in Laplace Transform).
- Consider a typical 2<sup>nd</sup> order system transfer function :



- This system contains 2 poles and a zero. The poles and zeros can be plotted on a complex plane, and their location affects the system behavior in the time-domain, e.g. whether the system is stable or unstable, and if stable whether the response is under-damped, critically damped or over damped.

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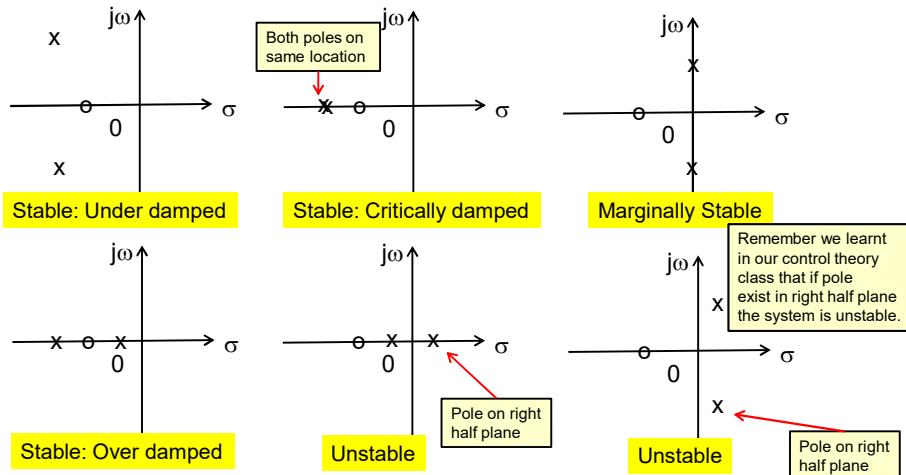
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## Poles-Zeros Location and System Behavior

**Extra**



## Analysis of 2<sup>nd</sup> Order System – Time Domain Response (1)

- In the spirit of **Control Theory**, the 2<sup>nd</sup> order **characteristic equations**, or the denominator polynomial in  $s$  of the transfer function is usually written in the following 'standard' form (also known as the **Canonical Form**) (see [2], [9]):

$$s^2 + a_1 s + a_0 = s^2 + 2\delta\omega_n s + \omega_n^2 \quad (3.2.1a)$$

$$\omega_n = \sqrt{a_0} \quad \text{Damping factor} \quad \text{Natural frequency}$$

$$(3.2.1b) \quad (3.2.1c)$$

$$\delta = \frac{a_1}{2\sqrt{a_0}} \quad (3.2.1c)$$

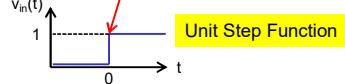
- This can be factored as follows, providing 2 roots, the roots can be real values or complex:

$$s^2 + 2\delta\omega_n s + \omega_n^2 = \left(s + \delta\omega_n + \omega_n \sqrt{\delta^2 - 1}\right) \left(s + \delta\omega_n - \omega_n \sqrt{\delta^2 - 1}\right) \quad (3.2.1d)$$

## Analysis of 2<sup>nd</sup> Order System – Time Domain Response (2)

- Now consider a 2<sup>nd</sup> order system with 1 zero, excited by a step input at  $t = 0$ , as shown below.

$$H(s) = \frac{as+b}{s^2 + 2\omega_n\delta s + \omega_n^2} = \frac{V_o(s)}{V_{in}(s)}$$



- Thus:

$$V_o(s) = \frac{(as+b)}{s^2 + 2\omega_n\delta s + \omega_n^2} V_{in}(s) = \frac{(as+b)}{s(s^2 + 2\omega_n\delta s + \omega_n^2)} \quad (3.2.2)$$

$$\Rightarrow V_o(s) = \frac{as+b}{s(s+\delta\omega_n + \omega_n\sqrt{\delta^2-1})(s+\delta\omega_n - \omega_n\sqrt{\delta^2-1})}$$

## Analysis of 2<sup>nd</sup> Order System – Time Domain Response (3)

- Taking the inverse Laplace Transform of (3.2.2), the response of the system to step input takes various forms depending on the value of  $\delta$ :

For  $\delta < 1$  (under damped):

$$v_o(t) = \left\{ \frac{b}{\omega_n^2} + \frac{e^{-\omega_n\delta t}}{j2\omega_n^2\sqrt{1-\delta^2}} \left[ \begin{array}{l} \frac{(b-a\omega_n\delta)-j(a\omega_n\sqrt{1-\delta^2})}{\delta+j\sqrt{1-\delta^2}} e^{-j\omega_n\sqrt{1-\delta^2}t} \\ \frac{(b-a\omega_n\delta)+j(a\omega_n\sqrt{1-\delta^2})}{\delta-j\sqrt{1-\delta^2}} e^{j\omega_n\sqrt{1-\delta^2}t} \end{array} \right] \right\} U(t) \quad (3.2.3a)$$

For  $\delta = 1$  (critically damped):

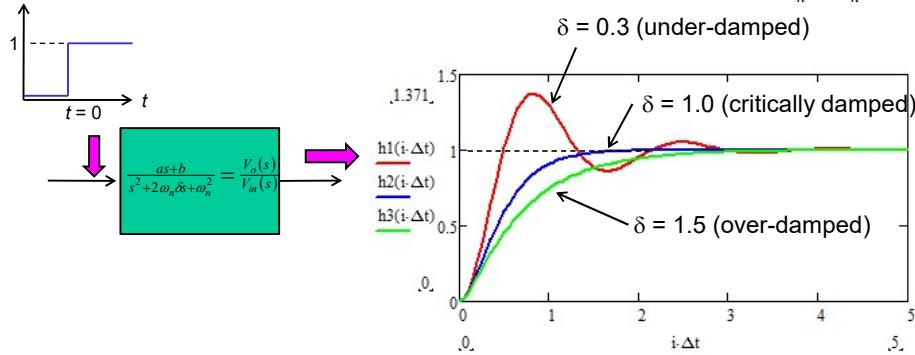
$$v_o(t) = \frac{b}{\omega_n^2} \left\{ 1 - e^{-\omega_n t} \left[ \frac{\delta - \frac{a}{\omega_n}}{\sqrt{1-\delta^2}} \sin(\omega_n \sqrt{1-\delta^2} t) - \cos(\omega_n \sqrt{1-\delta^2} t) \right] \right\} U(t) \quad (3.2.3b)$$

For  $\delta > 1$  (over damped):

$$v_o(t) = \left\{ \frac{b}{\omega_n^2} + \frac{e^{-\omega_n\delta t}}{2\omega_n^2\sqrt{\delta^2-1}} \left[ \frac{b-a\omega_n(\delta+\sqrt{\delta^2-1})}{\delta+\sqrt{\delta^2-1}} e^{-\omega_n(\sqrt{\delta^2-1})t} + \frac{-b+a\omega_n(\delta-\sqrt{\delta^2-1})}{\delta-\sqrt{\delta^2-1}} e^{\omega_n(\sqrt{\delta^2-1})t} \right] \right\} U(t) \quad (3.2.3c)$$

## Analysis of 2<sup>nd</sup> Order System – Time Domain Response (4)

- Example of time-domain plot using (3.2.3) for a 2<sup>nd</sup> order system excited by a unit step function is shown below, for the special case of  $a = 0$ , with:  
 $b = \omega_n^2$     $\omega_n = 4$



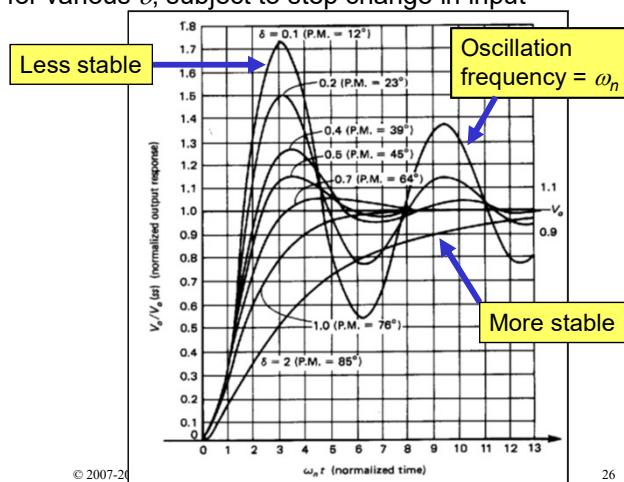
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## Analysis of 2<sup>nd</sup> Order System – Time Domain Response (5)

- Here we plot the normalized output of  $v_o(t)$  of the 2<sup>nd</sup> order system versus normalized time ( $\omega_n t$ ) for various  $\delta$ , subject to step change in input frequency  $f_{in}$ :



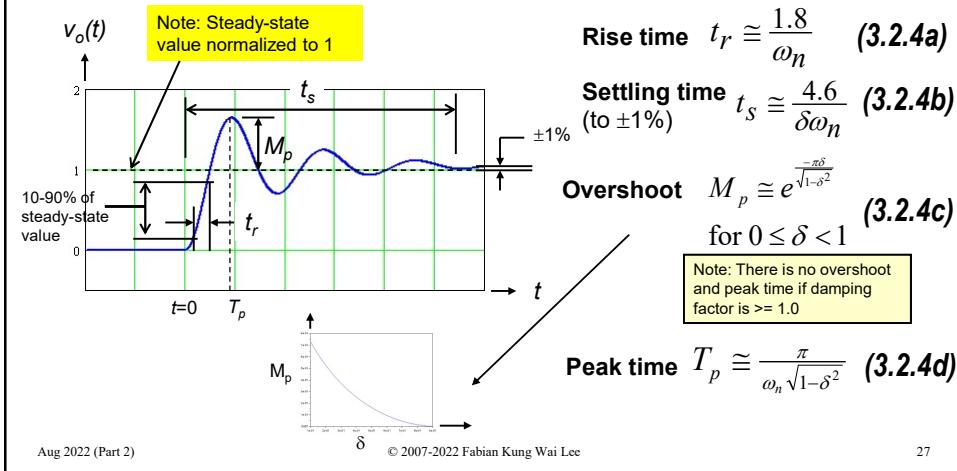
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## Common Benchmarks for Transient and Steady-State (1)

- The time-domain response of 2<sup>nd</sup>-order system depends on the damping factor  $\delta$  and natural frequency  $\omega_n$  [9]:



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## Common Benchmarks for Transient and Steady-State (2)

- The rise time and settling time relate to how fast the system can respond to external stimulus.
- Also for certain FB control system there exist a non-zero difference between the steady-state output and the user setting.
- The overshoot relates to the stability of the system. A less stable system has larger overshoot (and undershoot), the damped oscillatory trail after the overshoot is usually called **ringing**.
- In the case of unstable system the ringing never subsides! Rendering the system unusable.

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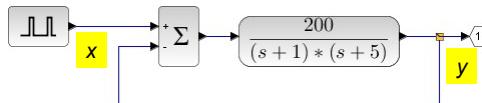
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**Extra**

## Example 3.2.1

- Consider a negative FB system as shown below.
- Find the closed loop transfer function, and estimate the overshoot and 1% settling time for the step input.



Here  $G(s) = \frac{200}{(s+1)(s+5)}$   $H(s) = 1$

Therefore  $T(s) = \frac{Y(s)}{X(s)} = \frac{G(s)}{1+GH(s)} = \frac{200}{s^2 + 6s + 205}$   $a_0 = 205$   $a_1 = 6$

From (3.2.1)  $\omega_n = 14.318 \text{ rad/sec}$   $\delta = 0.210$

From (3.2.4)  $t_s \cong \frac{4.6}{\delta\omega_n} = 1.533 \text{ sec}$   $M_p \cong e^{\frac{-\pi\delta}{1-\delta^2}} = 0.510$  or  $M_p \cong 51\%$

**Extra**

## Frequency Response (1)

- We have seen in Section 1 that for linear time-invariant (LTI) system, when the input is a continuous sine function of time, the output is also a sine function with the same frequency.
- As sinusoidal functions can be expressed in phasor form, the transfer function is generally a complex number.
- Hence we can plot the magnitude and phase of the transfer function as the input frequency is varied. The generated plot is called **Frequency Response** plot.
- The frequency response plot provides information on the system steady-state output when the input is a continuous sine function.
- There are many ways to combine the information from magnitude, phase, and frequency in the frequency response plots. Examples of frequency response plots are **Bode** plot, **Nyquist** diagram and **Nichols/Blackman** chart. Here we will only discuss Bode and Nyquist plots.

**Extra**

## Frequency Response (2)

- Frequency response plots can be applied to higher-order feedback systems, or when we do not know the exact mathematical model of the physical system.
- For example the data for Bode plot can be obtained experimentally via measurements.
- The damping factor  $\delta$  and natural frequency  $\omega_n$  can be estimated from the frequency response plot, which then yield important parameters like rise time, overshoot, settling time and stability.

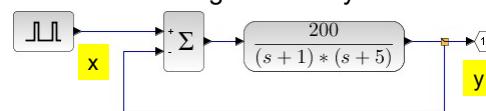
NOTE:

In this class we will use frequency response approach (Bode plot) as our primary tools to analyze and design our PLL/Frequency Synthesizer

**Extra**

## Example 3.2.2

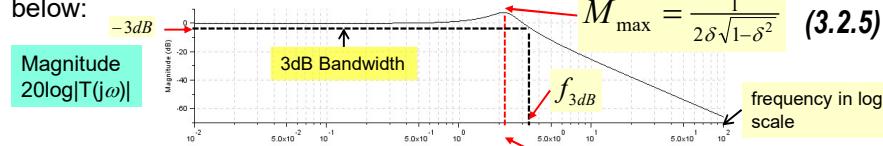
- Consider the negative FB system from Example 3.2.1 again:



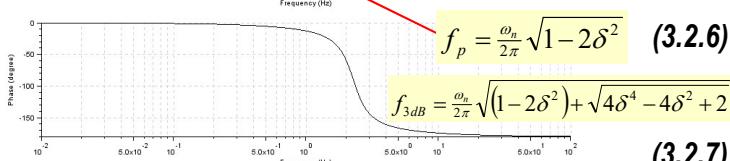
$$G(s) = \frac{200}{(s+1)(s+5)} \quad H(s) = 1$$

$$T(s) = \frac{Y(s)}{X(s)} = \frac{G(s)}{1+GH(s)} = \frac{200}{s^2 + 6s + 205}$$

- The Bode plot of the transfer function from 0.01 Hz to 100 Hz is shown below:



Phase  
 $\angle T(j\omega)$  in  
degrees



$$f_{3dB} = \frac{\omega_n}{2\pi} \sqrt{(1 - 2\delta^2) + \sqrt{4\delta^4 - 4\delta^2 + 2}} \quad (3.2.7)$$

**Extra**

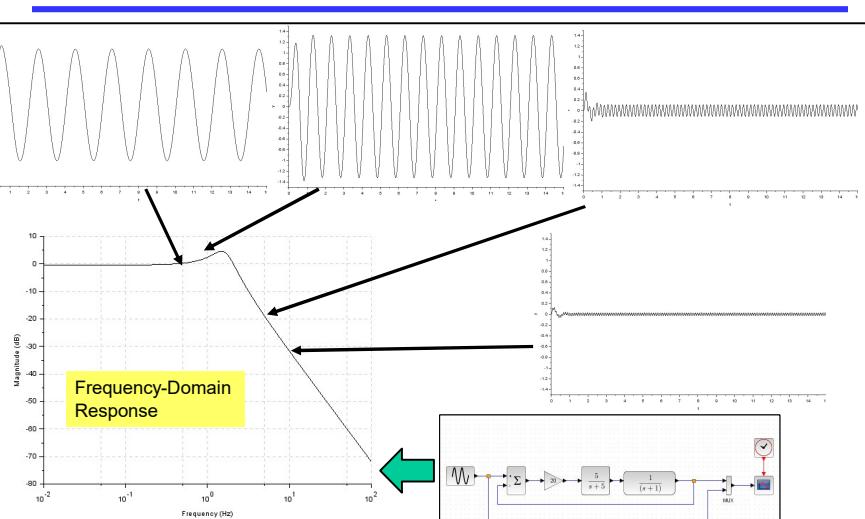
## Frequency Response (3)

- Thus we observe that for 2<sup>nd</sup> order system, the maximum magnitude  $M_{\max}$  and the corresponding frequency are related to damping factor and natural frequency exactly ( $M_{\max}$  only exists for  $\delta < 1$ ).
- Equations (3.2.5), (3.2.6) and (3.2.7) provide a way to extract  $\delta$  and  $\omega_n$  from the Bode plot. These can then be used to estimate the rise time, settling time and overshoot, and also check for stability.
- We can also get a rough estimate of the 3dB bandwidth of the FB system based on (3.2.7), as follows:

$$3\text{dB BW} \approx \begin{cases} \frac{\omega_n [\delta - \sqrt{\delta^2 - 1}]}{\omega_n \sqrt{1 - 2\delta^2}} & \delta \geq 1 \\ \frac{\omega_n}{\sqrt{1 - 2\delta^2}} & \delta < 1 \end{cases} \quad (3.2.8)$$

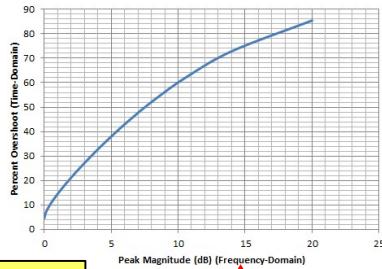
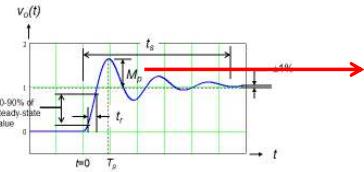
**Extra**

## Relationships Between Frequency and Transient Response (1)

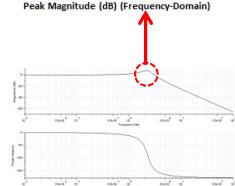


## Relationships Between Frequency and Transient Response (2)

**Extra**



1. Larger 'Peaking' of the magnitude response in frequency-domain leads to larger over-shoot (under-shoot) in step response in time-domain.



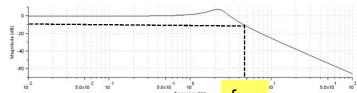
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## Relationships Between Frequency and Transient Response (3)

- Generally...



$$f_{3dB} \propto \omega_n$$

$$f_{3dB} \propto \frac{1}{t_s}$$



2. Bandwidth of the magnitude response in frequency-domain is inversely proportional to settling time.

$$f_{3dB} \propto \frac{1}{T_p}$$



3. Bandwidth of the magnitude response in frequency-domain is inversely proportional to peak time.

In a nutshell: Larger bandwidth in frequency-domain corresponds to faster response in time-domain

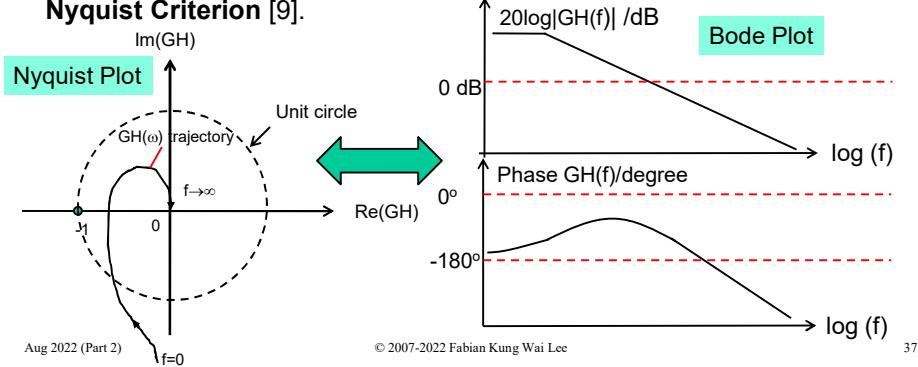
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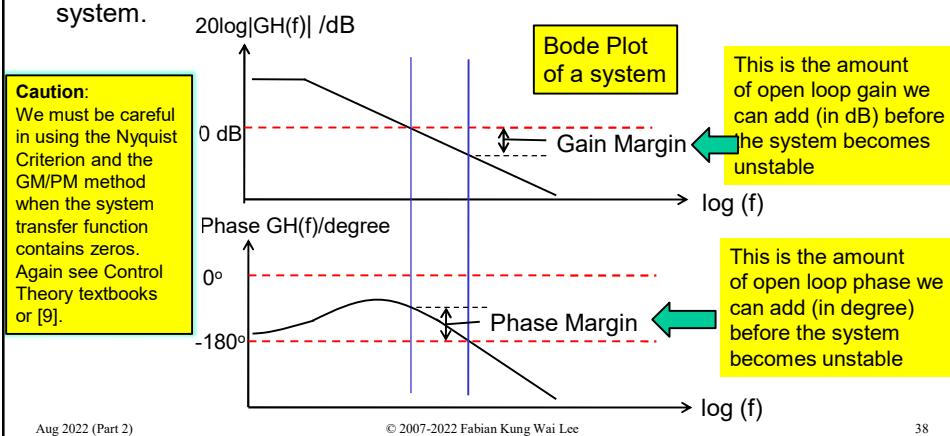
## Frequency Response and Stability – Gain and Phase Margin (1)

- The frequency response plots can also provide valuable information about the stability of the feedback system, and can be used to compare the relative stability of different systems using parameters such as **Gain** and **Phase Margins**.
- Bode plot or Nyquist diagram can be used for this purpose, based on **Nyquist Criterion [9]**.



## Frequency Response and Stability – Gain and Phase Margin (2)

- The Gain Margin (GM) is defined as the change in open-loop gain  $|GH|$  in dB, required when phase angle of  $GH$  is  $+180^\circ$  or  $-180^\circ$  to make the closed-loop system unstable. Negative GM indicates potentially unstable system.



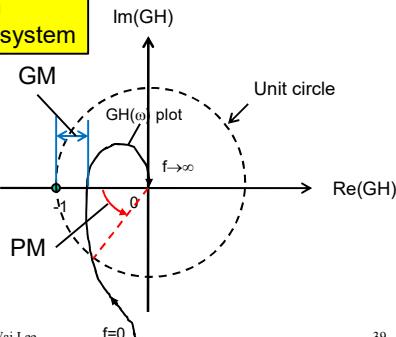
## Frequency Response and Stability – Gain and Phase Margin (3)

- The Phase Margin (PM) is the change in open-loop phase required at unity gain ( $|GH| = 1$ ) to make the closed-loop system unstable.
- The magnitude of GM and PM give an indication of how stable a system is and can be used to compare various feedback systems.
- For instance a good stability requires GM and PM of at least 10 dB and 45° respectively.

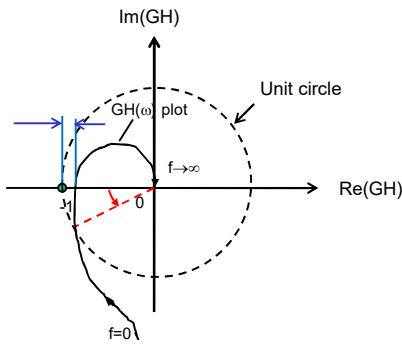
Nyquist Diagram  
of a closed-loop system

$$GH(\omega) = \frac{K}{j\omega(j\omega\tau_1 + 1)(j\omega\tau_2 + 1)}$$

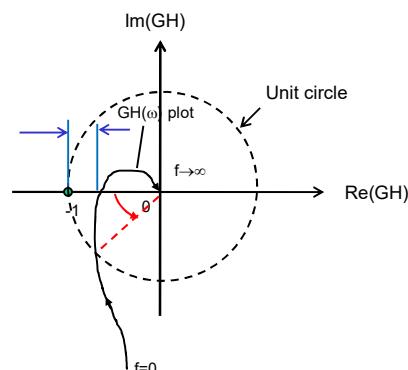
Note: The PM is related to the damping factor for 2<sup>nd</sup> order system, where a larger PM is associated with larger damping factor (see [9]).



## Frequency Response and Stability – Gain and Phase Margin (4)



Less Stable System  
- Smaller GM and PM



More Stable System  
- Larger GM and PM

**Extra**

## End Notes

- This is only a brief review, we did not discuss in details the concepts of compensation. That is when the system time-domain response is not satisfactory, we can influence it by adding a module in cascade or in the feedback path.
- Typical cascade compensation modules are lead, lag, lag-lead compensators, PD (proportional and differential), PI (proportional and integration) and PID compensators.
- Although we only focus on 2<sup>nd</sup> order FB systems, the formulae presented here are also useful for 3<sup>rd</sup> or higher order systems in the approximate sense, as long as a pair dominant pole exists. See [9] or any Control Theory textbooks.
- Finally what we have reviewed here is considered classical control theory, that applies to single-input-single-output (SISO) systems. Modern control methods use the techniques of State-Space and can be applied to MISO, MIMO systems.

## 3.3 – Time-Domain Response of PLL in Tracking Mode

### 3.3.1 – Digital PLL with Type 1 and Type 2 PD

## Digital PLL Using Type 1 and Type 2 PD

- Digital PLLs using Type 1 PD (XOR gate) and Type 2 PD (RS-FF or JK-FF) usually have **Type 1** loop gain.
- This means the Open-Loop Response (Loop Gain) has a pole at the origin.
- Using the various stability analysis tools in Control Theory, such as Root-Locus Plot, Bode Plot (to show gain and phase margin), Nyquist plot etc., we can show that the Type I PLL is inherently **stable**.
- In the next few slides we will show the time-domain response of digital PLL using XOR gate and RS-FF phase detector subject to variable input signal  $v_{in}$ .

Note: What do we mean by “stable”?

In a stable system, if you apply a small disturbance to the system, the effect of the disturbance will diminish with time. In unstable system, the effect will increase over time until the system ‘saturates’. Any definition of stable is bounded-input-bounded-output (BIBO). For LTI system, both definitions are equivalent.

## Simplified Model - 1st Order Transfer Function

- To simplify we initially assume the cutoff frequency of the LPF is much higher than the bandwidth of other loop components (We will see how to enforce this later). Consequently  $F(s) = 1$ .
- From (3.1.4), the transfer function obtained is called the 1st Order PLL, as it has only one pole.

$$\frac{\Delta V_o(s)}{\Delta \theta_{in}(s)} = \frac{sk_\phi k_A}{s + k_v}$$

Using  $f = \frac{s\theta}{2\pi} \rightarrow \Delta\theta = \frac{2\pi\Delta f}{s}$

$$\frac{\Delta V_o(s)}{\Delta f_{in}(s)} = \frac{2\pi k_\phi k_A}{s + k_v} = \frac{k_v / k_o}{s + k_v} \quad (3.3.1)$$

**Note that this is a Type I PLL since Loop Gain is:**

$$G(s)H(s) = \frac{1}{s} k_v F(s) = \frac{2\pi}{s} k_o k_\phi k_A$$

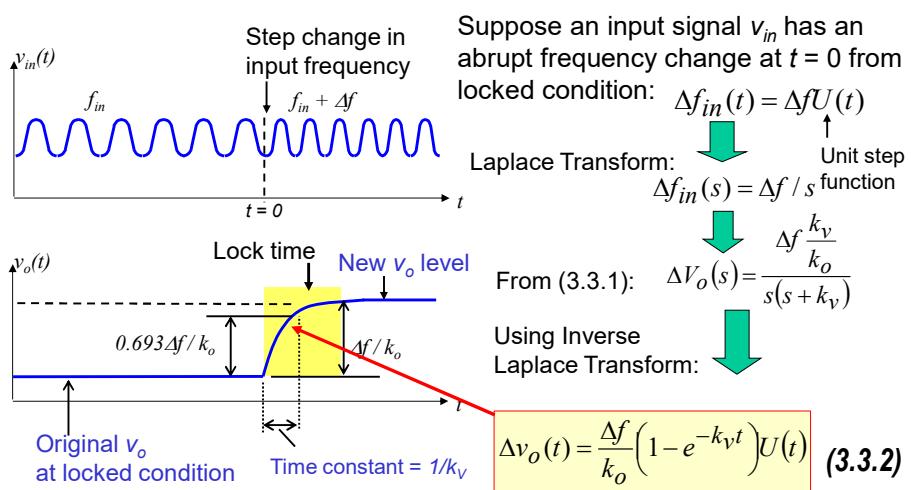
← 1 pole

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## Simplified Model - Time-Domain Response of 1st Order Transfer Function



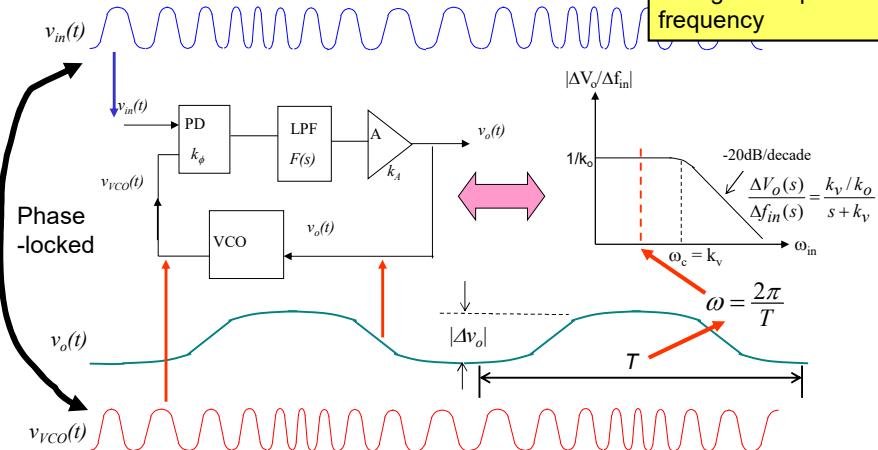
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## The Frequency Response of 1st Order Transfer Function (1)

The significance of  $k_v$  for 1<sup>st</sup> order PLL:



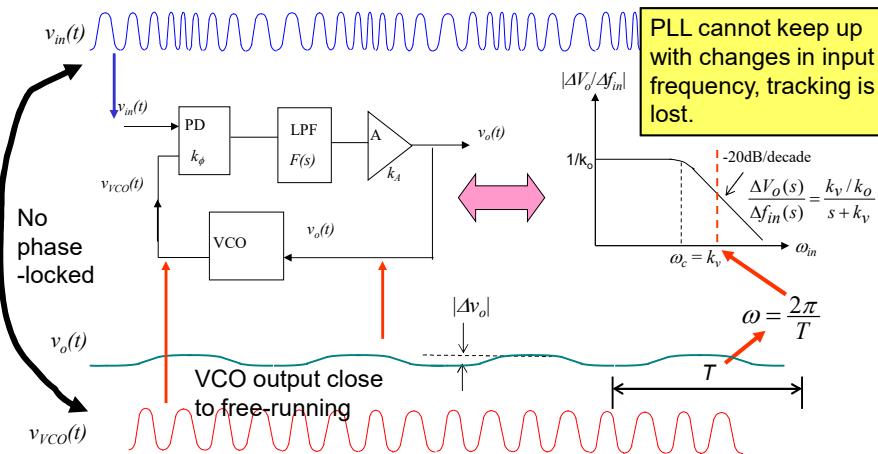
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## The Frequency Response of 1st Order Transfer Function (2)

The significance of  $k_v$  for 1<sup>st</sup> order PLL:



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## Improving the Time Domain Response (Loop Compensation) (1)

- The 1st order PLL time-domain response is controlled by  $k_v$ . The loop gain  $k_v$  also determines the lock or hold-in range.
- By lowering the cut-off frequency of the loop filter, we can use it to affect the dynamic response of the PLL.
- For instance when the loop filter is included into the Type 1 Digital PLL dynamic response, a 2<sup>nd</sup> order system is obtained:

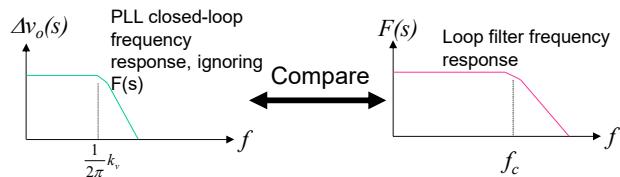
$$\frac{\Delta V_o(s)}{\Delta f_{in}(s)} = \frac{(k_v / k_o)F(s)}{s + k_v F(s)} \quad (3.3.3)$$

- By manipulating the form of  $F(s)$ , we can improve the time-domain response of the PLL, for instance we can make the PLL settle down faster.

## Improving the Time Domain Response (Loop Compensation) (2)

- Rule-of-thumb for when to include the effect of  $F(s)$ :

**Step 1 - Find loop gain  $k_v$  and the cut-off frequency  $f_c$  of loop filter  $F(s)$ .**



**Step 2 - If**  $f_c > 2\left(\frac{k_v}{2\pi}\right)$  **then**  $\frac{\Delta V_o(s)}{\Delta f_{in}(s)} = \frac{(k_v / k_o)}{s + k_v F(s)}$

**Else**  $\frac{\Delta V_o(s)}{\Delta f_{in}(s)} = \frac{(k_v / k_o)F(s)}{s + k_v F(s)}$  ← Loop filter affects the dynamic response of the PLL

## 2<sup>nd</sup> Order Transfer Function (1)

- Now consider the case when the loop filter affects the dynamic response.
- Assume a simple RC low-pass filter is used.

- Since

$$F(s) = \frac{1}{1+sRC} \quad \longleftrightarrow \quad \begin{array}{c} R \\ \diagup \quad \diagdown \\ V_i \quad V_o \\ \diagdown \quad \diagup \\ C \end{array}$$

**Important:** If loop filter is connected directly to VCO, We also needs to include the capacitance of the VCO input if it is using varactor for frequency tuning.

$$\frac{\Delta V_o(s)}{\Delta f_{in}(s)} = \frac{(k_v/k_o)F(s)}{s + k_v F(s)} = \frac{(k_v/k_o)}{s^2 RC + s + k_v} \quad (3.3.4)$$

This is a 2<sup>nd</sup> order PLL.  
It has 2 poles in the denominator of the transfer function

For a step change in input frequency  $f_{in}$ :

$$\Delta f_{in}(t) = \Delta f U(t)$$

$$\Delta V_o(s) = \frac{\Delta f(k_v/k_o)}{s(s^2 RC + s + k_v)} = \frac{\Delta f(k_v/k_o)}{s\left(s^2 + \frac{s}{RC} + \frac{k_v}{RC}\right)RC} \quad (3.3.5)$$

$$\omega_n = \sqrt{\frac{k_v}{RC}}$$

$$\delta = \frac{1}{RC} / 2\sqrt{\frac{k_v}{RC}}$$

## 2<sup>nd</sup> Order Transfer Function (2)

- Applying Inverse Laplace Transform to (3.3.5) (or see equation (3.2.3)):

$$\Delta v_o(t) = \frac{\Delta f}{k_o} \left[ 1 - \frac{e^{-\delta\omega_n t}}{\sqrt{1-\delta^2}} \sin(\omega_n t \sqrt{1-\delta^2} + \theta) \right] U(t) \quad (3.3.6a)$$

Note that this is only valid for  $\delta < 1$

Transient part, goes to zero when  $t$  is large

$$\omega_n^2 = k_v \left( \frac{1}{RC} \right) \quad \text{Natural Frequency of the system} \quad (3.3.6b)$$

$$\delta = \frac{1}{2\omega_n RC} = \frac{1}{2\sqrt{k_v RC}} \quad \text{Damping Factor of the system} \quad (3.3.6c)$$

$$\theta = \tan^{-1} \sqrt{\frac{1}{\delta^2} - 1}$$

The time constant of the system is given by

$$\tau = \frac{1}{\delta\omega_n} = 2RC \quad (3.3.7)$$

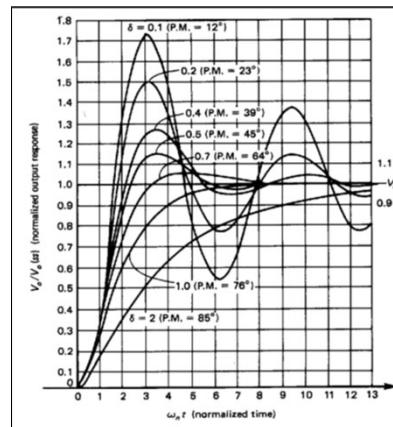
## Time-Domain Response of 2nd Order Transfer Function

$$\text{Rise time } t_r \cong \frac{1.8}{\omega_n} = 1.8\sqrt{\frac{RC}{k_V}}$$

$$\text{Settling time (to } \pm 1\%) \quad t_s \cong \frac{4.6}{\delta\omega_n} = \frac{2.3}{RC}$$

$$\text{Overshoot} \quad M_p \cong e^{\frac{-\pi\delta}{\sqrt{1-\delta^2}}} = e^{\frac{-\pi}{2\sqrt{k_V RC - \frac{1}{4}}}}$$

for  $0 \leq \delta < 1$



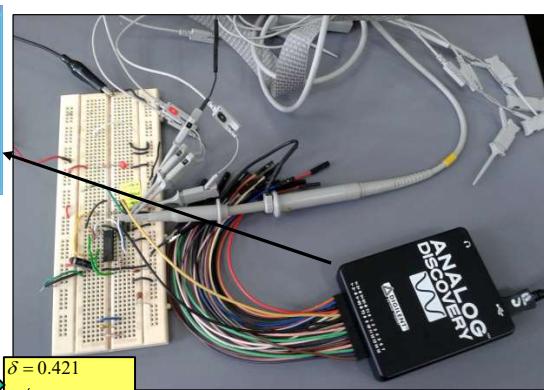
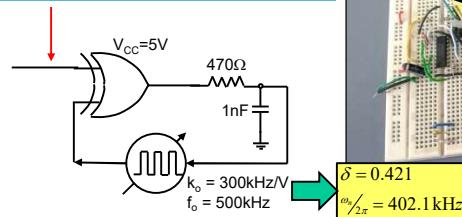
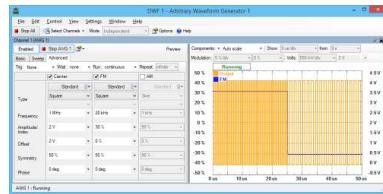
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## Example 3.3.1 – Type 1 Digital PD PLL Step Input Response

- In the following series of slides, we built a simple XOR gate type PLL using the 74HC4046 chip, and used an arbitrary function generator to provide the input to the PLL.

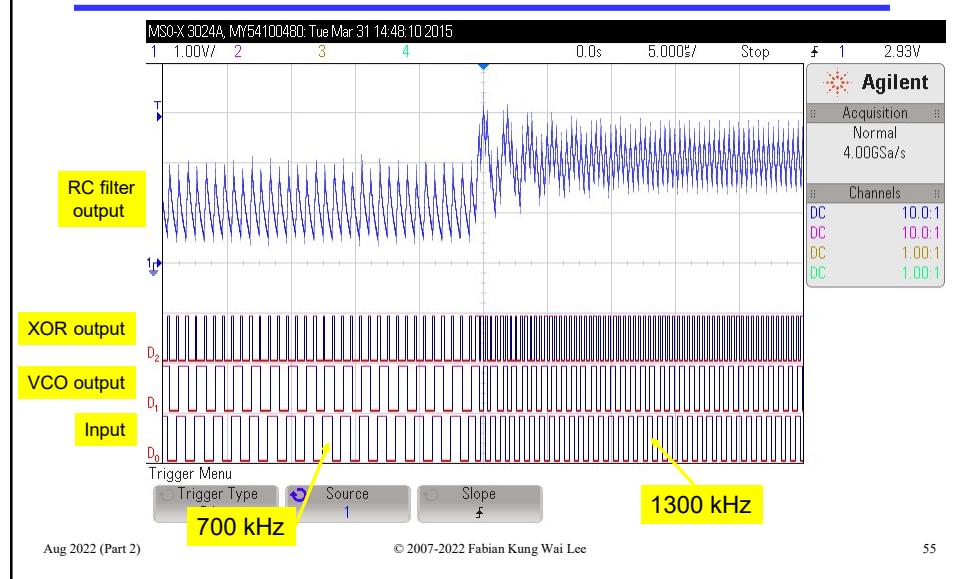


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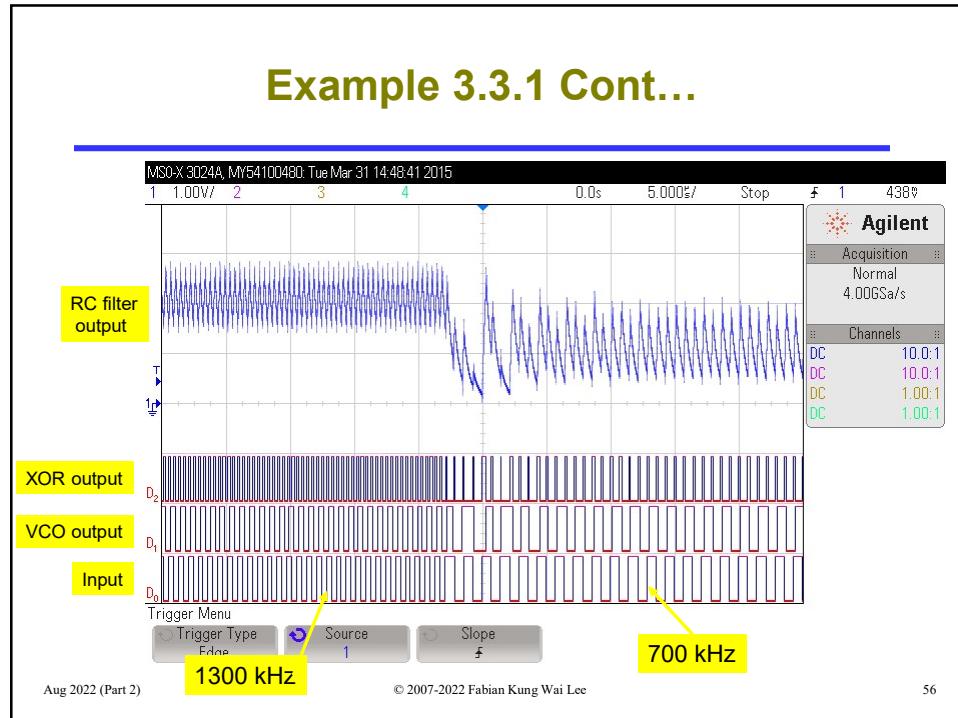
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### Example 3.3.1 Cont...



### Example 3.3.1 Cont...



## Example 3.3.2 – Using PLL as FSK Demodulator

Question:

A 1<sup>st</sup> order PLL with  $k_o = -0.75 \text{ kHz/V}$ ,  $f_o = 3.5 \text{ kHz}$ ,  $k_\phi = 0.3184 \text{ V/rad}$  and  $k_A = -5$  is used as a frequency-shift keying (FSK) demodulator. The input signal has  $f_S$  (space frequency) = 4 kHz and  $f_M$  (mark frequency) = 2 kHz. The baud rate is 1333 bits/sec and the binary data is ...0100...

Sketch the PLL output  $v_o(t)$ .

Solution:

Step 1 – Finding the static voltage values and time constant

For  $f_{in} = f_M = 2 \text{ kHz}$ ,

$$v_o = \Delta f/k_o = (2 - 3.5)/-0.75 = 2 \text{ V}$$

For  $f_{in} = f_S = 4 \text{ kHz}$ ,

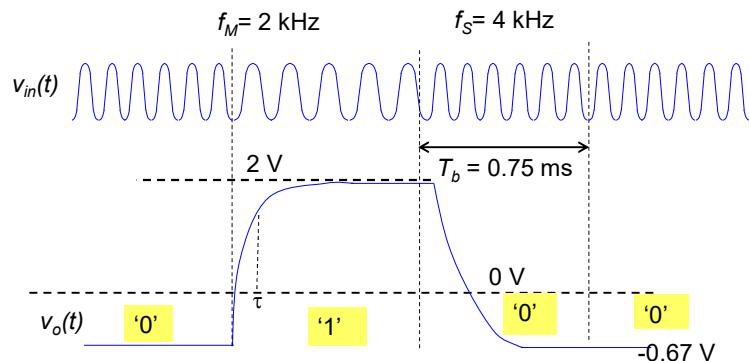
$$v_o = \Delta f/k_o = (4 - 3.5)/-0.75 = -0.67 \text{ V}$$

$$\text{Loop time constant} = \tau = 1/k_v = 1/7502 = 0.133 \text{ ms.}$$

## Example 3.3.2 Cont...

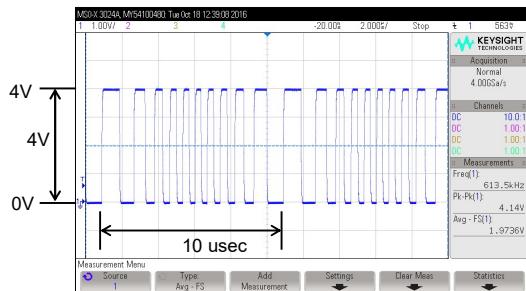
Step 2 – Sketch the voltage waveforms

$$\text{For baud} = 1333 \text{ bits/sec, period of 1 bit is: } T_b = \frac{1}{1333} \cong 0.750 \text{ msec}$$



### Example 3.3.3 - Type 1 Digital PD PLL Periodic Frequency Response

- In this experiment we put in an input signal consisting of a square wave with periodic sinusoidal FM modulation.
- The carrier frequency of the square wave is 1 MHz, and the FM modulation index is 30% (e.g. the carrier frequency will be changed from 0.7 MHz to 1.3 MHz in a sinusoidal fashion).



An example of the FM modulated input signal with carrier 1 MHz, 50% modulation index (sinusoidal) at a rate of 100 kHz.

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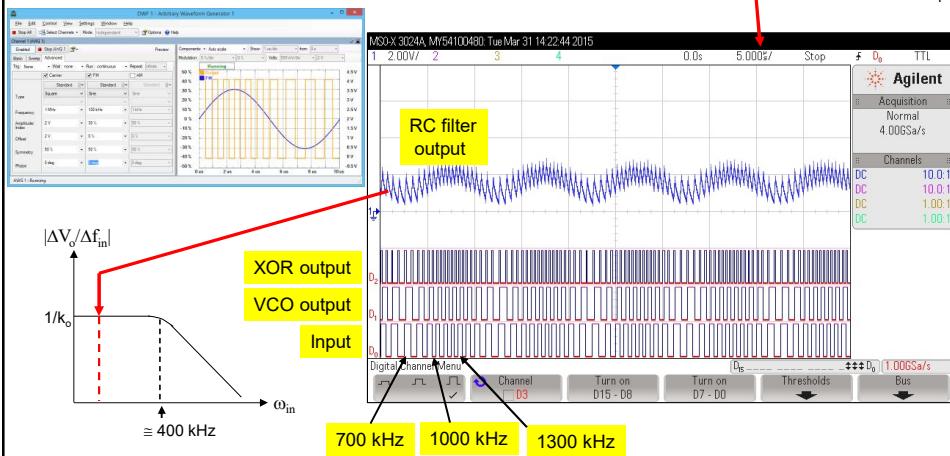
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### Example 3.3.3 Cont...

- FM modulation = 100 kHz.

Note the time-base



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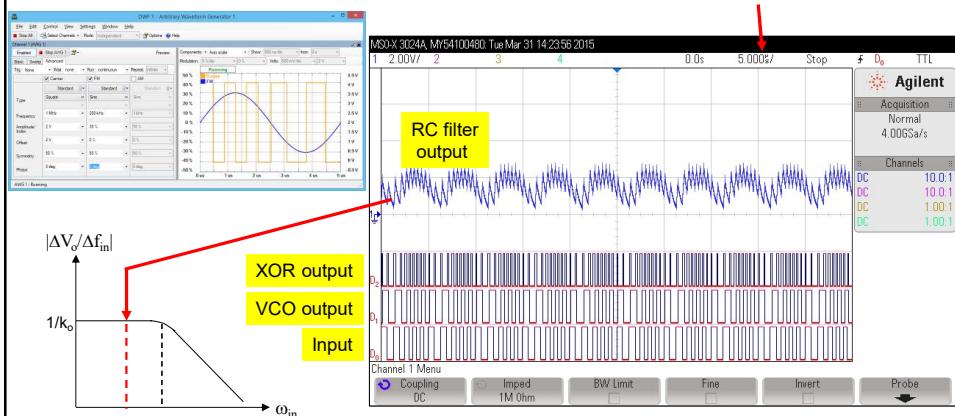
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### Example 3.3.3 Cont...

- FM modulation = 200 kHz.

Note the time-base



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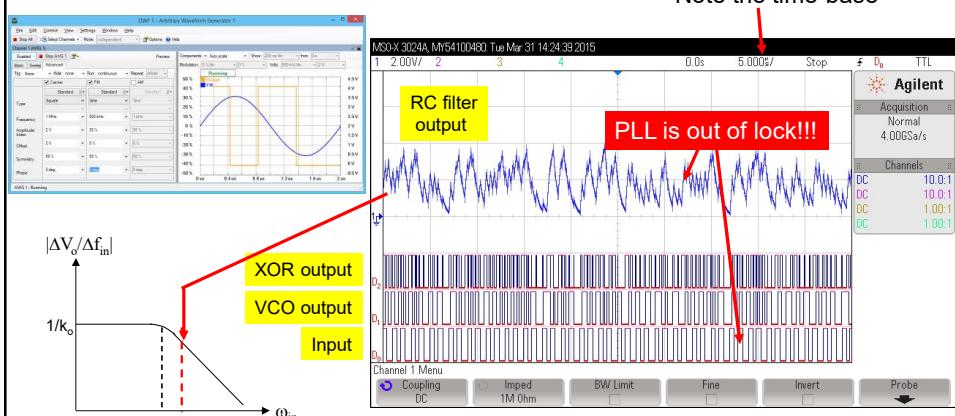
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### Example 3.3.3 Cont...

- FM modulation = 500 kHz.

Note the time-base



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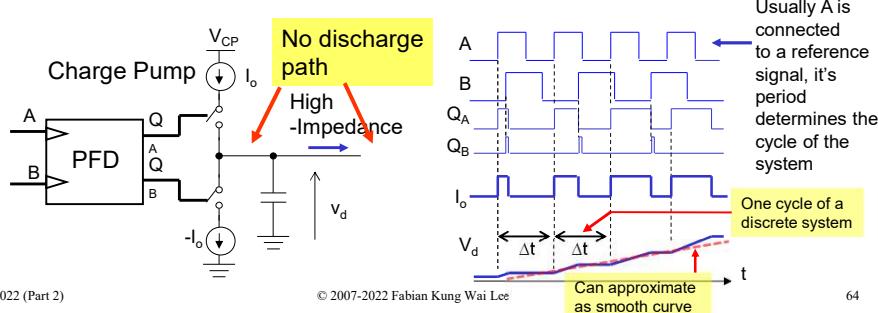
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### 3.3.2 – Digital PLL with Type 3 PD

### Transfer Function of PFD with Charge Pump (1)

- The PFD with charge pump is a discrete system, since it operates at when switch is closed at periodic interval and cut-off the loop when both switches in the CP are opened (no discharge path).
- If the loop bandwidth is much less than the input frequency, we can assume the state of the PLL changes by a small amount during each cycle. Using the average value of the PLL state during each cycle, we can approximate the PLL as a continuous-time system (Razavi [2]).

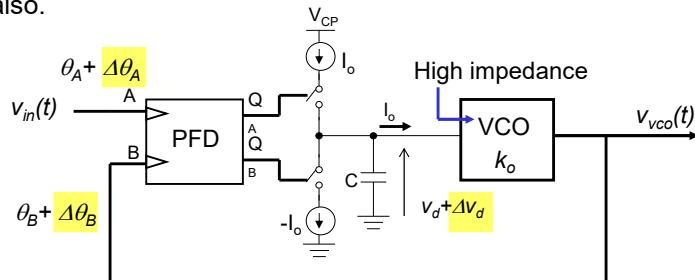


## Transfer Function of PFD with Charge Pump (2)

- We have seen in Section 2, the static phase error  $\theta_e$  for digital PLL using PFD with charge pump is 0 under phase-locked condition.
- Moreover for PFD with charge pump, the output  $v_d$  will increase or decrease until it reaches the limits of 0 or  $V_{cp}$  if there is a consistent phase difference between input A and B. Thus we would expect a pole at the origin for the frequency response of this PD.

## Transfer Function of PFD with Charge Pump (3)

- Extra**
- Now consider a simple digital PLL with PFD and charge pump as shown. Let the system be under phase-locked initially.
- $$\theta_A = \theta_B \quad \theta_e = \theta_A - \theta_B = 0$$
- As the instantaneous phase of the input  $\theta_A$  change by a small amount, a small change will result in small change of the output of the charge pump,  $v_d$ , which in turn causes the VCO output phase  $\theta_B$  to change also.



## Transfer Function of PFD with Charge Pump (4)

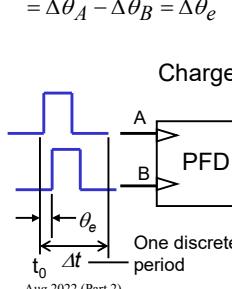
- During one discrete cycle at  $t = t_0$ , the phase difference between input A and B of the PFD is  $\theta_e$ .

Since  $\theta_A = \theta_B$   
during steady-state  

$$\begin{aligned} \theta_e &= (\theta_A + \Delta\theta_A) - (\theta_B + \Delta\theta_B) \\ &= \Delta\theta_A - \Delta\theta_B = \Delta\theta_e \end{aligned}$$

Since static phase error = 0 for PFD with charge pump

$$\frac{\theta_e}{2\pi} \Delta t = \frac{\Delta\theta_e}{2\pi} \Delta t$$



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The change in voltage across the capacitor C

$$\begin{aligned} v_d(t_0 + \Delta t) - v_d(t_0) &= i(t) \text{ is constant} \\ \Delta v_d|_{t_0} &= \frac{1}{C} \int_{t_0}^{t_0 + \Delta t} i(t) dt \\ &= \frac{I_o}{C} \left( \frac{\Delta\theta_e \Delta t}{2\pi} \right) = \frac{k_\phi}{C} \Delta\theta_e \Delta t \quad k_\phi = \frac{I_o}{2\pi} \end{aligned}$$

Summing up the total change in  $v_d$  over N discrete cycles:

$$\begin{aligned} \Delta v_d &= \Delta v_d|_{t_0} + \Delta v_d|_{t_1} + \dots + \Delta v_d|_{t_N} \\ &= \sum_{i=0}^N \Delta v_d|_{t_i} = \frac{k_\phi}{C} \sum_{i=0}^N \left( \Delta\theta_e|_{t_i} \right) \Delta t \quad (3.3.8) \end{aligned}$$

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## Transfer Function of PFD with Charge Pump (5)

- If the discrete period  $\Delta t$  is sufficiently small, the summation in (3.3.8) can be approximated by an integral:

This condition is equivalent to making  $1/\Delta t < 10\%$  of the bandwidth of the assumed continuous system.

$$\Delta v_d = \frac{k_\phi}{C} \sum_{i=0}^N \left( \Delta\theta_e|_{t_i} \right) \Delta t \approx \frac{k_\phi}{C} \int_0^t \Delta\theta_e(\tau) d\tau$$

- Thus the discrete time system can be approximated as a continuous time system. Now applying Laplace Transformation to the above relation:

$$\Delta V_d(s) \approx \frac{k_\phi}{C} \frac{\Delta\theta_e(s)}{s} = \frac{k_\phi}{sC} (\Delta\theta_A(s) - \Delta\theta_B(s))$$

- This can be rewritten as follows:

$$\Delta V_d(s) \approx k_\phi \left( \frac{1}{sC} \right) (\Delta\theta_A(s) - \Delta\theta_B(s)) \quad (3.3.9a)$$

Gain of PFD with charge-pump  $k_\phi = \frac{I_o}{2\pi}$  (3.3.9b)

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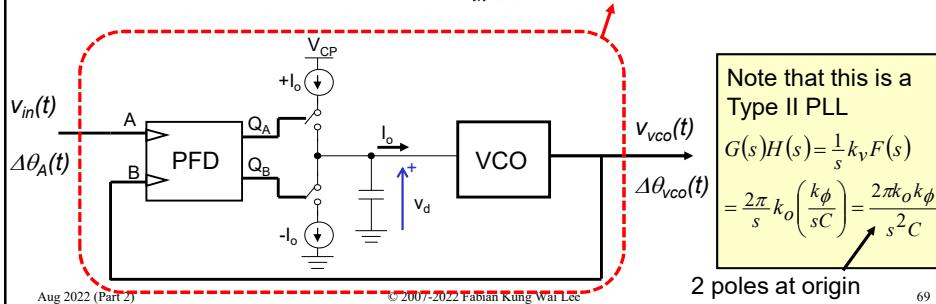
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## System Transfer Function (1)

- Now consider a simple PLL using PFD with charge pump, the loop filter consists of only a capacitor C.
- Hence  $F(s) = 1/sC$ ,  $k_A = 1$ .
- Using relation (3.3.9), substituting it into (3.1.4):

$$\frac{\Delta\theta_{vco}(s)}{\Delta\theta_{in}(s)} = \frac{k_v F(s)}{s + k_v F(s)} \rightarrow \frac{\Delta\theta_{vco}(s)}{\Delta\theta_{in}(s)} = \frac{2\pi k_o k_\phi \frac{1}{C}}{s^2 + 2\pi k_o k_\phi \frac{1}{C}} \quad (3.3.10)$$



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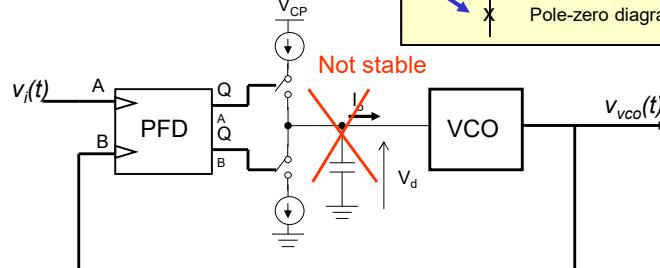
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## System Transfer Function (2)

- The frequency response as derived in (3.3.10) for the simple PLL is not stable due to the pair of poles on the imaginary axis.

$$\frac{\Delta\theta_{vco}(s)}{\Delta\theta_{in}(s)} = \frac{2\pi k_o k_\phi \frac{1}{C}}{s^2 + 2\pi k_o k_\phi \frac{1}{C}}$$



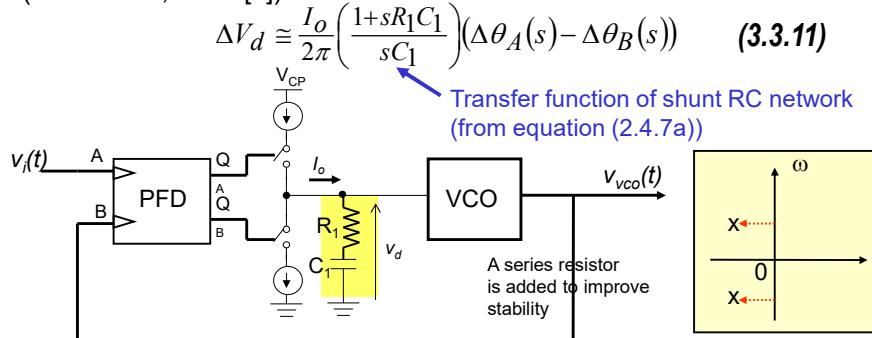
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## Stabilizing the Digital PLL Type 3 (1)

- To avoid instability, a zero must be added to the frequency response. This is done by using the 1<sup>st</sup> order loop filter with a zero as shown below. This will shift the poles to the left-hand side of the pole-zero plot.
- Using similar arguments as in derivation of (3.3.9a), we can show that (see Razavi, 2012 [2]):



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## Stabilizing the Digital PLL Type 3 (2)

- The final transfer function is:

Note: In some textbook like Razavi [2], a slight variation of the notation is used. There  $k_{vco} = 2\pi k_o$

$$\frac{\Delta\theta_{vco}(s)}{\Delta\theta_{in}(s)} = \frac{\frac{I_o}{C_1} k_o (1+sR_1C_1)}{s^2 + I_o k_o R_1 s + \frac{I_o}{C_1} k_o} \quad (3.3.12a)$$

- Or in terms of voltage and frequency:

$$\frac{\Delta V_d(s)}{\Delta f_{in}(s)} = \frac{1}{k_o} \frac{\omega_n^2 (1+sR_1C_1)}{s^2 + 2\delta\omega_n s + \omega_n^2} \quad (3.3.12b)$$

- With associated parameters:

$$\omega_n = \sqrt{\frac{I_o}{C_1} k_o} \quad \delta = \frac{R_1}{2} \sqrt{I_o C_1 k_o} \quad (3.3.13)$$

- Both the damping factor  $\delta$  and  $\omega_n$  can be increased by increasing  $I_o$  and  $k_o$  (the charge pump charging/discharging current and VCO's gain).

$$BW \cong \begin{cases} \omega_n [\delta - \sqrt{\delta^2 - 1}] & \delta \geq 1 \\ \omega_n \sqrt{1 - 2\delta^2} & \delta < 1 \end{cases} \quad (3.3.14)$$

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## Time-Domain Response (1)

- For a step change in input frequency from  $f_{in}$  to  $f_{in} + \Delta f$  at  $t = 0$ ,

$$\Delta f_{in}(t) = \Delta f U(t) \longrightarrow \Delta f_{in}(s) = \frac{\Delta f}{s}$$

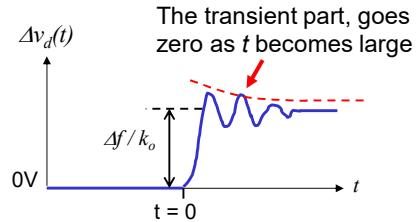
- We can rewrite (3.3.12b) as:

$$\rightarrow \Delta V_d(s) = \frac{\Delta f}{k_o} \frac{\omega_n^2 (1 + s R_1 C_1)}{s^2 + 2\delta\omega_n s + \omega_n^2} \quad (3.3.15)$$

## Time-Domain Response (2)

- We can perform Inverse Laplace Transform on (3.3.15) by referring to equation (3.2.3), assuming  $\delta < 1$ , with  $a = 1$ ,  $b = R_1 C_1$ :

$$\Delta v_d(t) = \frac{\Delta f}{k_o} \left\{ 1 - e^{-\omega_n \delta t} \left[ \frac{\sqrt{1-2R_1C_1\omega_n\delta+(R_1C_1\omega_n)^2}}{\sqrt{1-\delta^2}} \sin \left( \left( \omega_n \sqrt{1-\delta^2} \right) t + \left| \tan^{-1} \left( \frac{\sqrt{1-\delta^2}}{\delta - R_1 C_1 \omega_n} \right) \right| \right) \right] \right\} U(t) \quad (3.2.16)$$



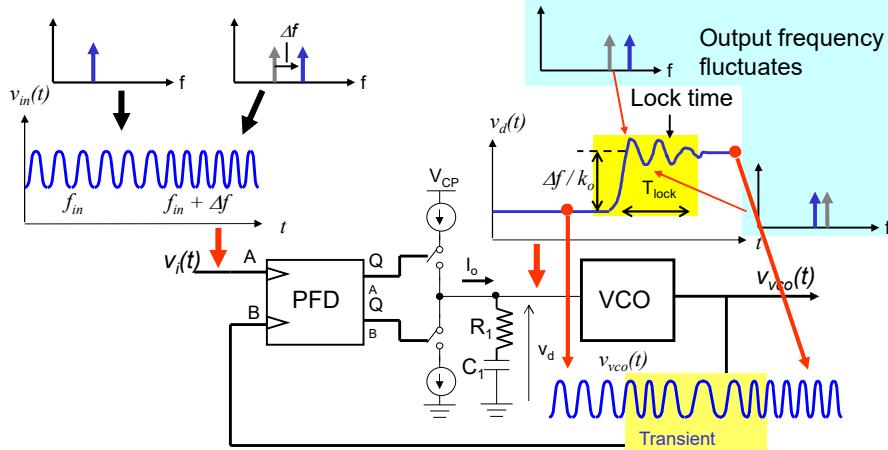
$$\text{Rise time } t_r \cong \frac{1.8}{\omega_n} = 1.8 \sqrt{\frac{C_1}{I_o k_o}}$$

$$\text{Settling time } t_s \cong \frac{4.6}{\delta \omega_n} = \frac{9.2}{R_1 I_o k_o} \quad (\text{to } \pm 1\%)$$

$$\text{Overshoot } M_p \cong e^{\frac{-\pi \delta}{\sqrt{1-\delta^2}}} = e^{\frac{-\pi R_1 \sqrt{I_o C_1 k_o}}{\sqrt{4-R_1^2 I_o C_1 k_o}}} \quad \text{for } 0 \leq \delta < 1$$

## Time-Domain Response (3)

- Equation (3.3.16) of course looks complicated. However it can be plotted out and its implication can be summarized in this picture...



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## Stability Limit of Digital PLL Type 3

- Finally, the stability limit for this PLL can be shown to be (see Razavi [2]):

$$\omega_n^2 < \frac{\omega_{in}^2}{\pi(R_1 C_1 \omega_{in} + \pi)} \quad (3.3.18)$$

Limit (3.3.18) indicates that  $R_1$  cannot be increased indefinitely

- In typical design,  $\omega_n$  is kept roughly one-tenth the input frequency to guarantee stability.

Rule-of-thumb  $\Rightarrow \omega_n \leq \frac{\omega_{in}}{10} \quad (3.3.19)$

- This stability limit sets an upper bound on  $\omega_n$ , which in turn slows down the time-domain response as can be seen from (3.3.16), since the PFD-charge pump PLL time constant is  $\tau = \frac{1}{\omega_n \delta} \quad (3.3.20)$

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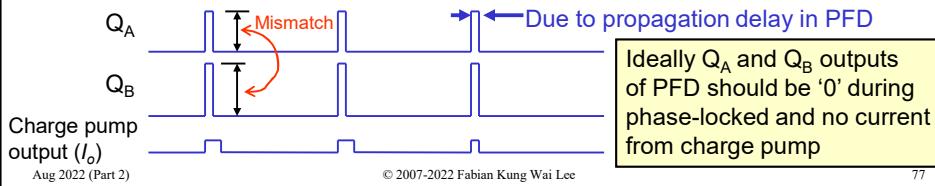
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## Reference Spurs in Digital PLL Type 3

### (1)

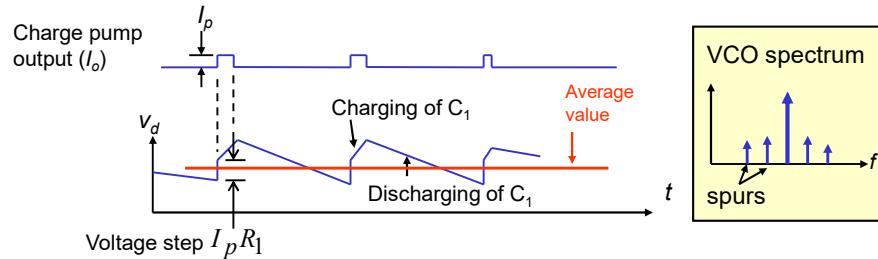
- The output of the PFD with charge pump contains ‘ripples’ due to the operation of the RC low-pass filter and the PFD.
- The two outputs of the PFD produce narrow pulses at every phase comparison instant even if the input phase difference is zero.
- This is due to the propagation delay in the logic gates and flip-flops in the PFD and mismatch of the charge pump.
- In the ideal case, the two pulses would have identical shape, and the current from the charge pump will cancel off at the loop filter.
- In practice, there will be mismatch at the outputs of the PFD, and also at the charge pump currents ( $+I_o$  not equal  $-I_o$ ).



## Reference Spurs in Digital PLL Type 3

### (2)

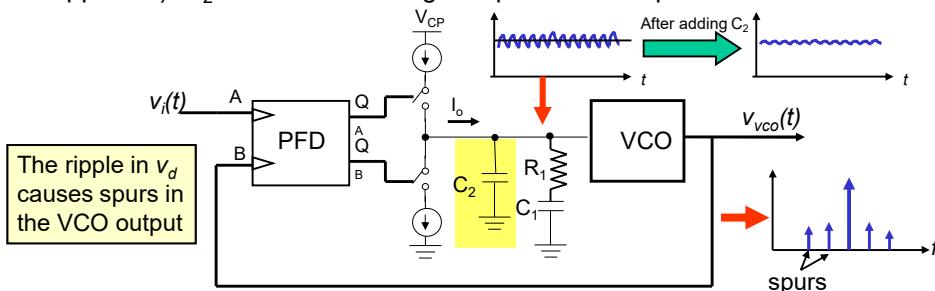
- There is also a voltage step due to the response of the series RC network being driven with a current pulse. This voltage step happens whenever there is a current pulse from the charge pump, regardless of phase-locked or not, and can cause some erratic behavior.



- This results in the VCO control voltage experiences a ripple at each phase comparison instant. This causes sidebands to appear at the output of the VCO, called the **reference spurs** (usually the input to the PLL is called the **reference signal**).

## Suppressing Reference Spur in the Digital PLL Type 3 (1)

- In the single-ended charge pump,  $R_1$  in series with  $C_1$  can introduce 'ripple' in the control voltage  $v_d$  of the VCO even when the loop is locked.
- To suppress this ripple, a second capacitor  $C_2$  can be connected from the output of the charge pump to ground. This modification introduces a third pole to the PLL, requiring further study of the stability (See Appendix).  $C_2$  reduces the voltage step seen in the previous waveforms.



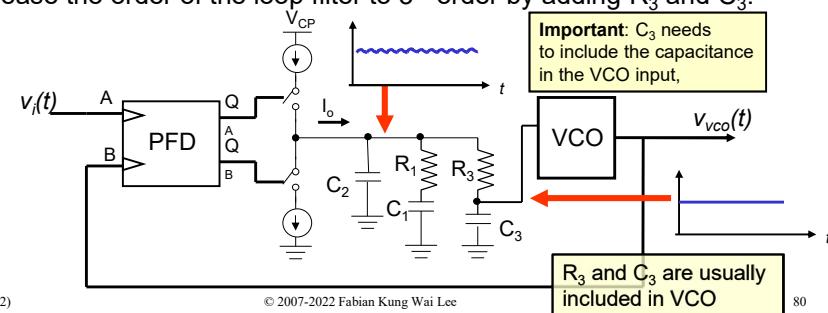
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## Suppressing Reference Spur in the Digital PLL Type 3 (2)

- Other approaches to suppress the reference spur is to reduce the gain of the VCO,  $k_o$  (this means the VCO is less sensitive to control voltage). However this is often not feasible for low voltage circuit (Razavi [2]).
- Another approach is to interpose a notch filter between the loop filter and the VCO.
- A popular approach to obtain even better spur suppression is to increase the order of the loop filter to 3<sup>rd</sup> order by adding  $R_3$  and  $C_3$ .



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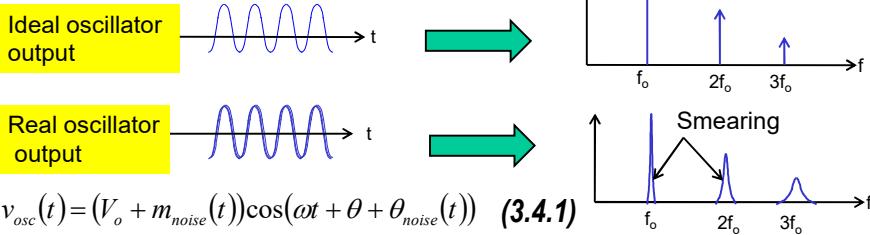
## Suppressing Reference Spur in the Digital PLL Type 3 (3)

- The additional pole due to  $R_3C_3$  must be lower than the input or reference frequency to the PFD with charge pump PLL for it to be effective.
- Typically one would need to generate the Bode plot or the Root-Locus plot to examine the time-domain behavior of digital PLL Type 3 with higher order loop filter.

## 3.4 – Noise Considerations

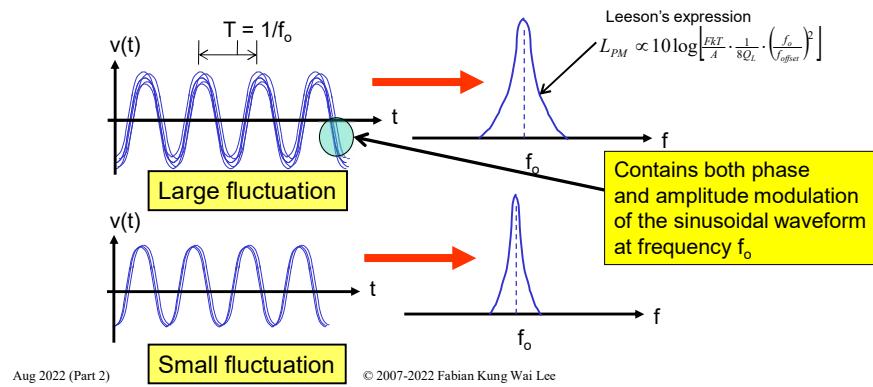
## Phase Noise in Oscillator (1)

- Assuming now we are treating the VCO output as the PLL output.
- Since the VCO is an oscillator, its output is periodic. In frequency domain we would expect a series of impulsive harmonics.
- In a practical oscillation system, the instantaneous frequency and magnitude of oscillation are not constant. These will fluctuate as a function of time.
- These random fluctuations are noise, and in frequency domain the effect of the spectra will 'smear out'.



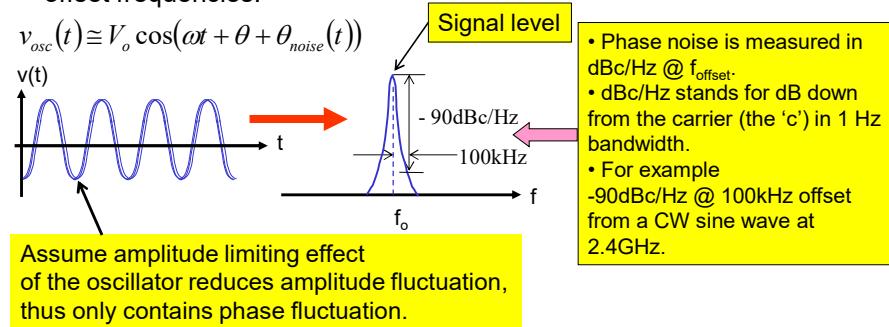
## Phase Noise in Oscillator (2)

- Mathematically, we can say that the instantaneous frequency and magnitude of oscillation are not constant. These will fluctuate as a function of time.
- The larger the fluctuation, the greater is the 'smearing' effect in frequency domain.



## Phase Noise in Oscillator (3)

- Typically the magnitude fluctuation is small (or can be minimized) due to the **oscillator nonlinear limiting process** under steady-state.
- Thus the spectra smearing is largely attributed to phase variation and is known as Phase Noise.
- Phase noise is measured with respect to the signal level at various offset frequencies.



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## Phase Noise in PLL (1)

- Here we only restrict ourselves to very small noise level under linear condition such that the effect of noise can be considered additive. For further discussion please see Gardner [5] and Bianchi [6].
- The electrical noise sources in PLL can be categorized as **internal** or **external** noise sources.
- External noise sources are those due to fluctuation in power supply to the PLL, Electromagnetic Interference (EMI) and those that are injected into the input of the PLL.
- Each component in the PLL also contribute noise at its output, in the form of voltage/current noise signal. These are the internal noise sources.
- The total effect of internal and external noises result in the random fluctuation of the VCO control voltage.
- This, together with VCO internal noise, causes the VCO output to exhibit phase-noise much like conventional oscillator.

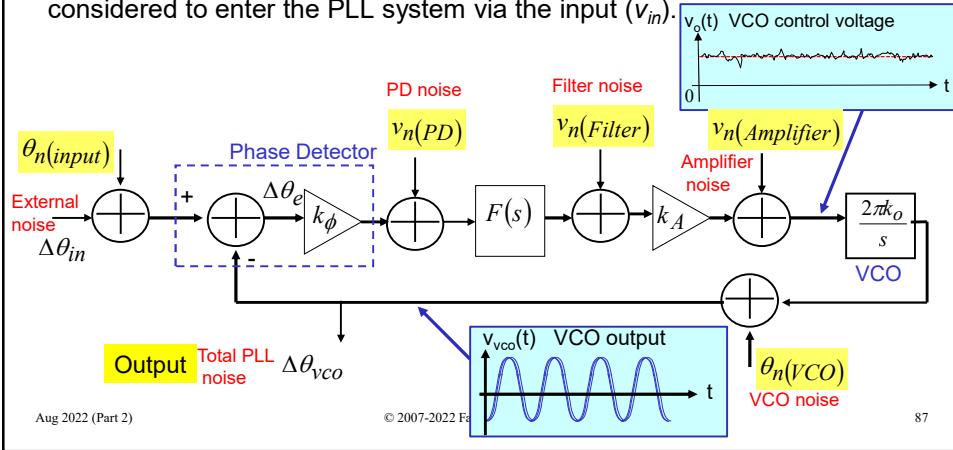
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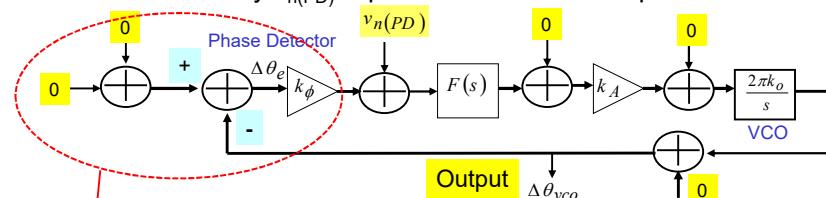
## Phase Noise in PLL (2)

- For the frequency synthesizer, the Frequency Divider also contribute noise in terms of phase or jitter noise.
- External noise can be controlled by proper physical design and will be considered to enter the PLL system via the input ( $v_{in}$ ).

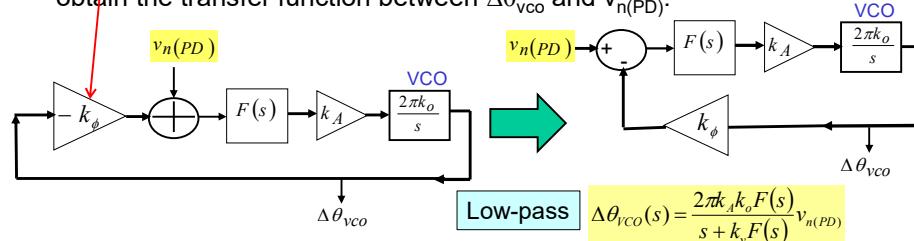


## PLL Phase Noise Transfer Function (1)

- Now consider only  $v_{n(PD)}$  is present and all other inputs are zero.



- This block diagram can be simplified, ignoring all the zero inputs, and we obtain the transfer function between  $\Delta\theta_{vco}$  and  $v_{n(PD)}$ :



## PLL Phase Noise Transfer Function (2)

- Proceeding in a similar manner for the other noise sources, and using superposition principle, we can show that total noise at VCO output is [6]:

$$\Delta\theta_{VCO}(s) = \frac{k_v F(s)}{s + k_v F(s)} \theta_{n(\text{input})} + \frac{2\pi k_A k_o F(s)}{s + k_v F(s)} v_{n(PD)} + \frac{2\pi k_o k_A}{s + k_v F(s)} v_{n(\text{filter})} \\ + \frac{2\pi k_o F(s)}{s + k_v F(s)} v_{n(\text{Amp})} + \frac{s}{s + k_v F(s)} \theta_{n(VCO)}$$

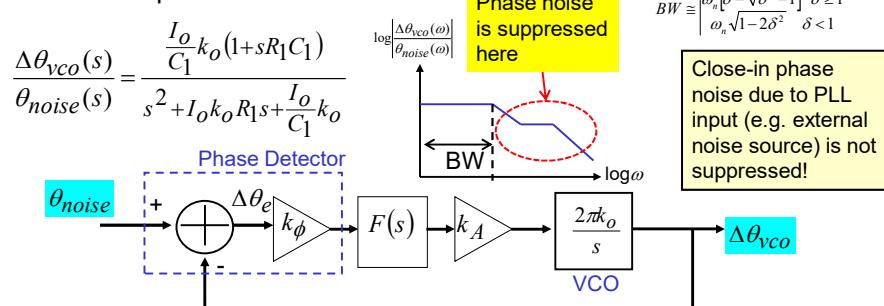
(3.4.2)

Low-pass      Low-pass  
Low-pass      Low-pass  
High-pass

- Of the internal noise sources, the VCO and loop amplifier are usually the most noisy blocks.
- Most PLL does not employ the loop amplifier, and filter noise is usually very low. Thus in the next few slides we consider the effect of external input noise, PD noise and VCO noise.

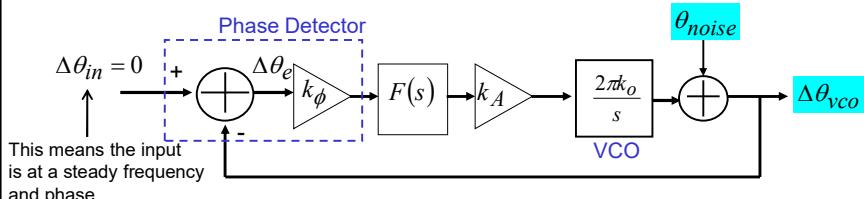
## Effect on PLL Phase Noise by External Noise Sources

- Consider now the effect of externally injected noise at the input and all other components are noiseless.
- It is not surprising that it has the same form as the transfer function of the PLL. The input phase noise spectrum of a PLL is shaped by the characteristic low-pass transfer function of the system when it appears at the VCO output.



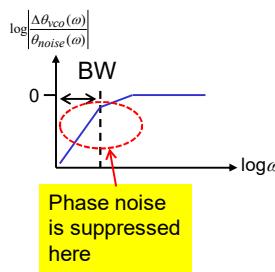
## Effect on PLL Phase Noise by VCO Internal Noise

- Phase noise at VCO.



$$\frac{\Delta\theta_{vco}(s)}{\theta_{noise}(s)} = \frac{s^2}{s^2 + I_o k_o R_1 s + \frac{I_o}{C_1} k_o}$$

$$BW \approx \begin{cases} \omega_n [\delta - \sqrt{\delta^2 - 1}] & \delta \geq 1 \\ \omega_n \sqrt{1 - 2\delta^2} & \delta < 1 \end{cases}$$



- Close-in phase noise due to VCO is suppressed.
- The larger the BW, the better will be the suppression of phase noise due to VCO.

## Some Comments on Controlling PLL Phase Noise

- Let us consider the VCO output as the PLL output.
- Generally external contribution to PLL phase noise can be minimized by enclosing the PLL in a metallic shield and keeping the power supply voltage stable.
- Assuming we do not use any loop amplifier, the other significant contributors to PLL phase noise are the VCO and the PD.
- If the VCO is the dominant contributor to phase noise, then we should use a large loop bandwidth.
- Noise due to PD is usually periodic, and appears as 'spurs' on the VCO output spectra. This can be controlled by reducing the loop bandwidth of the PLL.
- Typical low phase noise PLL also uses differential PD, differential loop filter and amplifier.
- The requirements above are contradictory, thus some compromises are needed.

## End Notes

---

- This is a very brief discussion on PLL.
- Digital PLL using PFD with Charge Pump is very important in high frequency circuits. Read more in Razavi [2], Smith [3], Egan [4] and Gardner [5], Barnejee [7] and other books.
- For higher order PLL ( $> 3^{\text{rd}}$  order), usually computer simulation is needed to quantify its performance (see [6]).
- Reference [7] provides equations to estimate PLL Phase Noise.

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## 4 – Frequency Synthesizer using PLL

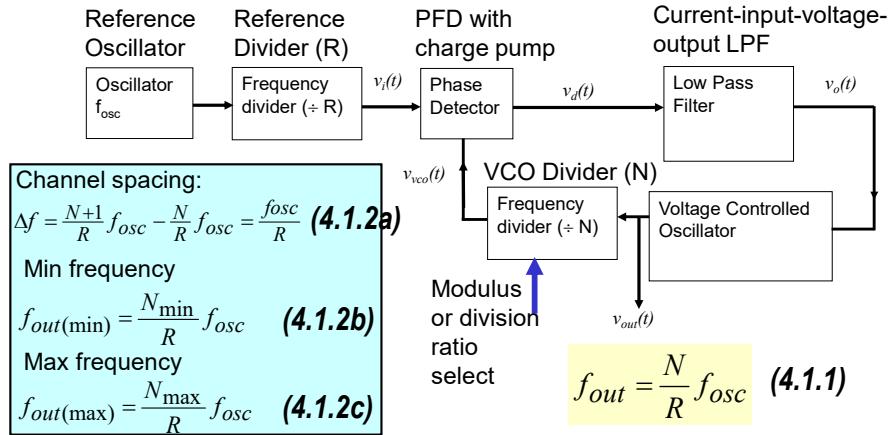
## Introduction

- A frequency synthesizer is a circuit that can generate a periodic signal with precise frequency. The frequency is selectable by the user.
- A PLL circuit can be easily modified to become a frequency synthesizer by incorporating digital dividers.

## 4.1 – Integer-N Architecture

## Integer-N Architecture (1)

- A basic frequency synthesizer architecture using digital divider is shown below.



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## Integer-N Architecture (2)

- Modern Frequency Synthesizers use PFD Charge-Pump or sample-and-hold type PDs, primarily because of small high frequency component from these PD.
- In compact system the PFD Charge-Pump phase detector is used due to each of integration and lesser complexity.
- Usually one would fix the reference divider ratio  $R$  and the reference oscillator's frequency  $f_{osc}$ .
- The output from the reference divider is usually called the reference frequency  $f_{ref}$ . This forms the input frequency to the PLL in the synthesizer.
- A stable oscillator is used for the reference oscillator, usually temperature compensated crystal oscillator (TCXO) is used. Metal shielding is also employed to prevent electromagnetic interference noise from external sources. Sometimes this crystal oscillator is put in a temperature controlled oven for added stability.

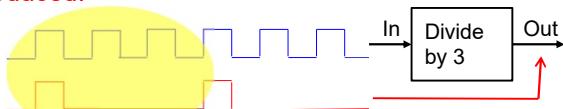
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## The Frequency Divider

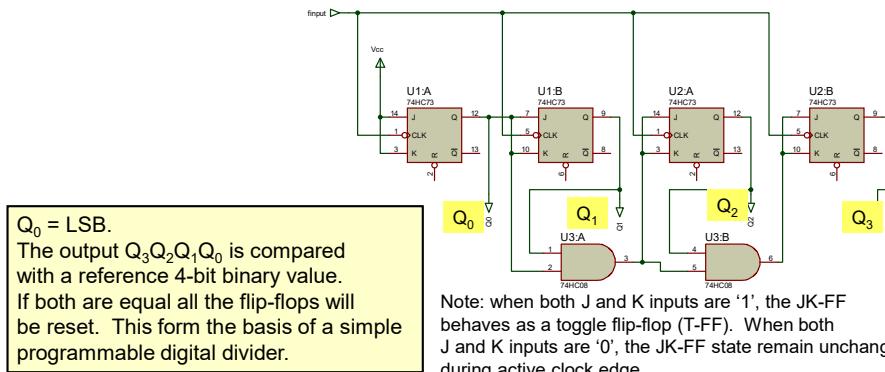
- The programmable frequency divider can be implemented in digital or analog form.
- The digital frequency divider is essentially a counter. For instance a counter that counts from 0 to 3 and the resets itself can be used as a divide by 3 counter, e.g. for every 3 input pulses, one output pulse is produced.



- In digital form, flip-flops (FF), D-FF, T-FF or JK-FF are used to form either Ring (or Ripple) Counter or Synchronous Counter.
- A binary comparator is often used in conjunction with the counter to form a programmable frequency divider.

## Examples of Frequency Divider (1)

- An example of a 4-stage synchronous digital frequency divider is shown below.
- For a complete schematic of programmable digital frequency divider, see Section 4.3.

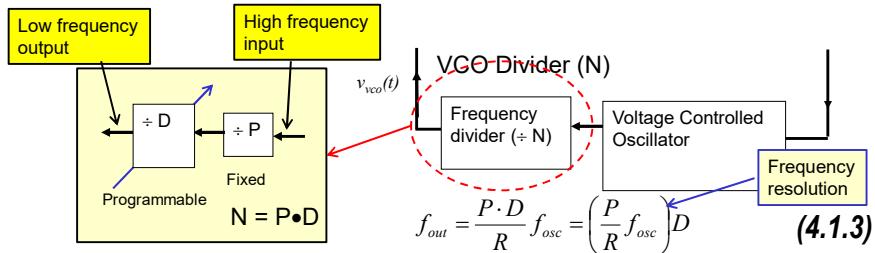


## Examples of Frequency Divider (2)

- The analog frequency divider often uses switching/sampling technique to sample the input waveforms. This will create an output containing harmonics of various sum and difference of the input frequencies. A suitable band-pass or low-pass filter will select the difference components, resulting in a low frequency output, see Egan [4] and Bianchi [6].
- An example of analog frequency divider is the **Sampling Phase Detector** (see Section 2.4), which uses an analog mixer and a periodic impulse source to sample the VCO input.
- The Sampling PD is often used with a VCO operating at microwave frequencies ( $> 3$  GHz) as even the pre-scalar digital divider might not work well at very high frequency.

## Practical Integer-N Frequency Synthesizer

- In modern implementation, the frequency divider consists of two blocks. A **fixed** high-frequency frontend, called the **Pre-scalar** which is usually built on SiGe, GaAs or other technologies and a **programmable** lower frequency backend built on CMOS technology.



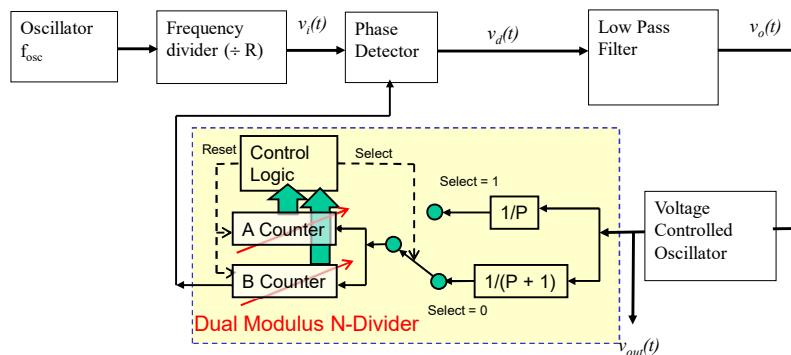
- For instance if the VCO frequency is 2000 MHz,  $P = 8$ , the output frequency of the pre-scalar is 250 MHz, which is within the limit of mature CMOS process such as 0.18μm.

## Limitation of Integer-N Frequency Synthesizer with Pre-scalar

- One of the limitations of using fixed pre-scalar is the limited resolution for the frequency output of the synthesizer.
  - Suppose  $f_{osc} = 10$  MHz,  $R=100$ ,  $P=8$ , and  $D = 1000$ . Then:
- $$f_{out}|_{D=1000} = \frac{P \cdot D}{R} f_{osc} = \frac{8 \times 1000}{100} 10 \times 10^6 = 800 \text{ MHz}$$
- If now  $D$  is incremented by 1,
- $$f_{out}|_{D=1001} = \frac{8 \times 1001}{100} 10 \times 10^6 = 800.8 \text{ MHz}$$
- The resolution is 0.8 MHz, as compared to  $f_{ref} = 10\text{MHz}/100 = 0.1$  MHz without the pre-scalar. Thus the resolution degrades by order of  $P$  with the addition of pre-scalar.

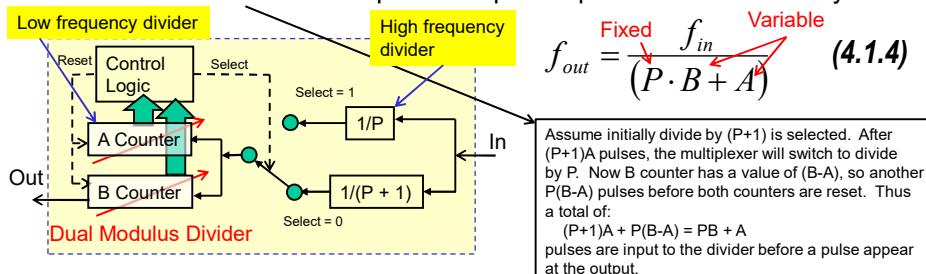
## Integer-N Frequency Synthesizer with Dual Modulus Pre-scalar

- Modern Integer-N frequency synthesizer overcomes the degradation of the resolution by the use of two or more pre-scalars.
- An Integer-N synthesizer with two pre-scalars, also called **Dual-Modulus N-Divider** is shown below:



## Dual Modulus Divider Operation (1)

- To function properly, the dual modulus divider requires that:
  - B and A counters are decremented every time a pulse is received.
  - $B > A$ .
  - When  $A > 0$ , 'Select' = 0, when  $A = 0$ , 'Select' = 1.
  - When both B and A counters are 0, the counters are reloaded with user preset values.
- We can show that the output and input frequencies are related by:



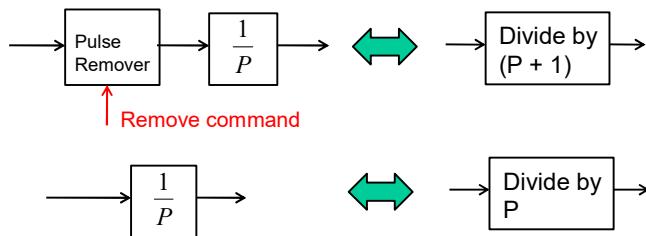
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## Dual Modulus Divider Operation (2)

- One way of implementing the dual modulus divider is by using a pulse removing scheme (pulse swallowing [2]), so that instead of two high frequency divider, we only need one.



- From previous slide the A counter is tied to divide by  $(P+1)$ , which uses pulse swallowing scheme, thus in some articles the A counter is called the **swallow counter**.

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## Example 4.1.1 – Dual-Modulus Integer-N Synthesizer

- Let  $f_{osc} = 10 \text{ MHz}$ ,  $R=100$ ,  $P=8$ .
- Find values A and B counters if outputs of 800 MHz and 800.1 MHz are needed.

$$\text{Nominal frequency resolution } \frac{10\text{MHz}}{100} = 100\text{kHz}$$

$$\text{For } f_{VCO} = 800 \text{ MHz: } N = P \cdot B + A = 8000$$

$$\Rightarrow A = 96, B = 988 \leftarrow \text{Many solutions available}$$

$$\text{For } f_{VCO} = 800.1 \text{ MHz: } N = P \cdot B + A = 8001$$

$$\Rightarrow A = 97, B = 988$$

B = N/P , ignoring the remainder, A = N mod P.

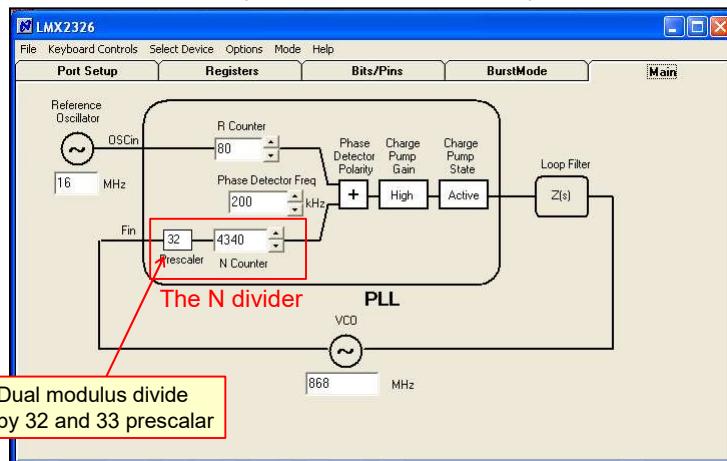
## Further Comments

- For a certain value of P, there is a limit to the minimum value of N=PB+A that is valid (e.g. B>A) for continuous division ratio.
- This value of N is called the **Minimum Continuous Divide (MCD)** ratio.
- To lower the MCD, quad modulus divider can be used [7].

Because A can range from 0 to P-1, minimum value of B is P-1.  
The minimum value of A is 0.  
The minimum legal value for N is:  $N_{min} = P(P-1)$

## Exercise 4.1.1 – Modeling the Static Operation of Integer-N Frequency Synthesizer using Codeloader 4™

From Codeloader 4 software by National Semiconductor (now part of Texas Instruments)



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## 4.2 – Dynamic Response and Noise of the Integer-N Frequency Synthesizer

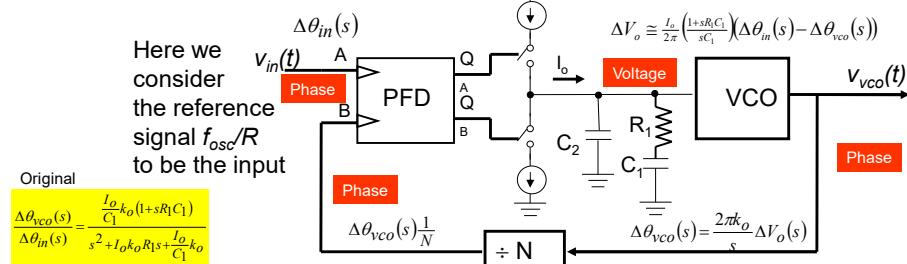
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## Transfer Function of the Integer-N Synthesizer (1)

- The integer-N synthesizer can be redrawn as shown, with the reference frequency source omitted for clarity.



- The close-loop transfer function can be obtained as:

$$\frac{\Delta\theta_{vco}(s)}{\Delta\theta_{in}(s)} = \frac{\frac{I_o k_o \left( \frac{1+sR_1 C_1}{s^2 C_1} \right)}{1 + I_o k_o \left( \frac{1+sR_1 C_1}{s^2 C_1} \right) \frac{1}{N}}}{1 + I_o k_o \left( \frac{1+sR_1 C_1}{s^2 C_1} \right) \frac{1}{N}} = \frac{\frac{I_o k_o (1+sR_1 C_1)}{C_1}}{s^2 + I_o \left( \frac{k_o}{N} \right) R_1 s + \frac{I_o k_o}{C_1 N}} \quad (4.2.1)$$

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## Transfer Function of the Integer-N Synthesizer (2)

- Comparing (4.2.1) with the standard 2<sup>nd</sup> order form (3.3.12) of Section 3:

$$\frac{\Delta\theta_{vco}(s)}{\Delta\theta_{in}(s)} = \frac{\frac{I_o k_o (1+sR_1 C_1)}{C_1}}{s^2 + I_o \left( \frac{k_o}{N} \right) R_1 s + \frac{I_o k_o}{C_1 N}} = \frac{\omega_n^2 (1+sR_1 C_1)}{s^2 + 2\delta\omega_n s + \omega_n^2} \quad (4.2.2a)$$

Note that both the damping factor and natural frequency are dependent on divider ratio  $N$

$$\omega_n = \sqrt{\frac{I_o}{C_1 N} k_o} \quad (4.2.2b) \qquad \delta = \frac{R_1}{2} \sqrt{\frac{I_o C_1 k_o}{N}} = \frac{R_1 C_1}{2} \omega_n \quad (4.2.2c)$$

- As usual transfer function (4.2.2a) can also be written in terms of  $\Delta V_d$  versus frequency change in  $f_{ref}$ :

$$\frac{\Delta V_d(s)}{\Delta f_{in}(s)} = \frac{1}{k_o} \frac{\omega_n^2 (1+sR_1 C_1)}{s^2 + 2\delta\omega_n s + \omega_n^2} \quad (4.2.3)$$

$$BW \equiv \begin{cases} \omega_n [\delta - \sqrt{\delta^2 - 1}] & \delta \geq 1 \\ \omega_n \sqrt{1 - \delta^2} & \delta < 1 \end{cases}$$

We also notice from (4.2.2c) that larger feedback divider ratio  $N$  results in smaller loop bandwidth if  $\delta > 1$

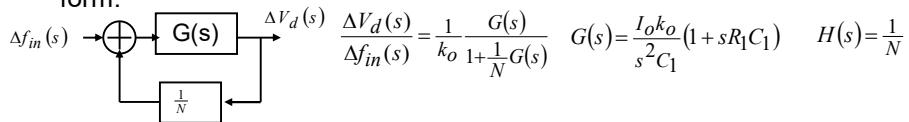
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## Transient Response When N-Divider Changes(1)

- In the integer-N architecture, the PLL undergoes a transient each time the N modulus (e.g. the divider ratio) changes.
- We can write the transfer function (4.2.3) in the standard close-loop form:



- For a small change of N divider from  $N$  to  $N + k$ :

$$\Delta f_{in}(s) \rightarrow \text{Summing Junction} \rightarrow G(s) \rightarrow \Delta V_d(s) \quad \frac{\Delta V_d(s)}{\Delta f_{in}(s)} = \frac{1}{k_o} \frac{G(s)}{1 + \left(\frac{1}{N+k}\right) G(s)} = \frac{1}{k_o} \frac{G(s)}{1 + \frac{G(s)}{N} \left[ \frac{1}{1 + \frac{k}{N}} \right]} = \frac{1}{k_o} \frac{G(s) \left(1 + \frac{k}{N}\right)}{1 + \frac{G(s)}{N} + \frac{k}{N}}$$

Can be ignored

$$k \ll N \quad \rightarrow \quad \Delta V_d(s) \approx \frac{1}{k_o} \frac{G(s)}{1 + \frac{1}{N} G(s)} \left(1 + \frac{k}{N}\right) \Delta f_{in}(s) \quad (4.2.4)$$

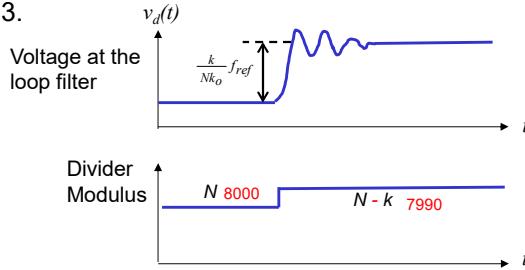
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## Transient Response When N-Divider Changes (2)

- Usually  $k \ll N$ , thus equation (4.2.4) is valid most of the time.
- If we assume the modulus is changed from  $N$  to  $N + k$  at  $t = 0$ , then (4.2.4) can be interpreted as a step change in the input from  $f_{ref}$  to  $(1+k/N)f_{ref}$  at  $t = 0$ .
- From this analysis, we infer that when the divider modulus changes, the loop exhibits a response to a step input, requiring a finite time to settle. The response is similar to the basic PLL using PFD with charge pump in Section 3.



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## Transient Response When N-Divider Changes (3)

- Since  $f_{out} = \frac{N}{R} f_{osc} = Nf_{ref}$  the initial and final frequency of the VCO should be:

$$f_{out}|_{initial} = Nf_{ref} \quad f_{out}|_{final} = (N+k)f_{ref}$$

- From (4.2.3), (4.2.2b) and (4.2.2c), the transition from initial  $f_{out}$  to final  $f_{out}$  can be obtained by modifying the result of Section 3 (for  $\delta < 1$ ):

$$f_{out}(t) = Nf_{ref} + \frac{kf_{ref}}{Nk_o} \left[ 1 - e^{-\omega_n \delta t} \left[ \frac{\sqrt{1-2R_1C_1\omega_n\delta+(R_1C_1\omega_n)^2}}{\sqrt{1-\delta^2}} \sin \left[ \begin{array}{l} \left( \omega_n \sqrt{1-\delta^2} \right) t \\ + \left| \tan^{-1} \left( \frac{\sqrt{1-\delta^2}}{\delta - R_1 C_1 \omega_n} \right) \right| \end{array} \right] \right] \right] U(t)$$

Where      Time constant

$$\omega_n = \sqrt{\frac{I_o}{C_1 N} k_o} \quad \delta = \frac{R_1}{2} \sqrt{\frac{I_o C_1 k_o}{N}} \quad \omega_n \delta = \frac{R_1 I_o k_o}{2N}$$

## Output Phase Noise of Integer-N Architecture (1)

- The analysis of output phase noise is similar to the procedures in Section 3.3, with the addition of the N divider in the feedback path.
- There is now additional component that contribute to output phase noise. It can be shown that the output phase noise over the N divider noise is also low-pass.**
- Because of the precautions taken on the reference oscillator, it has very low phase noise. Thus majority of the phase noise observed at the output of the Integer-N frequency synthesizer is contributed by the VCO, the PFD and charge-pump, N divider and also from the components of the loop filter.
- From the analysis of previous section, we observe that VCO noise contribution can be suppressed by having a large 3dB system bandwidth (BW).

$$BW \cong \begin{cases} \omega_n [\delta - \sqrt{\delta^2 - 1}] & \delta \geq 1 \\ \omega_n \sqrt{1 - 2\delta^2} & \delta < 1 \end{cases}$$

## Output Phase Noise of Integer-N Architecture (2)

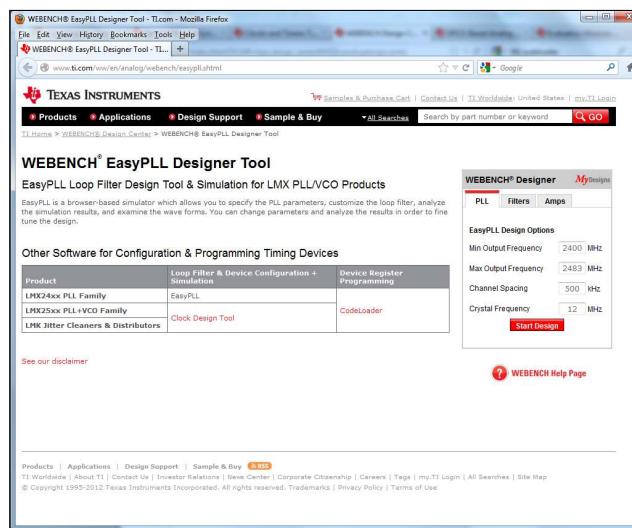
- If VCO is the main contributor of output phase noise, then having a large system bandwidth will suppress the output phase noise more.
- Because of the limitation placed on  $\omega_n$ , the system bandwidth is limited.
- Thus another drawback resulting from the limited loop bandwidth of the integer-N architecture is the higher close-in phase noise at the VCO output.

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### Example 4.2.1 – Using WEBENCH® EasyPLL Designer Tool from Texas Instruments to Design the Loop Filter



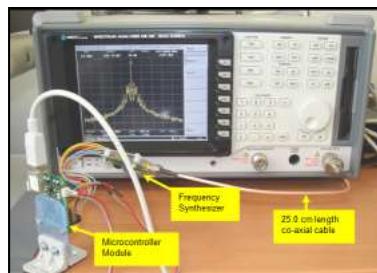
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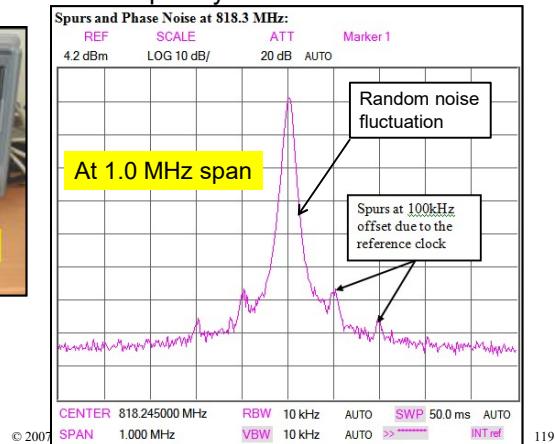
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## Example 4.2.2 – Integer-N Frequency Synthesizer 1

- Here is an example of the output of an integer-N frequency synthesizer based on LMX2326 from National Semiconductor (now becomes part of Texas Instruments). The reference frequency is 100 kHz.

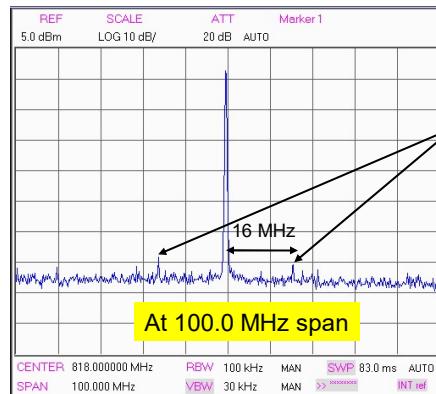


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## Example 4.2.2 Cont...

- Here we can see the spurs at 16.0 MHz offset due to bad power supply decoupling of the VCO.



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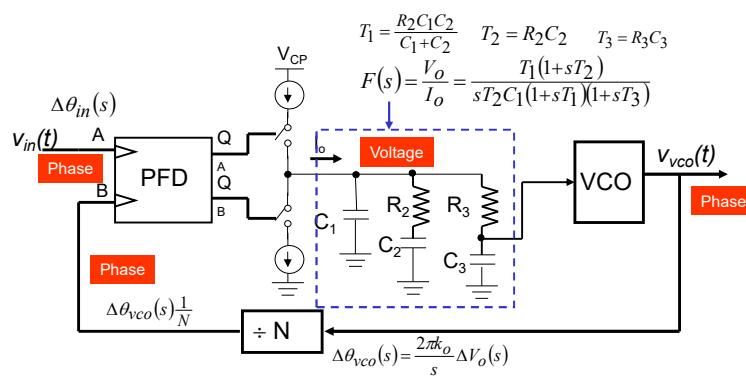
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## Summary – Design Trade-Off for Loop Bandwidth

Here we assume VCO is the most noisy components in the frequency synthesizer, and we should have large PLL bandwidth to suppress this noise.

PLL or Loop Bandwidth	Small	Large
Speed	Slower (larger lock-time)	Faster (smaller lock-time)
VCO contribution to close-in output phase noise	Medium suppression	Good suppression
Output phase noise contribution due to PD, filter, amplifier and divider	Good suppression	Medium suppression

## Appendix A – Transfer Function of Synthesizer with Higher Order Loop Filter (1)



## Appendix A – Transfer Function of Synthesizer with Higher Order Loop Filter (2)

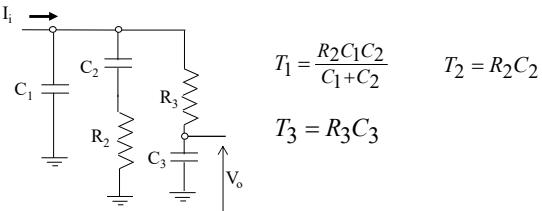
Open-loop gain:  $G(s) = \frac{k_o k_\phi}{sN} F(s) \quad k_\phi = \frac{I_o}{2\pi}$

Feedback:  $H(s) = \frac{1}{N}$

Close-loop response:  $\frac{\Delta\theta_{VCO}}{\Delta\theta_{in}} = \frac{\frac{k_o k_\phi}{s} F(s)}{1 + \frac{k_o k_\phi}{sN} F(s)}$

Third order RC

$$F(s) = \frac{V_o}{I_o} = \frac{T_1(1+sT_2)}{sT_2C_1(1+sT_1)(1+sT_3)}$$



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## 4.3 – Fractional-N and Other Architectures

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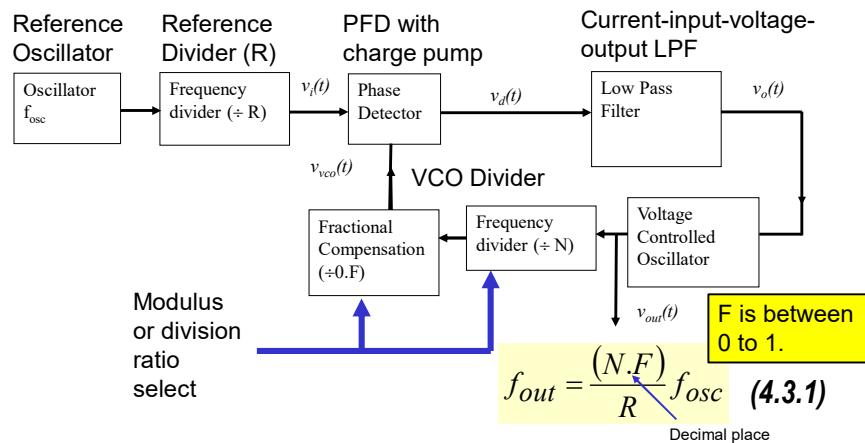
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## Fractional-N Architecture (1)

- In the integer-N architecture, the loop bandwidth and hence  $\omega_n$  is limited because the input reference frequency must be equal to the channel spacing.
- This results from the property that the output frequency changes by integer multiples of  $f_{ref}$ .
- For small channel spacing the reference frequency  $f_{ref}$  is small, and value of N large. **Small  $f_{ref}$  results in small loop bandwidth ( $BW < 0.1f_{ref}$ ), and large N results in small damping factor (See equation (4.2.2)), causing instability.**
- In the fractional-N synthesizers, the output frequency can vary by a fraction of the input frequency, allowing  $f_{ref}$  to be much greater than the channel spacing, and smaller divider ratio N.
- This in turn allows larger loop bandwidth, and as a result ‘speeds up’ the time-domain response of fractional-N synthesizer and results in better phase noise suppression of the VCO output.

## Fractional-N Architecture (2)

- Block diagram of a typical Fractional-N frequency synthesizer.



## Achieving Fractional Division

- Thus for example if  $f_{osc} = 10 \text{ MHz}$ ,  $R=10$ ,  $N = 800$ ,  $F=1$ .
- Let  $f_{ref}$  be the output from the R divider, then:

$$f_{ref} = \frac{10\text{MHz}}{10} = 1000\text{kHz}$$

$$f_{vco} = (800.1) \times 1000\text{kHz} = 800.1 \text{MHz}$$

(1) Reduce N  
 (2) Increase  
 f<sub>vco</sub>  
 (3) Maintain freq.  
 resolution.

- The fractional division is achieved by an averaging process. For instance if we divide with  $N = 800$  for 9 cycles of reference frequency  $f_{ref}$ , and divide with  $N+1 = 801$  for 1 cycle of  $f_{ref}$ , then the average division would be:

<u>N</u>	<u>M</u>	<u>m</u>	<u>Epiphany</u>
800	10	0	$\frac{800}{10} = 80$
800	10	1	$\frac{800 \cdot 1}{10} = 80$
800	10	2	$\frac{800 \cdot 2}{10} = 160$
⋮	⋮	⋮	⋮

$$M = 100 \quad m = 10 \quad \frac{1}{10} \quad \frac{2}{10}$$

$$N_{average} = 800.1 = 800 + \frac{1}{10} = N + \frac{m}{M}$$

$0.1 = \frac{1}{10} \leftarrow \text{Fraction}(m)$   
 $10 \leftarrow \text{Modulus}(M)$

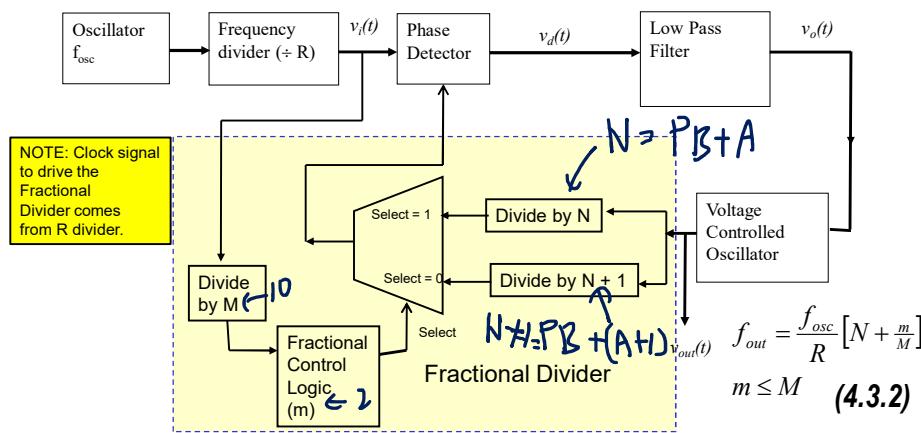
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## Implementing Fractional Divider (1)

- Based on averaging process [2], a modern fractional divider can be implemented with two digital dividers as shown.



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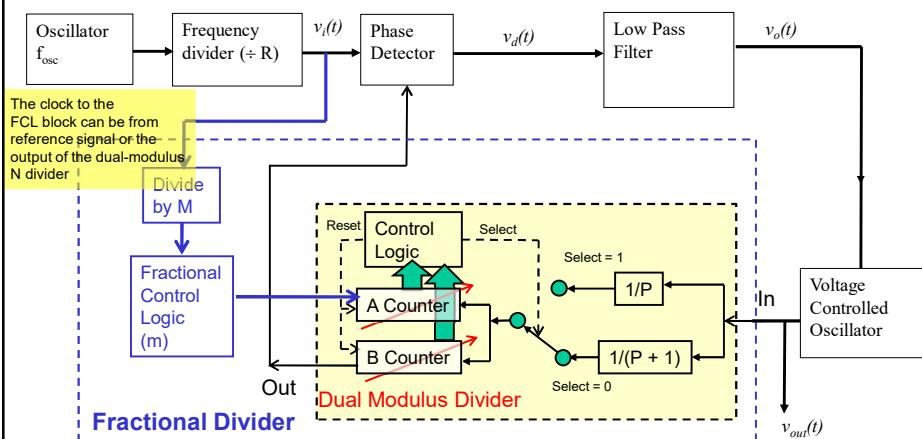
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## Implementing Fractional Divider (2)

- The divide-by-N and divide-by-(N+1) modules are similar to the dual-modulus divider discussed in Integer-N Frequency Synthesizer.
- For instance from (4.1.4):  $N = PB + A$
- To increment the division by 1, one method is to increase the A counter in the dual-modulus divider.  $N + 1 = PB + (A + 1)$
- Thus the Control Logic for fractional compensation will keep track of the reference cycles  $f_{ref}$ , and modulate the value in A counter periodically to achieve fractional compensation via average process [8].

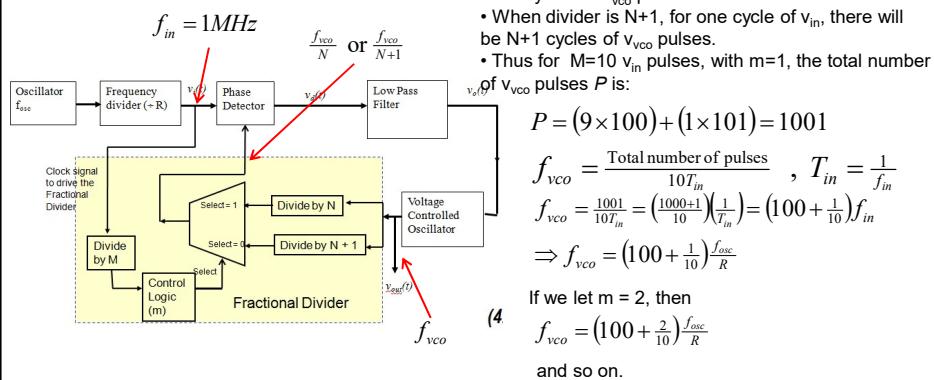
## Implementing Fractional Divider (3)

- Thus a Fractional-N synthesizer based on dual-modulus divider is typically implemented as shown [8]:



## Example 4.3.1 – Fractional Divider

- For instance let  $M = 10$ ,  $m = 1$ ,  $f_{osc} = 10\text{MHz}$ ,  $R=10$  and  $N = 100$ .
- This means the divider will divide the input with  $N$  for  $(M-1)$  times and divide by  $N+1$  for 1 time.



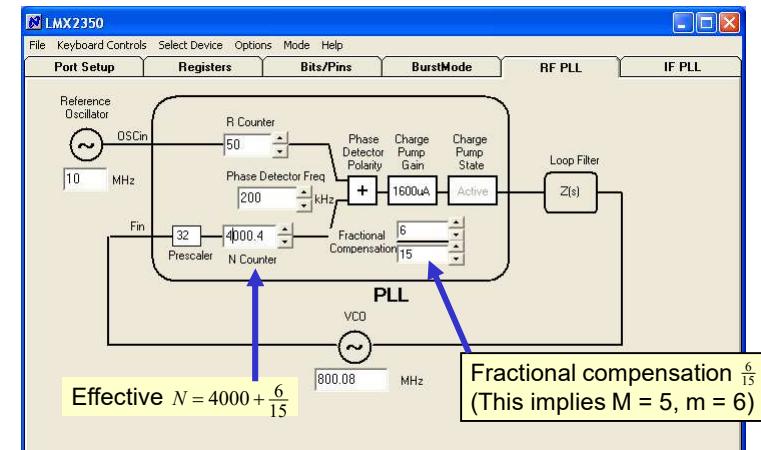
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## Exercise 4.3.1 - Fractional-N Synthesizer IC

- From Codeloader 4™ software, we choose LMX2350, a dual RF/IF synthesizer IC.



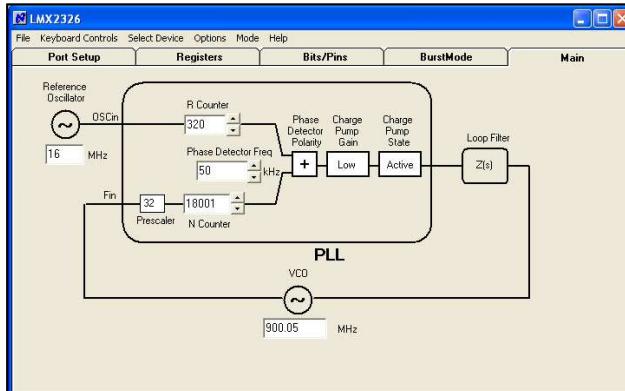
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## Exercise 4.3.1 Cont...

- Suppose we would like to built a frequency synthesizer with  $f_{osc} = 16.0$  MHz, and a channel spacing of 50.0 kHz. Using Integer-N PLL IC, LMX2326, we would need to set  $f_{ref} = 50.0$  kHz. To synthesize 900.05 MHz, the dividers in the IC would be set as follows:



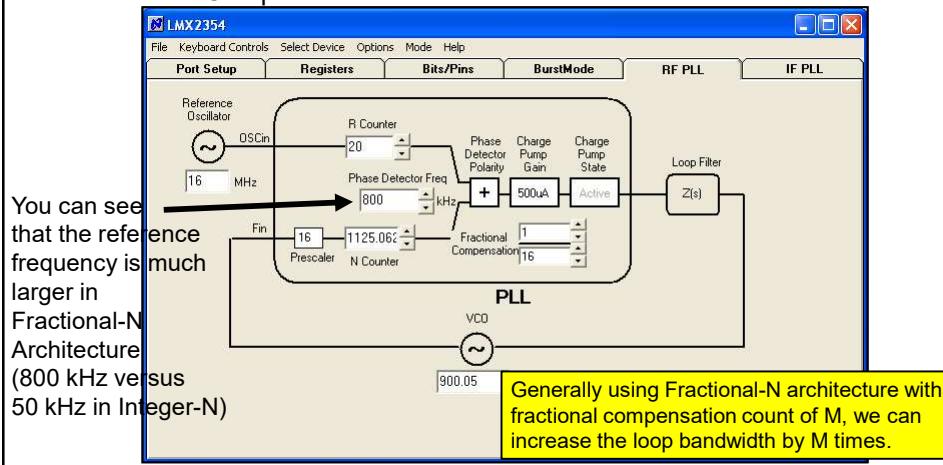
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## Exercise 4.3.1 Cont...

- If we use a fractional-N synthesizer IC, such as the LMX2354, with Fractional Compensation:



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## Spurs in Fractional-N Frequency Synthesizer (1)

- Fractional-N synthesizer suffers from a critical drawback called **Fractional Spurs**.
- Suppose the VCO frequency is fixed and is fed into a Fractional Divider.
- Due to the usage of two dividers (Divide by N and divide by N+1), the pulse width from the output of the Fractional Divider is not constant.
- When divided by N the pulse width is smaller (because higher frequency), and when divided by N+1 the pulse width is slightly larger.
- On the contrary the pulse width from the output of the Reference Divider is fixed.
- Thus when these two outputs are fed into the PFD, the output of the PFD contains pulses even when the PLL is locked.
- In general without any precaution, the fractional spurs are larger than the spur in Integer-N architecture and diminish any advantages of Fractional-N.

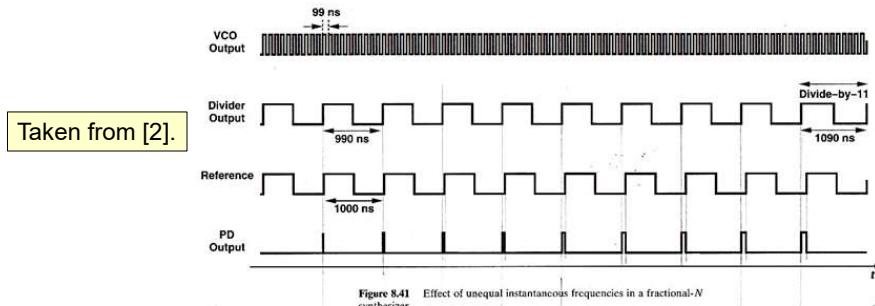
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## Spurs in Fractional-N Frequency Synthesizer (2)

- An illustration of the physical basis of the fractional spur. In this case the VCO frequency is 10.1MHz, and the reference frequency is 1MHz, thus the divider ratio is 10.1. To achieve this the N in the dual modulus is set to 10.



Thus the VCO output will be divided by 10 for 9 times and divided by 11 once for each cycle.

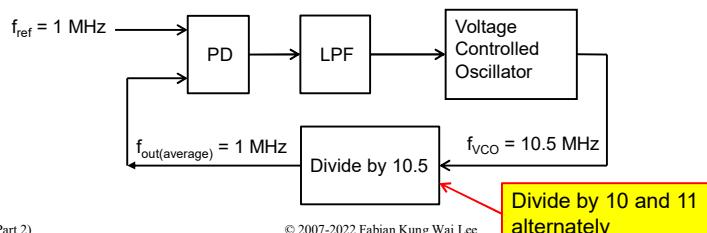
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## More on the Mechanism of Fractional Spurs (1)

- Consider the following Fractional-N synthesizer using PFD charge-pump PLL:
- $f_{ref} = 1 \text{ MHz}$ ,  $N = 10$
- $M = 2$ , and  $m = 1$ .
- Thus the effective divider ratio is  $N + m/M = 10 + (1/2) = 10.5$ .
- The VCO should be oscillating at 10.5 MHz during phase-locked. This is achieved by dividing the VCO output by 10 and 11 alternately.
- The next slides shows the waveforms under steady-state.



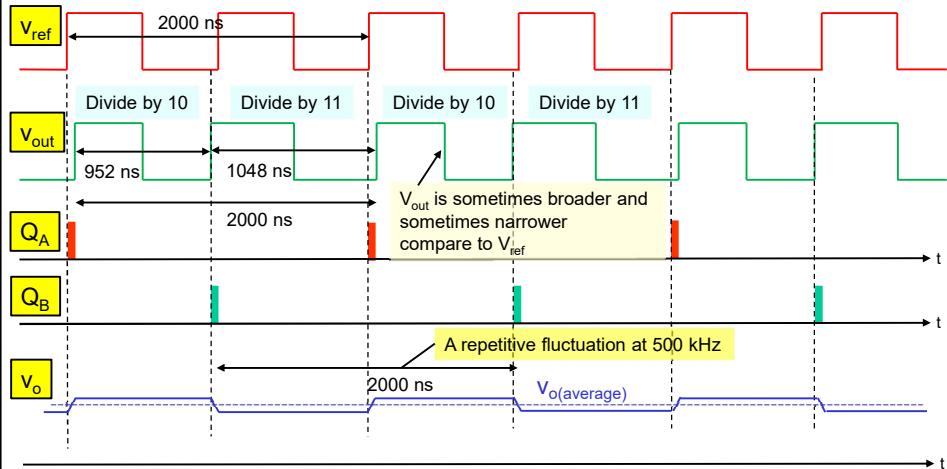
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## More on the Mechanism of Fractional Spurs (2)

- Waveforms at various points on the PLL during phase-locked.



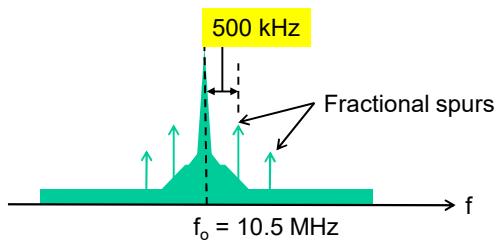
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## More on the Mechanism of Fractional Spurs (3)

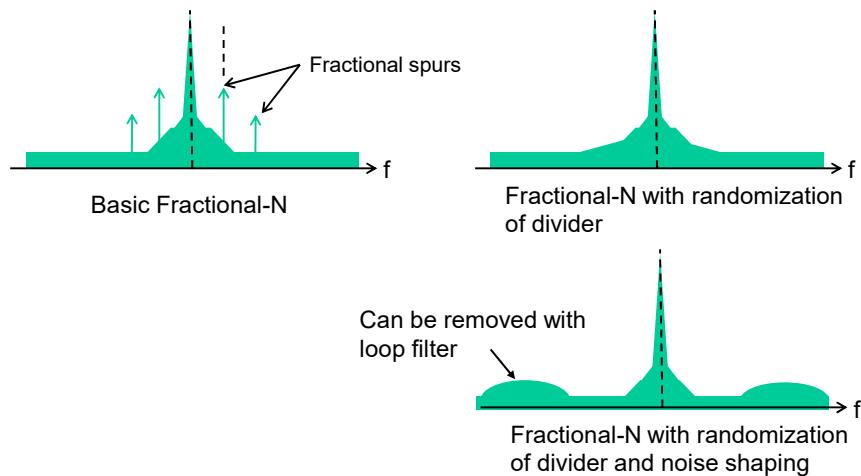
- The frequency spectra in the vicinity of the VCO output:



## Controlling Spurs in Fractional-N Frequency Synthesizer (1)

- A number of ways can be used to minimize fractional spurs.
  - Incorporate a second charge pump to compensate for the voltage ripple, this is usually called analog compensation.
  - Using more than 2 dividers in the Fractional Divider. For instance we have seen that to implement a divide by 100.25, we use N=100 and N=101. We can also use 4 dividers with N = 98, N=99, N=100 and N=101.
  - Incorporate a Randomizer and Noise Shaping, e.g. an algorithm that choose a pair of dividers from the many available in the Fractional Divider to cancel out the voltage ripples from the PFD with Charge Pump, or change the power spectral density of the phase noise from the divider via noise shaping. A standard method of noise shaping is using the Delta-Sigma modulator to select the divider, hence the term **Delta-Sigma Fractional-N synthesizer** ([2], [7]).
- And many others.

## Controlling Spurs in Fractional-N Frequency Synthesizer (2)



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## Example 4.3.2 – Fractional-N Frequency Synthesizer IC (ADF4156)

- Block diagram of Analog Devices ADF4156 RF fractional-N frequency synthesizer IC.

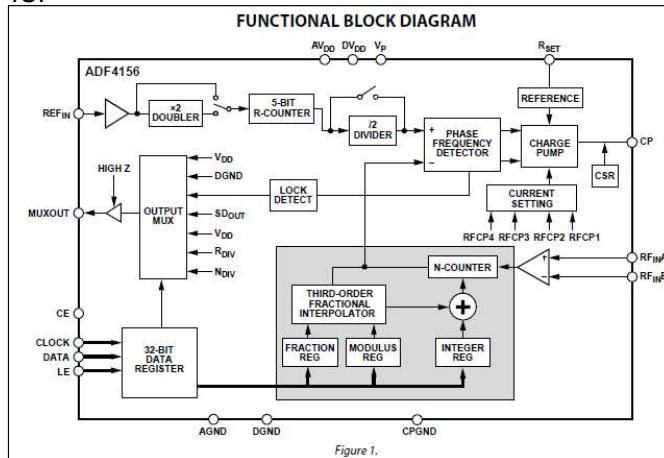


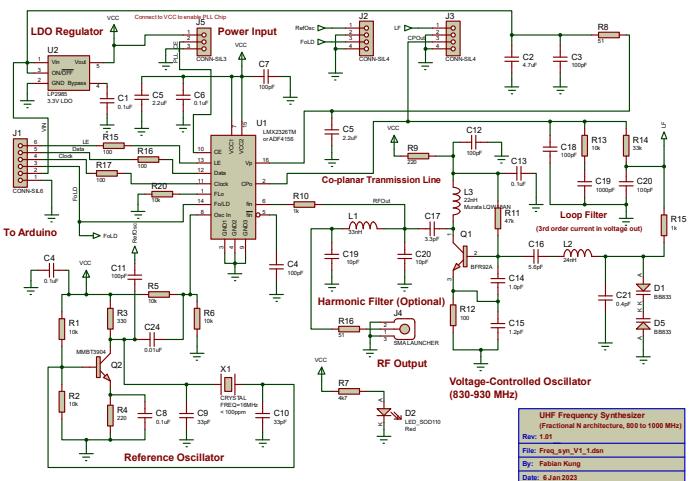
Figure 1.

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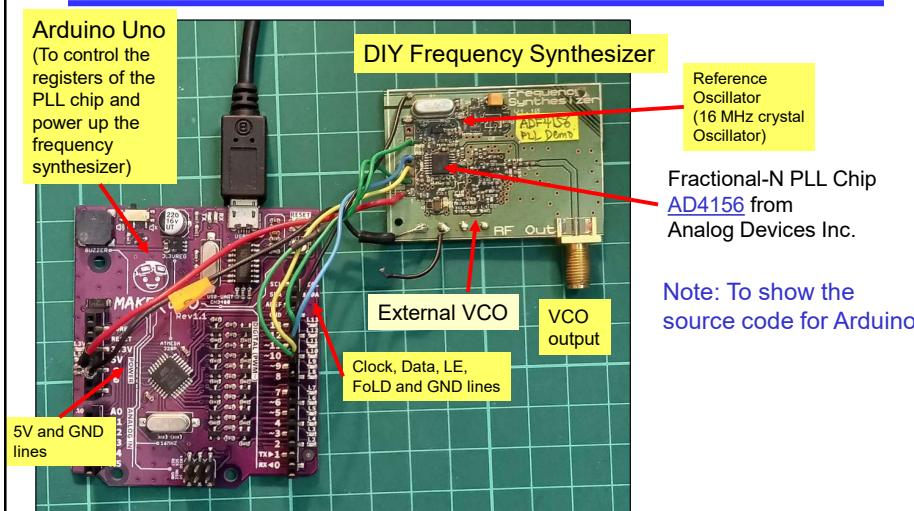
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### Example 4.3.3 – A DIY Fractional-N Frequency Synthesizer Module Using ADF4156 PLL Chip



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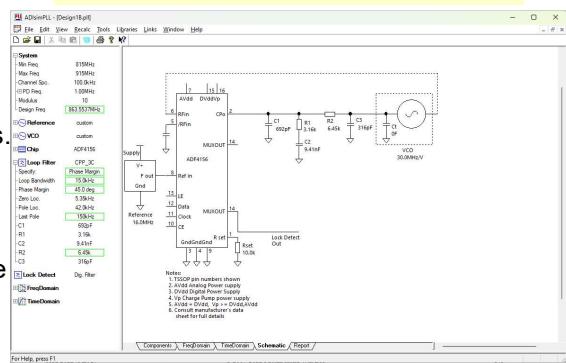
### Example 4.3.3 Cont...



## Example 4.3.3 Cont...

- Here we have constructed an RF Frequency Synthesizer using Fractional-N PLL chip ADF4156 (up to 6.2 GHz). We can also substitute the PLL chip with other families from ADI Corporation's ADF415x series or from Texas Instrument's LMX23xx series.
- The frequency synthesizer is powered from USB port via Arduino UNO single-board computer, the registers in the PLL chip are set using SPI (serial peripheral interface) protocol via Arduino UNO.

Screen shot of computer simulation using ADIPLL Software



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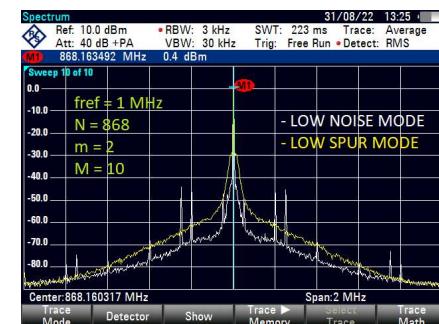
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## Example 4.3.3 – Fractional-N Frequency Synthesizer Output (1)

- Comparison between Low-Noise and Low-Spur Modes. Note that the spurs depends on the fractional value.



Frequency Divider in Integer Mode



Frequency Divider in Fractional Mode

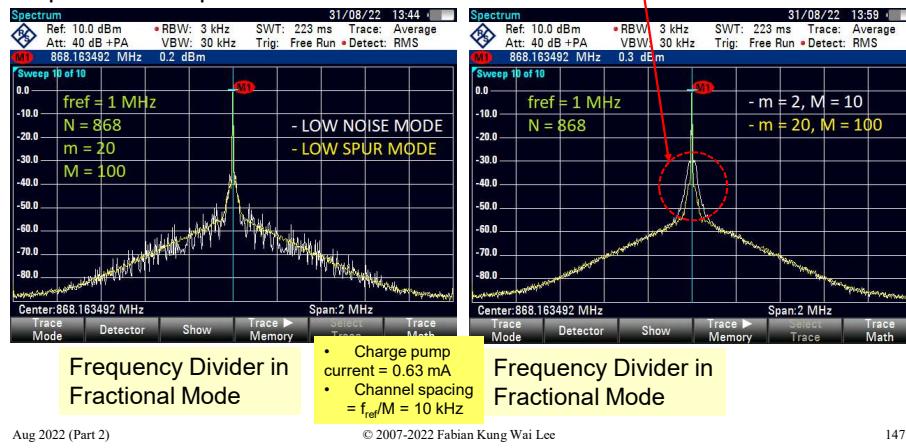
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## Example 4.3.3 – Fractional-N Frequency Synthesizer Output (2)

- Another comparison with VCO output set to 868.2 MHz at Low Noise Mode, with different modulus  $M$ . Notice that larger  $M$  gives better near-in phase noise performance.



## Example 4.3.3 – Fractional-N Frequency Synthesizer Output (3)

- The datasheet for ADF4156 also recommends using higher PFD comparison frequency to reduce phase noise: “*The on-chip reference doubler allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency, which in turn improves the noise performance of the system. Doubling the PFD frequency usually improves noise performance by 3 dB.*”

Most likely with smaller comparison interval, the voltage changes for  $V_{tune}$  is smaller, resulting in less periodic and Non-periodic fluctuation from the non-ideal effect of the PFD.

## Example 4.3.3 – Fractional-N Frequency Synthesizer Output (4)

- We can select different randomizer modes, comparison of spectrum between **low-spur** and **low-noise** spectrum shaping mode (e.g. randomizer),  $f_o = 860.60$  MHz.



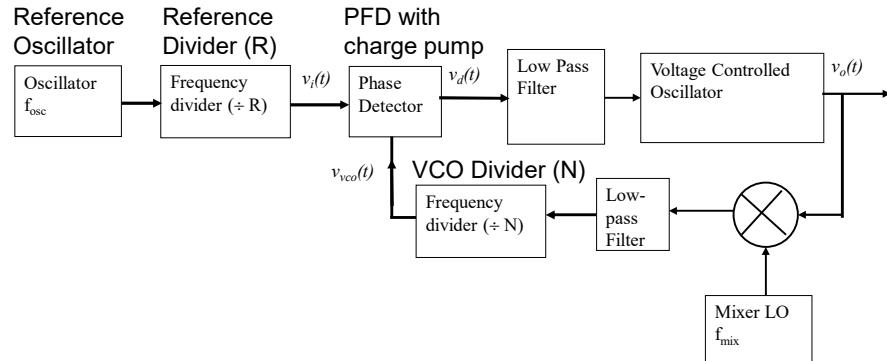
## Example 4.3.3 – Fractional-N Frequency Synthesizer Output (5)

- Control voltage to VCO during switching between 860 MHz and 870 MHz, PLL set to low noise mode.



## PLL Based Synthesizer with Heterodyning

- Adding a fixed mixer allows the VCO to operate at a frequency higher than the digital components.



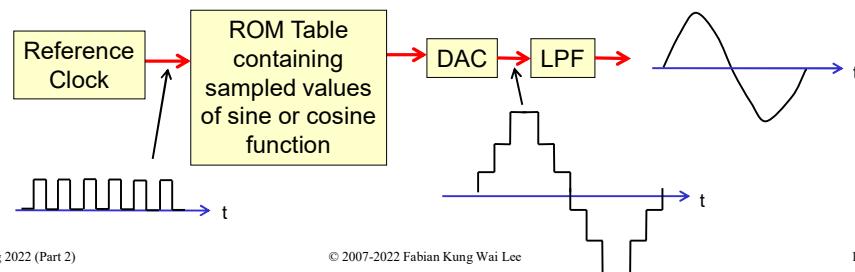
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## Direct Digital Synthesis (DDS) (1)

- DDS is another approach to generate a stable frequency with fine frequency step with certain advantages and disadvantages to phase-locked approach.
- The basic idea of DDS is to generate the signal in the digital domain using a powerful microprocessor or digital signal processing IC, utilize D/A (digital-to-analog) conversion and filtering to reconstruct the waveform in the analog domain.
- As with PLL synthesizer, a very stable reference clock is required.



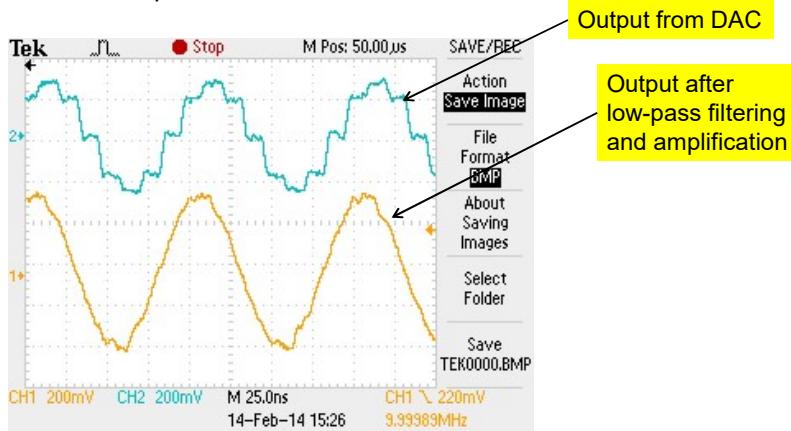
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## Direct Digital Synthesis (DDS) (2)

- A 10 MHz Sine Wave generated using FPGA (Altera Cyclone IV) and high-speed DAC chip with 160 MHz clock.



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## Direct Digital Synthesis (DDS) (3)

- Advantages of DDS:
  - Avoiding the use of analog VCO, DDS achieves a low phase noise, roughly that of the reference clock.
  - Provide very fine frequency steps, as low as 0.1 Hz.
  - Exhibit much faster channel/frequency switching, with continuous phase.
  - Allows direct modulation of the output signal in digital domain.
- Disadvantages of DDS:
  - Speed, at present is limited to 500 MHz and below to keep the cost reasonable. Typically the reference clock frequency needs to be 4x to 8x the **practical** maximum output frequency.
  - Higher cost compare to PLL based frequency synthesizer.
  - Higher power consumption.

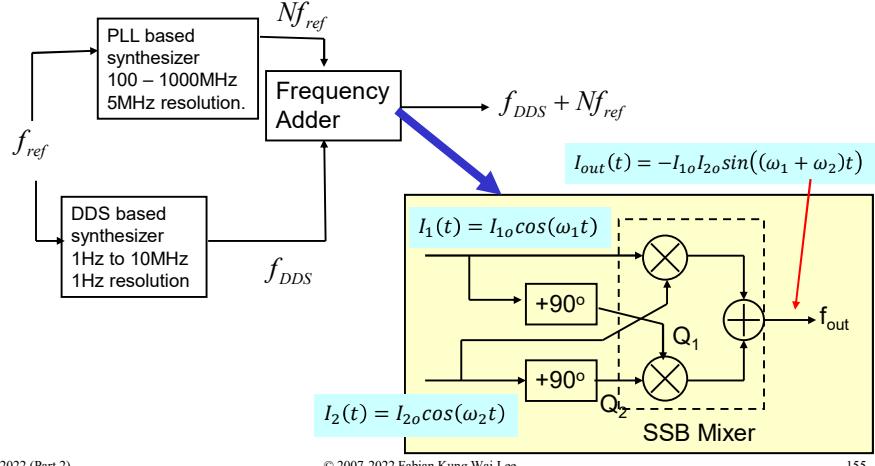
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## Combining DDS and PLL Based Frequency Source

- Another alternative approach to generating fine frequency steps.



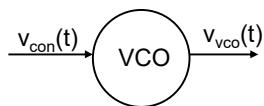
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## Appendix B – VCO Jitter Estimation from Phase Noise (1)

- Here we only focus on a sinusoidal waveform in time-domain.
- Assumption 1** - The phase noise can be assumed as due to FM modulation of the VCO output. This FM modulation is due to fluctuation of the control voltage of the VCO.
- Assumption 2** – The FM spectrum of the VCO output can be approximated as narrowband FM.
- Using Carson's Rule: (for instance see B. P. Lathi, "Modern digital and analog communication systems", 3<sup>rd</sup> edition, Oxford University Press, 1998)
$$B_{FM} = 2(\Delta f + B)$$
- Where:  $B_{FM}$  = Bandwidth of  $v_{vco}(t)$  spectrum in Hz.  
 $\Delta f$  = Frequency deviation in Hz.  
 $B$  = Bandwidth of modulating signal  $v_{con}(t)$ .



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## Appendix B – VCO Jitter Estimate from Phase Noise (2)

- The modulating signal bandwidth  $B$  can be taken as the loop filter bandwidth.  
$$B_{LF} = B$$

- With this in mind,

$$\Delta f = \frac{B_{FM}}{2} - B_{LF}$$

- $B_{FM}$  can be measured from Spectrum Analyzer, assuming it to be the frequency offset when the spectrum is 40 - 50 dB below the center frequency.

- Thus:  
$$f_{\max} = f_c + \frac{\Delta f}{2} \quad f_{\min} = f_c - \frac{\Delta f}{2}$$

- Where  $f_c$  is the center frequency. And the corresponding period is

$$T_{\max} = \frac{1}{f_{\min}} \quad T_{\min} = \frac{1}{f_{\max}}$$

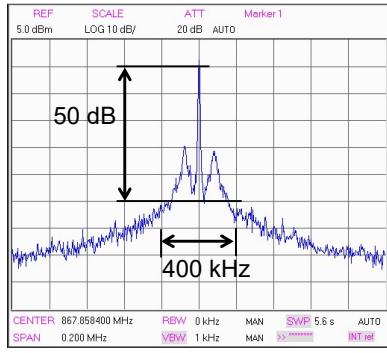
## Appendix B – VCO Jitter Estimate from Phase Noise (3)

- Hence the jitter estimate is:

$$\begin{aligned}\Delta t &= T_{\max} - T_{\min} = \frac{1}{f_c - \frac{\Delta f}{2}} - \frac{1}{f_c + \frac{\Delta f}{2}} \\ \Rightarrow \Delta t &= \frac{\Delta f}{f_c^2 - \left(\frac{\Delta f}{2}\right)^2} \approx \frac{\Delta f}{f_c^2} \\ \Rightarrow \Delta t &\approx \frac{\frac{B_{FM}}{2} - B_{LF}}{f_c^2}\end{aligned}$$

## Appendix B – VCO Jitter Estimate from Phase Noise (4)

- An example.
- Suppose center frequency is 868 MHz, bandwidth of the phase noise from measurement is 400 kHz, and the loop filter bandwidth is 10 kHz.



$$f_c := 868.0 \cdot 10^6 \quad BFM := 40000$$

$$BLF := 10000$$

$$\Delta t := \frac{BFM - BLF}{fc^2}$$

$$\Delta t = 2.522 \times 10^{-13}$$

## Lab – Build Your Own PLL

- In this exercise you will be given the opportunity to build a digital PLL using the CMOS integrated circuit 74HC4046.
- 74HC4046 contains a build-in relaxation VCO, Type 1, Type 2 and Type 3 digital PDs.
- See the attached datasheet and handout.
- Here you could use the Type 2 PD to build a 0.1 – 1.0 MHz PLL.
- Things to try out:
  - (a) Plot the VCO frequency versus the control voltage, get  $k_o$ .
  - (b) Calculate  $k_\phi$  and lock range of the PLL.
  - (c) Connect a square wave (50% duty cycle) signal generator to the input of the PLL, use oscilloscope to observe the acquisition transient.
  - (d) Demonstrate tracking mode by varying the frequency of the signal generator.

---

**THE END**