INTRODUCTION TO PHASE-LOCKED LOOP AND FREQUENCY SYNTHESIZER Part 1

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Agenda

- 1 - Review of basic concepts – signal representation. (Day 1)
- 2 - Introduction to Phase-Locked Loop (PLL) – Block diagram, behavior and components. (Day 1)
- 3 – Calculation Exercise and Demo of PLL. (Day 1)
- 4 – Dynamic model of PLL. (Day 2)
- 5 – Review of feedback control. (Day 2)
- 6 – Dynamic Performance of PLL – Loop bandwidth, lock time, spurs and noise. (Day 2)
- 7 – PLL-Based Frequency Synthesizer – Integer and Fractional-N architecture. (Day 2)
- 8 – Computer Analysis of PLL. (Day 2)
- 9 – Further discussion PLL-Based Frequency Synthesizer – Integer and Fractional-N dividers, Dynamic Performance and Noise. (Day 3)
- 10 – Case Study of Frequency Synthesizer Design and Demo. (Day 3)
- 11 – Other Topics of Interests – Other architectures, Direct Digital Synthesis, Delay-Locked Loop. (Day 3)

References

- [1] P. H. Young, “Electronic communication techniques”, 5th Edition, 2004 Prentice-Hall.
- [2] B. Razavi, “RF microelectronics”, 1998 Prentice-Hall (2nd edition, 2012 Prentice Hall is also used).
- [3] J. R. Smith, “Modern communication circuits”, 1998 McGraw-Hill.
- [4] W. F. Egan, “Frequency synthesis by phase lock”, 2000 John-Wiley & Sons.
- [5] F. Gardner, “Phaselock techniques”, 2nd Edition, 1979 John-Wiley & Sons. (3rd edition published in 2005 is also available)
- [6] G. Bianchi, “Phase-locked loop synthesizer simulation”, 2005 McGraw-Hill.
- [7] D. Banerjee, “PLL performance, simulation and design”, 5th edition 2017, Texas Instruments [https://www.ti.com/lit/ml/snaa106c/snaa106c.pdf].
- [8] C. Barrett, “Fractional/integer-N PLL Basics”, SWRA029, 1999, Texas Instruments Technical Brief.
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- [10] B. Razavi, “Design of CMOS phase-locked loops: From circuit level to architecture level”, 2020, Cambridge University Press.

1 - Review of Basic Concepts

1.1 – Sinusoidal Signal and Representation

Sinusoidal Signal – Magnitude, Frequency and Phase (1)

- In engineering we usually deal with sinusoidal signal. This is because many non-sinusoidal signals can be expressed as a combination of sinusoidal components by the use of **Fourier Series** and **Fourier Transform**.
- Consider a periodic sinusoidal voltage signal $v_1(t)$:

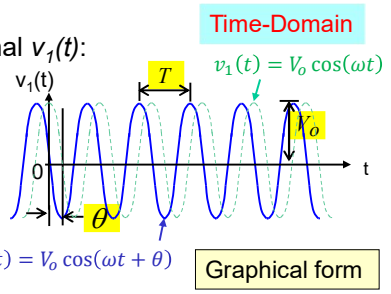
Frequency (radian/sec)

$$v_1(t) = V_o \cos(\omega t + \theta)$$

Magnitude (volts)

Excess Phase

Phase (radian)



Expression form (function of time *t*)

Graphical form

Frequency in Hertz $f = \frac{1}{T}$ ***(1.1.1a)***

Frequency in Rad/sec $\omega = 2\pi f = \frac{2\pi}{T}$ ***(1.1.1b)***

Note: $\alpha = \omega t + \theta$

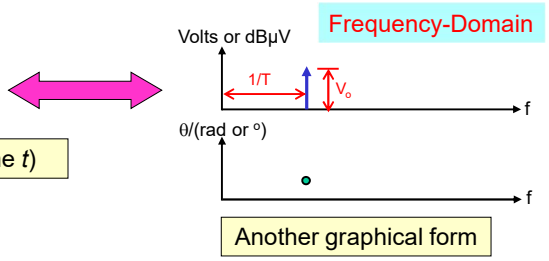
$\omega = \frac{d}{dt}(\alpha)$ ***(1.1.2)***

Sinusoidal Signal – Magnitude, Frequency and Phase (2)

- Another graphical representation of sine wave.

$$v_1(t) = V_O \cos(\omega t + \theta)$$

Expression form (function of time t)



Another graphical form

Signal Representations – Periodic and Non-Periodic Signals

$$v(t) = \sum_{n=-\infty}^{\infty} c_n e^{jn\frac{2\pi}{T}t}$$

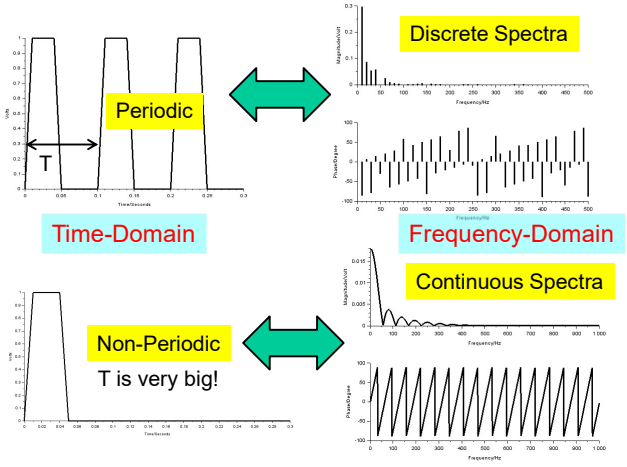
$$c_n = \frac{1}{T}\int_{-\infty}^{\infty} v(t) e^{-jn\frac{2\pi}{T}t} dt$$

Fourier Series

$$v(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} V(\omega) e^{j\omega t} d\omega$$

$$V(\omega) = \int_{-\infty}^{\infty} v(t) e^{-j\omega t} dt$$

Fourier Transform



1.2 – Voltage and Current Phasors

More Compact Representation of Sinusoidal Signal (1)

- Thus, we see that 3 parameters are needed to sufficiently describe a sinusoidal signal – frequency (f), magnitude (V_o) and excess phase (θ) (sometimes also called the phase shift).
- Of these, magnitude and excess phase usually carry more information about the signal if the system is **Linear**.
- In most linear system, if the source frequency is f_o, then we know that the frequency everywhere in the system will also be f_o. However the magnitude and excess phase of the voltage and current signals can vary from point to point.

More Compact Representation of Sinusoidal Signal (2)

- This prompt the introduction of a more compact representation of sinusoidal signals without *f*, called the voltage and current phasors.
- Whenever there is no ambiguity, it is a usual practice to refer the excess phase as the phase of the signal.
- **Thus, from now on, unless otherwise specified, we imply excess phase whenever we use the word phase**.

Phasor (1)

- A sinusoidal signal can be expressed in complex exponent form:

$e^{j\alpha} = \cos\alpha + j\sin\alpha$ (Euler's formula), $j = \sqrt{-1}$, $\alpha = \omega t + \theta$

$$V_o e^{j(\omega t+\theta)} = V_o\cos(\omega t+\theta) + jV_o\sin(\omega t+\theta)$$

Real Imaginary

- Thus $v_1(t) = V_o\cos(\omega t+\theta)$ can be written as:

$$v_1(t) = \mathrm{Re}\left\{V_o e^{j(\omega t+\theta)}\right\} = \mathrm{Re}\left\{V_o e^{j\theta} e^{j\omega t}\right\} \Leftrightarrow V_1(\omega) = V_o e^{j\theta} \quad \textbf{(1.2.3)}$$

Both can be dependent on frequency ω

Phasor

Take magnitude and excess phase, form complex exponent

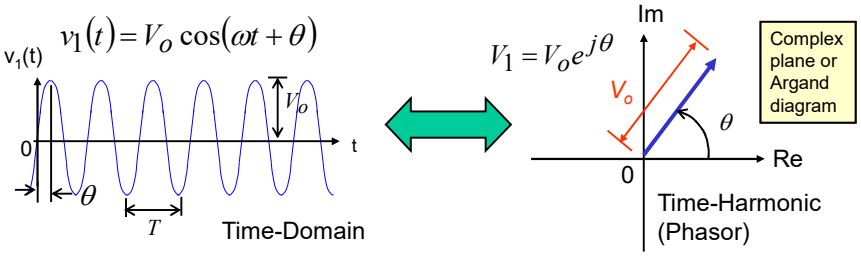
- The term $V_1 = V_o e^{j\theta}$ is called the phasor, or the time-harmonic form.
- As a convention we normally use the small letter to represent time-domain signal, and the capital letter to represent the phasor.

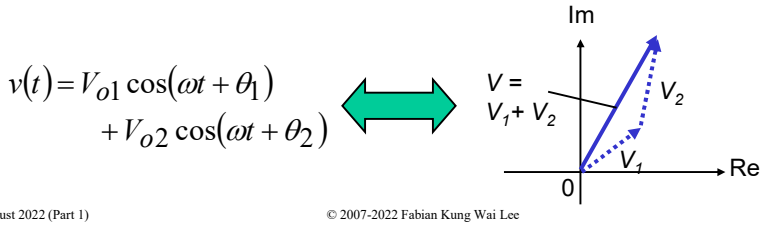
$v_1(t) \rightleftharpoons V_1(\omega)$

signal phasor

Phasor (2)

- The phasor can be visualized as a vector in graphical form:





Example 1.2.1

- Given a phasor, we can obtain the time-domain form as follows:
  - Multiply the phasor with $e^{j\omega t}$.
  - Take the real part of the product.
- Example:

Time-domain form of a current $i(t) = 0.25\cos\left(2\pi\left(2.0\times10^6\right)t + 0.125\pi\right)$

$f = 2.0\times10^6 = 2\ MHz \quad \theta = 0.125\pi$

Phasor $I = 0.25e^{j0.125\pi}$

To get back the time-domain form

$$i(t) = \mathrm{Re}\left\{Ie^{j2\pi\left(2.0\times10^6\right)t}\right\}$$

$$= 0.25\cos\left(2\pi\left(2.0\times10^6\right)t + 0.125\pi\right)$$

$e^{j\left(2\pi2\times10^6\right)t}$

Why Use Phasors ?

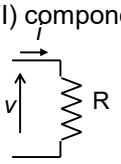
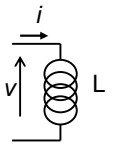
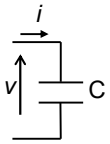
- In many engineering problems we are only interested in the steady-state sinusoidal response of a linear system, i.e. the transfer function, which can be conveniently represented in phasor form.
- Moreover using the phasor notation simplifies the integral-differential equations describing a physical system.
- In particular the differentiation and integration with respect to time *t* become multiplication and division with $j\omega$ respectively under phasor notation.

$$\frac{\partial v}{\partial t} \rightarrow j\omega V(\omega) \quad \text{and} \quad \int_{-\infty}^{t} v(\tau)d\tau \rightarrow \frac{1}{j\omega}V(\omega)$$

- For more discussion on the theory of phasor analysis and Fourier Transform, consult textbooks on electrical circuit and signal analysis.
- The concept of phasor can be extended to complex frequency, giving us Laplace Transformation, which is more general than Fourier Transform.

I-V Relations for RLC Components

- Some common I-V relationships in the time-domain and phasor form for **linear time-invariant** (LTI) components.

Time Domain		Time Harmonic or Phasor Form
$v(t) = Ri(t)$		$V(\omega) = RI(\omega)$
$v(t) = L\frac{di(t)}{dt}$		$V(\omega) = j\omega LI(\omega)$
$v(t) = \frac{1}{C}\int_{-\infty}^{t} i(\tau)d\tau$		$V(\omega) = \frac{1}{j\omega C}I(\omega)$

2 – Introduction Phase-Locked Loop (PLL)

Block Diagram, Behaviors and Components

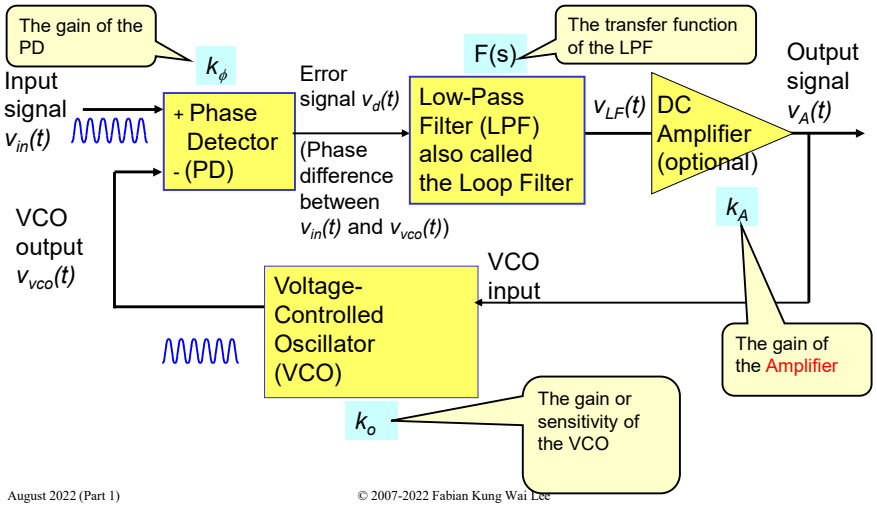
Background

Henri de Bellescize, "La réception synchrone," *L'Onde Électrique* (later: *Revue de l'Electricité et de l'Electronique*), vol. 11, pages 230-240 (June 1932).

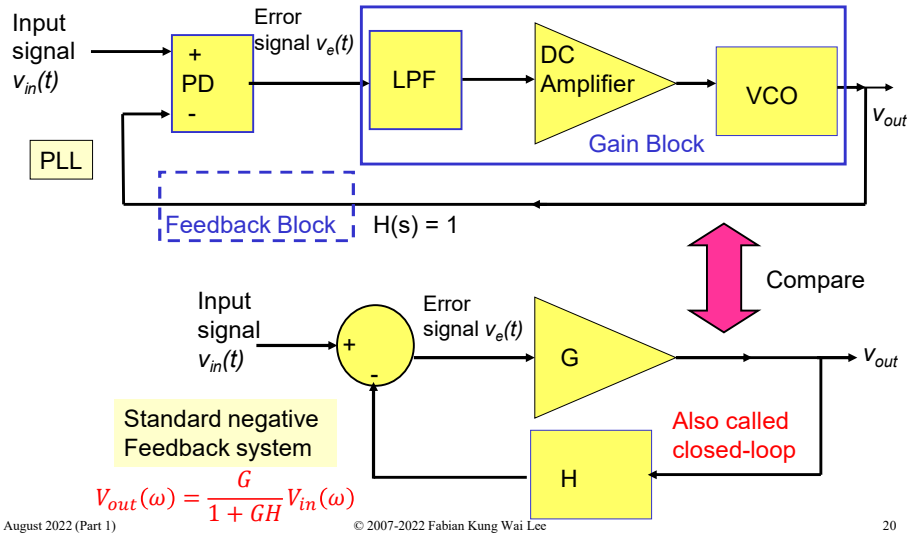
- PLL was introduced as far back as 1932, for synchronous radio detection by H. de Bellescize in France. It was developed as an alternative to American engineer E. Armstrong's super-heterodyne receiver architecture for FM radio demodulation.
- PLL became popular beginning in the 1980s due to the technology of integration - PLL integrated circuits were commercially available (some early well-known PLL ICs are the CD4046, LM565 series).
- Examples of usage:
  - Performs frequency modulation and demodulation on a carrier.
  - Clock synchronization and recovery circuit in communication receivers.
  - Very narrow bandwidth filter for space communication (see [1]).
  - Frequency synthesis (to generate a very stable periodic signal, selectable by user).
  - And many more, the application of PLL is limited only by your imagination.

Block Diagram of a PLL

- PLL is essentially a **negative feedback** system consisting of 4 blocks.

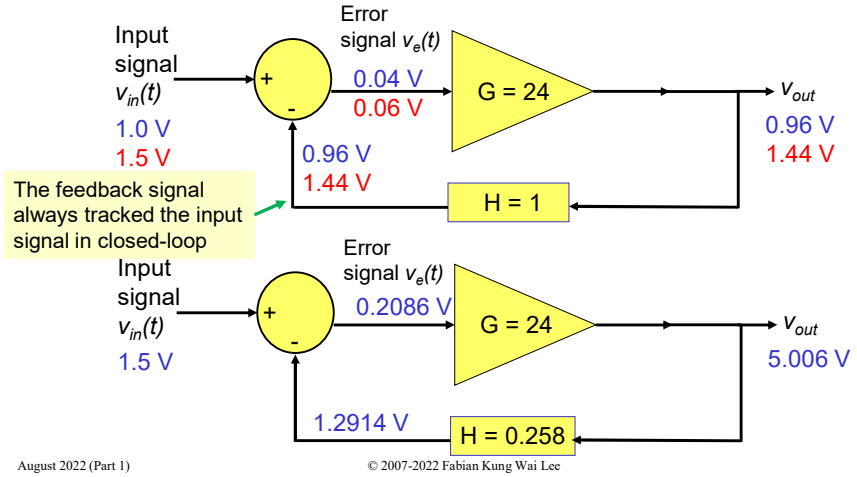


Comparison Between the PLL and a Standard Negative Feedback System



Some Intuitive Understanding of Negative Feedback Behaviors

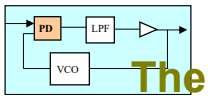
- Here we assume the system already achieved steady-state and is stable.



2.1 – Ideal Phase-Locked Loop Components

Components of PLL

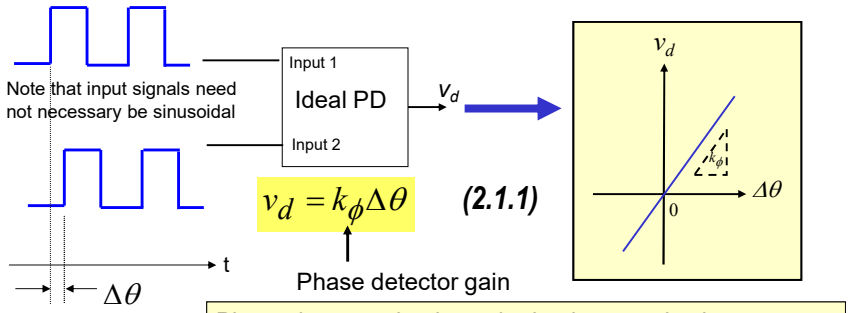
- Phase Detector (PD) - Compare the relative phase relationship of two input signals. A large phase difference between the inputs produces an output with a large dc value.
- Loop Filter - Performs two roles, (a) the loop filter helps to filter out the high frequency signal components generated by the Phase Detector, i.e. to average the output of PD (b) to control the dynamic response of the PLL, e.g. determines how the PLL behaves when the frequency and phase of $v_{in}(t)$ changes with time.
- Voltage Control Oscillator (VCO) - An oscillator whose instantaneous frequency is proportional to an input control voltage.
- Loop Amplifier – A DC voltage amplifier, e.g. amplifies both transient and DC electrical signals, also called a direct-coupled amplifier.



The Ideal Phase Detector (PD) (1)

- The ideal PD produces an output, usually a voltage whose DC or average value is proportional to the phase difference between two input signals.

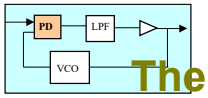
The ideal Phase Detector:



$$v_d = k_\phi \Delta\theta \quad (2.1.1)$$

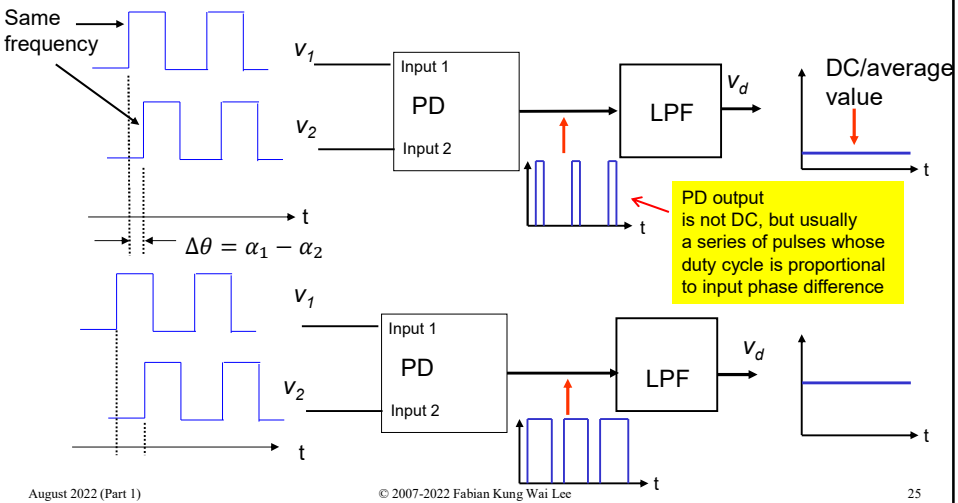
Phase detector gain

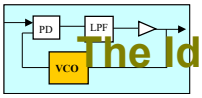
Phase detector circuit can be implemented using analog or digital components, or even entirely in software, hence the terms analog PD, digital PD and software PD.



The Ideal Phase Detector (PD) (2)

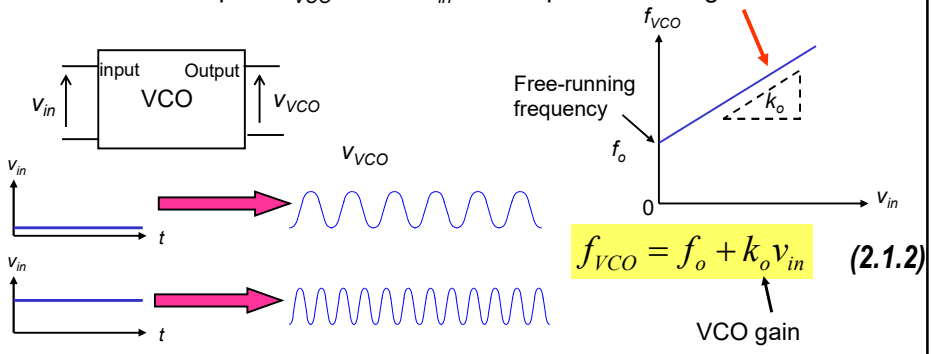
- To produce a DC output, usually a low-pass filter (LPF) is needed.





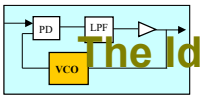
The Ideal Voltage-Controlled Oscillator (VCO) (1)

- The ideal VCO is an oscillator whose instantaneous output frequency f_{VCO} is proportional to a control voltage.
- The frequency when v_{in} = 0 is typically denoted f_o (free-running frequency).
- Note that the slope of f_{VCO} versus v_{in} can be positive or negative.



$$f_{VCO} = f_o + k_o v_{in} \quad (2.1.2)$$

VCO gain



The Ideal Voltage Controlled Oscillator (VCO) (2)

- From (2.1.2), we can write out the mathematical relationship between the output voltage of the VCO versus v_{in} in time domain (for sinusoidal waveform).

$$v_{VCO}(t) = A\cos\left(2\pi f_o t + 2\pi k_o \int_0^t v_{in}(\tau)d\tau + \theta_o\right) \quad \textit{(2.1.3)}$$

Magnitude; Free-running frequency; VCO gain; Excess phase

Compare

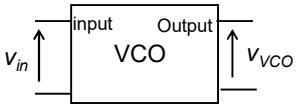
$$v(t) = V_o \cos(2\pi f t + \theta)$$

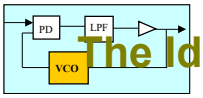
Instantaneous phase of the VCO:

$$\theta_{VCO}(t) = 2\pi f_o t + 2\pi k_o \int_0^t v_{in}(\tau)d\tau + \theta_o$$

Instantaneous frequency of VCO:

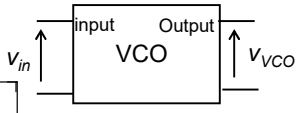
$$f_{VCO}(t) = \frac{1}{2\pi}\frac{d\theta_{VCO}}{dt} = f_o + k_o v_{in}(t)$$

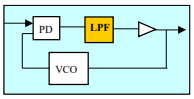




The Ideal Voltage Controlled Oscillator (VCO) (3)

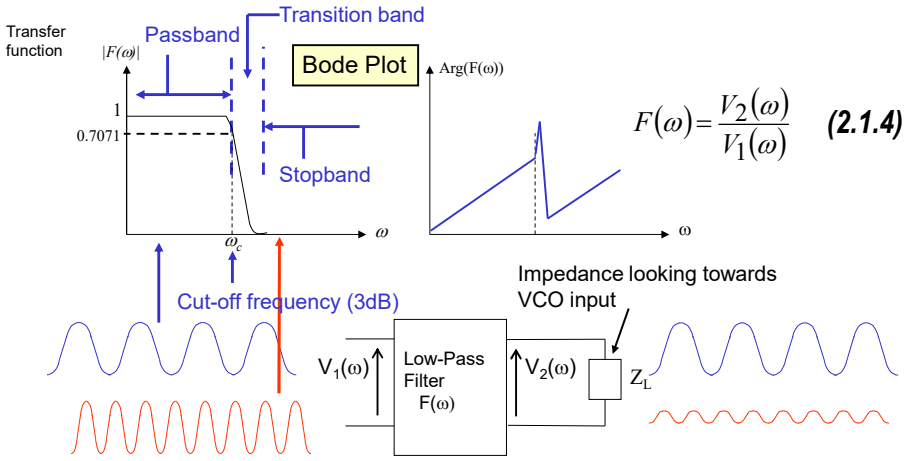
- For example when A=1, k_o= 5 MHz/Volt, f_o = 30 MHz, θ_o = 0.



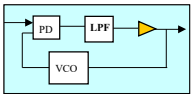


Loop Filter

- The loop filter is a low-pass filter (LPF).

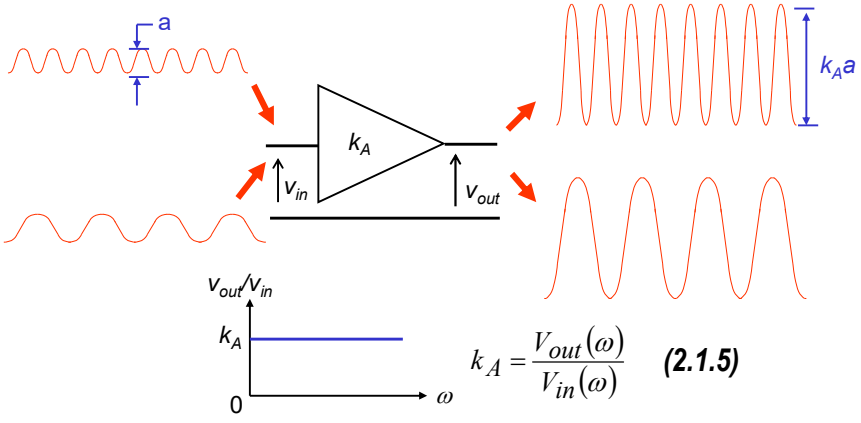


$$F(\omega)=\frac{V_2(\omega)}{V_1(\omega)} \qquad \textbf{(2.1.4)}$$



Loop Amplifier

- The ideal loop amplifier is a voltage amplifier.
- It will amplify AC and DC voltage signals.



$$k_A=\frac{V_{out}(\omega)}{V_{in}(\omega)} \qquad \textbf{(2.1.5)}$$

2.2 – Basic PLL Behaviors

The PLL as a Negative Feedback System (1)

- The idea of a negative feedback system is the output signal is compared with the input signal. The difference between them is amplified and fed back again to the system.
- If the input and output differ a lot, a large error signal results. This large error signal is used to drive the system output to close the 'gap' between input and output.
- In this way the system will self-correct any deviation between the input and output such that there is a consistent relationship between them, i.e. the output 'tracks' the input.
- Note that the output normally will not be equal to the input due to the presence of the feedback block **H(s)**, but there is a consistent relationship between them.

The PLL as a Negative Feedback System (2)

- In the PLL, we see from the block diagram that the output will 'track' the input in a properly designed PLL.
- Since the comparison block compares the input and output signal phase, it is the **phase** of the output signal that **tracks** the input signal's phase, e.g. the output and input signal's phase are **locked** under normal operation.

Phase-Locked

$$v_{in}(t) = V_o \cos(\omega_1 t + \theta_1) = V_o \cos(\alpha_1(t))$$

$$v_{vco}(t) = V_o \cos(\omega_2 t + \theta_2) = V_o \cos(\alpha_2(t))$$

$$\alpha_2(t) - \alpha_1(t) = \text{constant}$$

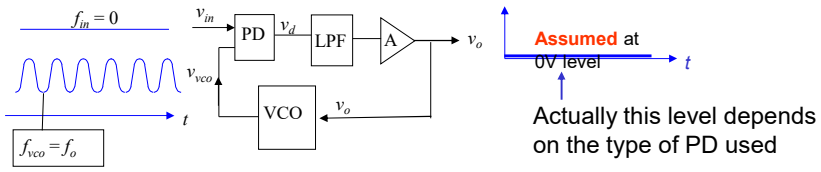
$$\omega_2 = \omega_1$$

- Thus one of the consequence of having input and output signal phase-locked, is they must have similar frequency.

Three Sequences of PLL Operation (1)

Free-Running

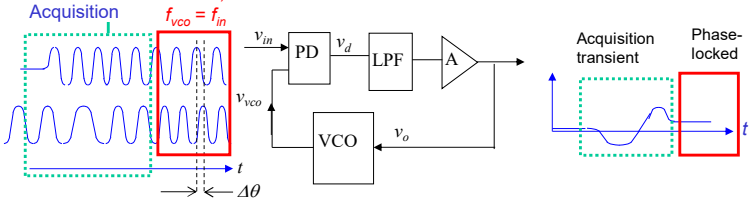
No signal at the input



Actually this level depends on the type of PD used

Acquisition

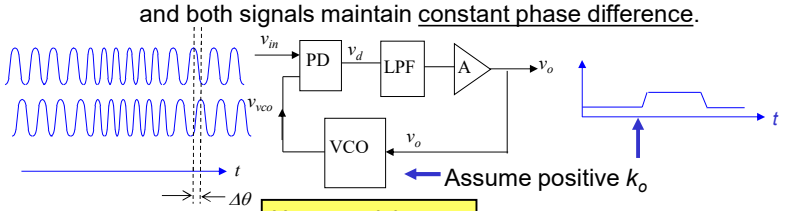
Signal applied at the input, VCO attempts to 'lock' to (or follows) the input, starting the acquisition process.



Three Sequences of PLL Operation (2)

Tracking

VCO then tracks the input signal. The instantaneous frequencies of the VCO input and the input are always the same and both signals maintain constant phase difference.



Upon applying an input

Free Running → Acquisition → Tracking

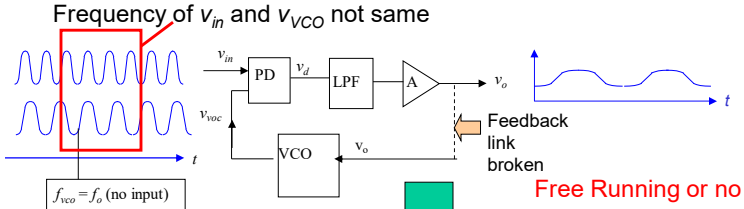
Upon power up

Unlocked

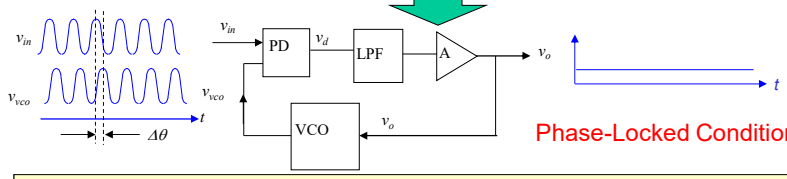
When input signal goes beyond the PLL tracking range

The Definition of Phase-Locked

Frequency of v_{in} and v_{VCO} not same



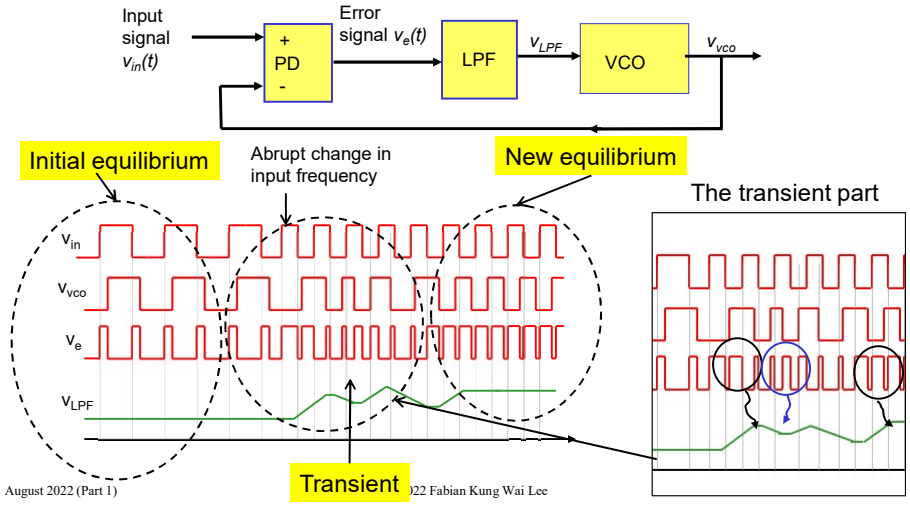
Free Running or no input



Phase-Locked Condition

The loop is said to be phase-locked when (1) the VCO frequency f_{VCO} and input frequency f_{in} are identical ($f_{VCO} = f_{in}$), and (2) both maintains a constant phase difference between them.

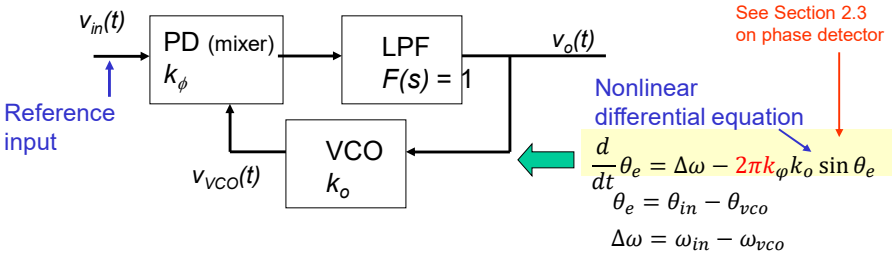
Example 2.1 – Illustration of Ideal PLL Tracking Input Signal Change



More on Acquisition (1)

Extra

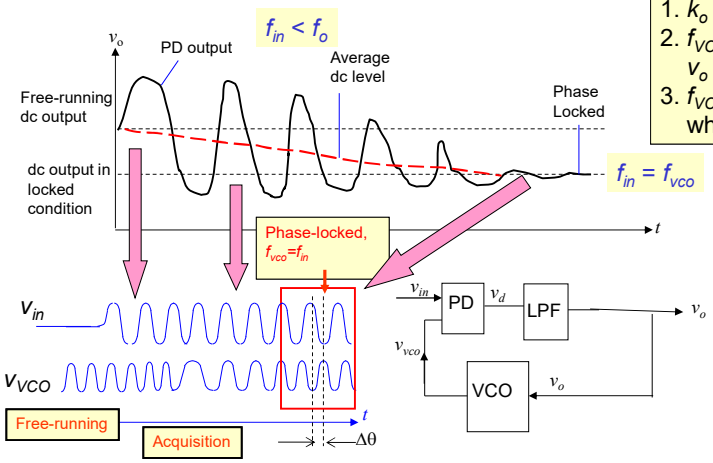
- The operation of a PLL system is described by a nonlinear integro-differential equation (most PD are nonlinear in nature).
- Thus acquisition is actually a nonlinear operation (see Gardner [5] for mathematical analysis and illustrations).
- Consider a simple PLL with analog mixer-type PD and no amplifier:



The detailed mathematical analysis is beyond our scope, so we will only have a qualitative discussion.

More on Acquisition (2)

The capture/acquisition process:



Assume:
1. k_o is positive,
2. f_{VCO} increases when v_o increases.
3. f_{VCO} decreases when v_o decreases.

This example is taken from the book:
P. R. Gray, R. G. Meyer, "Analysis and design of analog integrated circuits", 3rd edition, 1993, John-Wiley & Sons.

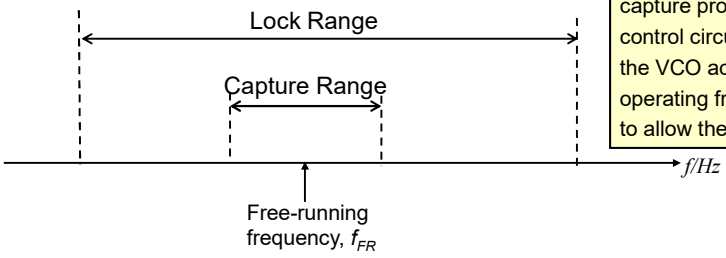
The Tracking Mode

- Once the loop is locked, the VCO output will track the changes in the input frequency.
- If the input frequency increases, the VCO output frequency increases, vice versa if the input frequency decreases, the VCO output frequency also decreases.
- In a real PLL, the PLL's VCO cannot track the input's frequency arbitrarily. There is a limited range of frequency where this tracking mode occurs, and is known as the Lock or Hold-In Range (f_H).
- Moreover, since the acquisition is a nonlinear process, there is also a limited range of frequency where the PLL can go from free-running state to the phase-locked state, this range is called the Capture or Acquisition Range.

Lock Range (f_H) and Capture Range

- **Lock or Hold-In Range,** f_H - The range of input frequency where the PLL can track the input signal.
- **Capture or Acquisition Range** - The range of input frequency where the PLL can lock to the input signal from Free-Running Condition. Typically capture range is smaller or equal to the lock range.

In some PLL, to aid the capture process, a control circuit can sweep the VCO across its operating frequency range to allow the PLL to lock.



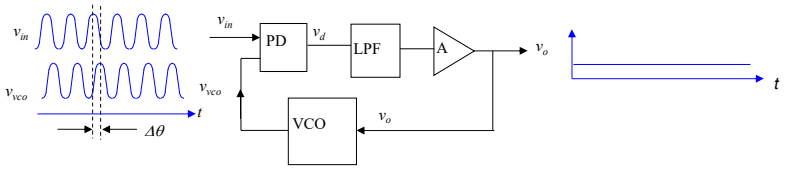
Tracking Mode Under Static Condition- Static Phase Error

- Assume **sufficient time** is given to the PLL to lock to an input signal, $f_{vco} = f_{in}$. This condition is called Static Condition.
- The phase difference between PLL input and the VCO output is known as the static phase error.

$$\Delta\theta = \theta_e = \theta_{in} - \theta_{vco} \qquad \textit{(2.2.1)}$$

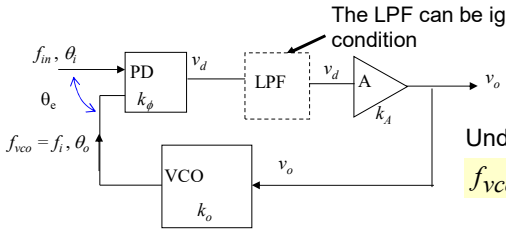
Phase of VCO's output
$v_{vco}(t) = V_{o1}\cos(\omega t + \theta_{vco})$

Phase of input
$v_{in}(t) = V_{o2}\cos(\omega t + \theta_{in})$



Tracking Mode Under Static Condition- Loop Gain

- We now strive to analyze the parameters along the PLL.



Under locked condition:

$$f_{vco} = f_o + \Delta f = f_{in} \quad \textbf{(2.2.2)}$$

The voltage needed to keep the VCO frequency f_{vco} equal to f_{in} is: $v_o = \dfrac{\Delta f}{k_o}$

From $v_d = \dfrac{v_o}{k_A} = \dfrac{\Delta f}{k_o k_A}$ and $\theta_e = \dfrac{v_d}{k_\phi}$

Loop gain of the PLL

$$\theta_e = \frac{\Delta f}{k_o k_A k_\phi} = \frac{\Delta f}{k_L} \quad \textbf{(2.2.3)}$$

$$k_L = k_\phi k_A k_o \quad \textbf{(2.2.4)}$$

Tracking Mode Under Static Condition- Loop Gain

- The loop gain k_L is an important parameter of a PLL.
- It determines the lock range of the PLL and the static phase error.
- For instance assume the PD of a PLL can only work properly when $|\theta_e| \le \theta_{e(\max)}$
- Thus from $\theta_e = \dfrac{\Delta f}{k_L}$ the maximum frequency deviation, or the lock range is:

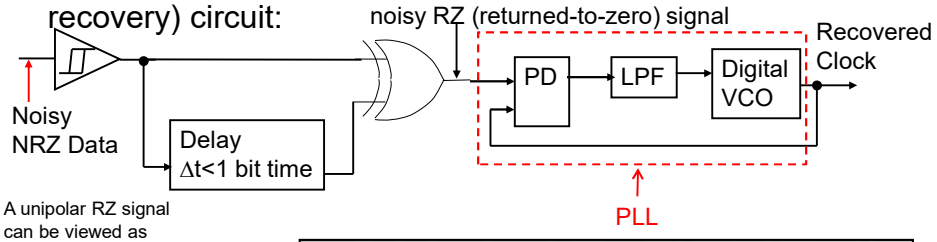
$$\Delta f_{\max} = \theta_{e(\max)} |k_L| = f_H \quad \textbf{(2.2.5)}$$

• In general the greater the loop gain k_L, the smaller the static phase error.
• Large loop gain increases the Lock Range or Tracking Range of the PLL (Assuming VCO is not the limiting factor)
• One way to increase k_L is by adding a loop amplifier with large k_A.

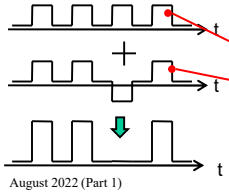
2.3 – Application Examples

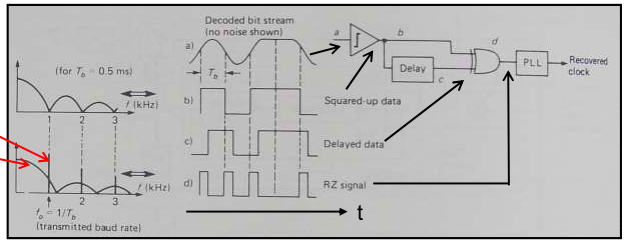
Clock Recovery in NRZ (Non-Return-to-Zero) Data

- From Young [1], this is an example of CDR (clock and data recovery) circuit:



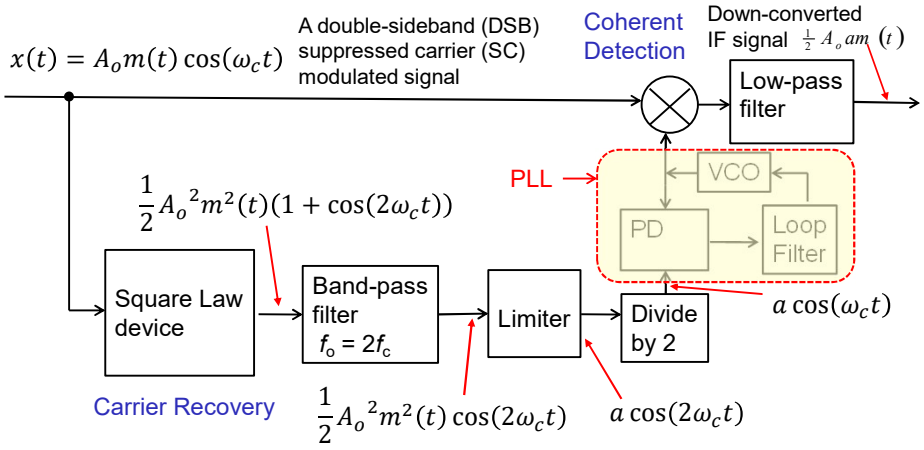
A unipolar RZ signal can be viewed as the sum of a periodic clock and a bipolar RZ signal





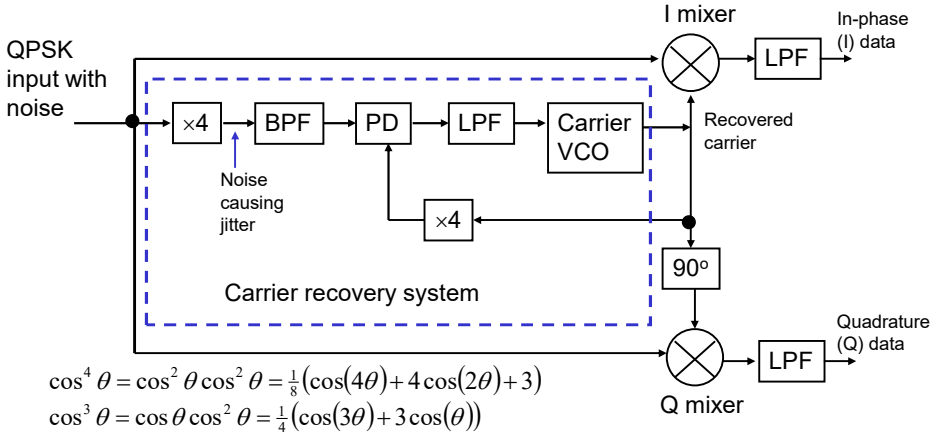
Double Sidebands-Suppressed Carrier (DSB-SC) Demodulation

- Telecommunication – analog modulation and demodulation.



Carrier Recovery in QPSK Demodulator

- From Young [1]. Same principle as carrier recovery for DSB-SC, with the input raised to the power of 4 for QPSK signals.

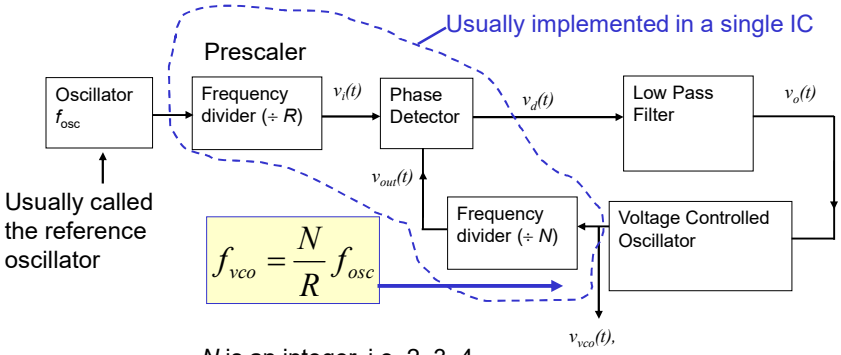


$\cos^4\theta = \cos^2\theta\cos^2\theta = \frac{1}{8}(\cos(4\theta)+4\cos(2\theta)+3)$

$\cos^3\theta = \cos\theta\cos^2\theta = \frac{1}{4}(\cos(3\theta)+3\cos(\theta))$

Frequency Synthesizer (1)

- Integer-N Architecture.

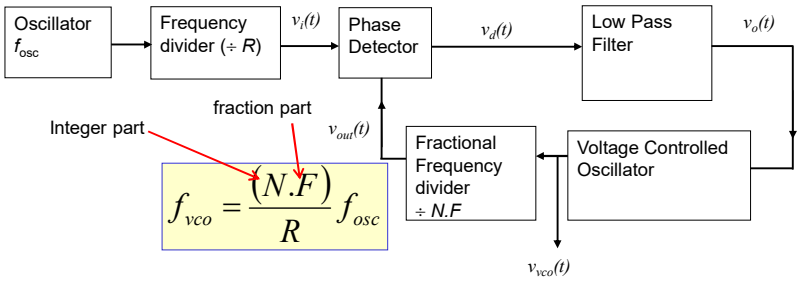


Usually called the reference oscillator

N is an integer, i.e. 2, 3, 4….
R is also an integer.

Frequency Synthesizer (2)

- Fractional-N Architecture.

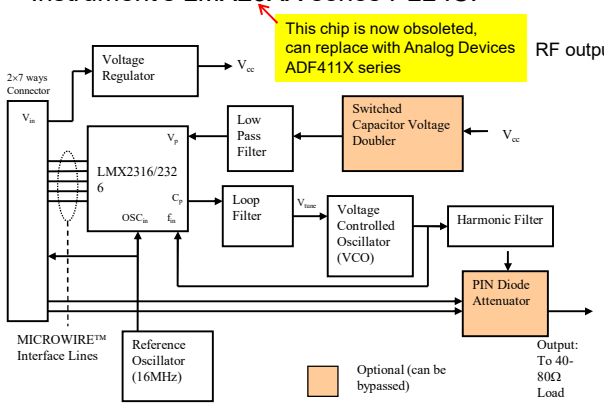


N.F is a rational number, i.e. 2.1, 2.3, 5.7….

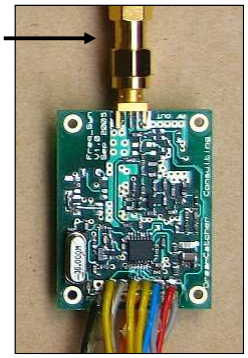
For more in-depth discussion see Razavi [2]

Practical Example – Integer-N Frequency Synthesizer Using LMX2326 IC (1)

- An Integer-N Frequency Synthesizer (up to 2.7 GHz) based on Texas Instrument's LMX23XX series PLL IC.

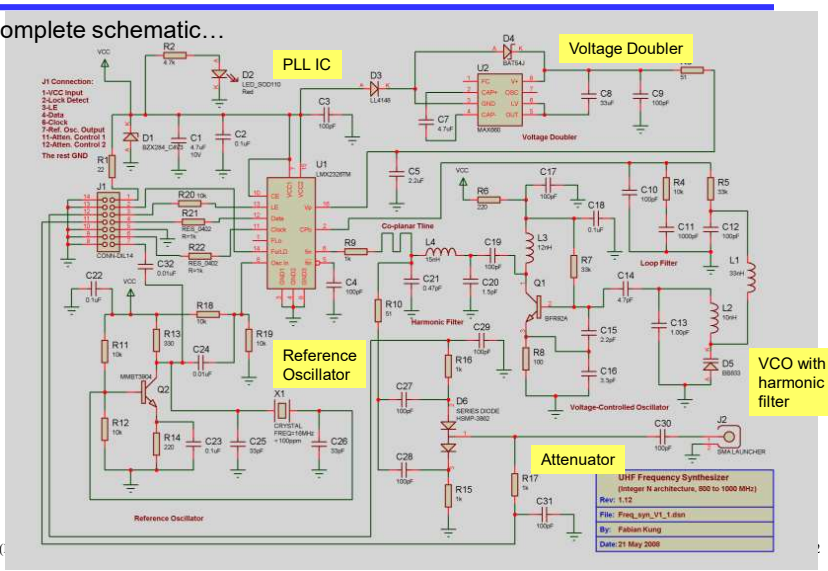


The actual hardware



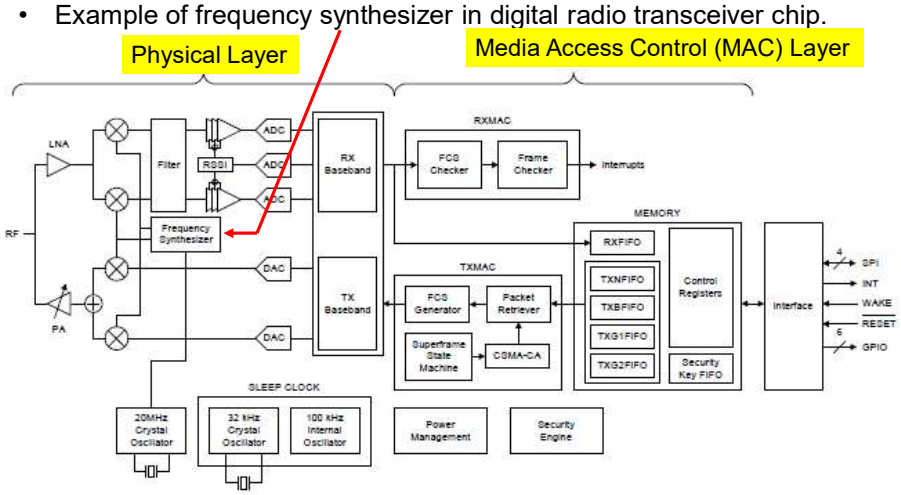
Practical Example – Integer-N Frequency Synthesizer Using LMX2326 IC (2)

The complete schematic…



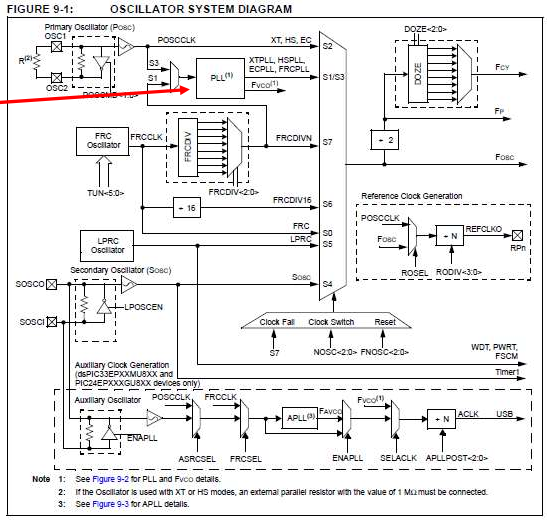
Frequency Synthesizer in Communication System

- Example of frequency synthesizer in digital radio transceiver chip.



Frequency Synthesizer in Micro-Controller/Processor Clocking System

- Oscillator block in micro-controller, with PLL based clock multiplier.



Source: dsPIC33EP256GP80x data, Microchip Technology Inc.

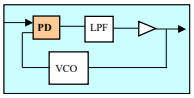
2.4 – Practical PLL Components

Introduction

- After discussing how each block of the PLL should behave ideally, in this part we will look at how one can implement the blocks physically using real electronic components.
- Here we will focus on implementation using discrete active and passive components, and MSI/LSI (medium/large scale integration) integrated circuits (IC).
- Today most commercial implementation of PLL is in the form of a single chip.

Phase Detectors

- The Phase Detector (PD) can be divided into analog and digital PDs.
- Analog PD typically works with sinusoidal signals, while digital PD works with square waves or pulse type signals.



Analog PD – Mixer (1)

- A classic implementation of the analog PD is a mixer (analog multiplier) in cascade with a low-pass filter (LPF).

$$v_d(t) = \frac{\alpha A_1 A_2}{2}\sin\left[(\omega_1 - \omega_2)t + (\theta_1 - \theta_2)\right]$$

$v_1(t) = A_1 \sin(\omega_1 t + \theta_1)$

Works with sinusoidal signal!

$v_2(t) = A_2 \cos(\omega_2 t + \theta_2)$

Mixer

LPF H(f) f

v_d

Mixer's gain

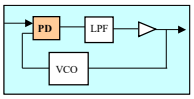
High frequency component, removed by LPF

$$v_m(t) = \alpha A_1 A_2 \sin(\omega_1 t + \theta_1)\cos(\omega_2 t + \theta_2)$$

$$= \frac{\alpha A_1 A_2}{2}\sin\left[(\omega_1 - \omega_2)t + (\theta_1 - \theta_2)\right] + \frac{\alpha A_1 A_2}{2}\sin\left[(\omega_1 + \omega_2)t + (\theta_1 + \theta_2)\right]$$

Low frequency component

Note: $\sin P + \sin Q = 2\sin\left(\frac{P+Q}{2}\right)\cos\left(\frac{P-Q}{2}\right)$



Analog PD – Mixer (2)

- When both input signals have the same frequency:

$$\omega_1 = \omega_2 \rightarrow v_d(t) = v_d = \frac{\alpha A_1 A_2}{2}\sin(\theta_1 - \theta_2)$$

- In the event when the phase difference is small, the output voltage approaches a linear response:

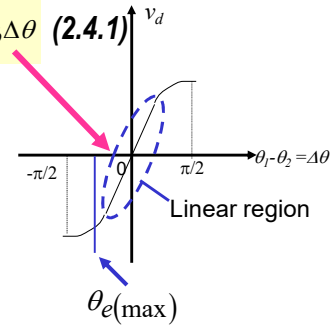
$\sin(\alpha) \cong \alpha$ for small α

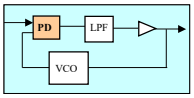
$$\theta_1 - \theta_2 \cong 0 \rightarrow v_d \cong \frac{\alpha A_1 A_2}{2}(\theta_1 - \theta_2) = k_\phi \Delta\theta \quad \textbf{(2.4.1)}$$

- The PD's gain is given as:

$$k_\phi = \alpha \frac{A_1 A_2}{2}$$

NOTE:
The Loop Filter performs the function of eliminating the high frequency component from the product of the analog multiplier.





Analog PD - Mixer (3)

- The mixer can be implemented using the classic diode ring, or analog multiplier.
- An example of a classic analog multiplier IC, using the Gilbert Cell's (for instance see P.R. Gray, R.G. Meyer, "Analysis and design of analog integrated circuit", 3rd edition, 1993, John-Wiley & Sons), is the MC1496, originally from Motorola Semiconductor.

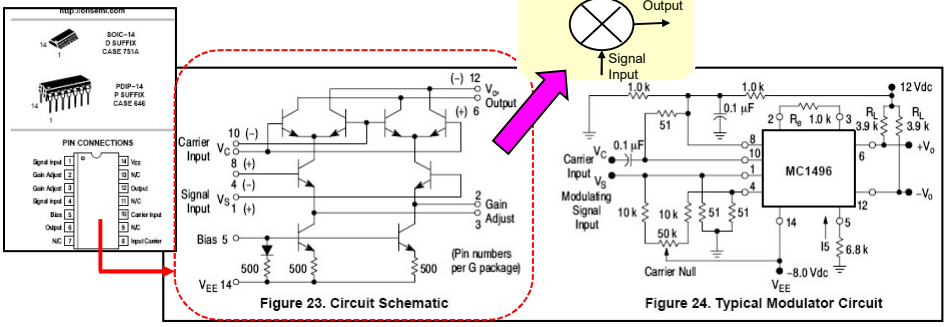
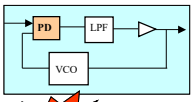


Figure 23. Circuit Schematic

Figure 24. Typical Modulator Circuit



Extra

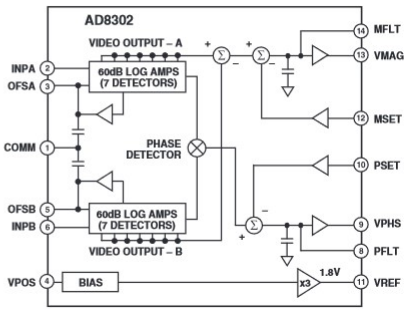
Analog PD – Mixer (4)

- Since equation (2.4.1) indicates that the mixer PD gain is a function of the input signal's amplitude, modern mixer PD chip includes an amplitude limiter. For example the block diagram for AD8302, DC to 2.7GHz amplitude and phase detector.

FEATURES
Measures Gain/Loss and Phase up to 2.7 GHz
Dual Demodulating Log Amps and Phase Detector
Input Range –60 dBm to 0 dBm in a 50 Ω System
Accurate Gain Measurement Scaling (30 mV/dB)
Typical Nonlinearity < 0.5 dB
Accurate Phase Measurement Scaling (10 mV/Degree)
Typical Nonlinearity < 1 Degree
Measurement/Controller/Level Comparator Modes
Operates from Supply Voltages of 2.7 V–5.5 V
Stable 1.8 V Reference Voltage Output
Small Signal Envelope Bandwidth from DC to 30 MHz

APPLICATIONS
RF/IF PA Linearization
Precise RF Power Control
Remote System Monitoring and Diagnostics
Return Loss/VSWR Measurements
Log Ratio Function for AC Signals

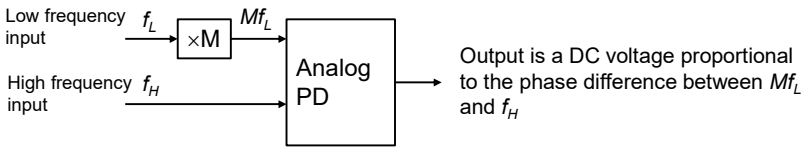
FUNCTIONAL BLOCK DIAGRAM



Extra

Analog PD – Sampling Phase Detector (1)

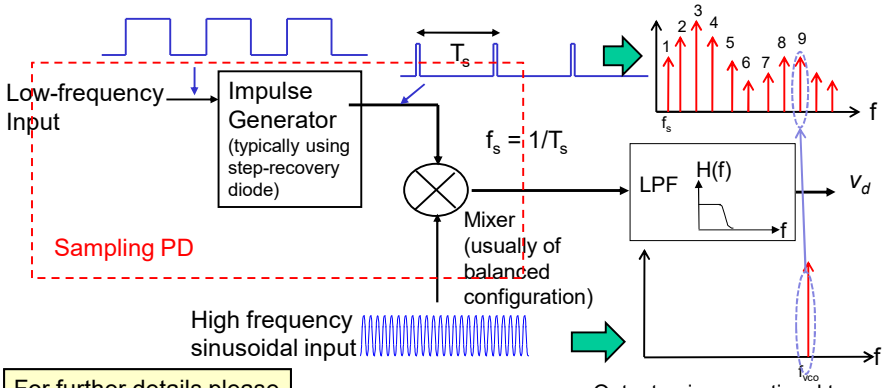
- A variation of the mixer type phase detector, usually used at microwave frequencies is the Sampling Phase Detector. This is also known as the High-Speed Sampler.
- This PD has two asymmetrical inputs, one for low frequency signal and another for high frequency signal.
- The Sampling PD compares the phase difference of the high frequency input with the integer multiple (*M*) of the low frequency signal.



Extra

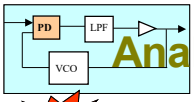
Analog PD – Sampling Phase Detector (2)

- An example of the Sampling PD implementation.



For further details please see [4] and [6].

Output v_d is proportional to phase difference between input and 9th Harmonic of Input



Extra

Analog PD – Sampling Phase Detector (3)

- An example of commercial Sampling Phase Detector from Macom using step-recovery diode (SRD) and Schottky diodes.

https://www.macom.com/products/rf-microwave-mmwave/phase-detectors

MSPD101x-xxx Series

MACOM

Sampling Phase Detectors
10 MHz - 20 GHz
Rev. V1

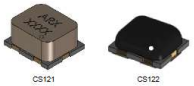
Features
- Surface Mount Package: 3.3 mm (L) x 2.8 mm (W) x 1.5 mm (H)
- RoHS* Compliant

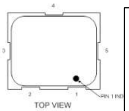
Applications
- Phase Lock Loops
- High Frequency Sampling

Description

The products of the MSPD101x-x series are fully-contained sampling phase detectors, each comprising a beam lead silicon step recovery diode, beam lead DC blocking capacitors and a beam lead series-tee pair of low-barrier silicon Schottky diodes mounted on a ceramic substrate. The semiconductors and chip capacitors are protected with an epoxy encapsulation on the top side of the ceramic substrate. These products are manufactured using a proven diode fabrication and assembly processes which optimize diode characteristics for optimal electrical performance and excellent reliability.

These low profile, compact surface mount components offer RF and microwave signal performance superior to comparable chip-and-wire discrete devices in leaded packages. These rugged devices are capable of reliable operation in all military, commercial and industrial applications.



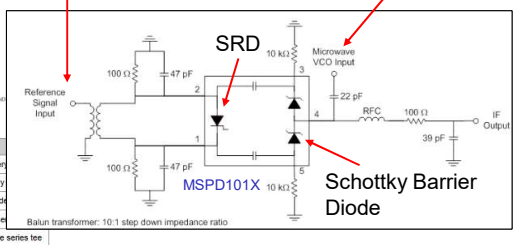


Pin Configuration

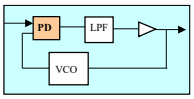
Pin #	Description
1	Cathode terminal of step recover
2	Anode terminal of step recovery
3	Cathode connection of Schottky diode
4	Center node of Schottky diode se
5	Anode connection of Schottky diode series tee

Low frequency reference oscillator

Microwave Signal

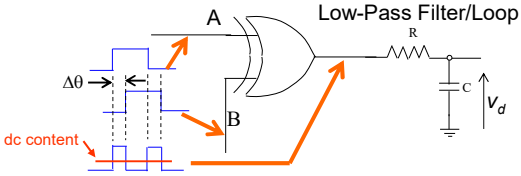


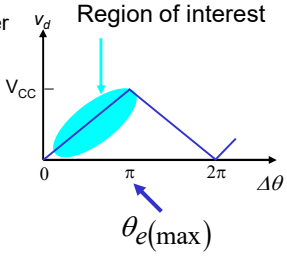
Schottky Barrier Diode



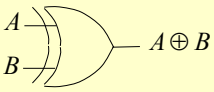
Digital PD – Type 1

- XOR Gate Type – This works with periodic square pulses with 50% duty cycle only.





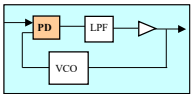
Truth table of XOR gate



A	B	A⊕B
L	L	L
L	H	H
H	L	H
H	H	L

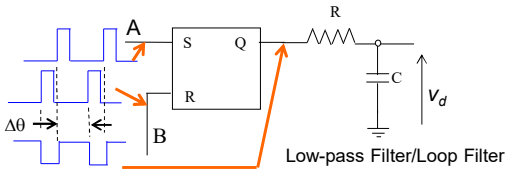
$$k_\phi = \frac{V_{cc}}{\pi} \quad \textbf{(2.4.2)}$$

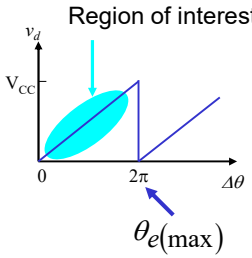
Disadvantage: High ripple



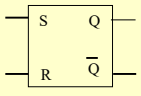
Digital PD – Type 2

- RS Flip-Flop Type – This type of PD also works with pulse, ideally the pulses should be an impulse, with duty cycle approaching 0%.





Truth table of RS-FF gate

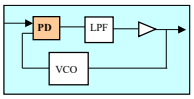


S	R	Q^{n+1}
L	L	Q^n
L	H	L
H	L	H
H	H	X

$$k_\phi = \frac{V_{cc}}{2\pi} \quad \textbf{(2.4.3)}$$

Disadvantage: High ripple

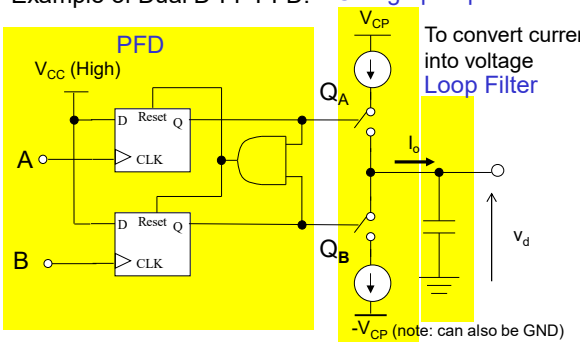
To demo during measurement



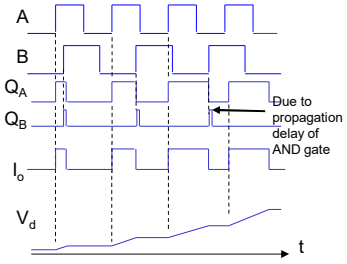
Digital PD – Type 3 (1)

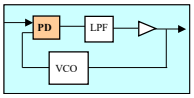
- Type 3 digital PD is called a Phase-Frequency Detector (PFD). It works with a Charge-Pump (CP) to generate a DC output to drive the VCO.
- There are a number of implementation (see Egan [4]), with one using D-flip-flop (D-FF) as shown here.

Example of Dual D-FF PFD:



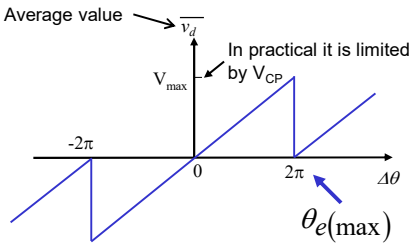
Note: Sometimes Q_A is also known as **Up** signal, Q_B as the **Down** signal.





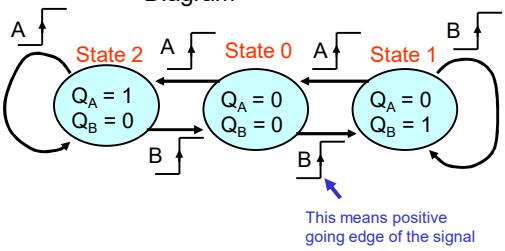
Digital PD – Type 3 (2)

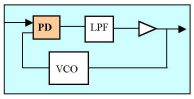
- The average value of $Q_A - Q_B$ is an indication of the frequency or phase difference between inputs A and B.



$$k_\phi = \frac{V_{CP}}{2\pi} \qquad \textbf{(2.4.4)}$$

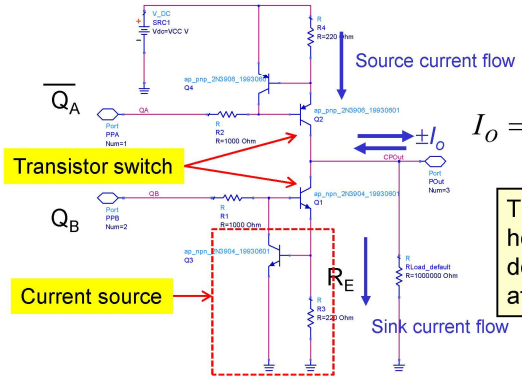
PFD State Transition Diagram





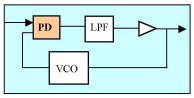
Digital PD – Type 3 (3)

- A typical charge-pump circuit can be implemented using a bipolar junction transistor or field-effect transistor (FET) current source.
- There are a number of approaches. Below is a simple implementation:



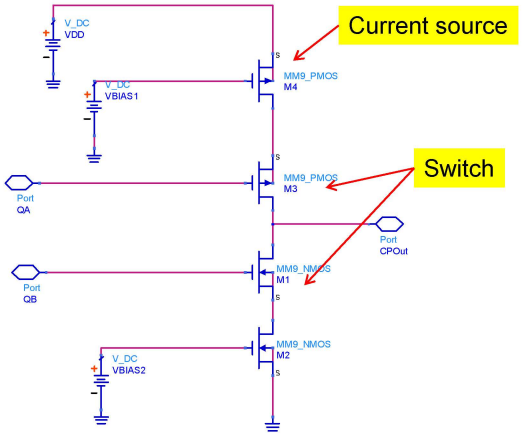
$$I_O = \frac{V_{BE}}{R_E} \qquad \textbf{(2.4.5)}$$

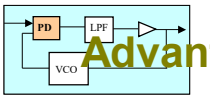
The important requirement here is I_o must not be dependent on the voltage at the charge pump output



Digital PD – Type 3 (4)

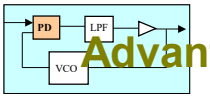
- Standard charge pump circuit implemented with PMOS and NMOS.





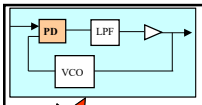
Advantages of PFD with Charge Pump (1)

- Lock range and capture range are equal in PLL using PFD with Charge Pump. In fact the lock and capture range of the PLL is limited by the operating range of the VCO and the Charge Pump supply voltage.
- For PLL using Type 1 and 2 digital PD, the capture range is smaller than the lock range, thus requiring extra circuit to aid the capture process.
- The Q_A and Q_B outputs of the PFD give an indication of the frequency difference between signals on input A and B. For instance, if f_A (frequency of Q_A) is much larger compare to f_B, there will be a lot of pulses coming out of Q_A within a certain period. If f_A is only slightly larger than f_B, then the rate of pulses from Q_A will be smaller.



Advantages of PFD with Charge Pump (2)

- A circuit that can detect both phase and frequency difference can significantly improves the acquisition speed of the PLL.
- Finally we shall see that for PLL using PFD with Charge Pump, the static phase error is zero under locked condition. This is desirable as it reduces the ripple in the v_o voltage.
- By far PFD with Charge Pump is the most used phase detector in PLL IC.

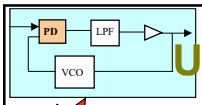


Extra

Non-Ideal Effects of PFD with Charge-Pump

- In principle, Q_A and Q_B are never high simultaneously. However because of the propagation delay of the logic gate and flip-flops, there is a short moment where both outputs are high. Ideally no current will come out of the Charge Pump, when timing and magnitude of both current sources are matched.
- Due to mismatch there is a small current sourced or sink from the Charge Pump when both Q_A and Q_B are high. This can result in ripple at the LPF output.
- A PLL using this PD also suffers from cross-over distortion (dead-band effect) during phase-locked. The problem is due to the fact that during phase-locked both inputs have zero phase difference, and the addition of physical delay results in the PD unable to response when the input phase difference is below a certain tolerance.

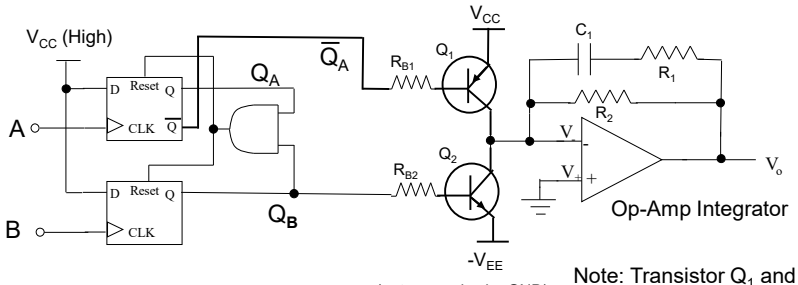
To demo during measurement



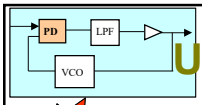
Extra

Using the PFD without a Charge-Pump (1)

- The Charge-Pump and loop filter essentially functions as an integrator.
- Thus, we can replace this using op-amp based integrator circuits. Two schemes are shown, with and without the switch.
- These are preferred when the Charge-Pump circuit is too complex or mismatch in the Charge-Pump is an issue.



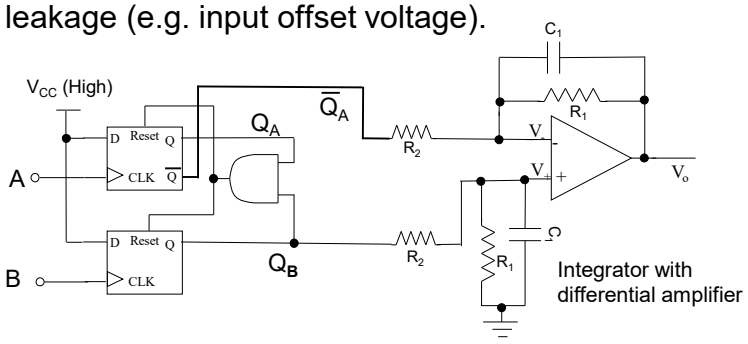
Note: Transistor Q_1 and Q_2 acts as switch, not current source

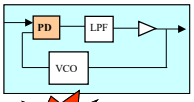


Extra

Using the PFD without a Charge-Pump (2)

- Another implementation using differential integrator.
- Note that the Op-Amp based integration also has it's own inherent issue, such as lower operating frequency, and leakage (e.g. input offset voltage).

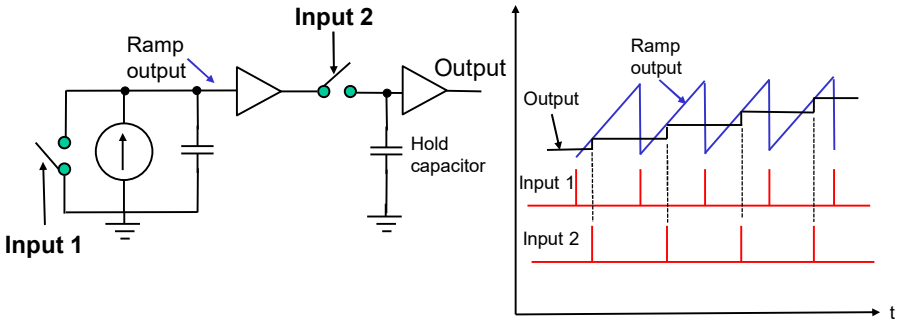


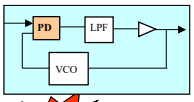


Extra

Sample-And-Hold Phase-Detector (Digital PD)

- In this phase detector, a ramp is created that is proportional to the timing difference between the two input pulses. Input 1 controls the ramp output, while input 2 controls the sample switch.
- Both inputs are pulses, and $\Delta\theta$ from 0 to 2π.



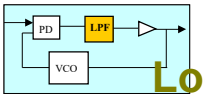


Extra

Comparison of PDs

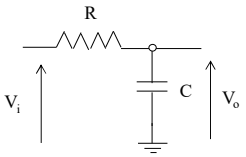
Type	Input Signal	Ripple at Output	$\Delta\theta$ Range	Complexity	Others
Mixer	Sine (or harmonics)	Low	$-\pi/2$ to $\pi/2$	High	Output depends on input amplitudes
Sampling	Sine (or harmonics)	Medium	$-\pi/2$ to $\pi/2^*$	High	Output depends on input amplitudes
XOR	Pulse (50%)	High	0 to π	Low	High order LPF needed, large delay which may cause instability
RS-FF	Pulse (0%)	High	0 to 2π	Low	Same as XOR
PFD	Pulse	Low	-2π to 2π	Medium	Dead-band (cross-over distortion), mismatch, can detect frequency difference
Sample-and-Hold	Pulse	Low	0 to 2π	High	No dead-band

* On the harmonics



Loop Filter - Low Pass Filter (1)

- Here we restrict ourselves to **single-ended passive filter** only.
- Voltage input voltage output.
- For use with Mixer, XOR gate and RS-FF.

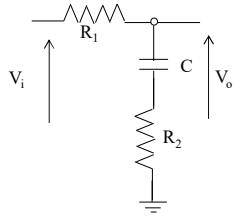


$$F(s)=\frac{V_o}{V_i}=\frac{1}{1+sRC}$$

1st order RC

(2.4.6a)

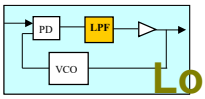
The denominator polynomial in s has power of s^1



$$F(s)=\frac{V_o}{V_i}=\frac{1+sR_2C}{1+s(R_1+R_2)C}$$

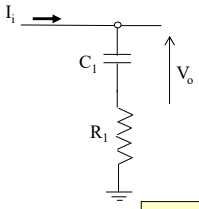
1st order RC with zero

(2.4.6b)



Loop Filter - Low Pass Filter (2)

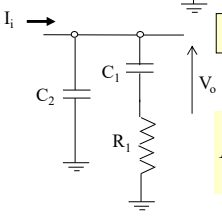
- Current input voltage output.
- For use with PFD with Charge Pump.



$$F(s)=\frac{V_o}{I_i}=\frac{1+sR_1C_1}{sC_1}$$

1st order RC with zero

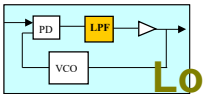
(2.4.7a)



2nd order RC with zero

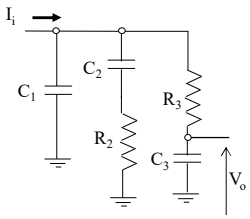
$$F(s)=\frac{V_o}{I_i}=\frac{1+sR_1C_1}{s(C_1+C_2+sR_1C_1C_2)}$$ ***(2.4.7b)***

The denominator polynomial in s has power of s^2



Loop Filter - Low Pass Filter (3)

Third order RC



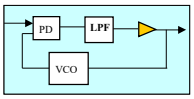
$$F(s)=\frac{V_o}{I_i}=\frac{T_1(1+sT_2)}{sT_2C_1(1+sT_1)(1+sT_3)}$$ ***(2.4.7c)***

$$T_1=\frac{R_2C_1C_2}{C_1+C_2}$$

$$T_2=R_2C_2$$

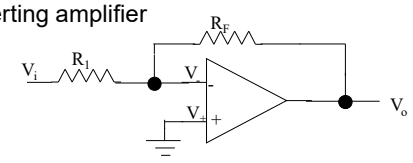
$$T_3=R_3C_3$$

To also show differential LPF if needed



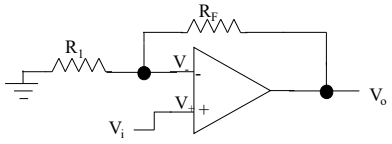
Loop Amplifiers

Inverting amplifier



$$k_A = \frac{V_o}{V_i} = -\frac{R_F}{R_1} \qquad \textit{(2.4.8a)}$$

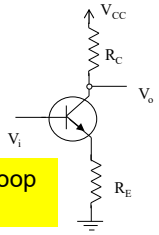
Non-Inverting amplifier



$$k_A = 1 + \frac{R_F}{R_1} \qquad \textit{(2.4.8b)}$$

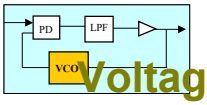
Loop amplifiers are optional.

Common-Emitter amplifier



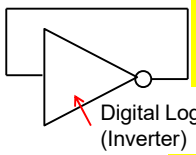
$$k_A = \frac{R_C}{R_E + \frac{1}{g_m}} \qquad \textit{(2.4.8c)}$$

Note: Active filter can be used in place of loop Amplifiers.



Voltage Controlled Oscillator (VCO) (1)

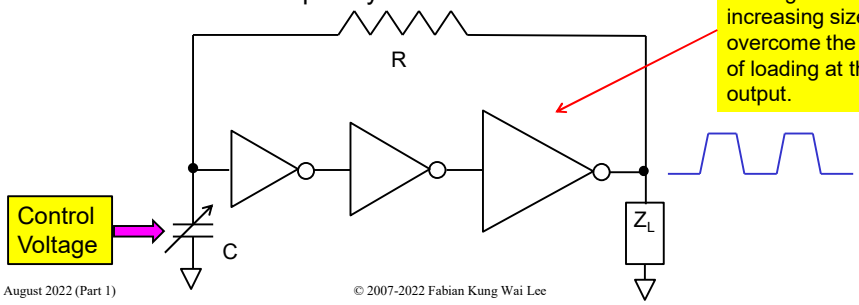
- Relaxation oscillator - Astable Multivibrator.
- The ring oscillator.
- Contains odd number of inverters connected in series.
- Modified by adding RC network to become a variable frequency oscillator.

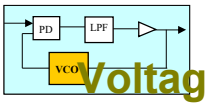


What happens when we connect like this?

Digital Logic Gate (Inverter)

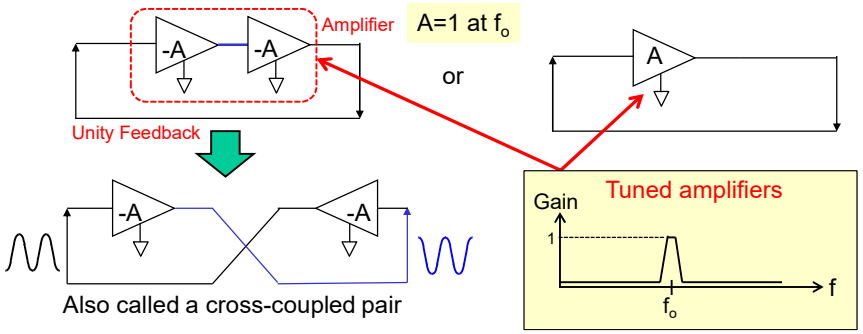
Typically we would use 3 gates of increasing size to overcome the effect of loading at the output.

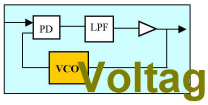




Voltage Controlled Oscillator (VCO) (2)

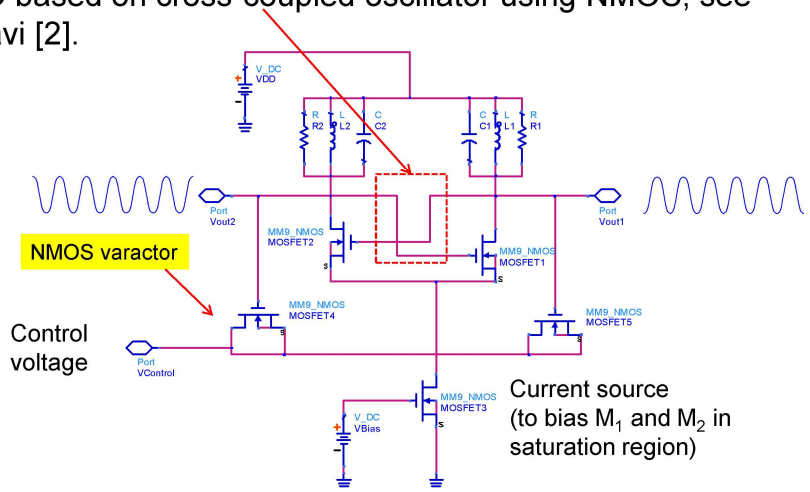
- Feedback oscillator - We can also employ unity feedback (e.g. F(s) = 1) system to create oscillator, this approach is popular with inverting amplifier and frequently used in CMOS IC based oscillator.
- The amplifiers in such oscillators are tuned to produce gain at a particular frequency f_o, so that oscillation only occurs at this frequency.

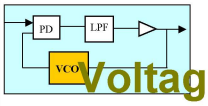




Voltage Controlled Oscillator (VCO) (3)

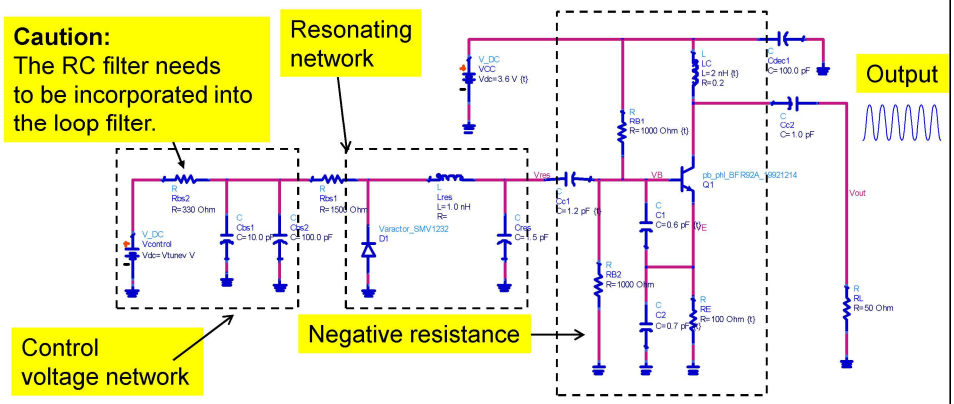
- VCO based on cross-coupled oscillator using NMOS, see Razavi [2].

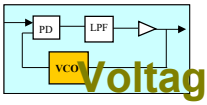




Voltage Controlled Oscillator (VCO) (3)

- Negative resistance oscillator, for instance see Smith [3].
- An example of UHF negative resistance VCO is shown below.





Voltage Controlled Oscillator (VCO) (4)

- An example of relaxation oscillator type VCO used in the 74VHC4046 PLL integrated circuit.

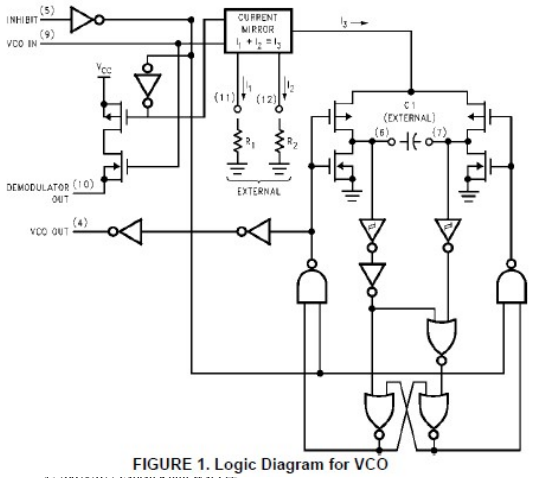
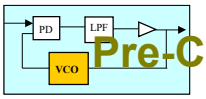
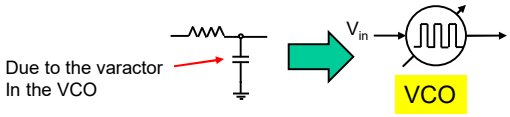


FIGURE 1. Logic Diagram for VCO



Pre-Cautions When Connecting Loop Filter to VCO

- Note the VCO input typically is equivalent to a series RC network. This will affect the performance of the loop filter and need to be taken into account.
- Alternatively the cut-off frequency of the series RC network can be made at least 5x higher than the cut-off frequency of the PLL loop filter, and the effect of series RC network can be neglected.



Equivalent impedance of the VCO input

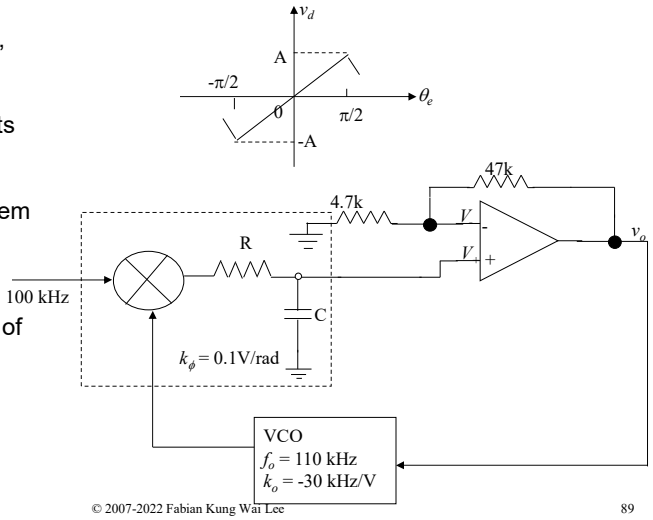
Categorization of PLL

- There is no agreed convention, but PLL is usually classified as digital or analog PLL. This is usually determined by the type of phase detector employed.
- If the PD is analog type, like the mixer PD, then the PLL is called the analog PLL. From this we see that if PD is digital type, it's a digital PLL.
- Modern PLL can also be implemented using microcontrollers, in this case the operation of phase detection, filtering, VCO etc can all be performed in the software/firmware of the microcontroller with digital signal processing capability. This is usually called Software PLL or All Digital PLL.
- Finally do bear in mind that in modern PLL, all the component discussed can be integrated into a single mixed-signal IC or an FPGA (field programmable gate array).

Example 2.4.1

Consider the PLL shown, find:

- The k_A for the amplifier.
- The loop gain k_L in units of Hz/rad and s^{-1}.
- The VCO output frequency when the system is locked.
- The static phase error.
- The lock range.
- The maximum value, A of v_d.



Example 2.4.1 Cont...

Solution:

$k_A = 1 + 47/4.7 = 11$

$k_L = 0.1 \times 11 \times -30000 = -33000$ Hz/rad $= -33$ kHz/rad

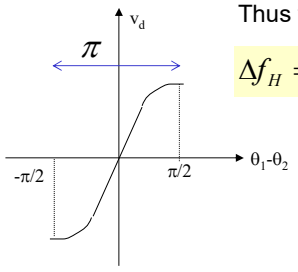
Since 1 Hz = 2π radian, k_V, the loop gain in s^{-1} is given by:
$k_V = 2\pi k_L = -20.7345 \times 10^3\ s^{-1}$

f_o = 100kHz.

$\theta_e = (100 - 110)/k_L = -10/-33 = 0.303$rad

$|\Delta f_H| = \pi \times 33 = 103.7$kHz.

$A = k_\phi \times (\pi/2) = 0.157$V.



For the mixer type PD, maximum static phase error:

$$\theta_{e(\max)} = \pi$$

Thus from $\theta_e = \frac{\Delta f}{k_L}$

$$\Delta f_H = \pi |k_L|$$

Exercise

- For the PLL with PFD with charge pump, find: (a) k_A of the amplifier (b) static phase error when the system is locked (c) VCO output frequency and v_d when locked (d) the lock range.