Phase-Locked Loop (PLL) Lab 1

1.0 Objective

To built a simple PLL using off-the-shelf CMOS integrated circuit and RC components.

2.0 Components, Tools and Instruments

Item	Description	Quantity
1	Project board	1
2	74HC4046 integrated circuit	1
3	Resistors (0.25W 5%): 470Ω	1
4	Resistors (0.25W 5%): 1000Ω	1
5	Resistors (0.25W 5%): 3300Ω	1
6	Resistors (0.25W 5%): 10000Ω	1
7	Capacitor (ceramic, 50V, 10%): 100pF	1
8	Capacitor (ceramic, 50V, 10%): 1nF	2
9	Capacitor (ceramic, 50V, 10%): 10nF	2
10	Capacitor (ceramic, 50V, 10%): 0.1μF	1
11	Capacitor (Electrolytic, 16V, 0%): 10μF	1
12	Digital sampling oscilloscope (min 50 MHz bandwidth), 2 channels	1
13	Power supply (DC)	2
14	Function generator (1 kHz to 10 MHz)	1
15	Single-core wire (red, blue and black)	1 reel for each color
16	Wire cutter	1
17	Tweezers	1
18	Pen knife	1
19	Long-nose pliers (optional)	1

3.0 Introduction

In this simple exercise you would build a phase-locked loop (PLL) using the popular CMOS integrated circuit (IC) 74HC4046. This IC has a built-in relaxation voltage-controlled oscillator (VCO) and three phase detectors (PD): e.g., an XOR gate PD, a RS flip-flop PD and a PFD with charge pump. In this lab we would utilize the XOR gate PD and the PFD to built a PLL. The block diagram of the 74HC4046 is shown in Figure 1.

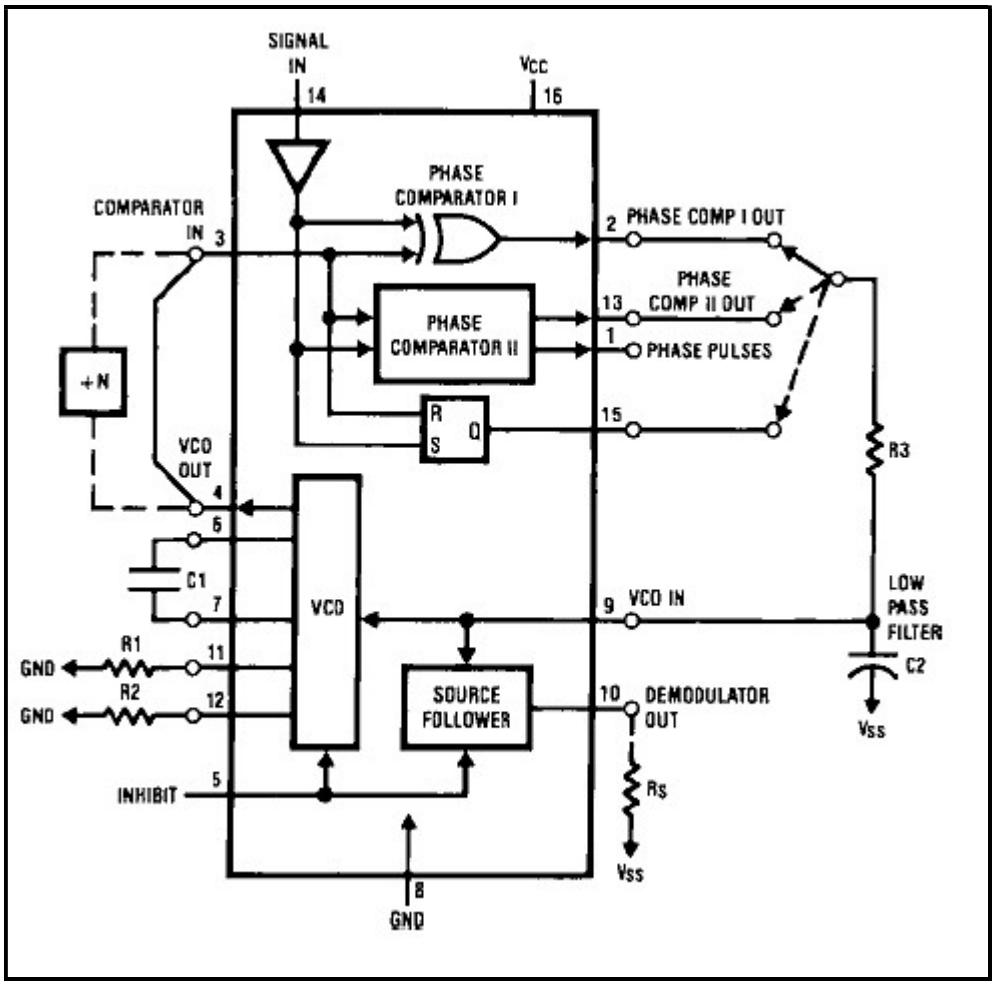


Figure 1 – 74HC4046 block diagram.

4.0 Part 1: XOR Gate PLL

Connect up the circuit as shown in Figure 2 on a project board. Be careful in handling the 74HC4046 IC as it is susceptible to electrostatic discharge damage. Use a tweezers or long-nose plier to pick up the IC. An example of the completed PLL is shown in Figure 3. Keep your circuit tidy, this will make debugging easy. One way to maintain neatness is to use the shortest connecting wire as possible, and to use the upper and lower rows of the project board for V_{cc} and GND buses (see Figure 3).

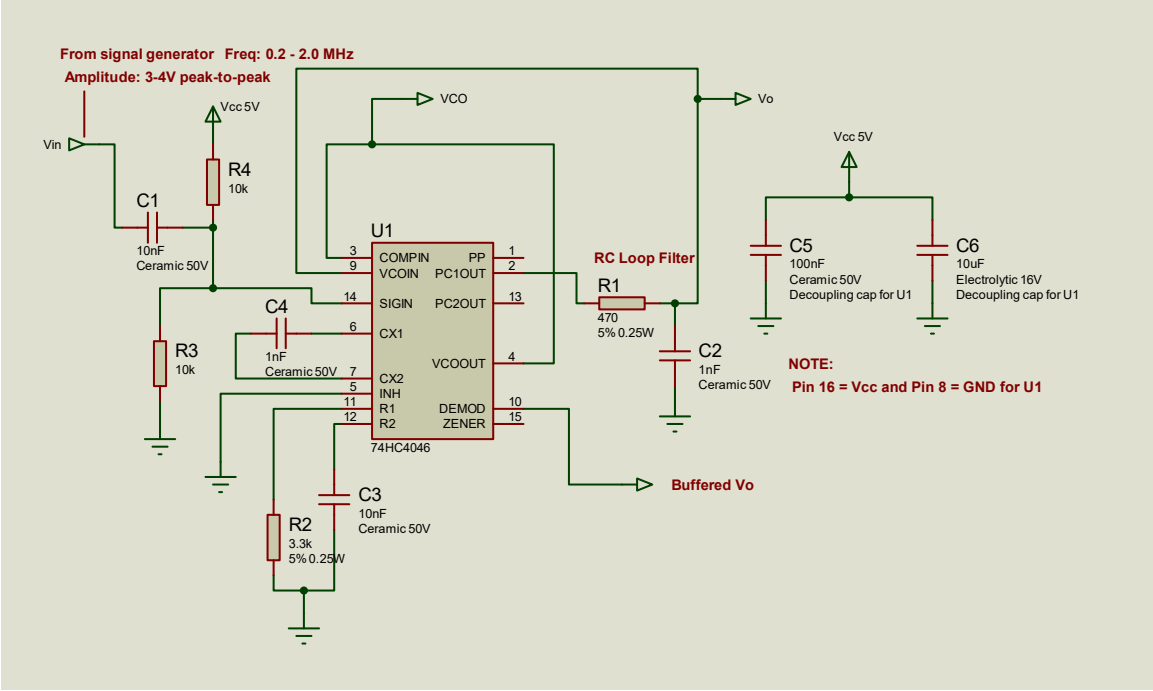


Figure 2 – PLL schematic using XOR gate PD.

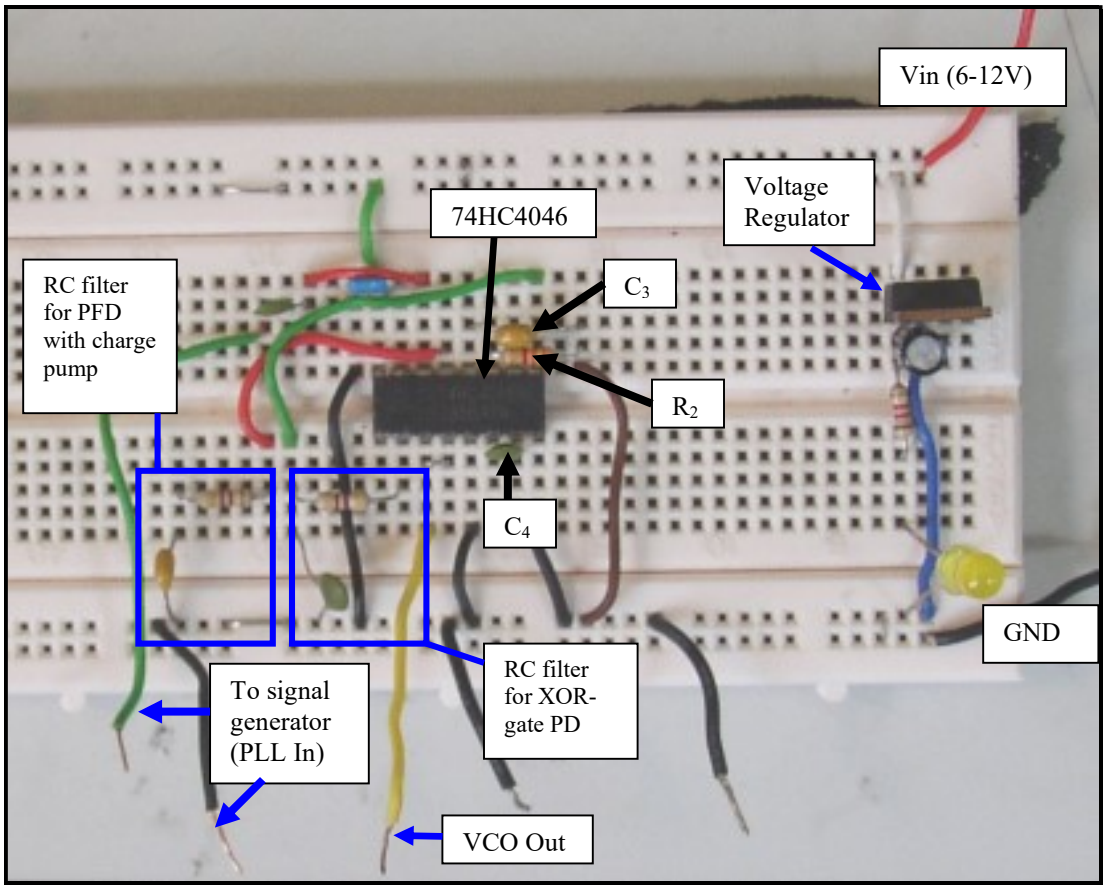


Figure 3 – The hardware based on schematic of Figure 2.

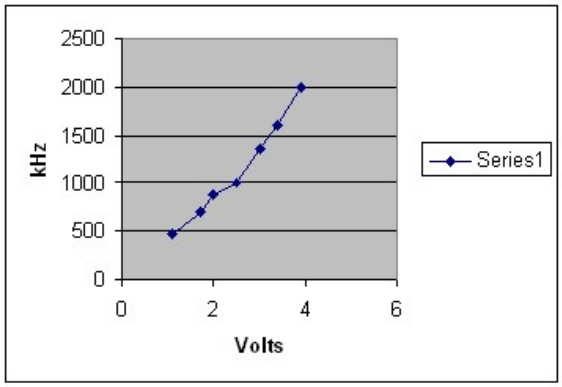
In this schematic, R_2 and C_4 determine the built-in VCO characteristics. These values allow the VCO oscillation frequency to vary from roughly 450 kHz to 3 MHz, for an input voltage of 0.5 V to 5V. Note that the oscillation range of the built-in VCO is highly dependent on the power supply voltage to the IC, and can vary as much as 100% for supply variation between 4.5V to 6.0V. Capacitor C_3 serves to stabilize the potential on pin 12 of U_1 (This pin is to be left as open circuit). Pin 2 of U_1 is the output of the XOR gate PD while pin 3 is the common input to all the internal PDs of the 74HC4046.

Step 1 – Measure the VCO gain

Open the PLL loop by disconnecting pin 9 of U_1. Power up the circuit with a DC power supply, setting the output voltage to 6.0V. Connect pin 9 of U_1 to a second DC power supply. Vary the second power supply output voltage from 0.5 V to 4.5 V in 0.5 V step. Record the frequency observed from the VCO's output. Plot a graph relating the frequency of the VCO's output versus VCO input. Calculate k_o. A sample result is shown in Table 1.

Table 1 – Sample measurement of f_{vco} versus V_o.

V_o / Volts	f_{vco} / kHz
1.1	470
1.7	700
2.0	870
2.5	1000
3.0	1360
3.4	1600
3.9	2000



Step 2 – Connect signal generator – Phase locked

Setup a signal generator to produce a 50% duty cycle square wave with peak-to-peak voltage of around 4.0 V and frequency of 1.5 MHz. Connect the output of the signal generator to pin 14 of U_1 via coupling capacitor C_1. The PLL should immediately lock to the input signal. Observe the voltage V_o, V_{in} and V_{vco} during phase-locked. A sample measurement is shown below. Note that V_{in} leads V_{vco} in phase. This phase difference, together with the operation of the XOR gate and RC filter results in a voltage V_o with a ripple at a certain dc average value.

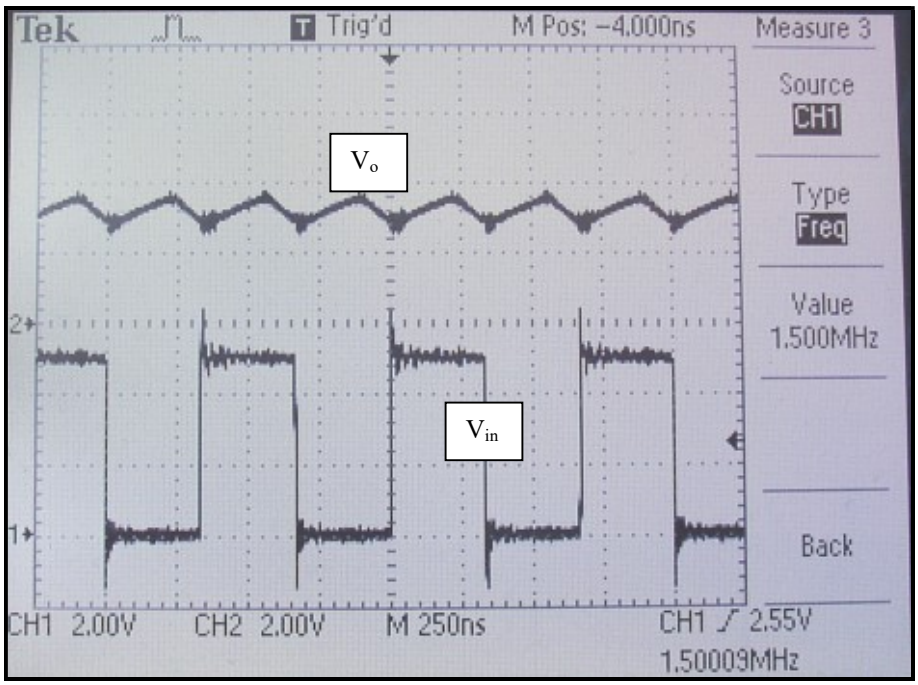


Figure 4 – The input voltage to the VCO, V_o and the input signal V_{in} versus time.

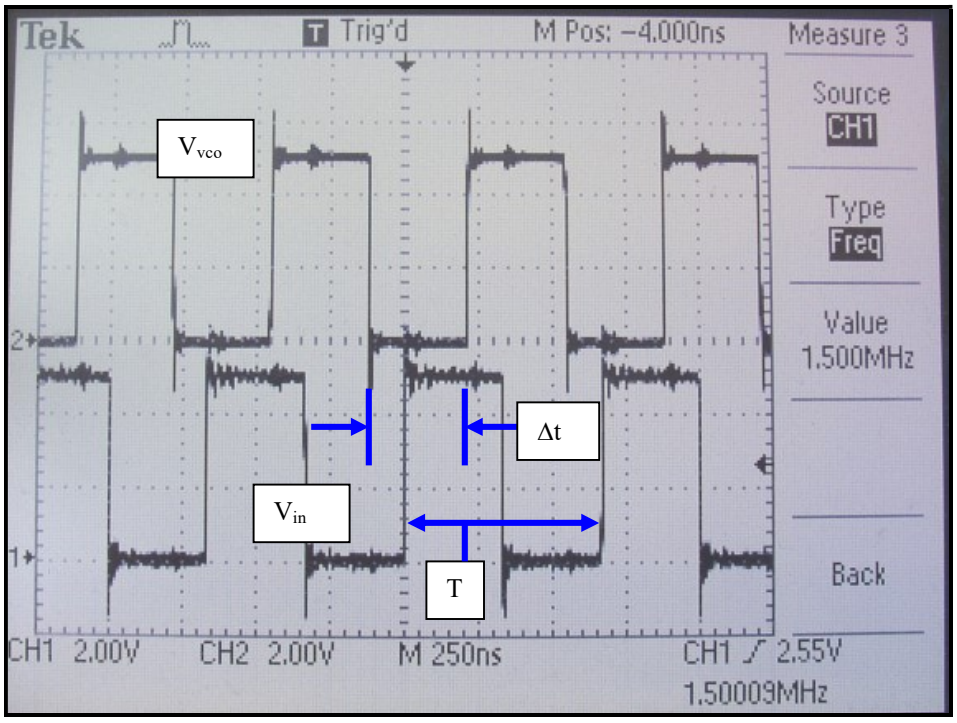


Figure 5 – VCO's output V_{vco} and V_{in} versus time.

Step 3 – Tracking mode observation and hold-in range measurement

Now you can increase and decrease the frequency of the input signal and watch the VCO tracks the input signal. Measure the lock or hold-in range (f_H) of this PLL and compare this with theory.

Step 4 – Static phase error measurement

Set the input signal frequency to 1.0 MHz. From the waveforms, compute the difference between the excess phase of the input signal and the VCO, θ_e. The phase difference can be computed from the timing difference by (see Figure 5):

$$\theta_e = \frac{\Delta t}{T}\left(360^o\right) \qquad (1)$$

Repeat this with other frequencies, for instance 750 kHz and 1.5 MHz. Validate that the values of θ_e obtained, average value of V_o (this can be obtained from pin 10 of U_1) and VCO's oscillating frequency all correlate well with theory.

Step 5 – Determine the capture range

Disconnect the signal generator from the PLL. Set its frequency to 450 kHz and connect it back to PLL. See if the PLL can lock to the input signal. Repeat this at 250 kHz step until you reach 2.5 MHz. From this result we can estimate the capture range (or acquisition range) of this PLL. Here we would observe that the capture range for XOR gate PLL depends on the cut-off frequency of the RC filter. The lower the cutoff frequency, the smaller the capture range. You can verify this by changing C_2 to 10 nF and repeat the above steps.

5.0 Part 2: PFD with Charge Pump PLL

Modify the circuit as in Figure 6. Here we are using the internal PFD with charge pump of 74HC4046. The loop filter is also modified accordingly to convert current into voltage.

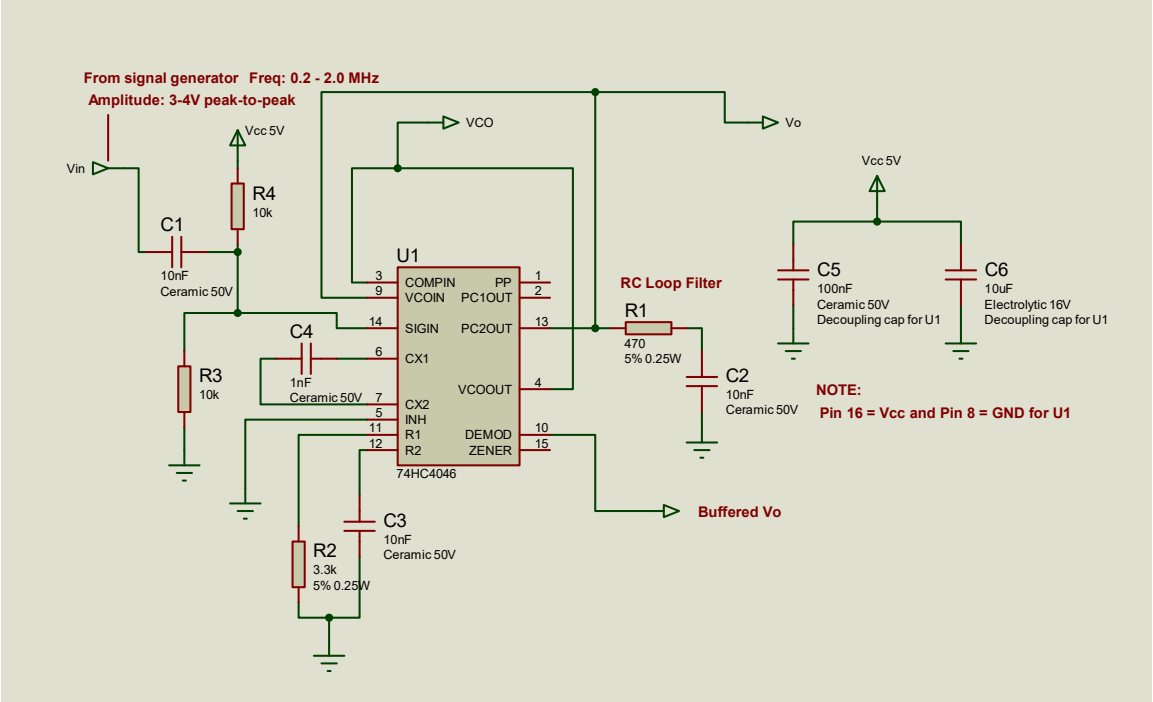


Figure 6 – PLL using PFD with charge pump.

Repeat Step 2 and Step 4 of Part 1 for this PLL. After this as an interesting experiment change C_2 to 1 nF, see if the PLL is stable. Figure 7 shows a sample measurement of the VCO's output and V_{in} signals during phase-locked at 1.5 MHz. Trace 2 is the VCO output and Trace 1 is V_{in}. Figure 8 shows the spike at the charge pump output due to mismatch within the positive and negative current source and non-ideal properties of the PFD.

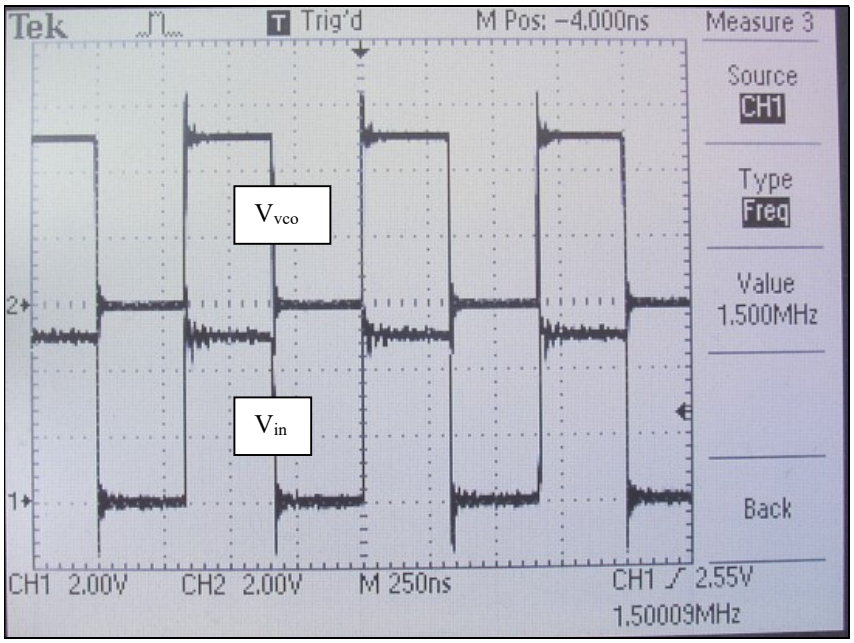


Figure 7 – Comparison of V_{vco} and V_{in} during phase-locked at 1.5 MHz.

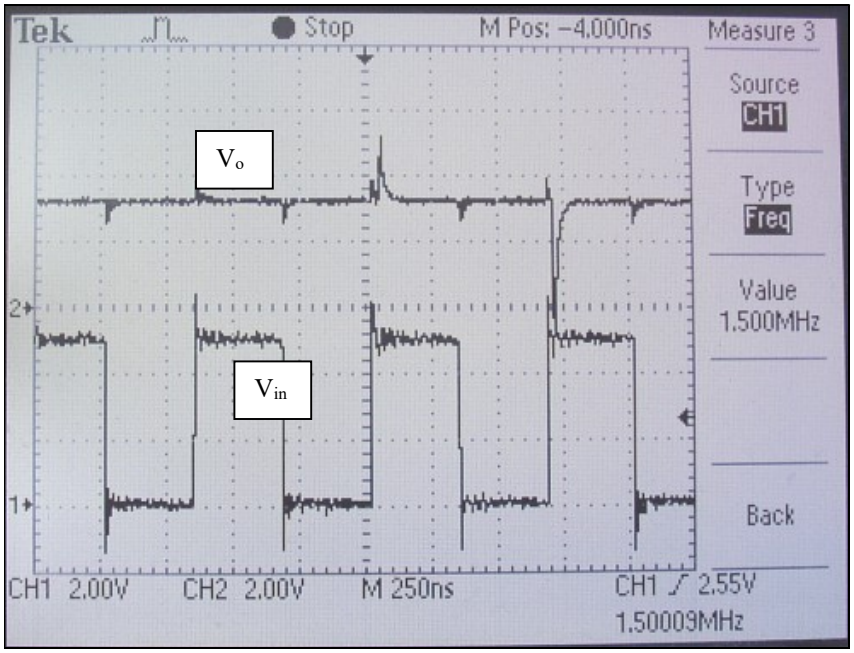


Figure 8 – Voltage spikes at the charge pump output during phase-locked at 1.5 MHz.

Appendix - Extra Observation for PFD with Charge Pump PLL

It is discovered that the output of the VCO exhibits significant jitter during tracking mode. Although the VCO frequency seems to track the input signal V_{in}'s frequency, there is some random jitter on the VCO waveforms. Upon closer inspection the author confirms that this is due to non-ideal behavior of the PFD with charge pump of 74HC4046. When the static phase error θ_e between the input signal and VCO is very small (as in during phase-locked), the average dc voltage of the PFD with charge pump exhibit nonlinear behavior known as the 'dead-zone' or cross-over distortion. This is largely due to the internal propagation delay of the PFD components. Figure A1 shows an example of cross-over distortion measurement taken from Chapter 5 of the book by *W. F. Egan, "Frequency synthesis by phase lock", 2000 John-Wiley & Sons*. Figure A2 is the capture waveforms of the VCO output and V_o at f_{in} = 1.00 MHz. Note the jitter and the periodic up and down spike, causing the VCO output to jitter. A display persistence of 1 second is used to show both up and down voltage spike in one screen shot.

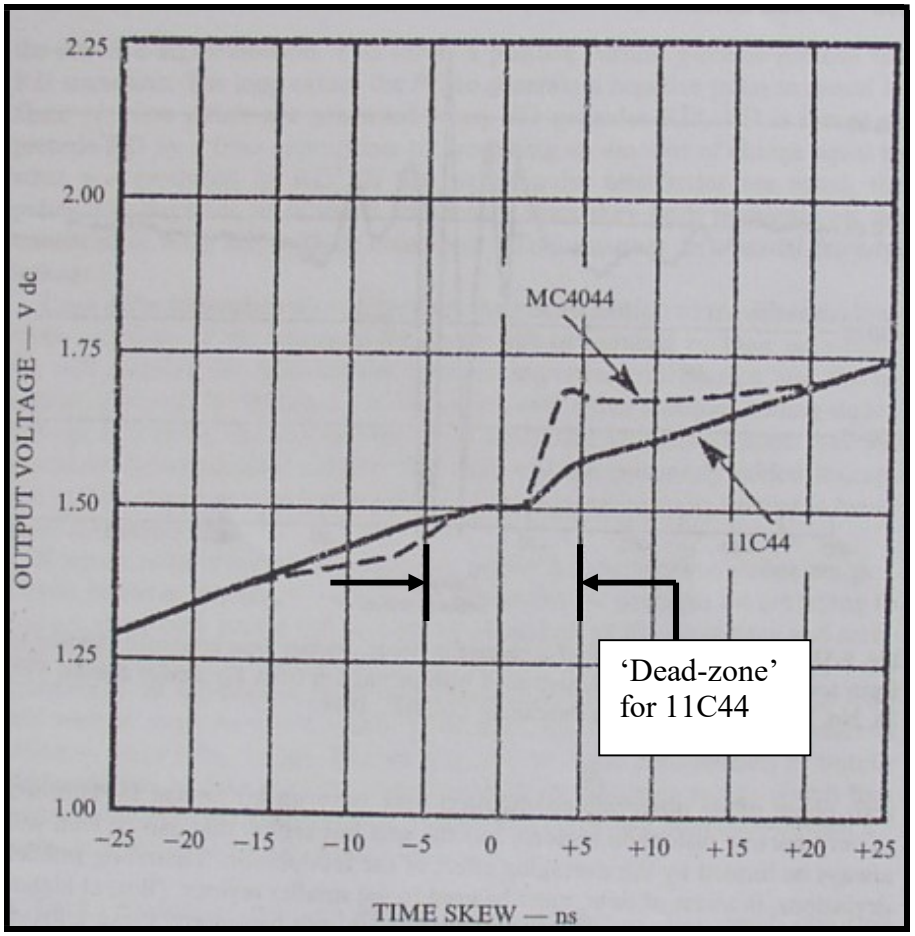


Figure A1 – Crossover distortion of some PFD with charge-pump, from the datasheet for 11C44, ©Fairchild Semiconductor Corporation, 1975. From *W. F. Egan, "Frequency synthesis by phase lock", 2000 John-Wiley & Sons*.

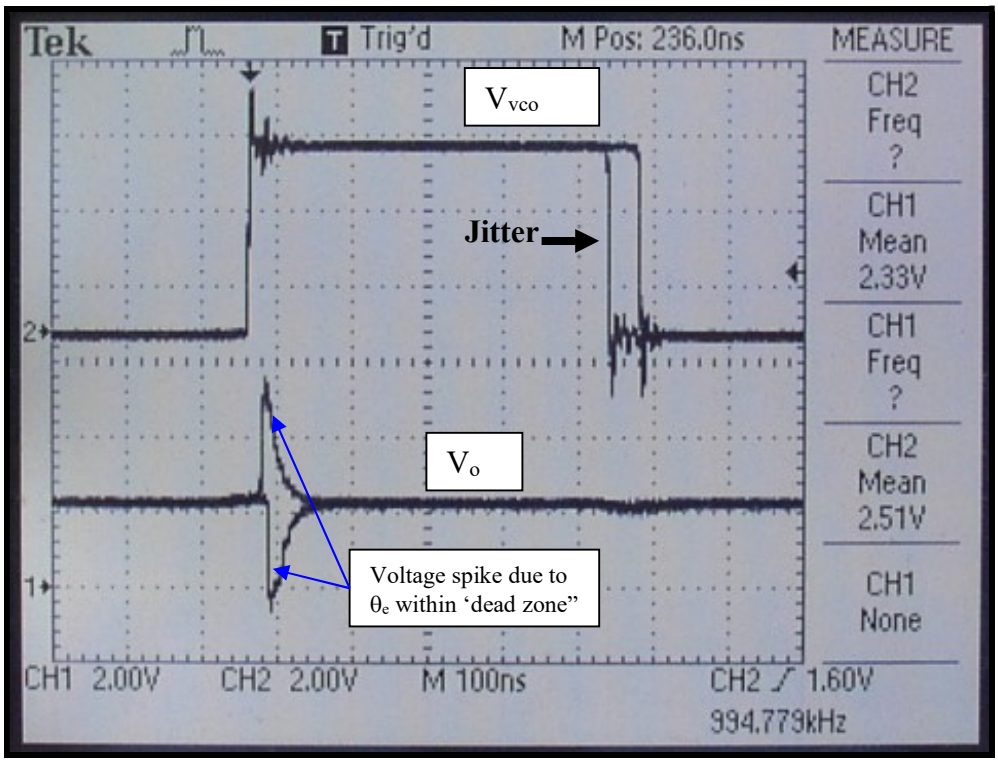


Figure A2 – V_{vco} (trigger source) and V_o waveform, at f_{in} = 1.00 MHz. Display persistence of 1 second is used.

One way to overcome this is to introduce a non-zero static phase error θ_e during phase-locked, so that θ_e is always larger than the 'dead-zone' limit within the frequency range of interest. A simple way to achieve this is to add a shunt resistor across the original series RC network. This is shown in Figure A3. Resistor R_B acts as a 'bleeding' resistor, it will discharge C_2 continuously, so that a constant pulse from the charge-pump is needed to maintain a fixed average dc voltage to the VCO input. Effectively this means a small phase error is required between VCO output and V_{in} during phase-locked. This resistor value is typically chosen to be $10R_1$ (4.7 kΩ in this case). Figure A4 shows the jitter in VCO output dissapear after this modification, while Figure A5 compares the VCO and V_{in} waveforms to show the static phase error that results in the fix voltage pulse of V_o in Figure 4.

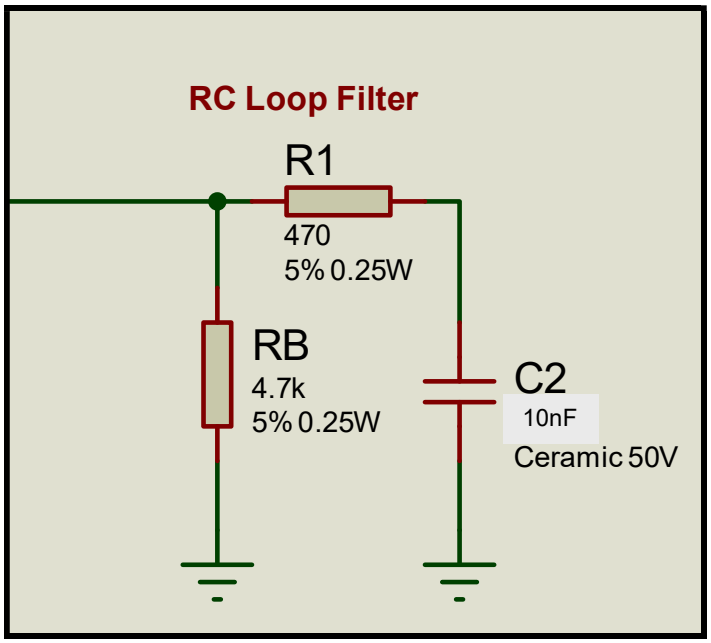


Figure A3 – Introducing the 'bleeding' resistor R_B to eliminate VCO output jitter.

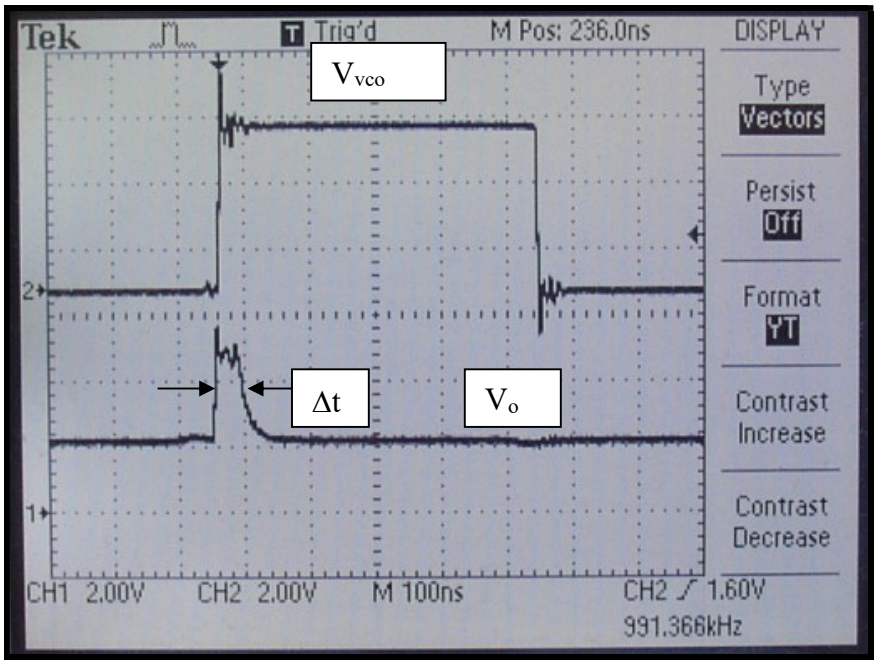


Figure A4 - V_{vco} (trigger source) and V_o waveform, at f_{in} = 1.00 MHz.

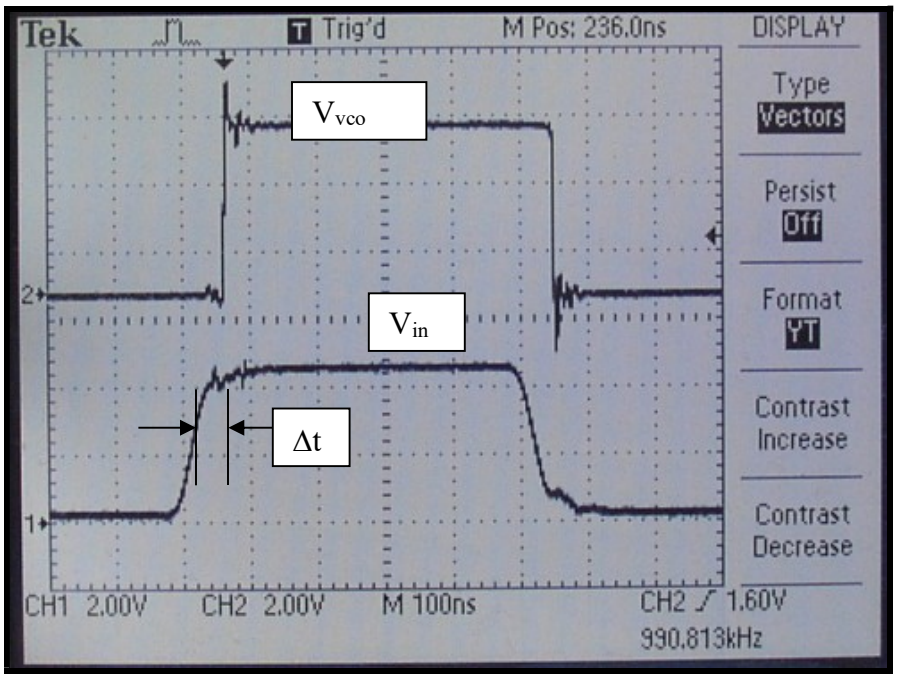


Figure A5 - V_{vco} (trigger source) and V_{in} waveform, at f_{in} = 1.00 MHz.

Figure A6 shows the comparison of VCO and Vin at fin = 1.70 MHz. Note that the static phase error increases in this case as a broader pulse from the charge-pump is needed to generate a higher dc average voltage from the modified RC network. If the value of R_B is too large, it is not effective because the required static phase error is still within the 'dead-zone' limit. If R_B is too small, it will affect the dynamic response of the PLL, moreover this also reduces the lock range (as the maximum frequency trackable by the PLL is limited to $\theta_e = 180^o$).

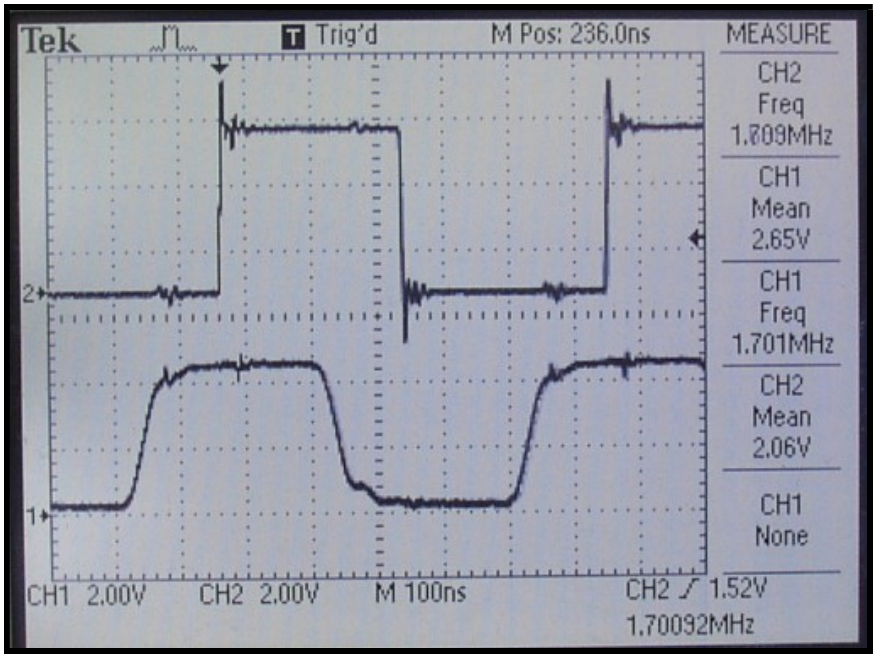


Figure A6 - V_{vco} (trigger source) and V_{in} waveform, at f_{in} = 1.70 MHz.