6- Passive and Active RF Lumped Components

References

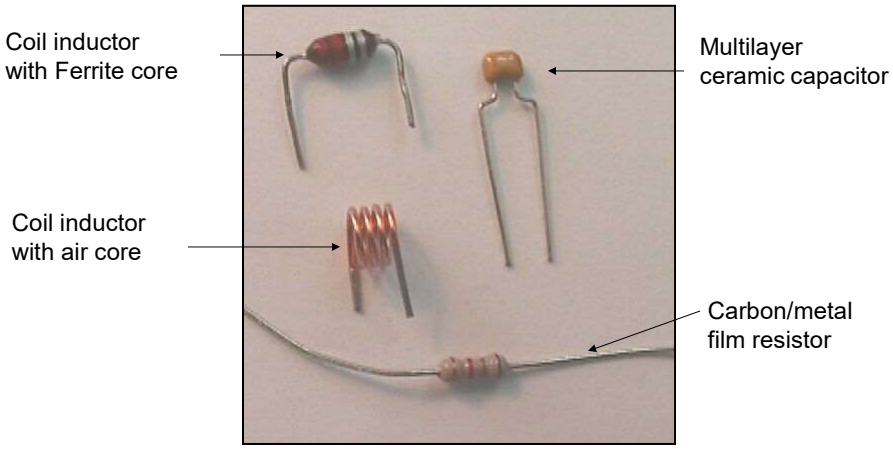
- [1] Ludwig R., Bretchko P., “RF circuit design - theory and applications”, 2000, Prentice Hall.
- [2] Laverghetta T.S., "Practical Microwaves", 1996, Prentice-Hall.
- [3] Robertson I. D., Lucyszyn S. (Editors), “RFIC and MMIC design and technology”, 2001, IEE Circuits, Devices and Systems Series 13.
- [4] Gray P. R., Meyer R. G., “Analysis and design of analog intergrated circuits”, 3rd Edition, 1993, John-Wiley & Sons. Note: 5th (2009) edition of this book is available with newer materials.
- [5] Millman J., Halkias C. C.,”Integrated electronics”, 1972, McGraw-Hill.
- [6] Massobrio G., Antognetti P., “Semiconductor device modeling with SPICE”, 2nd edition 1993, McGraw-Hill.
- [7] Sze S. M., “Semiconductor devices – physics and technology”, 3rd edition 2012, John-Wiley & Sons.
- [8] Gilmore R., Besser L.,”Practical RF circuit design for modern wireless systems”, Vol. 1 & 2, 2003, Artech House.
- [9]* D.M. Pozar, “Microwave engineering”, 4th Edition, 2011 John-Wiley & Sons.

Agenda

- Passive lumped components at RF.
- Surface-mounted packaging.
- A review of bipolar junction transistor (BJT) operation and model.
- Overview of other active RF components.
- Biasing circuit design for BJT and basic amplifier circuit.
- Frequency response for basic amplifier circuit (S-parameters).
- Appendix – examples of active RF circuits.

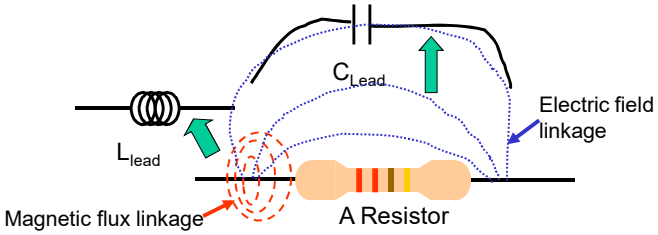
1.0 Lumped Components at Radio Frequency (RF)

Passive Lumped Components for Medium Frequency (up to 300MHz)



Effect of Packaging

- How the component is packaged is very important at high frequencies.
- When a component is energized (e.g. voltage and current applied):

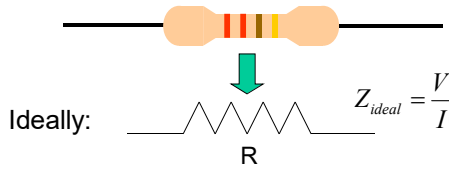


- To reduce unwanted lead inductance and capacitance, a smaller package size with shorter leads is preferred. This results in the birth of surface-mounted technologies (SMT). SMT also enable miniaturization of the physical circuits.

Passive Lumped Components at RF (1)

- At radio frequencies a component is not what it appears to be.
- For instance consider a resistor in leaded package:

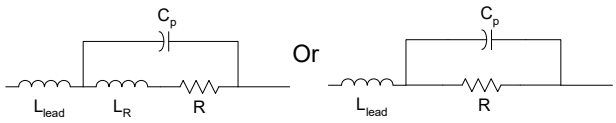
Note: Make sure you understand the meaning of 'lumped', and its opposite, the 'distributed'.



$$Z_{ideal} = \frac{V(\omega)}{I(\omega)} = R$$

A more accurate representation would be:

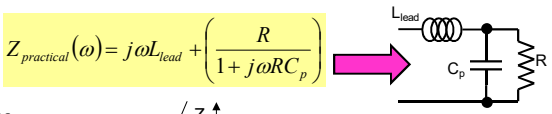
$$Z_{practical}(\omega) = j\omega L_{lead} + \left(\frac{R}{1 + j\omega RC_p}\right)$$

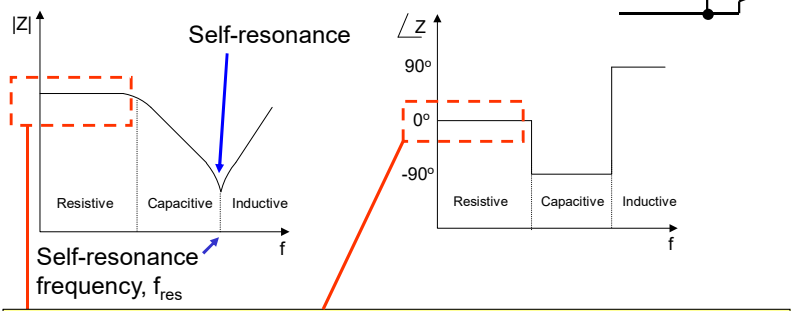


Passive Lumped Components at RF (2)

- The magnitude and phase of the resistor's impedance as a function of frequency:

$$Z_{practical}(\omega) = j\omega L_{lead} + \left(\frac{R}{1 + j\omega RC_p}\right)$$

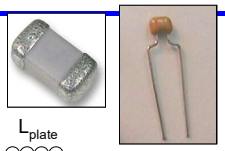


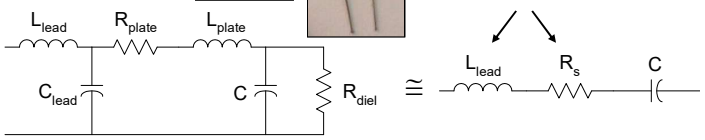


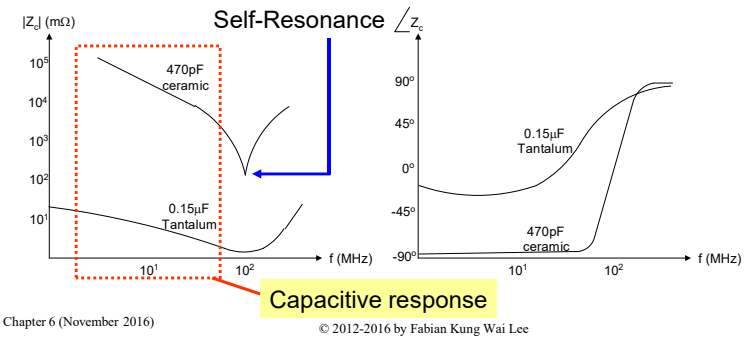
Only in this range will the component behave as an ideal resistor, usually f_{res} is < 250MHz for leaded resistors

Passive Lumped Components at RF (3)

- For a capacitor:

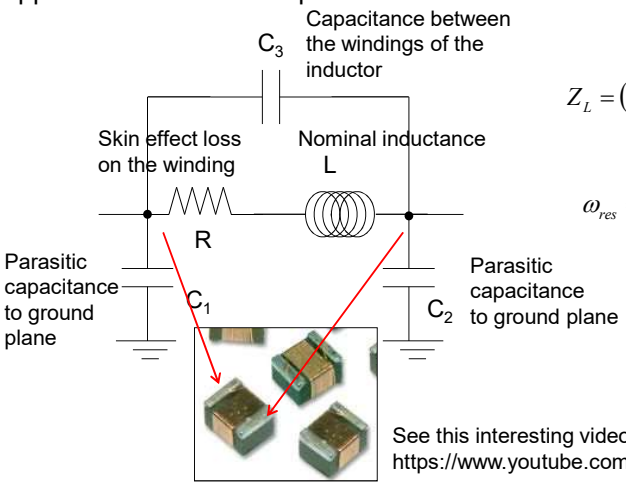






Passive Lumped Components at RF (4)

- Approximate model for a practical inductor:



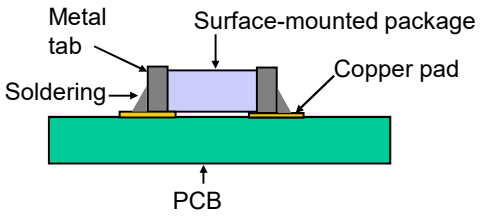
$$Z_L = (R + j\omega L) // \left(\frac{1}{j\omega C}\right)$$

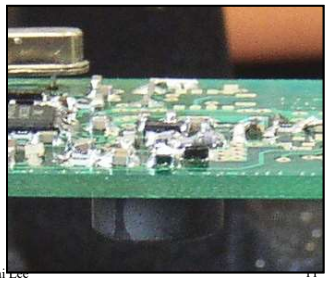
$$\omega_{res} = \sqrt{\frac{1}{LC} - \left(\frac{R}{L}\right)^2}$$

See this interesting video by Keysights:
https://www.youtube.com/watch?v=fwD_82dzsx8

Surface-Mounted Package

- Surface-mount technology (SMT) was developed in the 1960s and became widely used in the late 1980s. Much of the pioneering work in this technology was done at the then IBM.
- Instead of leads, components were mechanically redesigned to have small metal tabs or end caps to be directly soldered to the surface of the PCB.
- Components became much smaller. Elimination of leads also reduces parasitic inductance and capacitance or the component, allowing operation at higher frequency.

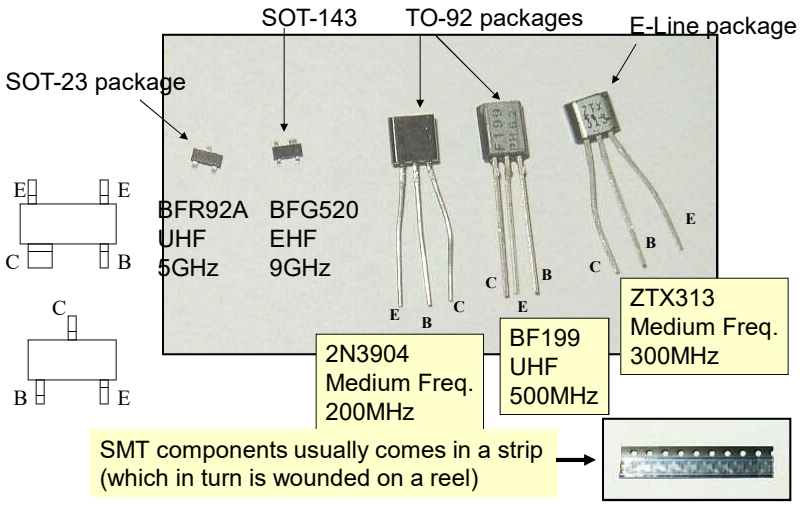




Who Determines the Package Dimension ?

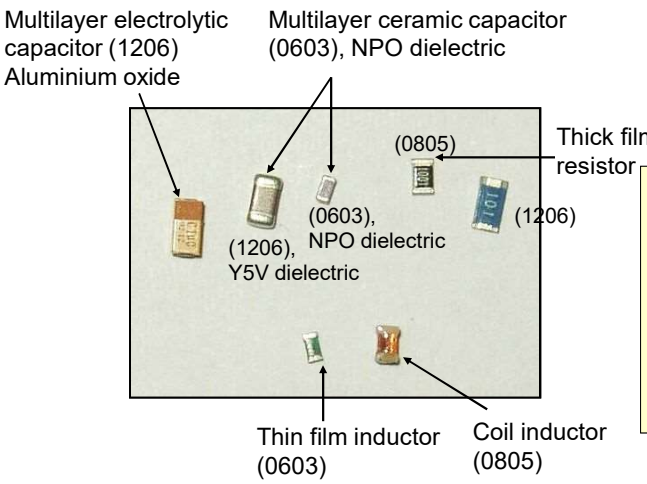
- A package dimension and style is usually determined by the needs of the electronic industry.
- Usually a dominant component manufacturing company will introduce a new package type based on current needs. The mechanical design will be proposed to a standard making body.
- If sufficient players adopt the package, it will become an accepted standard and a formal document is drafted to describe its characteristics.
- At present in North America the standards for SMT and other components is drafted by the **JEDEC** Solid State Technology Association (JEDEC - **J**oint **E**lectron **D**evice **E**ngineering **C**ouncil), http://www.jedec.org/ . JEDEC members consist of electronics and semiconductor companies worldwide.
- JEDEC also works closely with Electronic Industries Association of Japan (EIAJ) to focus on similar package outlines from each organization into one world-wide standard package outline.

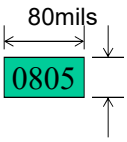
Active Lumped Component - Bipolar Junction Transistor



SMT components usually comes in a strip (which in turn is wounded on a reel)

Passive Lumped Components for Ultra High Frequencies (UHF) (>300MHz) Application



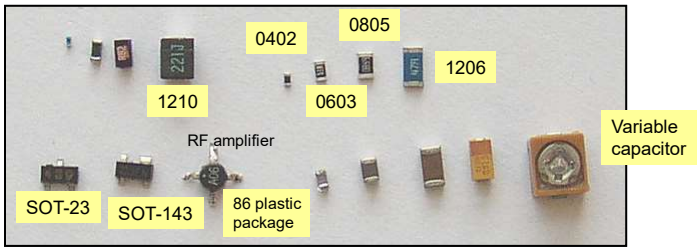


Other standard sizes are:
- 0402, smaller than 0603.
- 0201, even smaller than 0402.
- 1210, bigger than 0805.

More Examples (1)

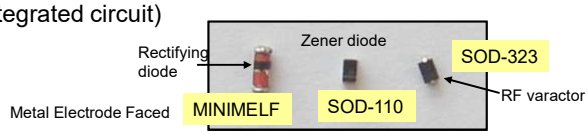
Inductors

Thick film Resistors



Transistors and MMIC (monolithic microwave integrated circuit)

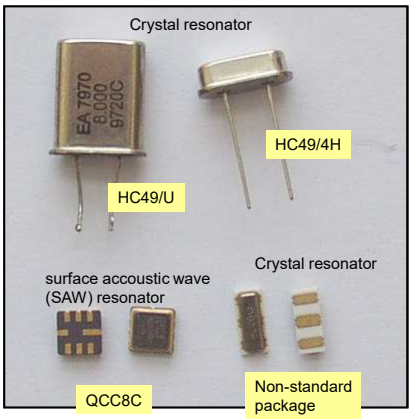
Various types of capacitors



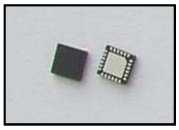
Various types of diodes

More Examples (2)

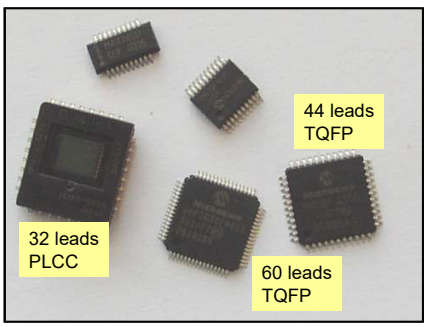
Various packaging for Piezoelectric crystal and related components



24 Leads QFN

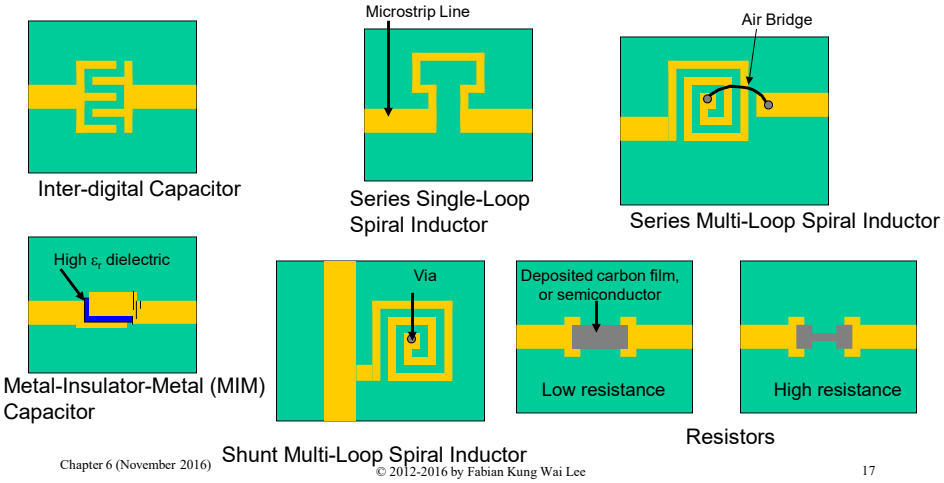


Various SOIC and QFP packages



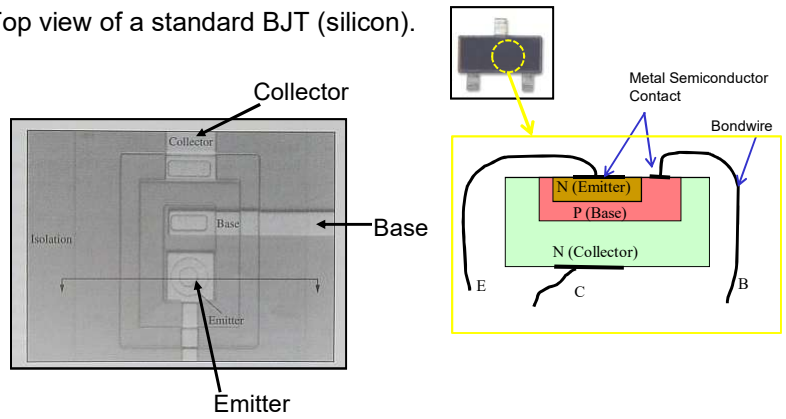
Passive Lumped Components for Incorporation into PCB and other Substrates

- Lumped components directly incorporated onto the surface of PCB. Typical for operation in GHz region.



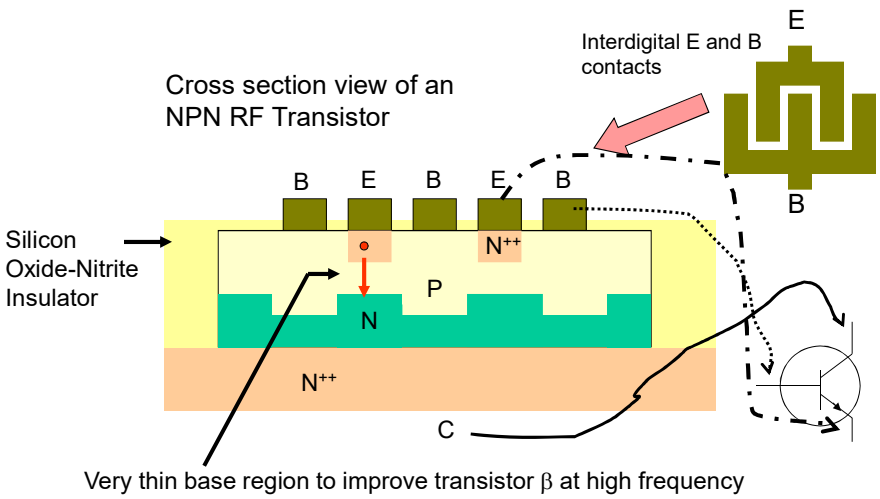
Bipolar Junction Transistor (BJT)

- Top view of a standard BJT (silicon).



Source: R. C. Jaeger, T. N. Blalock, "Microelectronics circuit design", 2nd edition 2003, McGraw-Hill.

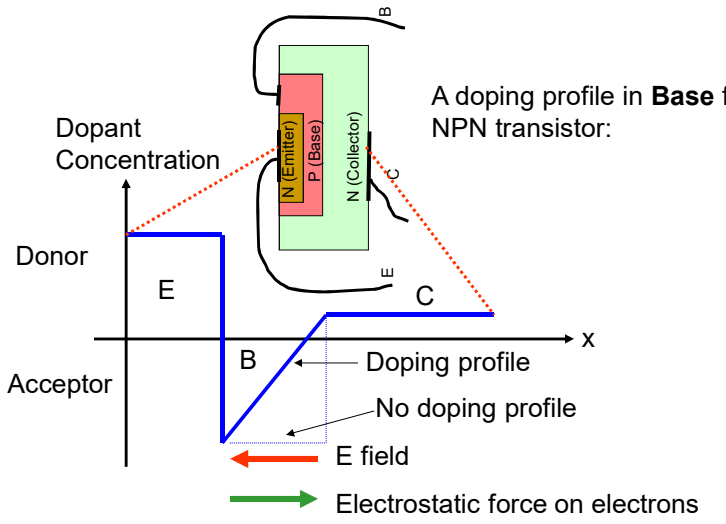
RF Bipolar Junction Transistor (RF BJT)



RF BJT Construction (1)

- Almost all RF transistors are NPN, because mobility of electron is much higher than hole in Silicon ($\mu_e = 0.13 m^2V^{-1}s^{-1}$, $\mu_h = 0.05 m^2V^{-1}s^{-1}$). The mobility is inversely proportional to the base transit time, τ.
- The **Base** thickness is very thin, to improve current gain h_{fe} at high frequencies. The h_{fe} is related to a parameter known as base transit time τ, smaller τ yields larger h_{fe}.
- Inter-digital **Base** and **Emitter** contacts are employed to reduce base spreading resistance $r_{b'b}$ and to reduce the noise generated by the transistor.
- The base transit time τ can be reduced further if electrons are accelerated across the base by electric field (**E**). This is achieved by deliberately introducing doping concentration profile in the base.
- Low-cost commercial RF transistors in discrete form can have f_T up to 10 GHz. Examples of RF BJT are BFR92A (f_T = 5 GHz) and BFG520 (f_T = 9 GHz), from NXP Semiconductors (www.nxp.com) and Infineon Technologies.

RF BJT Construction (2)

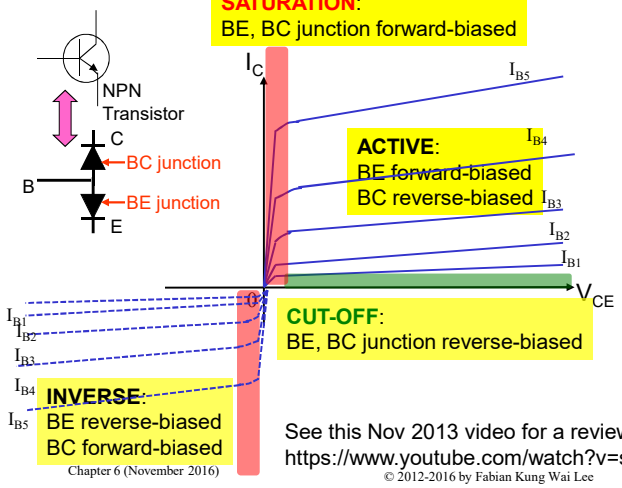


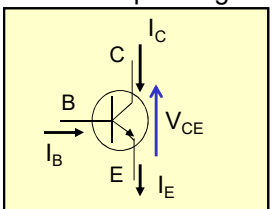
A doping profile in **Base** for NPN transistor:

BJT Operating Regions

Extra

- We can view the BJT as 2 back-to-back PN junctions with 4 operating regions.





$I_C = \beta I_B$

$I_E = I_C + I_B$

$\Rightarrow I_E = I_B(\beta + 1)$

$\Rightarrow I_E = I_C\left(\frac{\beta+1}{\beta}\right)$

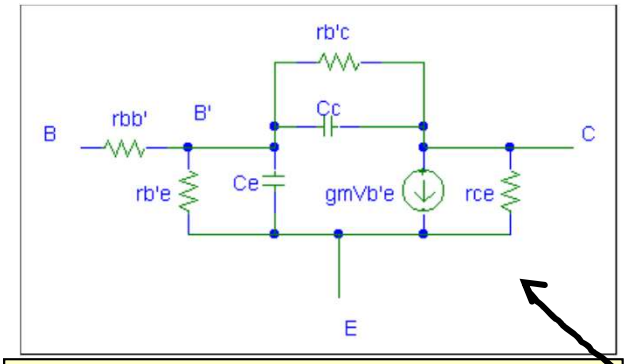
Only V_{CE} and I_C are needed to know the state of the BJT

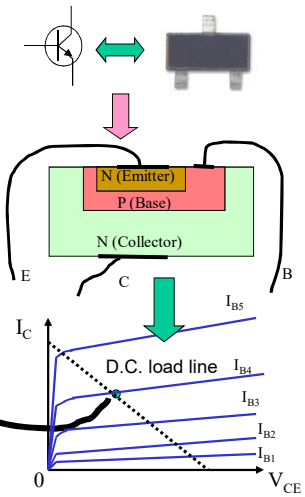
See this Nov 2013 video for a review:
https://www.youtube.com/watch?v=s69o0AmYyjo

Small-Signal Model of Transistor at High Frequency - The Hybrid Pi Model

Extra

The Hybrid-Pi Model (Gray & Meyer [4]):





Fixing the d.c. I_C, I_B and V_{CE} , the response of the transistor for small variation I_C+i_c , I_B+i_b and $V_{CE}+v_{ce}$ is given by the small-signal model. How to fix the d.c. current and voltage, known as biasing the transistor will be discussed shortly.

The Parameters of Hybrid-Pi Model (1)

Extra

- The names of the various parameters:
  $r_{bb'}$ - Base spreading resistance (also given as r_x)
  g_m – Transconductance (it relates voltage to current)
  C_e - Emitter capacitance
  C_c - Collector capacitance
  $r_{b'c}$ - Collector to base resistance (also given as r_μ)
  $r_{b'e}$ - Base to emitter resistance (also given as r_π)
  r_{ce} - Output resistance (also given as r_o)

Alternatively see the proof by F. Kung on how to get the hybrid-Pi model of a BJT using Taylor Series Expansion of the V-I relationship of BE and BC junctions, March 2000.

The Hybrid-Pi model is a fairly accurate description of the BJT small-signal response up to GHz frequency range. You can find more information on the Hybrid-Pi model in [4].

The Parameters of Hybrid-Pi Model (2)

Extra

- Physical explanation of the Hybrid-Pi parameters…

$r_{bb'}$	**The base-spreading resistance** – The base region is very thin. Current, which enters the base region across the emitter junction, must flow through a long narrow path to reach the base terminal. Hence the ohmic resistance of the base is very much larger than that of the collector or emitter. The manufacturer of the transistor usually provides this value.
g_m	**The transconductance** – The transconductance is defined as: $g_m = \frac{dI_C}{dV_{BE}} = \frac{qI_C}{kT} \cong \frac{I_C(\text{in mA})}{26}$ at T=25°, q= electronic charge, $1.602\text{x}10^{-19}$C Where I_C is the dc collector current.
C_e	**The emitter capacitance** – C_e represents the sum of the emitter diffusion capacitance C_{DE} (or base charging capacitance) and the emitter junction depletion region capacitance C_{TE}. $C_e = C_{DE} + C_{TE}$ C_{DE} is due to finite charge transit time in the emitter PN junction, it is given by Gray & Meyer [4], chapter 1 and Millman & Halkias [5], chapter 11 as: $C_{DE} = \tau_F g_m$ Where τ_F= forward baised base transit time. The depletion region capacitance depends on the biasing voltage across the PN junction and the doping profile of the junction. The expression is rather lengthy, the interested reader can consult Gray & Meyer [4], chapter 1.

The Parameters of Hybrid-Pi Model (3)

Extra

$r_{b'e}$	**The input resistance –** This resistance is defined by Gray & Meyer [4], chapter 1: $r_{b'e} = \frac{dV_{B'E}}{dI_B} = \frac{h_{fe}}{g_m}$
$r_{b'c}$	**The collector to base resistance** – In active region, the collector junction of a transistor is reverse biased. Hence when V_{CE} changes, the depletion region width of the collector junction also changes, this modulates the effective length of the base and a change in total minority carrier charge Q_m stored in the base. I_C is a function of Q_m , consequently the collector current also changes. This effect is modeled by the inclusion of $r_{b'c}$. $r_{b'c} = h_{fe} r_{ce}$ Usually $r_{b'c} >> r_{b'e}$ and can be ignored.
C_C	**The collector capacitance** – C_C is the depletion region capacitance between the collector and base PN junction. It is important as Miller effect can greatly increases its effect.
r_{ce}	**The output resistance** – The output resistance is due to base-width modulation effect or the Early effect. It is given by (Gray & Meyer [4], chapter 1): $r_{ce} = \frac{V_A}{I_C} = \frac{qV_A}{kTg_m}$ Where V_A is known as the Early voltage and I_C is the dc collector current.

Validity of the Hybrid - Pi Model

Extra

- The Hybrid-Pi model is only valid under small-signal conditions. Exactly what do we imply by small-signal is shown below.

Approximate relationship between I_C and V_{BE}: (BJT under active region)

$$I_C \cong I_S \exp\left(\frac{V_{BE}}{V_T}\right)$$

Say $V_{BE} \to V_{BE} + \Delta V_{BE}$ ⇒

$$I_C' = I_S \exp\left(\frac{V_{BE}+\Delta V_{BE}}{V_T}\right) = I_S \exp\left(\frac{V_{BE}}{V_T}\right)\exp\left(\frac{\Delta V_{BE}}{V_T}\right)$$

Upon using Taylor's expansion:

$$I_C' = I_C \exp\left(\frac{\Delta V_{BE}}{V_T}\right) = I_C\left(1+\frac{\Delta V_{BE}}{V_T}+\frac{1}{2}\left(\frac{\Delta V_{BE}}{V_T}\right)^2+\frac{1}{6}\left(\frac{\Delta V_{BE}}{V_T}\right)^3+\ldots\right)$$

These higher-order terms (HOT) are ignored

Let : $i_C = I_C' - I_C = \Delta I_C \qquad \Delta V_{BE} = v_{B'E} << V_T$

Then : $i_C = \Delta I_C \cong \frac{I_C}{V_T} v_{B'E} = g_m v_{B'E}$ ⇔ $g_m = \frac{dI_C}{dV_{BE}} \cong \frac{i_C}{v_{BE}} = \frac{I_C}{V_T}$

Conditions When Hybrid-Pi Model Can Be Applied

Extra

1. Only valid for small-signal operation, not valid for power amplifier.
2. Extra conditions:
   - h_{fe} close to h_{FE} (small-signal current gain similar to large-signal current gain).
   - $\Delta V_{BE} = v_{B'E} << V_T$

See the book by Millman & Halkias [5], Gray & Meyer [4] for further information.

Example

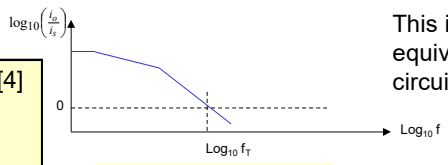
Assuming $\Delta V_{BE} << V_T$ implies $\Delta V_{BE} < 0.1 V_T$.
ΔV_{BE} must be smaller than 2.6mV
for the hybrid pi model to be accurate.

$k = 1.381\times10^{-23} JK^{-1}$
$T = 300K \left(\text{about } 27^o C\right)$
$q = 1.602\times10^{-19} C$
$V_T = \frac{kT}{q} \cong 0.0259V \cong 26mV$

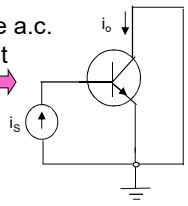
Useful BJT Figure of Merit (1) - The Transition Frequency (f_T)

- The transition frequency, f_T is the frequency where the small signal current gain i_o/i_s of the circuit approaches unity.
- It is dependent on the small signal capacitance C_e and C_c.

See Gray & Meyer [4] for derivation, note that a similar definition to f_T can also be applied to FET.



This is the a.c. equivalent circuit!



$$f_T \cong \frac{1}{2\pi}\frac{g_m}{C_e + C_C}$$

- Beyond f_T, a transistor is useless as an amplifier (for both current and voltage amplification). Hence f_T fixes the upper usable frequency of a BJT device.
- f_T is a function of D.C. condition, $f_T(I_C, V_{CE})$, can you explain why?

Useful BJT Figure of Merit (2) – The f_{max}

- Another useful figure of merit is the maximum frequency of oscillation, f_{max}.
- This is the maximum frequency where the transistor circuit, with output connected to the input (with appropriate impedance matching network), oscillates.
- Typically $f_{max} > f_T$.
- f_{max} corresponds to the frequency where maximum available power gain (G_{amax}) of the transistor equals to 1.

PN Junction Capacitance and the Base Transit Time

Extra

- The PN junction capacitance can be written as $C_X = C_{DX} + C_{TX}$ for BC and BE junction, x = C or E.
- C_{DX} is the diffusion capacitance while C_{TX} is the depletion region capacitance (also called the space charge capacitance).
- C_{DX} is negligible when the PN junction is reverse biased and is the dominant capacitance when the PN junction is forward biased.
- Thus for a BJT operating in Active Region, $C_E \approx C_{DE}$ and $C_C \approx C_{TC}$.
- Where $C_{DE} = \tau_F g_m$ and C_{TC} is given by:

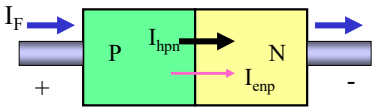
$$C_{TX} \cong \frac{C_{jx}}{\left(1 - \frac{V_{BX}}{V_{jX}}\right)^m} \quad \text{x = C or E}$$

- τ_F is the base transit time (the average life time of minority charge carrier in base - for NPN transistor this is the average life time of electrons in the Base before being 'sucked' into the Collector region).
- C_{jx} is the depletion region capacitance when $V_{BX}=0$ and m and V_{jx} are parameters usually determined empirically from measurement. A smaller τ_F will yield a larger f_T.

More on PN Junction Capacitance (1)

Extra

- The diffusion capacitance is given by (see Chapter 3, [5], charge-control description of a PN junction):

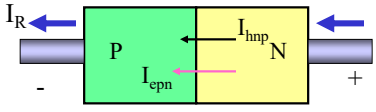


PN junction is Forward biased

$$C_D = \frac{\tau_h I_{hpn}}{\eta V_T} + \frac{\tau_e I_{enp}}{\eta V_T}$$

$$V_T = \frac{kT}{q}$$

- I_{hpn} is the current component due to injection of holes from P to N region, while I_{enp} is the component from injection of electrons from N to P region. Together they constitute the forward biased current I_F.
- Similarly under reverse biased the diffusion capacitance is given by:



PN junction is Reverse biased

$$C_D = \frac{\tau_e I_{epn}}{\eta V_T} + \frac{\tau_h I_{hnp}}{\eta V_T}$$

- Since I_{epn} and I_{hnp} are extremely small, C_D is also very small (<10^{-13} typical).

More on PN Junction Capacitance (2)

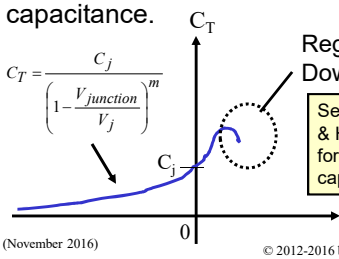
Extra

- For a typical NPN transistor, the N-type region of the Emitter is highly doped and P-type region of the Base is lightly doped.
- Thus under forward biased (BE junction forward biased), $I_{hpn} << I_{enp}$, $I_E \cong I_{epn}$. And C_{DE} can be approximated as:

$$C_{DE} \cong \frac{\tau_e I_{enp}}{\eta V_T} \cong \frac{\tau_e I_E}{\eta V_T} \cong \frac{\tau_e I_C}{\eta V_T}$$

- Recognizing that $\tau_F = \tau_e$ ⇒ $C_{DE} \cong \frac{\tau_F I_C}{\eta V_T} = g_m \tau_F$

- A plot of C_T versus junction voltage is shown below (see Chapter 1, [4]). Again charge-control description of a PN junction is used to derive the capacitance.

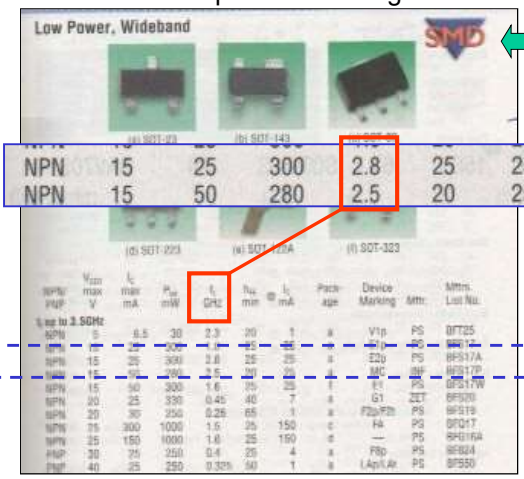


Region where the expression breaks Down.

See books by Gray & Meyer [4], Millman & Halkias [5] or any semiconductor device physic text for further discussion about junction capacitance and transistor.

RF Transistor Selection (1)

- Example of how the parameters of RF devices are tabulated in electronic components catalog.



Adapted from the catalogue of Farnell Components. (now known as **Element14** in Malaysia)

- f_T
- Power dissipation
- $V_{CE\ (max)}$
- $h_{FE\ (min)}$
- $P_{m(max)}$

RF Transistor Selection (2)

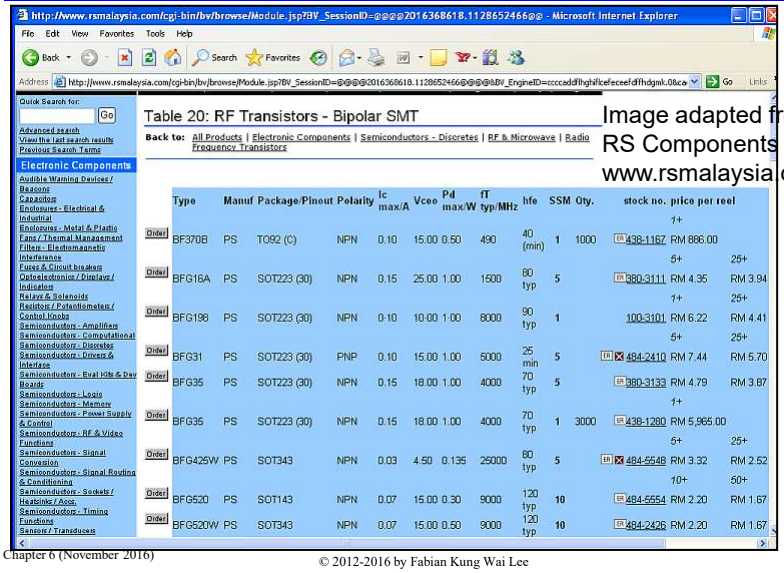
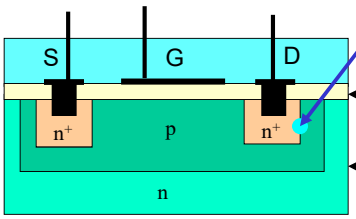


Image adapted from RS Components Malaysia www.rsmalaysia.com

Other Active Devices – MOSFET and MESFET (1)

Extra

N-channel Metal-Oxide Semiconductor Field Effect Transistor (MOSFET)



PN junction contact

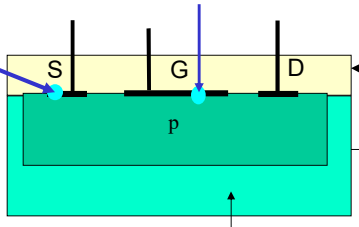
Oxide Layer

The substrate (usually made of element semiconductor such as Silicon)

Metal-Semiconductor rectifying contact

Ohmic Metal-Semiconductor contact

N-channel Metal-Semiconductor Field Effect Transistor (MESFET) (Today this device is not so popular)



Oxide layer

The substrate (usually made of composite semi-conductor such as Gallium Arsenide)

Semi-insulating layer (usually undoped semiconductor)

MOSFET and MESFET (2)

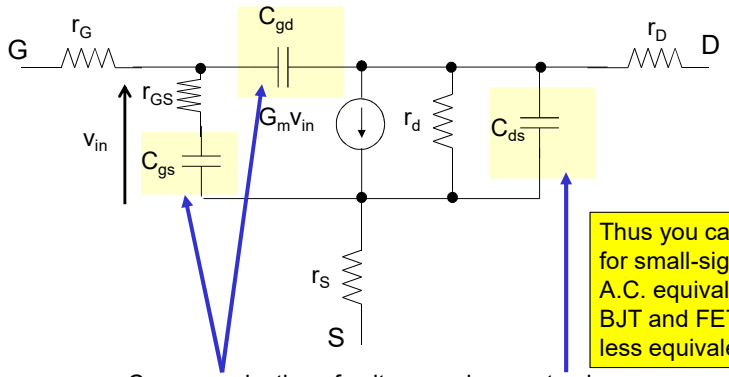
Extra

- For operating frequency > 2GHz, FET are usually used in place of BJT in microwave circuits. Typically MESFET is used in both discrete and integrated circuit form, while MOSFET is only used in integrated circuit.
- Among BJT, MOSFET and MESFET, MESFET has the highest transition frequency f_T and is often used for high-performance RF/microwave circuits:

- (1) FET has better noise characteristic (lower noise figure).
- (2) FET such as MESFET can be constructed from compound semiconductor such as Gallium Arsenide (GaAs) (the so-called III-V compound) which has higher electron mobility than Silicon.
- (3) Smaller Gate capacitance in MESFET structure. The Schottky barrier (Metal-Semiconductor contact) on the Gate of MESFET has smaller capacitance as compared to the gate oxide capacitance of MOSFET, the PN junction in JFET or the C_π of BJT.
- (4) Also ohmic contact on the Drain and Source on MESFET reduces the corresponding Drain and Source capacitance.
- (2), (3) and (4) contributed to much higher f_T in MESFET.

Small-Signal Model for FET

Extra



Thus you can see that for small-signal or A.C. equivalent circuit, BJT and FET are more or less equivalent.

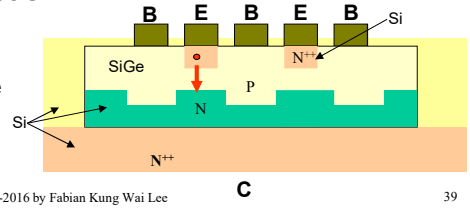
Causes reduction of voltage and current gain at high frequency

HBT and HEMT (1)

Extra

- Most modern high-performance RF/microwave circuits employ FET, for instance GaAs (Gallium Arsenide) MESFET for operating frequency > 3GHz. GaAs MESFET can operate in excess of 10GHz.
- Since late 1990s, **Hetero-junction Bipolar Transistor (HBT)** is introduced commercially. In HBT different semiconductor material is used for the Base, Emitter and Collector region. For instance P-type GaAs for Base, N-type GaAs for Collector and N-type AlGaAs for Emitter. Another example of HBT is the SiGe (Silicon-Germanium) on Silicon process. Here a compound of SiGe is used for the Base. An example of discrete SiGe HBT is BFP620 from Infineon Technologies (www.infineon.com) with f_T of 65GHz!

An example of SiGe HBT



HBT and HEMT (2)

Extra

- The hetero-junction structure results in valence band discontinuity between the Base and Emitter of an NPN structure [7].
- This discontinuity reduces the injection of holes from Base to the Emitter, while allowing the injection of electron from Emitter to Base. This effect improves emitter efficiency (γ).
- The emitter efficiency is further improved by being able to construct a transistor with heavily doped and very thin Base region, thus base-spreading resistance ($r_{b'b}$) and base-transit time (τ_F) are reduced.
- Smaller τ_F results in smaller C_e. $f_T \cong \frac{1}{2\pi}\frac{g_m}{C_e + C_C}$

HBT and HEMT (3)

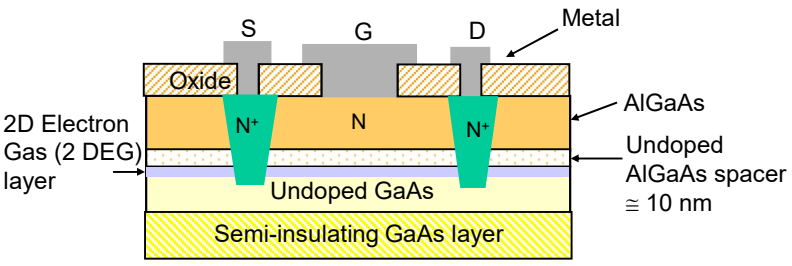
Extra

- Hetero-junction approach is also applied to MESFET, in the channel region of the FET, called Modulation-Doped Field Effect Transistor (MODFET) [7].
- However since FET operation does not depend on charge injection, but of charge transport in the channel between the Drain and Source terminals, the introduction of hetero-junction structure in the channel serves to increase the electron mobility, allowing very rapid exchange of electrical signal between Drain and Source. This improves the f_T of the FET.
- Although based on MODFET approach, the resulting FET is usually called **High Electron Mobility Transistor (HEMT)**. Higher electron mobility allows the device to response to rapid changes in its Gate. Effectively this reduces C_{gs}.
- Such transistor can operate well into the millimeter wave region or in excess of 100GHz.

HBT and HEMT (4)

Extra

- An example of HEMT using GaAs as the substrate.



Usually in depletion mode.
But can be designed to work in both depletion and enhancement mode

End Notes on Active RF Components

Extra

- Since 2006, the CMOS technology, where the main active component is the MOSFET, is also used extensively for applications up to a few GHz. This is usually implemented in integrated circuit form.
- For all these active devices, the small-signal equivalent are almost similar to the hybrid-pi model of the BJT, so in this course we only concentrate on RF circuit design using BJT. The major difference is in the way we bias the active devices. FET active devices, which come in enhancement and depletion mode will require different biasing circuits.
- Also depletion mode device sometimes requires negative d.c. supply.
- Refer to Roberson & Lucyszyn [3], Gilmore & Besser (Vol. II) [8] for more information. More advanced and updated information can also be obtained from Sze [7].

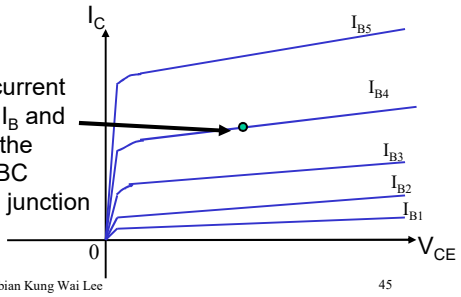
2.0 Review of BJT Amplifier Biasing and S-Parameters Computation

D.C. Biasing for BJT and FET (1)

- Biasing means putting proper d.c. voltages and currents at a transistor terminals (Collector, Base, Emitter) so that the device is in the required operating region, when no a.c. signal is applied.
- A bipolar junction transistor (BJT) has 4 operating regions: Active, Cut-off, Saturation and Inverse.
- For small-signal amplifier, we bias the transistor in the Active region.
- Small-signal amplifiers is usually of type Class-A, because it needs to have linear response.

Key point of BJT biasing for small-signal operation, NPN transistor: $V_C > V_B > V_E$ (Active region)

We fix the d.c. current and voltage, I_C, I_B and V_{CE} of a BJT to the Active Region (BC junction RB, BE junction FB)



D.C. Biasing for BJT and FET (2)

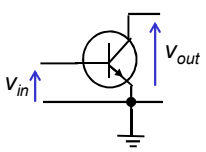
- For large-signal amplifier, we may bias the transistor in the Active and the Cut-off regions, depending on the Class of the amplifier.
- Biasing also applies to field effect transistor (FET), which has 4 distinct operating regions: Active (also called Saturation), Linear, Cut-off and Inverse.
- Small-signal FET amplifier is usually biased in Active region.
- Large-signal FET amplifier can be biased in Active and Cut-off regions.

Key point of FET biasing for small-signal operation, N-channel:
$V_D > V_G > V_S$ (Active region)
$V_{DS} > V_{GS} - V_{TN}$

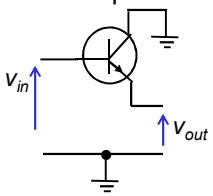
Threshold voltage

BJT Amplifier Configurations

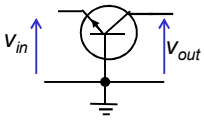
- A transistor is a 3 terminals device. Thus 2 of the terminals can be used to for signal input and output. The third terminal can be grounded, usually A.C. grounded with respect to the other terminals.
- This grounded terminal is thus called the common terminal, and hence the name for transistor amplifier configuration.



Common-Emitter (CE)



Common-Collector (CC)



Common-Base (CB)

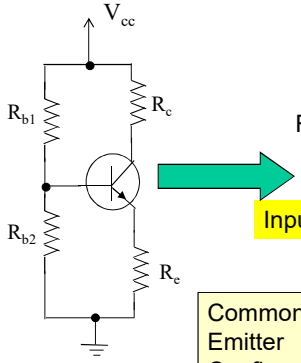
Can you explain why there is no other permutations?

- Note that a similar situation exist for FET amplifier, we call these **Common-Source**, **Common-Drain** and **Common-Gate** FET amplifiers.

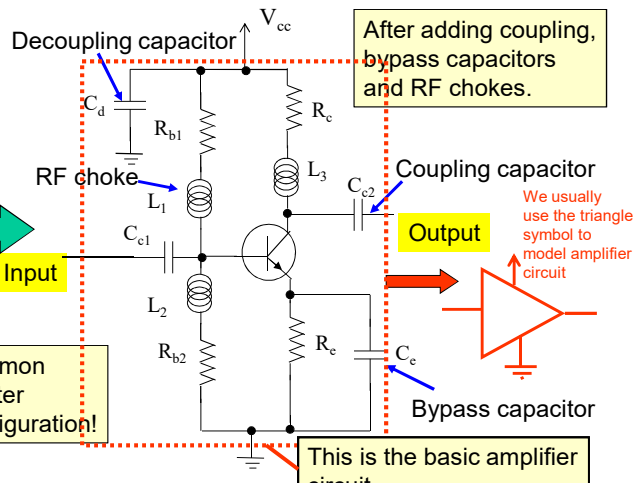
Typical D.C. Biasing Circuits for BJT (1)

- **Emitter Feedback Bias** (suitable for low frequency up to UHF band):

Basic biasing network



Decoupling capacitor



After adding coupling, bypass capacitors and RF chokes.

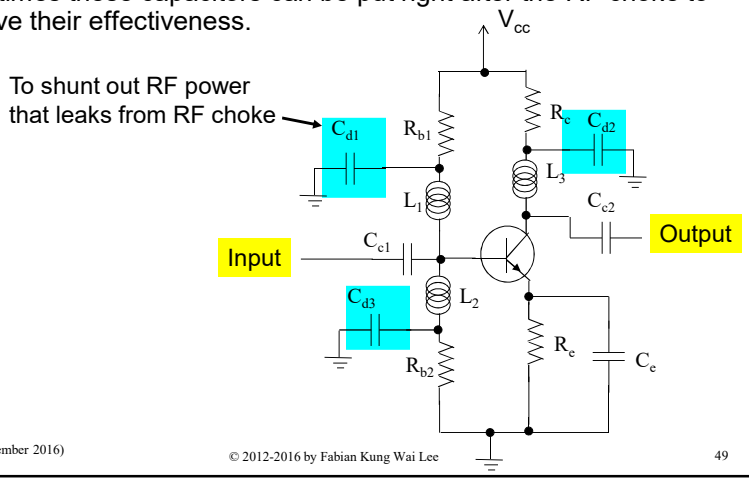
We usually use the triangle symbol to model amplifier circuit

Common Emitter Configuration!

This is the basic amplifier circuit

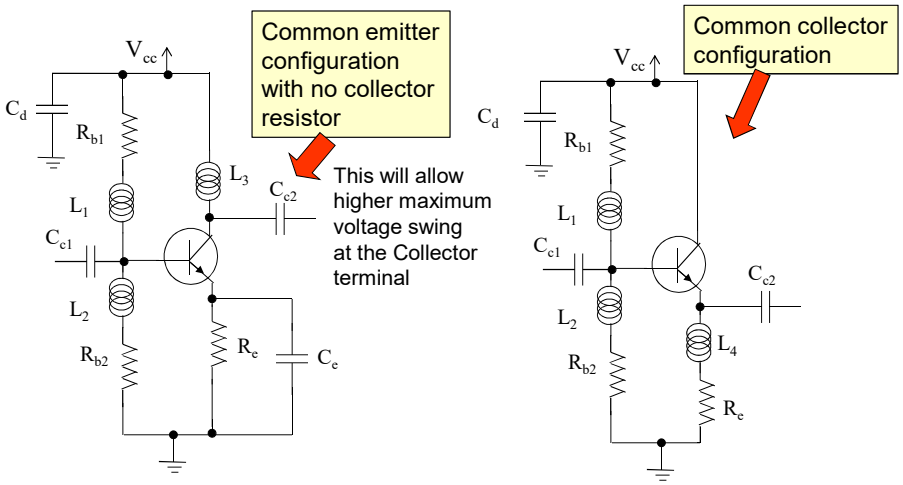
Typical D.C. Biasing Circuits for BJT (2)

- Bypass or decoupling capacitors are used to stabilize the d.c. voltage and current levels and to isolate RF signals from other circuitry.
- Sometimes these capacitors can be put right after the RF choke to improve their effectiveness.



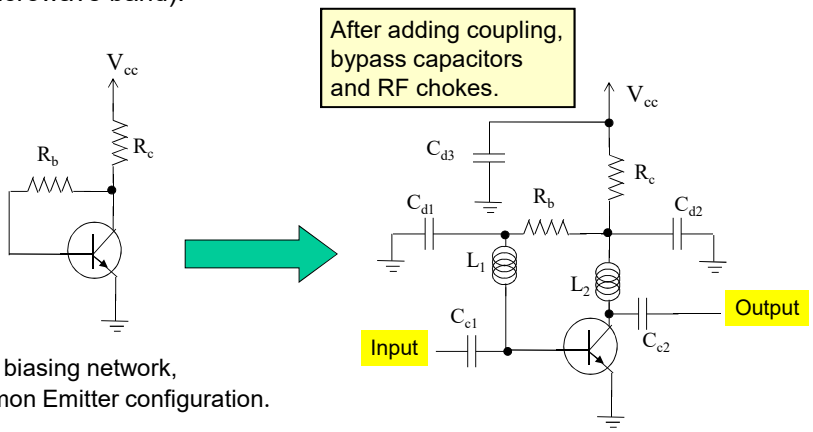
Typical D.C. Biasing Circuits for BJT (3)

- Other forms of **Emitter Feedback Bias**:



Typical D.C. Biasing Circuits for BJT (4)

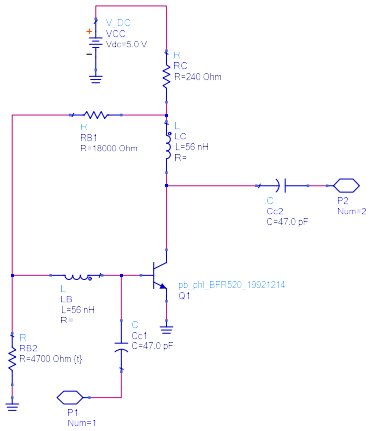
- Voltage or **Collector Feedback Bias** (suitable for low frequency up to microwave band):



Basic biasing network,
Common Emitter configuration.

Typical D.C. Biasing Circuits for BJT (5)

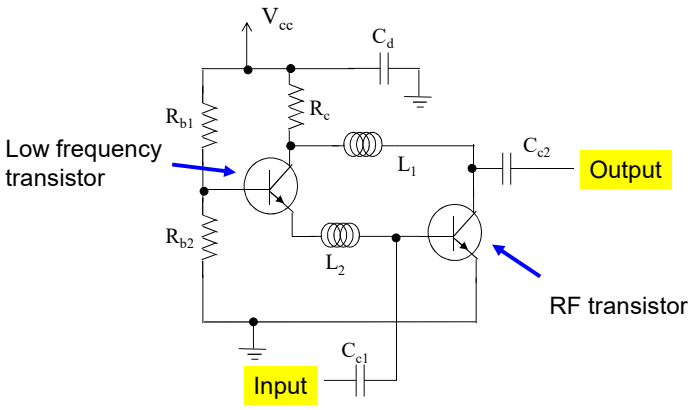
- **Base Feedback Bias**, better DC stability compare to Collector Feedback Bias (suitable for low frequency up to microwave band):



Basic biasing network,
Common Emitter configuration.

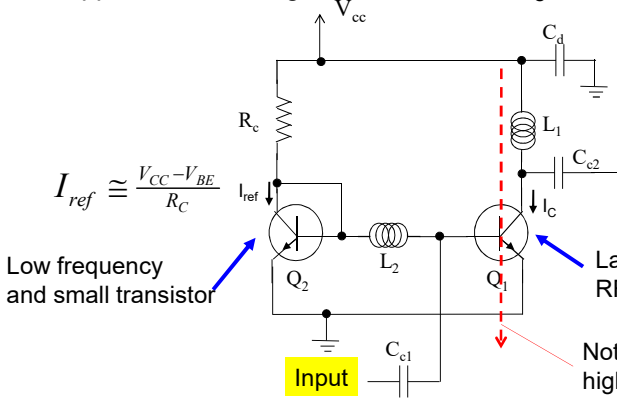
Typical D.C. Biasing Circuits for BJT (6)

- **Active Bias** (suitable for low frequency to microwave band):



Typical D.C. Biasing Circuits for BJT (7)

- Another form of Active Bias using current mirror, popular for high power application with large Collector current I_C. Usually $I_C >> I_{ref}$.



$$I_{ref} \cong \frac{V_{CC} - V_{BE}}{R_C}$$

$$I_C \cong \frac{A_{E1}}{A_{E2}} I_{ref}$$

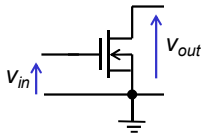
Where:
A_{E1} = Emitter area for transistor Q_1
A_{E2} = Emitter area for transistor Q_2

Some Issues Concerning D.C. Biasing

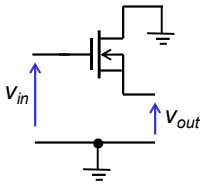
- Biasing network must not interfere with the flow of RF energy during normal operation. Hence the quality of the bypass capacitors and RF chokes is vital.
- Temperature stability. Bias point or quiescent point (i.e. I_C, V_{CE}) of the BJT must not change a lot with temperature variation, to ensure that the performance of the active circuit is not affected by temperature variation. In this sense, active bias is the most stable, followed by Emitter bias and voltage feedback bias.
- Compensation for temperature variation using diode in Emitter bias is available, for instance see Millman & Halkias [5].
- Stability against parameters variation of the BJT. Again active bias and emitter feedback bias are less susceptible, followed by base feedback bias and collector feedback bias. See Milman & Halkias [5] for analysis.

FET Amplifier Biasing

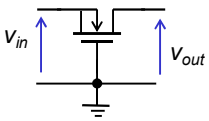
- Due to time constraint we will not focus on field-effect transistor (FET).
- However it needs to be mentioned that the FET amplifier can also be classified into Common-Source (CS), Common-Gate (CG) and Common-Drain (CD).
- The DC biasing circuit discussed can also be modified to accommodate FET based active device. Again for RF/microwave circuits typically N-channel device is used.



Common-Source (CS)



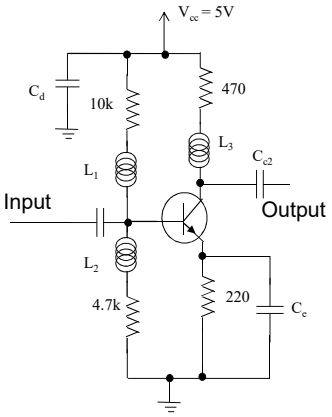
Common-Drain (CD)



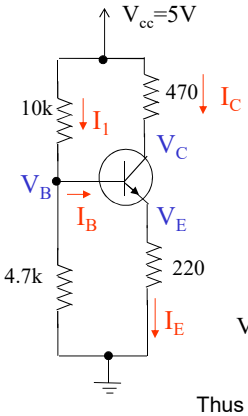
Common-Gate (CG)

Example 2.1 - BJT Amplifier Biasing and Small-Signal Equivalent Circuit

- Determine the quiescent point (Q) of the transistor and its D.C. stability. Given $h_{FE(min)}$=100, $h_{FE(max)}$= 200.
- Derive the approximate small-signal equivalent circuit of the following amplifier schematic. Use hybrid pi model for the BJT. Given V_A=74.03V, C_{jc}=3.638pF, C_{je}=4.493pF, $r_{b'b}$=10, h_{fe}=300, V_{jc}=0.75, m=0.3085, τ_F = 301.2pS.
- If the circuit is going to be used at 430MHz, suggest suitable values for C_{c1}, C_{c2}, C_e and the required RF choke inductance.
- Finally suggest suitable value for C_d.



Example 2.1 Solution



(1) DC Analysis:

Assuming h_{FE} is large, $I_1 >> I_B$. $V_B \cong \frac{4.7}{4.7+10} \cdot 5 = 1.60V$

Assuming transistor is in active region, $V_{BE} = 0.6V$. $V_E = V_B - 0.6 = 1.00V$

Using Ohm's Law: $I_E = \frac{V_E}{220} = 4.545mA$

V_{CE} and I_C constitute the Q point

Assuming h_{FE} is large, $I_C >> I_B$. $I_E = I_C + I_B \cong I_C$

$\Rightarrow I_C \cong 4.545mA$

Using Kirchoff's Voltage Law: $V_C = V_{cc} - 470 \cdot I_C = 2.864V$

Verify that transistor is under Active Region:

$V_{BC} = V_B - V_C = 1.6 - 2.864 = -1.264V$

Thus BC junction is reverse biased. And in previous slide it has been shown that BE junction is forward biased, so the transistor is biased in Active Region, the circuit is destined for Class A operation.

Example 2.1 Solution Cont…

(2) D.c. biasing stability analysis (Stability Factor)
(see derivation in Chapter 9 of Millman & Halkias [5]):

$$\frac{\partial I_c}{\partial I_{co}} = (1+h_{FE})\frac{1+R_b/R_e}{1+h_{FE}+R_b/R_e} = (1+150)\frac{1+3197}{1+150+3197} = 14.17$$

$$R_b = \frac{R_{b1}R_{b2}}{R_{b1}+R_{b2}} \cong 3197 \quad , \text{use } h_{FE} = \frac{1}{2}\left(h_{FE(\max)} + h_{FE(\min)}\right) = 150$$

Variation of I_c when I_{co} changes

$$\frac{\partial I_c}{\partial V_{BE}} = \frac{-h_{FE}/R_e}{1+h_{FE}+R_b/R_e} = \frac{-150/220}{1+150+3197} = -0.0042$$

Variation of I_c when V_{BE} changes due to temperature change

$$\frac{\partial I_c}{\partial h_{FE}} \cong \frac{\left(I_c|_{h_{FE}=h_{FE(\min)}}\right)\cdot\left(\frac{\partial I_c}{\partial I_{co}}\Big|_{h_{FE}=h_{FE(\max)}}\right)}{h_{FE(\min)}\left(1+h_{FE(\max)}\right)} \cong \frac{0.00454\cdot 14.486}{100(1+200)} = 3.272\times 10^{-6}$$

Variation of I_c due to device parameter variation

Example 2.1 Solution Cont…

(3) Deriving small-signal Hybrid-Pi model parameters:

$$g_m \cong \frac{I_C}{26} = \frac{4.545}{26} = 0.1748\Omega^{-1}$$

$$r_{b'e} = \frac{h_{fe}}{g_m} = 1.682k\Omega$$

$$r_{ce} = \frac{V_A}{I_C} = 16.288k\Omega$$

$$r_{b'c} = h_{fe}r_{ce} = 4.886\,\text{M}\Omega$$ ← Can be ignored, considered open circuit

Example 2.1 Solution Cont…

Since BE junction is forward biased:

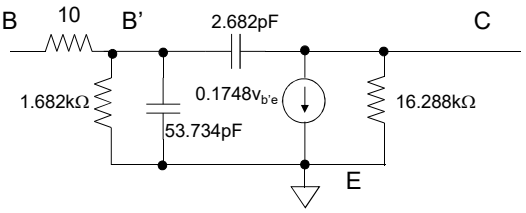
$$C_E = C_{DE} + C_{TE} \cong C_{DE}$$

$$\Rightarrow \; C_E \cong \tau_F \; g_m = 53.734 pF$$

Since BC junction is reverse biased:

$$C_C = C_{DC} + C_{TC} \cong C_{TC} = \frac{C_{jc}}{\left(1 - \frac{V_{BC}}{V_{jc}}\right)^m} = \frac{3.638\times10^{-12}}{\left(1 - \frac{-1.264}{0.75}\right)^{0.3085}} = 2.682 pF$$

The small-signal equivalent circuit:



Example 2.1 Solution Cont…

(4) Finding the values of coupling capacitors, bypass capacitor and RF choke.

Typically, values of L_1, L_2 and L_3 should be chosen such that the reactance of the inductors is greater than 1000 at the operating frequency. The values C_{c1}, C_{c2} and C_e are chosen such that the reactance of the capacitors is less than 1 at the operating frequency. Care must be taken to ensure that the actual component self-resonance frequency be at least 50% higher than the operating frequency.

$$|Z_L| = 2\pi f L > 1000$$

$$\Rightarrow L > \frac{1000}{2\pi\left(430\times10^6\right)} = 370.128 nH$$

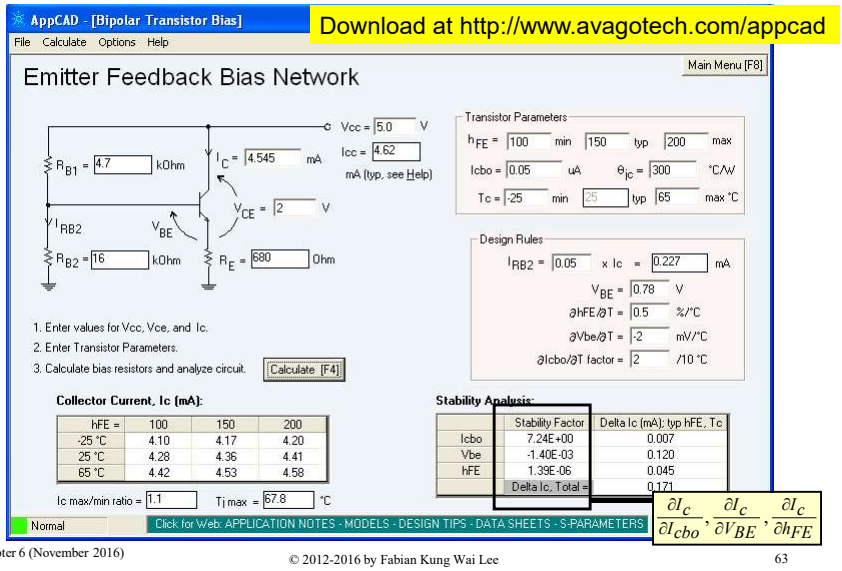
$$|Z_C| = \frac{1}{2\pi f C} < 1$$

$$\Rightarrow C > \frac{1}{2\pi\left(430\times10^6\right)} = 370.128 pF$$

• Thus we can use 390nH (standard value) for L_1, L_2 and L_3. Make sure that the self-resonance frequency and Q-factor of the chosen practical inductor is sufficient for this purpose.

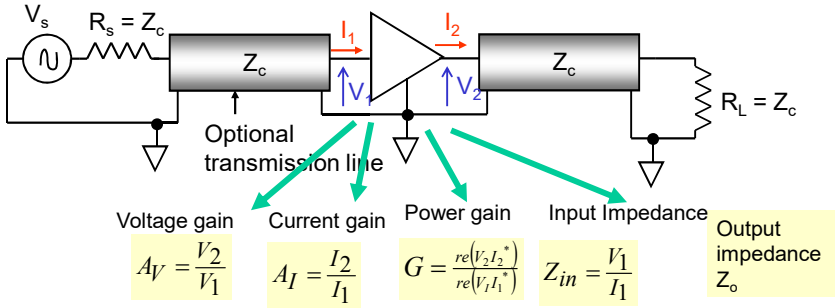
• Similarly 390pF is chosen for C_{c1}, C_{c2} and C_e.

D.C. Biasing Design with AppCAD



Characterizing the Frequency Response of the Basic Amplifier Circuit

- We would like to find out how the circuit will behave if a sinusoidal voltage of certain frequency is injected into it's input.
- It is reasonable to expect that the amplifier circuit to behave differently at different frequencies.
- Of interest is the ratio of the various voltages and currents on the terminals of the basic amplifier circuit, i.e. the classical parameters.



Summary of Amplifier Parameters Based on Configurations

- The voltage gain, current gain, input and output impedance of CE, CC and CB transistor amplifier configurations are summarized here ([4], [5]), similar conclusions can be derived for FET based amplifiers.

Amplifier configuration	Voltage Gain	Current Gain	Input Impedance	Output Impedance	Phase Output/Input Voltage	Linearity
CE	High	High	Moderately high	Moderately low	180°	Moderate
CC	≅ 1	High	High	Low	0°	Moderate
CB	High	≅ 1	Low	High	0°	High

- Each configuration has it uses, for instance CE type amplifier is usually used for general purpose amplifier. CC is good for buffer or isolation. CB is typically used in multi-stage amplifiers and oscillators, and for low-frequency operation, CB can be used as current source for its high output impedance.

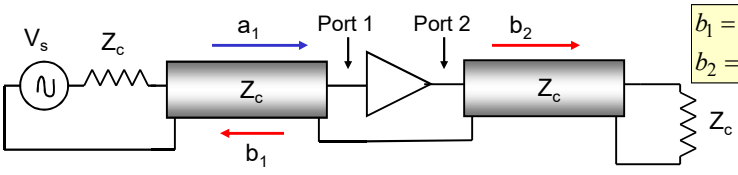
Two-Stage Amplifiers

- Here we only focus on single-stage amplifier.
- However we would like to mention that two-stages amplifiers are also very important, as they can combine the individual benefits of single-stage amplifiers.
- Example of popular two-stages amplifiers are CE-CB (cascade, for high linearity and high voltage gain), CC-CC (Darlington pair), CE-CE (for high power gain), CE-CC (to drive high current load or power gain).
- The FET equivalent will be CS-CG, CD-CD, CS-CS and CS-CD.

Characterizing the Frequency Response of the Amplifier Circuit at RF/Microwave Band

- For amplifier operating at RF and microwave frequencies, a more convenient set of parameters are the S-parameters.
- The amplifier is considered as a 2-port network, and the S-parameters s_{11}, s_{12}, s_{21} and s_{22} can be measured or derived. Bear in mind here that we assume the amplifier to be linear or small-signal.
- S-parameters can be reliably measured at RF and microwave frequencies using instrument called **Vector Network Analyzer** or derived from linear circuit analysis.
- Instead of dealing with absolute voltage and current phasors, S-parameters deal with the ratio of incident and reflected waves. This is based on the fact that high frequency amplifier can be connected to transmission lines/waveguides at both its terminals. Of course in the extreme case the transmission line can be so short that it vanishes.
- The next slide shows how S-parameters are obtained. For more information please refer to the notes of RF Circuit Design – Passive Circuit.

Measurement of S-parameter for 2-port Networks

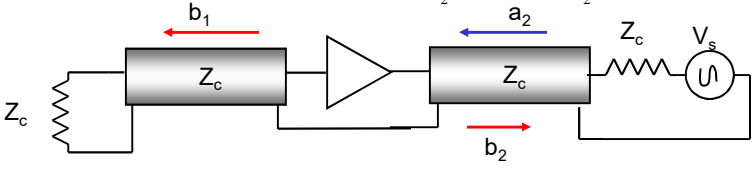


$$b_1 = S_{11}a_1 + S_{12}a_2$$
$$b_2 = S_{21}a_1 + S_{22}a_2$$

$$a_1 = \frac{V_1^+}{\sqrt{Z_c}} = I_1^+\sqrt{Z_c}$$
$$a_2 = \frac{V_2^+}{\sqrt{Z_c}} = I_2^+\sqrt{Z_c}$$
$$b_1 = \frac{V_1^-}{\sqrt{Z_c}} = I_1^-\sqrt{Z_c}$$
$$b_2 = \frac{V_2^-}{\sqrt{Z_c}} = I_2^-\sqrt{Z_c}$$

Measurement of s_{11} and s_{21}:

$$s_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \qquad s_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0}$$



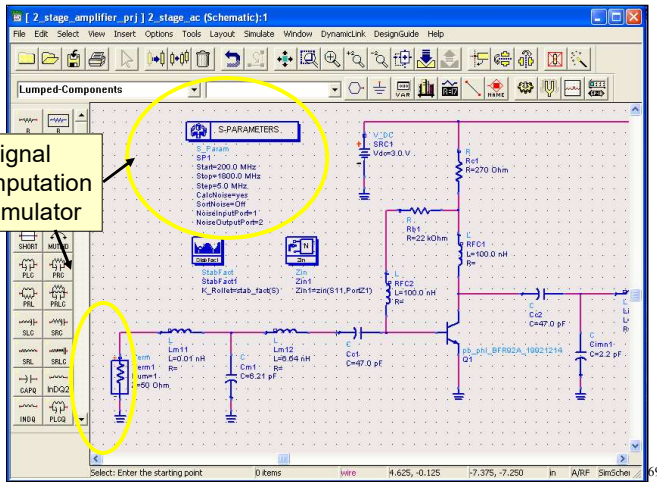
Measurement of s_{22} and s_{12}:

$$s_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \qquad s_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}$$

Example 2.2 – Computing S-Parameters from Circuit Simulator

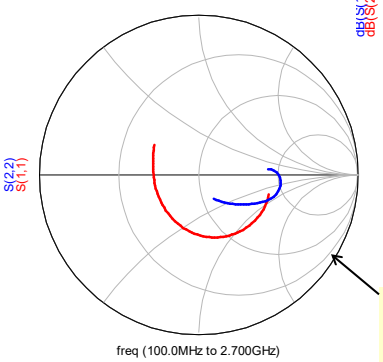
Extra

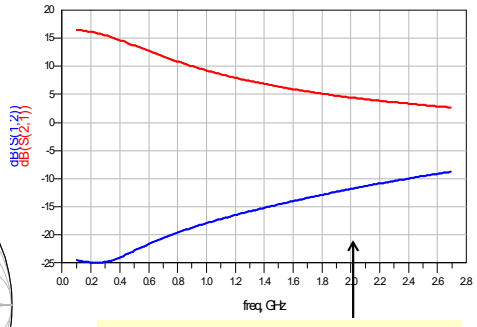
- Here is a screen shot of the schematic drawn using Agilent's Advanced Design System (ADS) software.



Example 2.2 Cont…

Note that S-parameters, like voltage and current phasor, are complex values.





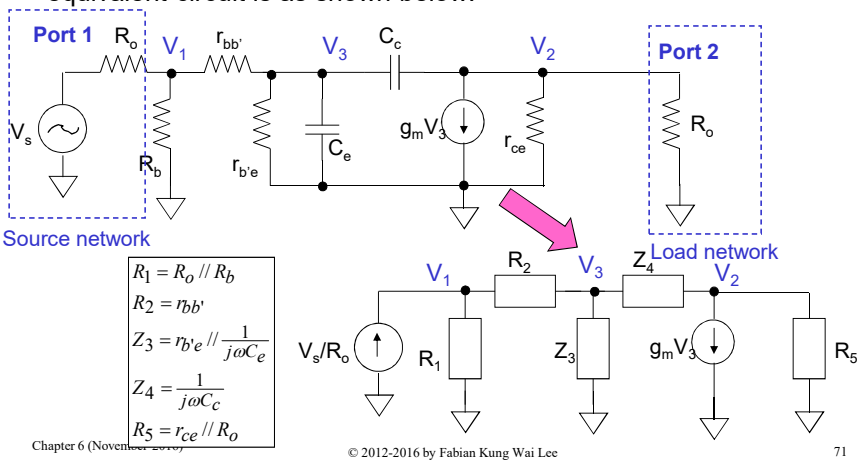
Magnitude of S_{21} and S_{12} (in dB) versus frequency, plotted on XY chart.

Complex values of S_{11} and S_{22} versus frequency, plotted on Smith Chart

Example 2.3 – Obtaining Small-Signal S-Parameters for BJT Amplifier Analytically

Extra

- Consider the circuit of Example 2.1 being terminated with source and load impedance of R_o. Ignoring the package parasitic, the small-signal equivalent circuit is as shown below.



$R_1 = R_o \,//\, R_b$

$R_2 = r_{bb'}$

$Z_3 = r_{b'e} \,//\, \frac{1}{j\omega C_e}$

$Z_4 = \frac{1}{j\omega C_c}$

$R_5 = r_{ce} \,//\, R_o$

Example 2.3 Solution

Extra

Using Nodal Analysis…

Node 1: $\frac{V_1 - V_3}{R_2} + \frac{V_1}{R_1} = \frac{V_s}{R_o}$

$\Rightarrow V_1(G_1 + G_2) - G_2 V_3 = I_s$ (1)

Let $G_2 = \frac{1}{R_2}, G_1 = \frac{1}{R_1}, Y_3 = \frac{1}{Z_3}, G_5 = \frac{1}{R_5}, I_s = \frac{V_s}{R_o}$

Node 3: $G_2(V_3 - V_1) + Y_4(V_3 - V_2) + Y_3 V_3 = 0$

$\Rightarrow -G_2 V_1 - Y_4 V_2 + (G_2 + Y_3) V_3 = 0$ (2)

Node 2: $Y_4(V_2 - V_3) + g_m V_3 + G_5 V_2 = 0$

$\Rightarrow (Y_4 + G_5) V_2 + (g_m - Y_4) V_3 = 0$ (3)

From (1): $V_1 = \frac{I_s + G_2 V_3}{G_1 + G_2}$ (4)

From (2): $V_2 = \frac{Y_4 - g_m}{Y_4 + G_5} V_3$ (5)

Example 2.3 Solution Cont…

Extra

Putting (4) & (5) into (2): $-G_2\left(\frac{I_s+G_2V_3}{G_1+G_2}\right)-Y_4\left(\frac{Y_4-g_m}{Y_4+G_5}\right)V_3+(G_2+Y_3)V_3=0$

$$\Rightarrow V_3=\frac{\frac{G_2I_s}{G_1+G_2}}{G_2+Y_3-\left(\frac{{G_2}^2}{G_1+G_2}\right)-\left(\frac{{Y_4}^2-Y_4g_m}{Y_4+G_5}\right)} \qquad (6)$$

Using (4):

$$V_1=\frac{I_s}{G_1+G_2}\left[\frac{\frac{G_2}{G_1+G_2}\cdot G_2}{G_2+Y_3-\left(\frac{{G_2}^2}{G_1+G_2}\right)-\left(\frac{{Y_4}^2+Y_4g_m}{Y_4+G_5}\right)}\right]$$

$$\Rightarrow V_1=\frac{V_s}{R_o(G_1+G_2)}\left[1+\frac{{G_2}^2}{G_1G_2+G_1Y_3+G_2Y_3-Y_4(G_1+G_2)\left(\frac{Y_4-g_m}{Y_4+G_5}\right)}\right] \qquad (7)$$

Using (5):

$$V_2=\left(\frac{Y_4-g_m}{Y_4+G_5}\right)\frac{G_2V_s}{R_o\left[G_1G_2+G_1Y_3+G_2Y_3-Y_4(G_1+G_2)\left(\frac{Y_4-g_m}{Y_4+G_5}\right)\right]} \qquad (8)$$

Example 2.3 Solution Cont…

Extra

$$I_1=\frac{V_S-V_1}{R_o} \qquad (9)$$

$$I_2=\frac{-V_2}{R_o} \qquad (10)$$

Using the relationship between port voltage, current and the normalized voltage waves in S-parameter theory (see Chapter 2):

$a_1=\frac{1}{2\sqrt{R_o}}(V_1+R_oI_1)=\frac{1}{2\sqrt{R_o}}V_s$ ← From (9)

$b_1=\frac{1}{2\sqrt{R_o}}(V_1-R_oI_1)=\frac{1}{2\sqrt{R_o}}(2V_1-V_s)$ ↙

$b_2=\frac{1}{2\sqrt{R_o}}(V_2-R_oI_2)=\frac{1}{2\sqrt{R_o}}(2V_2)=\frac{V_2}{\sqrt{R_o}}$

$a_2=0$

Example 2.3 Solution Cont…

Extra

Hence:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} = \frac{2V_1 - V_s}{V_s} = 2\frac{V_1}{V_s} - 1$$

$$\Rightarrow S_{11} = \left(\frac{2}{R_o(G_1+G_2)}\right)\left(1 + \frac{{G_2}^2}{G_1G_2 + G_1Y_3 + G_2Y_3 - Y_4(G_1+G_2)\left(\frac{Y_4 - g_m}{Y_4+G_5}\right)}\right) - 1$$

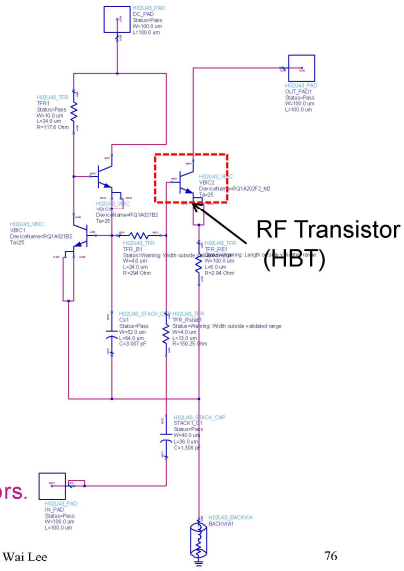
$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} = \frac{2V_2}{V_s}$$

$$\Rightarrow S_{21} = \left(\frac{Y_4 - g_m}{Y_4+G_5}\right)\left(\frac{2G_2}{R_o\left(G_1G_2 + G_1Y_3 + G_2Y_3 - Y_4(G_1+G_2)\left(\frac{Y_4 - g_m}{Y_4+G_5}\right)\right)}\right)$$

By injecting the source at output we can obtain expression for s_{22} and s_{12}. This is the procedure used by most CAD tools to obtain S-parameters for linear circuits.

Example 2.4 – A Transistor Biasing Circuit in Integrated Circuit (IC)

- Here is an example of a active biasing for a power amplifier circuit. The transistor on the right is a RF power transistor. This is an example of active biasing using a Current Mirror [4].



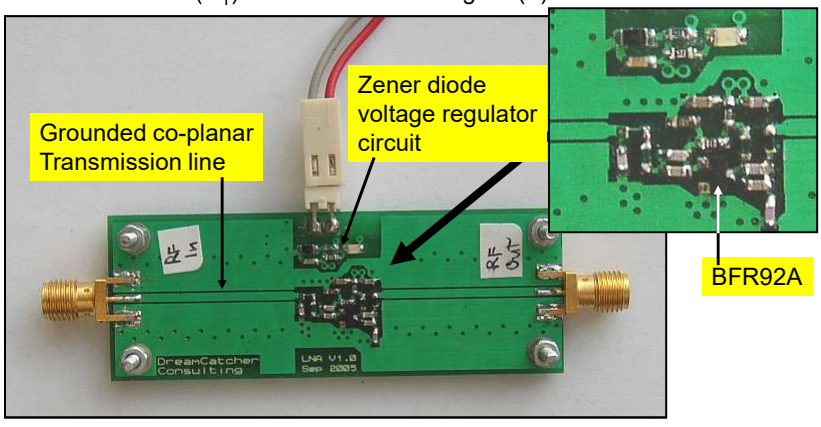
Class-A/AB Single power cell unit block:
1 power HBT (2umx20um emitter, 2 fingers)
using TFR resistors with Stack coupling capacitors.

Appendix 1
Some Do-It-Yourself (DIY) Active RF Circuits

UHF Low-Noise Amplifier

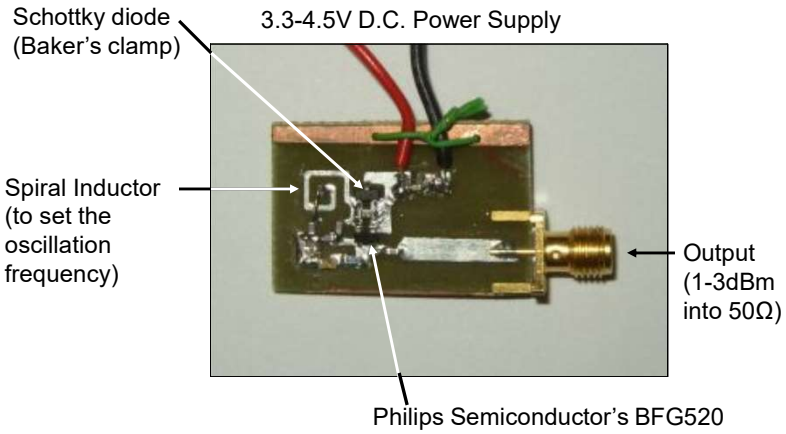
Extra

Supply: 3.0-4.0V
Bandwidth: 850-910 MHz
Transducer Power Gain (G_T): 11-12 dB Noise Figure (F): < 1.45



L-Band (1.8 GHz) Fixed Frequency Oscillator

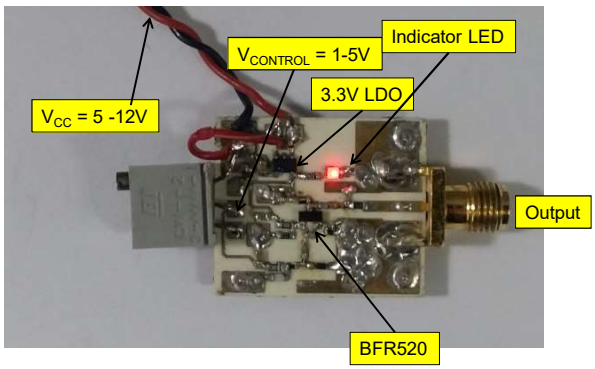
Extra



2.2-2.6 GHz Microwave Voltage-Controlled Oscillator (VCO)

Extra

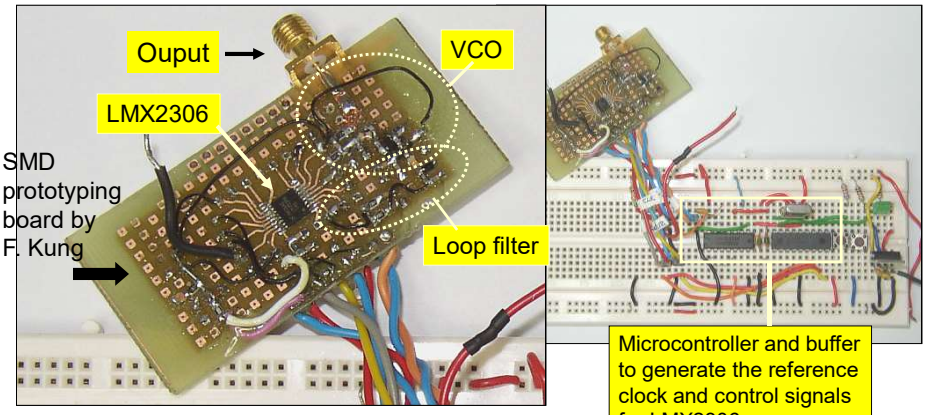
- Example of microwave oscillator prototype, built on 0.8 mm thick Rogers 4350 substrate with top and bottom side copper.



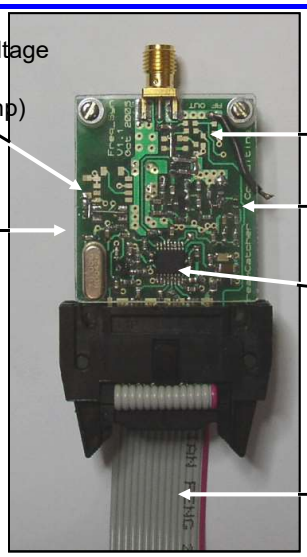
400 to 550 MHz UHF Frequency Synthesizer Prototype

Extra

This is a low-cost frequency synthesizer using a digital phase-locked loop PLL integrated circuit from National Semiconductor, LMX2306 (now obsoleted). The voltage controlled oscillator (VCO) is designed using techniques presented in this course.

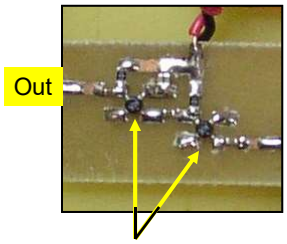


810 to 930 MHz UHF Frequency Synthesizer



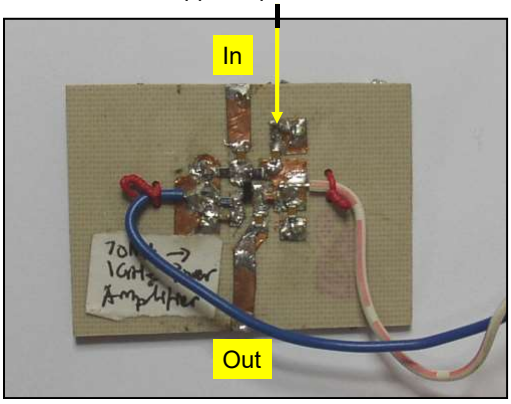
MMIC Amplifier and SMT Prototyping of RF Circuits

2-stage wideband amplifier



MMIC Amplifier

3M™ Copper tape



RF amplifier