AXI Timer documentation (AT)

I/Os

Signal Name	I/O	Initial State	Description
ap_clk(s00_axi_aclk)	I	NA	AXI Clock
ap_rst_n (s00_axi_aresetn)	I	NA	AXI Reset, active-Low
s_axi_control* (s00_axi*)	NA	NA	AXI4-Lite Slave Interface signals
interrupt	O	0x0	Indicates that the condition for an interrupt on this timer has occurred. (timer rolled over) 0 = No interrupt has occurred 1 = Interrupt has occurred
o_t0_out	O	0x0	Timer generated blinking for led (timer rolled over condition toggles signal)

Register space

Adress Offset	Register Name	Description
0x00	GCSR	General/Global Control and Status Register
0x04	GIER	Global Interrupt Enable Register
0x08	IPIER	IP Interrupt Enable Regsiter
0x0C	IPISR	IP Interrupt Status Regsiter (Interrupt Pending)
0x10	IDR	ID Register
0x14	VERR	Version Register
0x18	SCSR0	Special Control and Status Register
0x1C	CR0	Counter Register
0x20	LR0	Load Register
0x24	reserved	reserved

Register description (MSB bit31 LSB bit0)

0x00 GCSR

Bit	Name	Access Type	Reset Value	Description
0	ap_start	R/W	0	Asserted when the kernel can start processing data. Cleared on handshake with ap_done being asserted.
1	ap_done	R	0	Asserted when the kernel has completed operation. Cleared on read.
2	ap_idle	R	0	Asserted when the kernel is idle.
3	*reserved (ap_ready)*	R	0	Asserted by the kernel when it is ready to accept the new data (used only by AP_CTRL_CHAIN))
4	*reserved (ap_continue)*	R/W	0	Asserted by the XRT to allow kernel keep running (used only by AP_CTRL_CHAIN)
5:6	reserved			
7	auto_restart	R/W	0	Used to enable automatic kernel restart This bit determines whether the counter reloads the load register value and continues running or holds at the termination value.

				0 = Hold counter 1 = Reload load regitser value
31:8	reserved			

0x04 GIER

Bit	Name	Access Type	Reset Value	Description
0	gie	R/W	0	When asserted, along with the IP Interrupt Enable bit, the interrupt is enabled.
31:1	reserved			

0x08 IPIER

Bit	Name	Access Type	Reset Value	Description
0	ipie	R/W	0	When asserted, along with the Global Interrupt Enable bit, the interrupt is enabled. (default: uses the internal ap_done signal to trigger an interrupt)
31:1	reserved			

0x0C IPISR

Bit	Name	Access Type	Reset Value	Description
0	ipis	R/W	0	Toggle on write. (write 1 to clear(W1C))
31:1	reserved			

0x10 IDR

Bit	Name	Access Type	Reset Value	Description
31:0	ID	R	0x8001DEEF	Distinct ID

0x14 VERR

Bit	Name	Access Type	Reset Value	Description
31:0	VER	R	0x80001000	Version

0x18 SCSR0

Bit	Name	Access Type	Reset Value	Description
0	reserved (ENALL)	R/W	0	ap_start is used Enable All Timers 0 = No effect on timers 1 = Enable all timers (counters run) This bit is mirrored in all control/status registers and is used to enable all counters simultaneously. Writing a 1 to this bit sets ENALL, EN0, and EN1. Writing a 0 to this register clears ENALL but has no effect on EN0 and EN1.
1	reserved (en0)	R/W	0	ap_start is used Enable Timer 0 0 = Disable timer (counter halts) 1 = Enable timer (counter runs)
2	ent0_out	R/W	0	Enable external pin t0_out

				0 = Disable 1 = Enable
3	reserved			
4	load0	R/W	0	Load Timer 0 0 = No load 1 = Loads timer with value in LR0 Setting this bit loads counter register (CR0) with a specified value in the load register (LR0). This bit prevents the running of the timer/counter; hence, this should be cleared alongside setting Enable Timer/ Counter (EN0) bit.
5	ud0	R/W	0	Up/Down Count Timer 0 0 = Timer functions as up counter 1 = Timer functions as down counter
6	reserved			
7	reserevd			
8	reset_ip	R/W	0	Stops the whole IP and resets all values
9	freeze_ip	R/W	0	Stops the whole IP but does not reset the values (useful for debugging)
10	reserved			
11	reserved			
31:12	reserved			

0x1C CR0

Bit	Name	Access Type	Reset Value	Description
31:0	CR0	R	0x0	Counter Register 0

0x20 LR0

Bit	Name	Access Type	Reset Value	Description
31:0	LR0	R/W	0x0	Load Register 0