1. Overview

Figure 1: LCD Module

Features
-16×2 character LCD with parallel interface
- 192 predefined characters including 93 ASCII characters
- Up to 8 user-definable characters
- Read and write capability to and from the display
- Small PCB size for flexible designs 2.3“ × 3.3” (5.8 cm × 8.4 cm)

a) Module Pinout

Header J1 - Top Half		
Pin	Signal	Description
1	DB0	Data Bit 0
2	DB1	Data Bit 1
3	DB2	Data Bit 2
4	DB3	Data Bit 3
5	GND	Power Supply Ground
6	VCC	Positive Power Supply[1]

Header J1 - Bottom Half		
Pin	Signal	Description
7	DB4	Data Bit 4
8	DB5	Data Bit 5
9	DB6	Data Bit 6
10	DB7	Data Bit 7
11	GND	Power Supply Ground
12	VCC	Positive Power Supply[1]

Header J2		
Pin	Signal	Description
1	RS	Register Select: High for Data Transfer, Low for Instruction Transfer
2	R/W	Read/Write signal: High for Read mode, Low for Write mode
3	E	Read/Write Enable: High for Read, falling edge writes data
4	NC	Optional back-light enable (not connected on the PmodCLP
5	GND	Power Supply Ground
6	VCC	Positive Power Supply

Figure 2: LCD Module pinout

Note: 1. VCC: For Revision A of the Module this must be at 5V. For Revision B, this must be at 3.3V

b) Functional Overview and Working principle

The LCD controller contains a character-generator ROM (CGROM) with 192 preset 5×8 character patterns (see table below), a character-generator RAM (CGRAM) that can hold 8 user-defined 5×8 characters, and a display data RAM (DDRAM) that can hold 80 character codes.
Character codes written into the DDRAM serve as indexes into the CGROM (or CGRAM). Writing a character code into a particular DDRAM location will cause the associated character to appear at the corresponding display location. The write-only IR directs display operations (such as clear display, set DDRAM address, etc).
The display has more DDRAM locations than can be displayed at any given time. DDRAM locations 00H to 27H map to the first display row, and locations 40H to 67H map to the second row. Figure 3 shows the default address for the 32 character locations on the display. The
upper line of 16 characters is stored between addresses 0x00 and 0x0F. The second line of 16 characters is stored between addresses 0x40 and 0x4F.

	Character Display Addresses																Undisplayed Addresses		
1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	…	27
2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	…	67
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	...	40

*Figure 3: Association Display Positions and Lines (**BOLD**) to DDRAM Hexadecimal Addresses (normal)*

Address register contents, set via the Instruction Register, can be automatically incremented after each read or write operation. The LCD display uses ASCII character codes. Codes up through 7F are standard ASCII (which includes all “normal” alphanumeric characters). Codes above 7F produce various international characters (see Figure 4) (see also Section 3 for details).

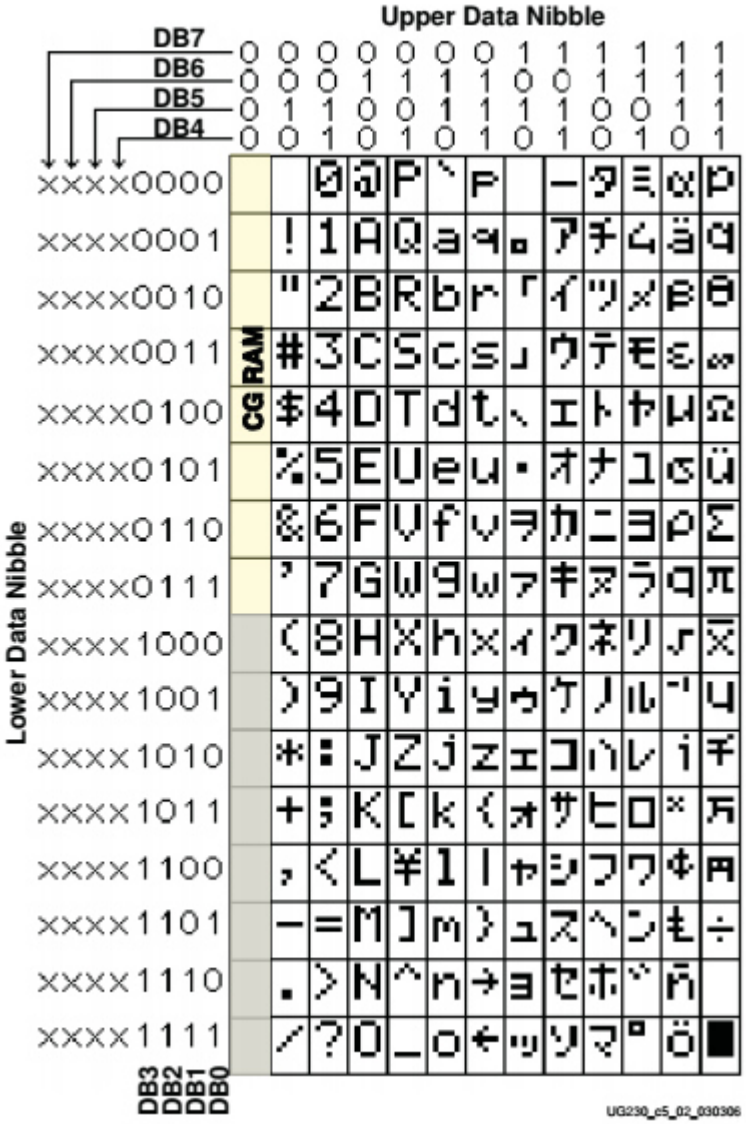

Figure 4: DDRAM DATA: Supported characters

2. Interfacing the Display

The display communicates with the host board via a parallel protocol. The LCD chip supports two modes (4-bit or nibble data mode and 8-bit data mode). In basic 4-bit operation mode, each 8-bit command is sent as two 4-bit nibbles on DB3-DB0. The upper nibble is transferred first, followed by the lower nibble.
Apart of the data signals, three additional control signals RS, R/W and E are used in basic operation. The protocol requires specific timings.

a) Commands

Figure 5 summarizes the available LCD controller commands and bit definitions.

Instruction	Instruction bit assignments										Description
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear display by writing a 20H to all DDRAM locations; set DDRAM address register to 00H; and return cursor to home.
Return Home	0	0	0	0	0	0	0	0	1	X	Return cursor to home (upper left corner), and set DDRAM address to 0H. DDRAM contents not changed.
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	I/D = '1' for right-moving cursor and address increment; SH = '1' for display shift (direction set by I/D bit).
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking cursor (B) on or off.
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	X	X	S/C = '0' to shift cursor right or left, '1' to shift entire display right or left (R/L = '1' for right).
Function Set	0	0	0	0	1	DL	N	F	X	X	Set interface data length DL ('1' for 8 bit), number of display lines N ('1' for 2 lines), font F ('0' for 5×8 dots)
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address counter AC5 - AC0
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address counter AC5 - AC0
Read busy flag/address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read busy flag (BF) and address counter AC6-AC0
Write data toRAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into DDRAM or CGRAM, depending on which address was last set
Read data toRAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data into DDRAM or CGRAM, depending on which address was last set

Figure 5: LCD Character Display Command Set

b) Timing Considerations

8-bit mode

When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7.

4-bit mode (nibble mode)

When interfacing data length are 4-bit, only 4 ports, from DB4 to DB7, are used as data bus. At First, the higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7), and then the lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred (see Figure 6). So two nibble transfers are required for a command.

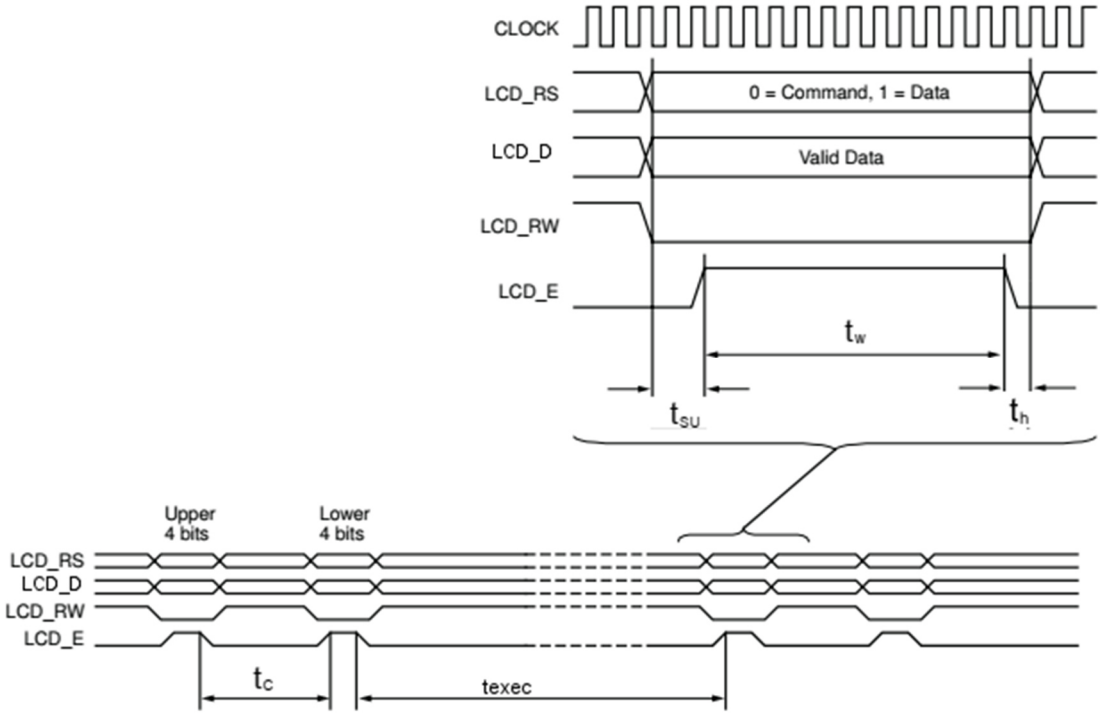

Figure 6: Bus timing Diagram (4-bit mode) for a whole 8-bit command consisting of two nibbles

i. Timing characteristics (AC characteristics)

Figure 7 presents min and max values for the definitions in the timing diagram above in dependency of the used supply voltage.

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	$t_R t_F$	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu1	60	-	-	
	R/W and RS Hold Time	t_{H1}	20	-	-	
	Data Setup Time	tsu2	195	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	t_R, t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu	60	-	-	
	R/W and RS Hold Time	t_H	20	-	-	
	Data Output Delay Time	t_D	-	-	360	
	Data Hold Time	t_{DH}	5	-	-	

Figure 7: AC Characteristics (Vdd=2.7V ~4.5V, Ta =-30~+85°C)

ii. Initialization

Before writing any command to the display controller you have to wait for 30ms after powering on. Then function set command should be written, then other set up commands can follow (Entry Mode, Display Clear, Display ON/OFF control, …)

1) Special considerations for 8-bit mode:
   The function set command is written once
2) Special considerations for 4-bit mode:
   The upper nibble (4-bit) of function set commands has to be written two times (0x2) then the lower nibble of function set is written.

iii. Execution time of commands

The Execution times (Texec) of the commands are as follows:

Instruction	Execution time (fosc=270kHz)
Clear Display	1.53 ms (1.64ms recommended for compatibility)
Return Home	1.53 ms (1.64ms recommended for compatibility)
Entry Mode Set	39 us (40us recommended for compatibility)
Display ON/ OFF Control	39 us (40us recommended for compatibility)
Cursor or Display Shift	39 us (40us recommended for compatibility)
Function Set	39 us (40us recommended for compatibility)
Set CGRAM Address	39 us (40us recommended for compatibility)
Set DDRAM Address	39 us (40us recommended for compatibility)
Read Busy Flag and Address	0 us
Write Data to RAM	39 us (40us recommended for compatibility)
Read Data from RAM	39 us (40us recommended for compatibility)

3. Details of the LCD chip

a) Functional Description

Figure 8 gives a more detailed overview of the LCD chip.

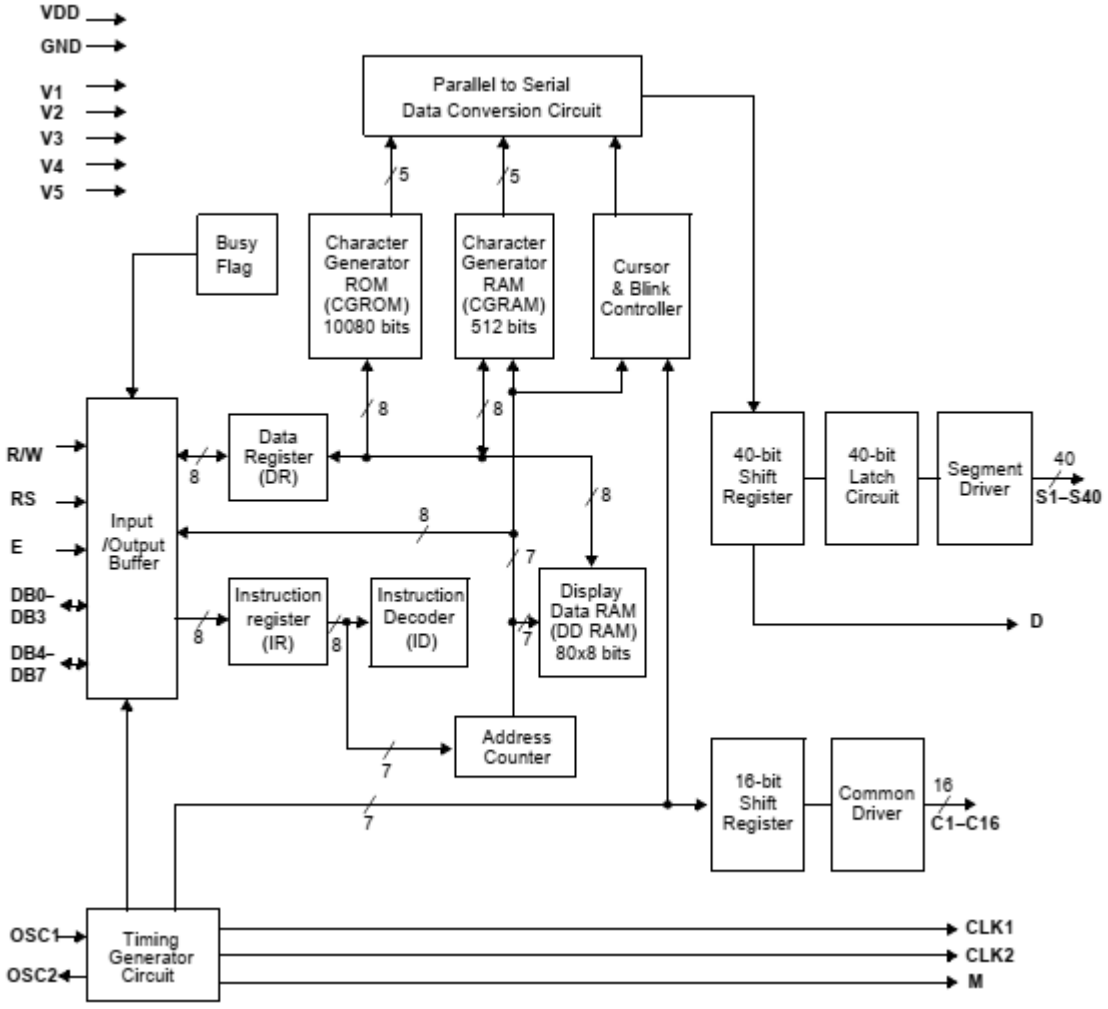

Figure 8: Block didagram of the LCD chip

System Interface

This LCD chip has both kinds of interface type: 4-bit bus and 8-bit bus for a Microprocessor Unit (MPU) to access. 4-bit bus and 8-bit bus are selected by the DL bit in the instruction register. During read or write operation, two 8-bit registers are used. One is the data register (DR), and the other is the instruction register (IR)

The data register (DR) is used as a temporary data storage place for being written into or read from DDRAM/CGRAM. The target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. Thus, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register (IR) is used only to store instruction codes transferred from MPU. MPU cannot use it to read instruction data.

To select a register, you can use RS input pin in 4-bit/8-bit bus mode.

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
L	H	Read Busy flag(DB7) and address counter (DB0 to DB6)
H	L	Data Write operation (MPU writes data into DR)
H	H	Data Read operation (MPU reads data from DR)

Figure 9: Meaning of control signals RS and R/W

Busy Flag (BF)
BF = “High”, indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read through DB7 port when RS = “Low”and R/W = “High”(Read Instruction Operation). Before executing the next instruction, be sure that BF is not “High”.

Address Counter (AC)
The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.
After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.
When RS = “Low”and R/W = “High”, AC can be read through ports DB0 to DB6.

Display Data RAM (DDRAM)
DDRAM stores display data of maximum 80x8 bits (80 characters).
DDRAM address is set in the address counter(AC) as a hexadecimal number (see Figure 3)

CGROM(Character Generator ROM)
CGROM has 192 character patterns of 5x8 dots (and 32 character patterns of 5x11 dots) (See Figure 10).

Figure 10: CGROM/CGRAM Predefined Character Table

CGRAM(Character Generator RAM)
CGRAM has up to 8 5x8 dots characters.
By writing font data to CGRAM, user defined characters can be used (See Figure 11)

Character Code (DDRAM data)								CGRAM Address						CGRAM Data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	×	0	0	0	0	0	0	0	0	0	×	×	×	0	1	1	1	0	pattern 1
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	
0	0	0	0	×	1	1	1	0	0	0	0	0	0	×	×	×	1	0	0	0	1	pattern 8
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	1	
											1	0	0				1	0	0	0	1	
											1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	

Figure 11: relationship between Character Code (DDRAM) and Charakter Pattern (CGRAM)

Timing Generation Circuit
Timing generation circuit generates clock signals for the internal operations

LCD Driver Circuit
LCD Driver circuit has 16 common and 40 segment signals for LCD driving.
Data from CGRAM/CGROM is transferred to a 40-bit segment latch serially, and then is stored to 40-bit shift latch. When each common is selected by 16-bit common register, segment data is also output through segment driver from a 40-bit segment latch. In case of 1-line display mode, COM1 to COM8 have 1/8 duty or COM1 to COM11 have 1/11 duty, and in 2-line mode, COM1 to COM16 have a 1/16 duty ratio.

Cursor/Blink Control Circuit
It controls the cursor/blink ON/OFF at cursor position.

Summarized, the LCD controller contains a character-generator ROM (CGROM) with 192 preset 5×8 character patterns (see table below), a character-generator RAM (CGRAM) that can hold 8 user-defined 5×8 characters, and a display data RAM (DDRAM) that can hold 80 character codes. Character codes written into the DDRAM serve as indexes into the CGROM (or CGRAM). Writing a character code into a particular DDRAM location will cause the associated character to appear at the corresponding display location. Display positions can be shifted left or right by setting a bit in the Instruction Register (IR). The write-only IR directs display operations (such as clear display, shift left or right, set DDRAM address, etc).
A busy flag shows whether the display has competed the last requested operation; prior to initiating a new operation, the flag can be checked to see if the previous operation has been completed.
The display has more DDRAM locations than can be displayed at any given time. DDRAM locations 00H to 27H map to the first display row, and locations 40H to 67H map to the second row. Normally, DDRAM location 00H maps to the upper left display corner (the “home” location, and 40H to the lower left). Figure 3 shows the default address for the 32 character locations on the display. The

upper line of 16 characters is stored between addresses 0x00 and 0x0F. The second line of 16 characters is stored between addresses 0x40 and 0x4F.
Shifting the display left or right can change this mapping. The display uses a temporary data register (DR) to hold data during DDRAM /CGRAM reads or writes, and an internal address register to select the RAM location. Address register contents, set via the Instruction Register, can be automatically incremented after each read or write operation. The LCD display uses ASCII character codes. Codes up through 7F are standard ASCII (which includes all “normal” alphanumeric characters). Codes above 7F produce various international characters (see Figure 4 for details).

b) Commands

Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H”(space code) to all DDRAM address, and set DDRAM address to “00H”into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on the first line of the display. Make the entry mode increment (I/D = “High”)

Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

* “-”: dont care

Return Home is cursor return home instruction. Set DDRAM address to “00H”into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.
I/D: Increment / decrement of DDRAM address (cursor or blink)
When I/D = “High”, cursor/blink moves to right and DDRAM address is increased by 1. When I/D = “Low”, cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.
SH: Shift of entire display
When DDRAM read (CGRAM read/write) operation or SH = “Low”, shifting of entire display is not performed. If SH = “High”and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = “High”: shift left, I/D = “Low”: shift right)

Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.
D: Display ON/OFF control bit
When D = “High”, entire display is turned on. When D = “Low”, display is turned off, but display data remains in DDRAM.
C: Cursor ON/OFF control bit
When C = “High”, cursor is turned on. When C = “Low”, cursor is disappeared in current display, but I/D register preserves its data.

B: Cursor Blink ON/OFF control bit
When B = “High”, cursor blink is on, which performs alternately between all the “High” data and display characters at the cursor position. When B = “Low”, blink is off.

Cursor or Display Shift Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data. This instruction is used to correct or search display data (See Figure 12). During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line. Note that display shift is performed simultaneously in all the lines. When displayed data is shifted repeatedly, each line is shifted individually. When display shift is performed, the contents of the address counter are not changed.

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

Figure 12: Shift Patterns According to S/C and R/L Signals

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL: Interface data length control bit
When DL = “High”, it means 8-bit bus mode with MPU. When DL = “Low”, it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode. When 4-bit bus mode, it needs to transfer 4-bit data twice.
N: Display line number control bit
When N = “Low”, 1-line display mode is set. When N = “High”, 2-line display mode is set.
F: Display font type control bit
When F = “Low”, 5 ´8 dots format display mode is set. When F = “High”, 5 ´11 dots format display mode.

Set CGRAM Address:

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU. When 1-line display mode (N = Low), DDRAM address is from “00H”to “4FH”. In 2-line display mode (N = High), DDRAM address in the 1st line is from “00H”to “27H”, and DDRAM address in the 2nd line is from “40H”to “67H”.

Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether the LCD chip is in internal operation or not.
If the resultant BF is “High”, internal operation is in progress and should wait until BF is to be Low, which by then the next instruction can be performed. In this instruction you can also read the value of the address counter.

c) Timing Considerations

i. General timing considerations

8-bit mode

When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7.
Example of timing sequence is shown below (see Figure 13).

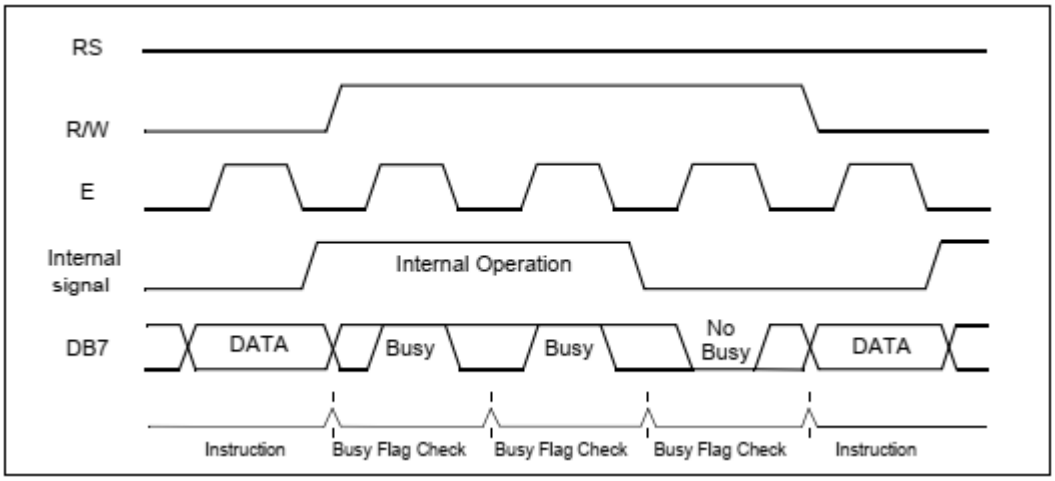

Figure 13: Bus Timing Diagramm (8-bit mode)

4-bit mode (nibble mode)

When interfacing data length are 4-bit, only 4 ports, from DB4 to DB7, are used as data bus. At First, the higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7), and then the lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred (see Figure 14). So two nibble transfers are required.

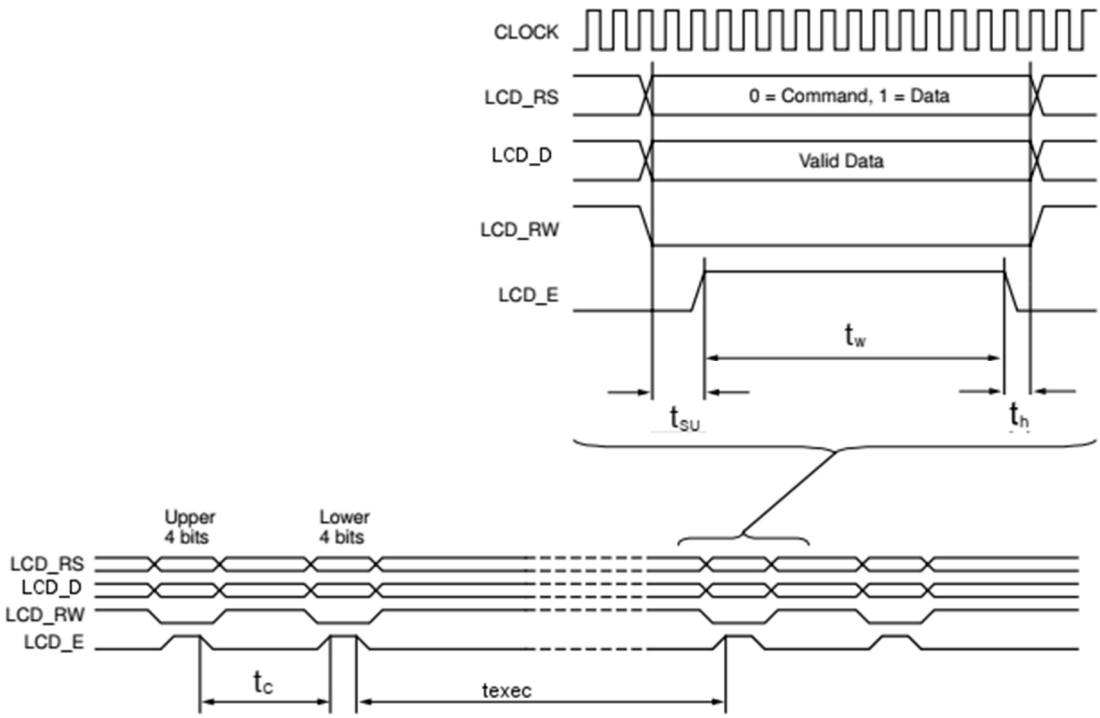

Figure 14: Bus timing Diagram (4-bit mode) for a whole 8-bit command consisting of two nibbles

Busy Flag outputs “High” after the second transfer is ended.
Example of timing sequence is shown below (See Figure 15).

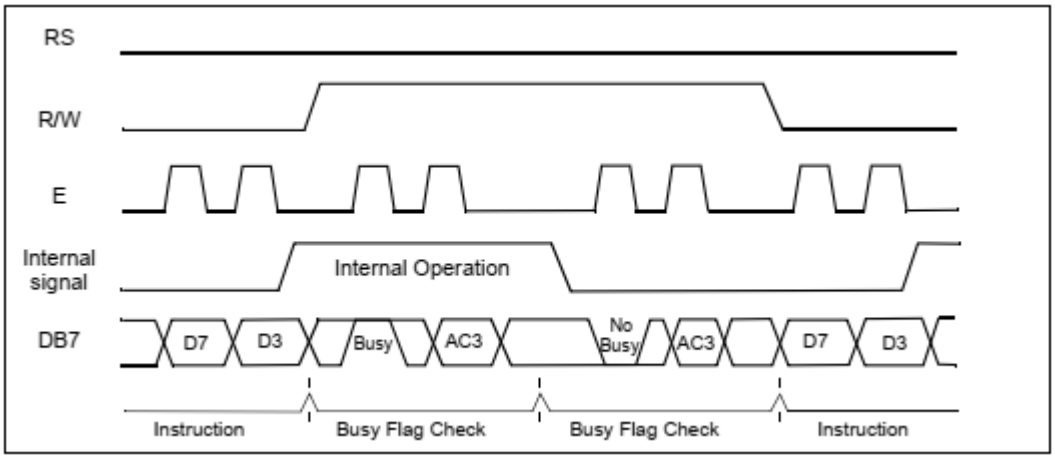

Figure 15: Bus Timing Diagramm (4-bit mode)

ii. Timing characteristics (AC characteristics)

Figure 16 and Figure 17 describe the timing diagram for write and for read commands.
Figure 18 and Figure 19 present min and max values for the definitions in the timing diagrams in dependency of the used supply voltage.

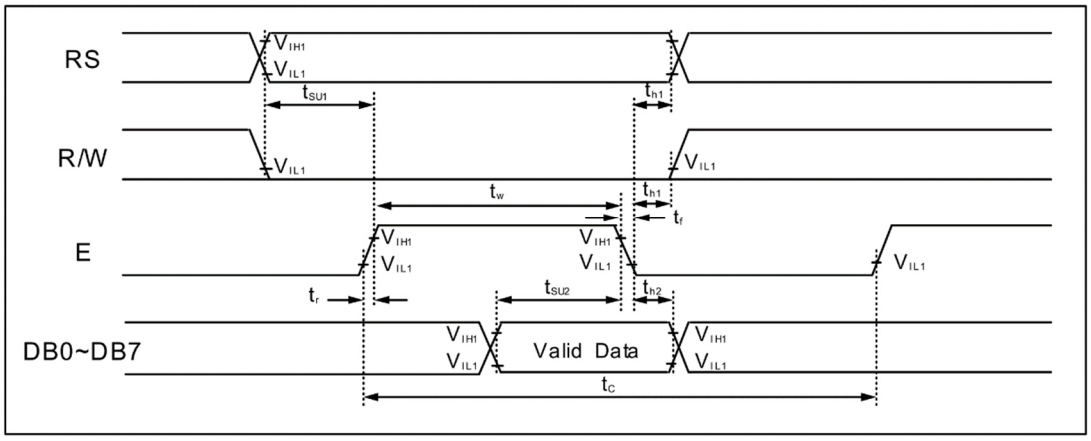

Figure 16: Timing Diagram (for write commands)

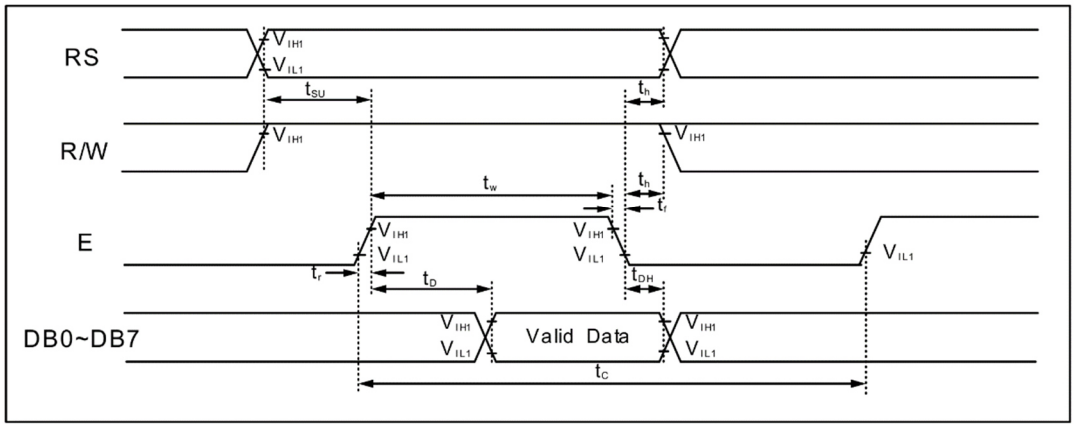

Figure 17: Timing Diagram (for read commands)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu1	40	-	-	
	R/W and RS Hold Time	t_{H1}	10	-	-	
	Data Setup Time	tsu2	80	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu	40	-	-	
	R/W and RS Hold Time	t_H	10	-	-	
	Data Output Delay Time	t_D	-	-	120	
	Data Hold Time	t_{DH}	5	-	-	

Figure 18: AC Characteristics (Vdd=4.5V ~5.5V, Ta =-30~+85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	$t_R t_F$	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu1	60	-	-	
	R/W and RS Hold Time	t_{H1}	20	-	-	
	Data Setup Time	tsu2	195	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	t_R, t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu	60	-	-	
	R/W and RS Hold Time	t_H	20	-	-	
	Data Output Delay Time	t_D	-	-	360	
	Data Hold Time	t_{DH}	5	-	-	

Figure 19: AC Characteristics (Vdd=2.7V ~4.5V, Ta =-30~+85°C)

iii. Initialization

Before writing any command to the display controller you have to wait for 30ms after powering on. Then function set command should be written, then other set up commands can follow (Entry Mode, Display Clear, Display ON/OFF control, …)

3) Special considerations for 8-bit mode:
   The function set command is written once
4) Special considerations for 4-bit mode:
   The upper nibble (4-bit) of function set commands has to be written two times (0x2) then the lower nibble of function set is written.

iv. Execution time of commands

The Execution times (Texec) of the commands are as follows:

Instruction	Execution time (fosc=270kHz)
Clear Display	1.53 ms (1.64ms recommended for compatibility)
Return Home	1.53 ms (1.64ms recommended for compatibility)
Entry Mode Set	39 us (40us recommended for compatibility)
Display ON/ OFF Control	39 us (40us recommended for compatibility)
Cursor or Display Shift	39 us (40us recommended for compatibility)
Function Set	39 us (40us recommended for compatibility)
Set CGRAM Address	39 us (40us recommended for compatibility)
Set DDRAM Address	39 us (40us recommended for compatibility)
Read Busy Flag and Address	0 us
Write Data to RAM	39 us (40us recommended for compatibility)
Read Data from RAM	39 us (40us recommended for compatibility)