## PMod Max Sonar IP – Register Mapping

### I/Os

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal Name** | **I/O** | **Initial State** | **Description** |
| ap\_clk(s00\_axi\_aclk) | I | NA | AXI Clock |
| ap\_rst\_n (s00\_axi\_aresetn) | I | NA | AXI Reset, active-Low |
| s\_axi\_control\* (s00\_axi\*) | NA | NA | AXI4-Lite Slave Interface signals |
| interrupt | O | 0x0 | Indicates that the condition for an interrupt has occurred. (new sensor reading)  0 = No interrupt has occurred  1 = Interrupt has occurred |
| rx\_in | I | NA | UART receive from sensor |
| tx\_out | O | 0x1 | UART transmit to sensor |

## Register Space

|  |  |  |
| --- | --- | --- |
| **Adress Offset** | **Register Name** | **Description** |
| 0x00 | GCSR | General/Global Control and Status Register |
| 0x04 | GIER | Global Interrupt Enable Register |
| 0x08 | IPIER | IP Interrupt Enable Register |
| 0x0C | IPISR | IP Interrupt Status Register (Interrupt Pending) |
| 0x10 | IDR | ID Register |
| 0x14 | VERR | Version Register |
| 0x18 | SCSR0 | Special Control and Status Register |
| 0x1C | DIST0 | Distance Value Register |
| 0x20 | URSR | UART Receiver Status Register |
| 0x24 | ADSR | ASCII Decoder Status Register |

## Register description (MSB bit31 LSB bit0)

##### 0x00 GCSR

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Name** | **Access Type** | **Reset Value** | **Description** |
| 0 | ap\_start | R/W | 0 | Asserted when the kernel is able to do sensor readings. Cleared on handshake with ap\_done being asserted. |
| 1 | ap\_done | R | 0 | Asserted when the kernel has completed a sensor read. Cleared on read. |
| 2 | ap\_idle | R | 0 | Asserted when the kernel is idle. |
| 3 | *reserved (ap\_ready)* | R/W | 0 | *Asserted by the kernel when it is ready to accept the new data (used only by AP\_CTRL\_CHAIN))* |
| 4 | *reserved (ap\_continue)* | R/W | 0 | *Asserted by the XRT to allow kernel keep running (used only by AP\_CTRL\_CHAIN)* |
| 5:6 | reserved |  |  |  |
| 7 | auto-restart | R/W |  | Used to enable automatic kernel restart. This bit determines whether only one sensor reading is processed or the sensor reading is continously updated.  0 = single reading  1 = free running mode |
| 31:8 | reserved |  |  |  |

##### 0x04 GIER

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Name** | **Access Type** | **Reset Value** | **Description** |
| 0 | gie | R/W | 0 | When asserted, along with the IP Interrupt Enable bit, the interrupt is enabled. |
| 31:1 | reserved |  |  |  |

##### 0x08 IPIER

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Name** | **Access Type** | **Reset Value** | **Description** |
| 0 | ipie | R/W | 0 | When asserted, along with the Global Interrupt Enable bit, the interrupt is enabled. (default: uses the internal ap\_done signal to trigger an interrupt) |
| 31:1 | reserved |  |  |  |

##### 0x0C IPISR

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Name** | **Access Type** | **Reset Value** | **Description** |
| 0 | ipis | R/W | 0 | Toggle on write. (write 1 to clear(W1C)) |
| 31:1 | reserved |  |  |  |

##### 0x10 IDR

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Name** | **Access Type** | **Reset Value** | **Description** |
| 31:0 | ID | R | 0x534F4E52 | Distinct ID (ASCII for SONR) |

##### 0x14 VERR

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Name** | **Access Type** | **Reset Value** | **Description** |
| 31:0 | VER | R | 0x80001000 | Version |

##### 0x18 SCSR0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Name** | **Access Type** | **Reset Value** | **Description** |
| 0 | powerup\_done | R | 0 | Asserted when the powerup time of the sonar sensor has passed |
| 1 | config\_done | R | 0 | Asserted when the configuration of the sonar sensor is done |
| 2 | read\_valid | R | 0 | Signals if the current values in the DIST0 Register are valid.  In single reading mode the flag is asserted when completed a sensor read without an error. When a new reading starts the flag is cleared.  In free running mode the flag is set when the first error free sensor reading was conducted. If the current sensor reading is older 100ms, the flag is cleared. |
| 5:3 | reserved |  |  |  |
| 6 | reset\_ip | R | 0 | Stops the whole IP and resets all values |
| 7 | freeze\_ip | R | 0 | Stops the whole IP but does not reset the values (useful for debugging) |
| 31:8 | reserved |  |  |  |

##### 0x1C DIST0

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Name** | **Access Type** | **Reset Value** | **Description** |
| 15:0 | dist\_cm | R | 0x0000 | Distance in cm   * 0x000F - 0x0288 * 15cm - 648cm * 0x000 no valid reading yet |
| 23:16 | dist\_in | R | 0x00 | Distance in inches   * 0x06 - 0xFF * 6in - 255in * 0x000 no valid reading yet |
| 31:24 | reserved |  |  |  |

##### 0x20 URSR

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Name** | **Access Type** | **Reset Value** | **Description** |
| 0 | ur\_error | R | 0 | Set to one, if the UART Receiver moves into the error state. Cleared on reset. |
| 7:1 | reserved |  |  |  |
| 15:8 | ur\_data | R | 0x0 | Current status of the UART Receive Buffer (for Debug Purposes) |
| 31:16 | reserved |  |  |  |

##### 0x24 ADSR

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Bit** | **Name** | **Access Type** | **Reset Value** | **Description** |
| 0 | ad\_error | R | 0 | Set, if the ASCII Decoder moves into error state (the packet structure „Rxxx\r“ violated) |
| 3:1 | reserved |  |  |  |
| 7:4 | ad\_err\_pos | R | 0x0 | One-hot bitmask of the ASCII Char which caused the error  0x1 = first number  0x2 = second number  0x4 = third number  0x8 = cariage return |
| 15:8 | ad\_err\_char | R | 0x00 | ASCII character which caused the error |