Synchronous Switch-Mode Battery Charge Controller for Solar Power With Maximum Power Point Tracking

Check for Samples: bq24650

FEATURES

- **Maximum Power Point Tracking (MPPT) Capability by Input Voltage Regulation**
- **Programmable MPPT Setting**
- **5V-28V Input Solar Panel**
- **600kHz NMOS-NMOS Synchronous Buck Controller**
- **Resistor Programmable Float Voltage**
- **Accommodates Li-Ion/Polymer, LiFePO4, Lead Acid Chemistries**
- **Accuracy**
  - **±0.5% Charge Voltage Regulation**
  - **±3% Charge Current Regulation**
  - **±0.6% Input Voltage Regulation**
- **High Integration**
  - **Internal Loop Compensation**
  - **Internal Digital Soft Start**
- **Safety**
  - **Input Over-Voltage Protection**
  - **Battery Temperature Sensing**
  - **Battery Absent Detection**
  - **Thermal Shutdown**
- **Charge Status Outputs for LED or Host Processor**
- **Charge Enable on MPPSET Pin**
- **Automatic Sleep Mode for Low Power Consumption**
  - **<15µA Off-State Battery Discharge Current**
- **Small 3.5 × 3.5 mm² QFN-16 Package**

APPLICATIONS

- **Solar Powered Applications**
- **Remote Monitoring Stations**
- **Portable Handheld Instruments**
- **12V to 24V Automotive Systems**
- **Current-Limited Power Source**

DESCRIPTION

The bq24650 is a highly integrated switch-mode battery charge controller. It provides input voltage regulation, which reduces charge current when input voltage falls below a programmed level. When the input is powered by a solar panel, the input regulation loop lowers the charge current so that the solar panel can provide maximum power output.

The bq24650 offers a constant-frequency synchronous PWM controller with high accuracy current and voltage regulation, charge preconditioning, charge termination, and charge status monitoring.

The bq24650 charges the battery in three phases: pre-conditioning, constant current, and constant voltage. Charge is terminated when the current reaches 1/10 of the fast charge rate. The pre-charge timer is fixed at 30 minutes. The bq24650 automatically restarts the charge cycle if the battery voltage falls below an internal threshold and enters a low quiescent current sleep mode when the input voltage falls below the battery voltage.

The bq24650 supports a battery from 2.1V to 26V with VFB set to a 2.1V feedback reference. The charge current is programmed by selecting an appropriate sense resistor. The bq24650 is available in a 16 pin, 3.5×3.5 mm² thin QFN package.
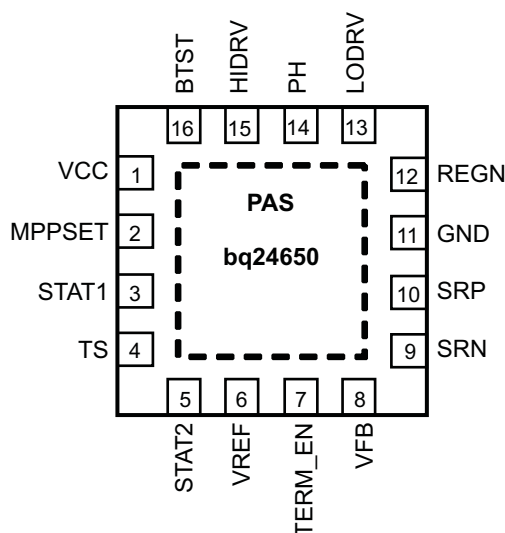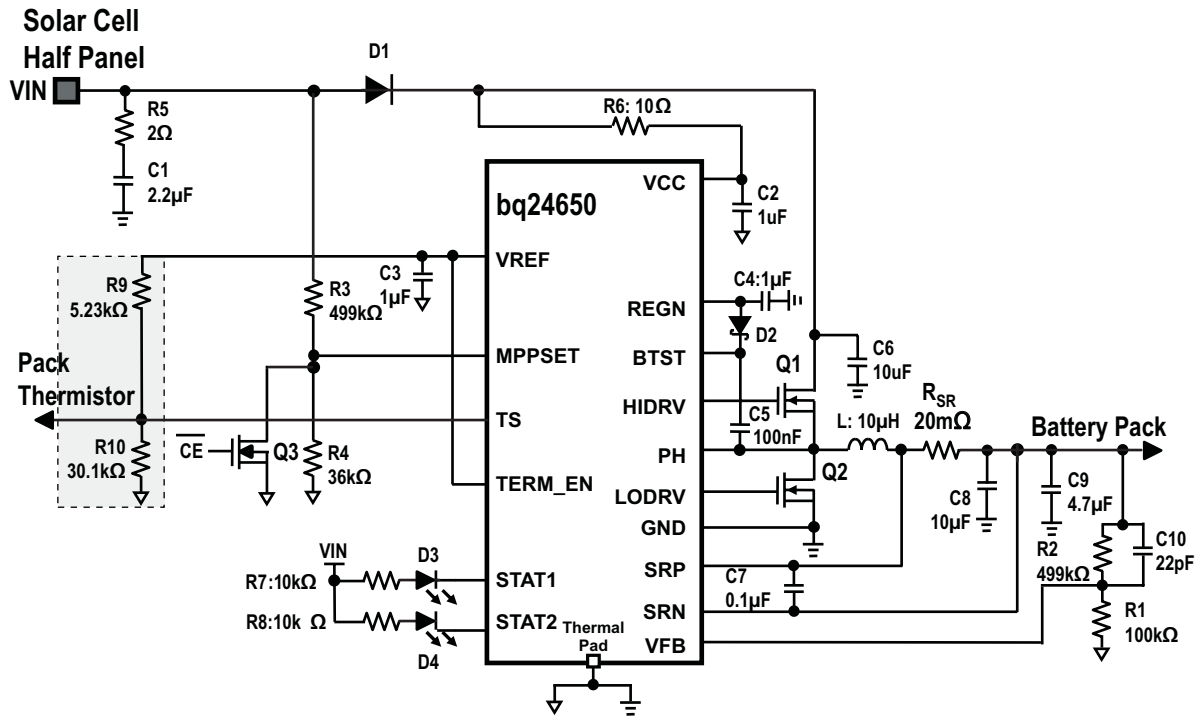
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION

Solar Panel 21 V, MPPT = 18 V, 2-cell, I_{CHARGE} = 2 A, $I_{PRECHARGE}$ = I_{TERM} = 0.2 A, TS = 0 - 45°C

Figure 1. Typical System Schematic

ORDERING INFORMATION

PART NUMBER	PACKAGE	ORDERING NUMBER (Tape and Reel)	PART MARKING	QUANTITY
bq24650	16-Pin 3.5×3.5 mm QFN	bq24650RVAR	PAS	3000
		bq24650RVAT		250

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1][2][3]

		VALUE	UNIT
Voltage range (with respect to GND)	VCC, STAT1, STAT2, SRP, SRN	−0.3 to 33	V
	PH	−2 to 36	
	VFB	−0.3 to 16	
	REGN, LODRV, TS, MPPSET, TERM_EN	−0.3 to 7	
	BTST, HIDRV with respect to GND	−0.3 to 39	
	VREF	−0.3 to 3.6	
Maximum difference voltage	SRP–SRN	−0.5 to 0.5	V
Junction temperature range, T_J		−40 to 155	°C
Storage temperature range, T_{stg}		−55 to 155	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.
(3) Must have a series resistor between battery pack to VFB if battery pack voltage is expected to be greater than 16V. Usually the resistor divider top resistor takes care of this.

THERMAL INFORMATION

THERMAL METRIC[1]		bq24650	UNITS
		QFN	
		16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance[2]	43.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter[3]	0.6	
ψ_{JB}	Junction-to-board characterization parameter[4]	15.77	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

RECOMMENDED OPERATING CONDITIONS

		VALUE	UNIT
Voltage range (with respect to GND)	VCC, STAT1, STAT2, SRP, SRN	−0.3 to 28	V
	PH	−2 to 30	
	VFB	−0.3 to 14	
	REGN, LODRV, TS, MPPSET, TERM_EN	−0.3 to 6.5	
	BTST, HIDRV with respect to GND	−0.3 to 34	
	VREF	3.3	
Maximum difference voltage	SRP–SRN	−0.2 to 0.2	V
Junction temperature range, T_J		−40 to 125	°C
Storage temperature range, T_{stg}		−55 to 155	°C

ELECTRICAL CHARACTERISTICS

5.0V ≤ V_{VCC} ≤ 28V, −40°C < T_J + 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
OPERATING CONDITIONS						
V_{VCC_OP}	VCC input voltage operating range		5		28	V
QUIESCENT CURRENTS						
I_{BAT}	Total battery discharge current (sum of currents into VCC, BTST, PH, SRP, SRN, VFB), VFB ≤ 2.1V	VCC < VBAT, VCC > V_{UVLO} (SLEEP)			15	µA
	Battery discharge current (sum of currents into BTST, PH, SRP, SRN, VFB), VFB ≤ 2.1V	VCC > VBAT, VCC > V_{UVLO}, CE = LOW			5	µA
		VCC > VBAT, VCC > $V_{VCCLOWV}$, CE = HIGH, Charge done			5	µA
I_{AC}	Adapter supply current (sum of current into VCC pin)	VCC > VBAT, VCC > V_{UVLO}, CE = LOW		0.7	1	mA
		VCC > VBAT, VCC > $V_{VCCLOWV}$, CE = HIGH, charge done		2	3	mA
		VCC > VBAT, VCC > $V_{VCCLOWV}$, CE = HIGH, Charging, Qg_total = 10nC [1]		25		mA
CHARGE VOLTAGE REGULATION						
V_{REG}	Feedback regulation voltage			2.1		V
	Charge voltage regulation accuracy	T_J = 0°C to 85°C	−0.5%		0.5%	
		T_J = −40°C to 125°C	-0.7%		0.7%	
I_{VFB}	Leakage current into VFB pin	VFB = 2.1 V			100	nA
CURRENT REGULATION – FAST CHARGE						
V_{IREG_CHG}	SRP-SRN current sense voltage range	$V_{IREG\_CHG} = V_{SRP} – V_{SRN}$		40		mV
	Charge current regulation accuracy	V_{IREG_CHG} = 40 mV	−3%		3%	
CURRENT REGULATION – PRE-CHARGE						
V_{PRECHG}	Precharge current sense voltage range	$V_{IREG\_PRCHG} = V_{SRP} – V_{SRN}$		4		mV
	Precharge current regulation accuracy	V_{IREG_PRECH} = 4 mV	−25%		25%	
CHARGE TERMINATION						
$V_{TERMCHG}$	Termination current sense voltage range	$V_{ITERM} = V_{SRP} – V_{SRN}$		4		mV
	Termination current accuracy	V_{ITERM} = 4 mV	−25%		25%	
	Deglitch time for termination (both edges)			100		ms
t_{QUAL}	Termination qualification time	$V_{BAT} > V_{RECH}$ and $I_{CHG} < I_{TERM}$		250		ms
I_{QUAL}	Termination qualification current	Discharge current once termination is detected		2		mA
INPUT VOLTAGE REGULATION						
V_{MPPSET}	MPPSET regulation voltage			1.2		V
	Input voltage regulation accuracy		−0.6%		0.6%	
I_{MPPSET}	Leakage current into MPPSET pin	V_{MPPSET} = 7 V, T_A = 0 − 85°C			1	µA
V_{MPPSET_CD}	MPPSET shorted to disable charge				75	mV
V_{MPPSET_CE}	MPPSET released to enable charge		175			mV
INPUT UNDER-VOLTAGE LOCK-OUT COMPARATOR (UVLO)						
V_{UVLO}	AC under-voltage rising threshold	Measure on VCC	3.65	3.85	4	V
V_{UVLO_HYS}	AC under-voltage hysteresis, falling			350		mV
VCC LOWV COMPARATOR						
$V_{VCC\ LOWV\_fall}$	Falling threshold, disable charge	Measure on VCC		4.1		V
$V_{VCC\ LOWV\_rise}$	Rising threshold, resume charge			4.35		V
SLEEP COMPARATOR (REVERSE DISCHARGING PROTECTION)						
V_{SLEEP_FALL}	SLEEP falling threshold	$V_{VCC} – V_{SRN}$ to enter SLEEP	40	100	150	mV
V_{SLEEP_HYS}	SLEEP hysteresis			500		mV
	SLEEP rising shutdown deglitch	VCC falling below SRN		100		ms
	SLEEP falling powerup deglitch	VCC rising above SRN, Delay to exit SLEEP mode		30		ms

ELECTRICAL CHARACTERISTICS (continued)

5.0V ≤ V_{VCC} ≤ 28V, −40°C < T_J + 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
BAT LOWV COMPARATOR						
V_{LOWV}	Precharge to fast charge transition (LOWV threshold)	Measure on VFB pin	1.54	1.55	1.56	V
V_{LOWV_HYS}	LOWV hysteresis			100		mV
	LOWV rising deglitch	VFB falling below V_{LOWV}		25		ms
	LOWV falling deglitch	VFB rising above V_{LOWV} + V_{LOWV_HYS}		25		ms
RECHARGE COMPARATOR						
V_{RECHG}	Recharge threshold (with respect to V_{REG})	Measure on VFB pin	35	50	65	mV
	Recharge rising deglitch	VFB decreasing below V_{RECHG}		10		ms
	Recharge falling deglitch	VFB increasing above V_{RECHG}		10		ms
BAT OVER-VOLTAGE COMPARATOR						
V_{OV_RISE}	Over-voltage rising threshold	As percentage of V_{FB}		104%		
V_{OV_FALL}	Over-voltage falling threshold	As percentage of V_{FB}		102%		
INPUT OVER-VOLTAGE COMPARATOR (ACOV)						
V_{ACOV}	AC over-voltage rising threshold on VCC		31	32	33	V
V_{ACOV_HYS}	AC over-voltage falling hysteresis			1		V
	AC over-voltage deglitch (both edges)	Delay to changing the STAT pins		1		ms
	AC over-voltage rising deglitch	Delay to disable charge		1		ms
	AC over-voltage falling deglitch	Delay to resume charge		20		ms
THERMAL SHUTDOWN COMPARATOR						
T_{SHUT}	Thermal shutdown rising temperature	Temperature increasing		145		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis			15		°C
	Thermal shutdown rising deglitch	Temperature increasing		100		µs
	Thermal shutdown falling deglitch	Temperature decreasing		10		ms
THERMISTOR COMPARATOR						
V_{LTF}	Cold temperature rising threshold	As percentage to V_{VREF}	72.5%	73.5%	74.5%	
V_{LTF_HYS}	Rising hysteresis		0.2%	0.4%	0.6%	
V_{HTF}	Hot temperature rising threshold		46.7%	47.5%	48.3%	
V_{TCO}	Cut-off temperature rising threshold		44.3%	45%	45.7%	
	Deglitch time for temperature out of range detection	$V_{TS} < V_{LTF}$, or $V_{TS} < V_{TCO}$, or $V_{TS} < V_{HTF}$		400		ms
	Deglitch time for temperature in valid range detection	$V_{TS} > V_{LTF} - V_{LTF\_HYS}$ or $V_{TS} > V_{TCO}$, or $V_{TS} > V_{HTF}$		20		ms
CHARGE OVER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)						
V_{OC}	Charge over-current rising threshold	Current rising, in synchronous mode measure ($V_{SRP} - V_{SRN}$)		80		mV
CHARGE UNDER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)						
$V_{ISYNSET}$	Charge under-current falling threshold	Switch from CCM to DCM, $V_{SRP} > 2.2V$	1	5	9	mV
BATTERY SHORTED COMPARATOR (BATSHORT)						
V_{BATSHT}	BAT short falling threshold, forced non-synchronous mode	V_{SRP} falling		2		V
V_{BATSHT_HYS}	BAT short rising hysteresis			200		mV
t_{BATSHT_DEG}	Deglitch on both edges			1		µs
LOW CHARGE CURRENT COMPARATOR						
V_{LC}	Low charge current falling threshold	Measure $V_{(SRP-SRN)}$		1.25		mV
V_{LC_HYS}	Low charge current rising hysteresis			1.25		mV
t_{LC_DEG}	Deglitch on both edges			1		µs
VREF REGULATOR						
V_{VREF_REG}	VREF regulator voltage	$V_{VCC} > V_{UVLO}$, 0 – 35 mA load	3.267	3.3	3.333	V
I_{VREF_LIM}	VREF current limit	$V_{VREF} = 0$ V, $V_{VCC} > V_{UVLO}$	35			mA

ELECTRICAL CHARACTERISTICS (continued)

5.0V ≤ V_{VCC} ≤ 28V, –40°C < T_J + 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

| PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
REGN REGULATOR						
V_{REGN_REG}	REGN regulator voltage	V_{VCC} > 10 V, MPPSET > 175 mV	5.7	6.0	6.3	V
I_{REGN_LIM}	REGN current limit	V_{REGN} = 0 V, V_{VCC} > V_{UVLO}, MPPSET < 75 mV	40			mA
BATTERY DETECTION						
t_{WAKE}	Wake timer	Max time charge is enabled		500		ms
I_{WAKE}	Wake current	R_{SENSE} = 10 mΩ	50	125	200	mA
$t_{DISCHARGE}$	Discharge timer	Max time discharge current is applied		1		sec
$I_{DISCHARGE}$	Discharge current			6		mA
I_{FAULT}	Fault current after a timeout fault			2		mA
I_{QUAL}	Termination qualification current			2		mA
t_{QUAL}	Termination qualification time			250		ms
V_{WAKE}	Wake threshold (with respect to V_{REG})	Voltage on VFB to detect battery absent during wake		50		mV
V_{DISCH}	Discharge threshold	Voltage on VFB to detect battery absent during discharge		1.55		V
PWM HIGH SIDE DRIVER (HIDRV)						
$R_{DS\_HI\_ON}$	High side driver (HSD) turn-on resistance	VBTST – VPH = 5.5 V		3.3	6	Ω
$R_{DS\_HI\_OFF}$	High side driver turn-off resistance			1	1.4	Ω
$V_{BTST\_REFRESH}$	Bootstrap refresh comparator threshold Voltage	VBTST – VPH when low side refresh pulse is requested	4.0	4.2		V
PWM LOW SIDE DRIVER (LODRV)						
$R_{DS\_LO\_ON}$	Low side driver (LSD) turn-on resistance			4.1	7	Ω
$R_{DS\_LO\_OFF}$	Low side driver turn-off resistance			1	1.4	Ω
PWM DRIVERS TIMING						
	Driver dead-time	Dead time when switching between LSD and HSD, No load at LSD and HSD		30		ns
PWM OSCILLATOR						
V_{RAMP_HEIGHT}	PWM ramp height	As percentage of VCC		7%		
	PWM switching frequency		510	600	690	kHz
INTERNAL SOFT START (8 steps to regulation current ICHG)						
	Soft start steps			8		step
	Soft start step time			1.6		ms
CHARGER SECTION POWER-UP SEQUENCING						
	Charge-enable delay after power-up	Delay from MPPSET > 175 mV to charger is allowed to turn on		1.5		s
LOGIC IO PIN CHARACTERISTICS (STAT1, STAT2, TERM_EN)						
V_{OUT_LOW}	STAT1, STAT2 output low saturation voltage	Sink current = 5 mA			0.5	V
I_{OUT_HI}	Leakage current	V = 32 V			1.2	µA
V_{IN_LOW}	TERM_EN input low threshold voltage				0.4	V
V_{IN_HI}	TERM_EN input high threshold voltage		1.6			V
I_{IN_BIAS}	TERM_EN bias current	V_{TERM_EN} = 0.5 V			60	µA

TYPICAL CHARACTERISTICS

V_{CC} = 25V, bq24650 Application Circuit, T_A = 25°C unless otherwise noted
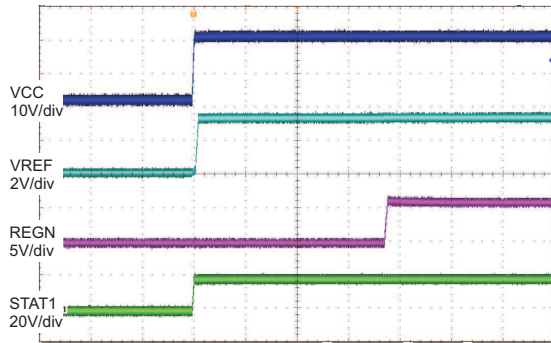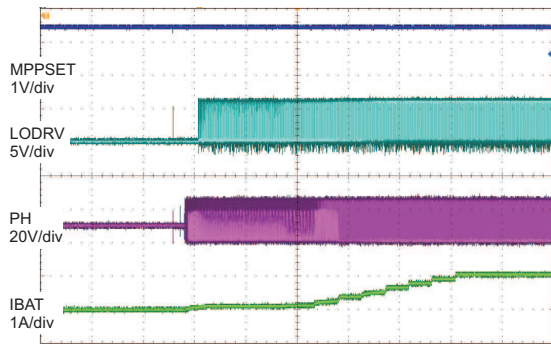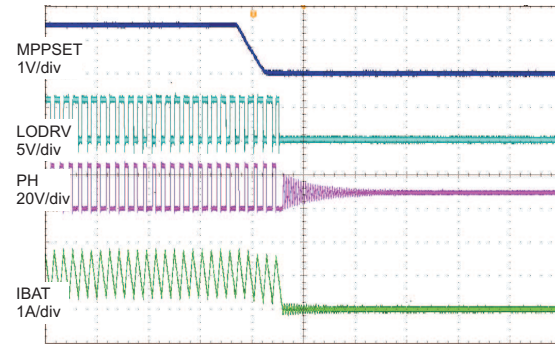

800 μs/div

Figure 2. Power Up on V_{CC}
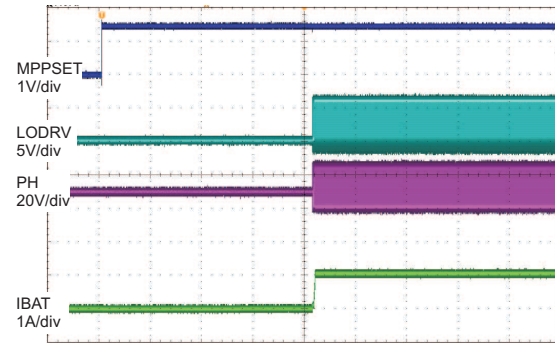
400 ms/div

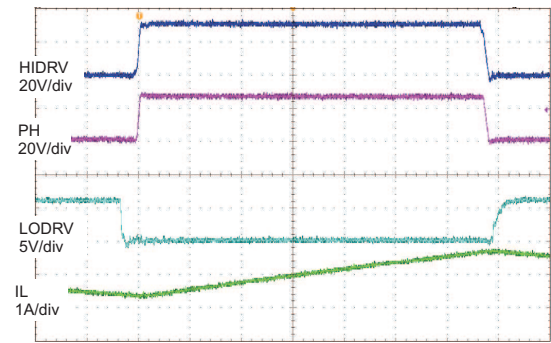**Figure 3. Charge Start on MPPSET**

4 ms/div

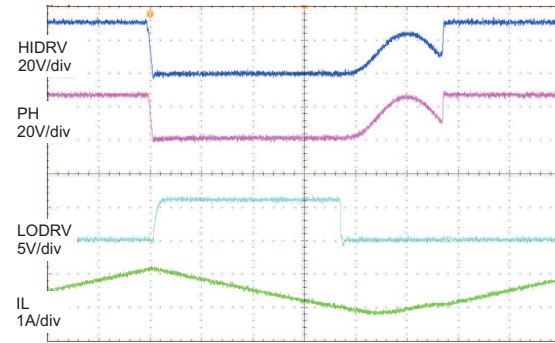**Figure 4. Charge Soft Start on MPPSET**

10 μs/div

Figure 5. Charge Stop on MPPSET

100 ns/div

Figure 6. Switching in Continuous Conduction Mode

200 ns/div

Figure 7. Switching in Discontinuous Conduction Mode

Product Folder Link(s): bq24650

TYPICAL CHARACTERISTICS (continued)

V_{CC} = 25V, bq24650 Application Circuit, T_A = 25°C unless otherwise noted
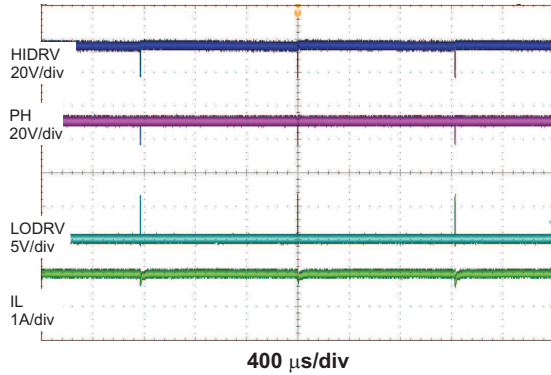
Figure 8. Switching at 100% Duty Cycle
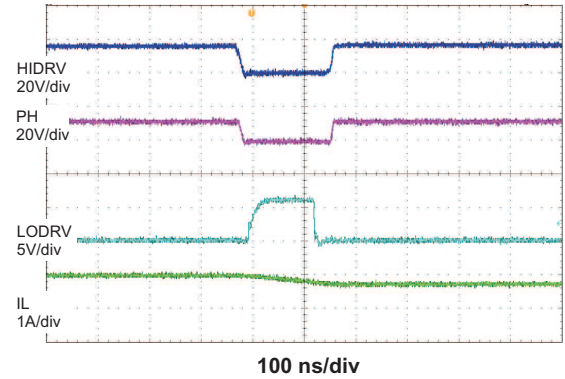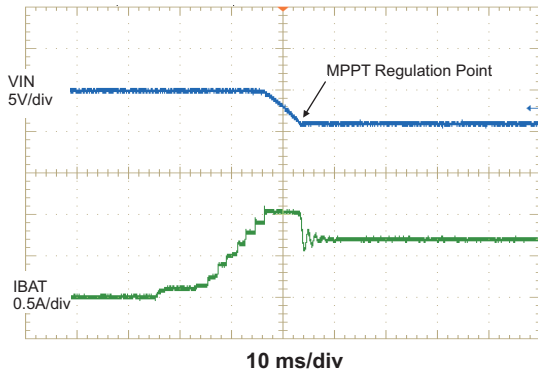

Figure 9. Recharge the BTST-PH Capacitor

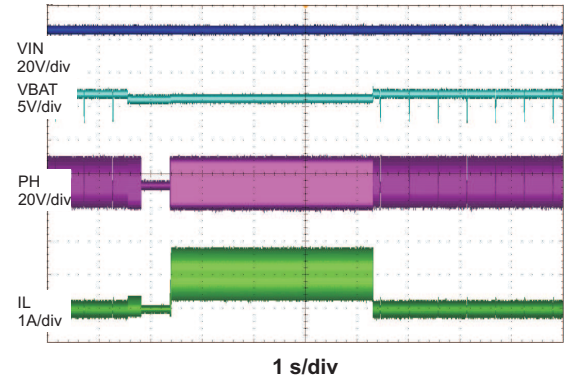**Figure 10. MPPT Regulation During Soft Start**

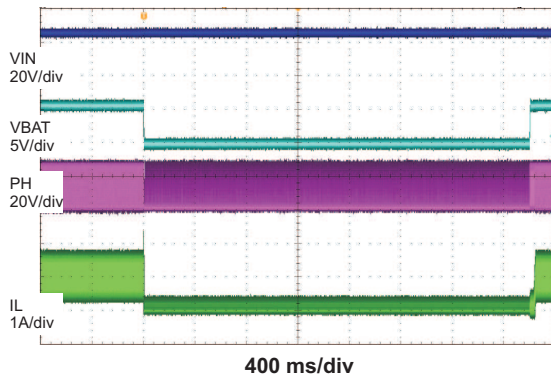**Figure 11. Battery Insertion and Removal**
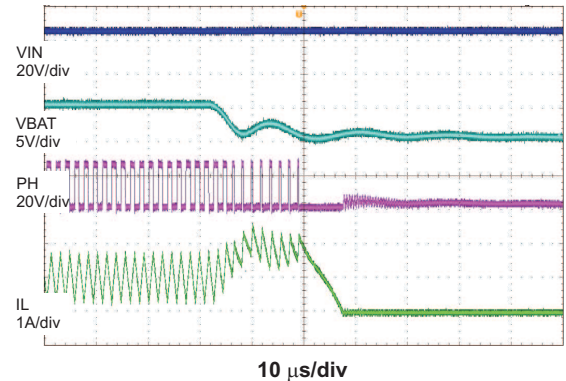

Figure 12. Short Battery Response

Figure 13. Charge Reset During Battery Short

TYPICAL CHARACTERISTICS (continued)

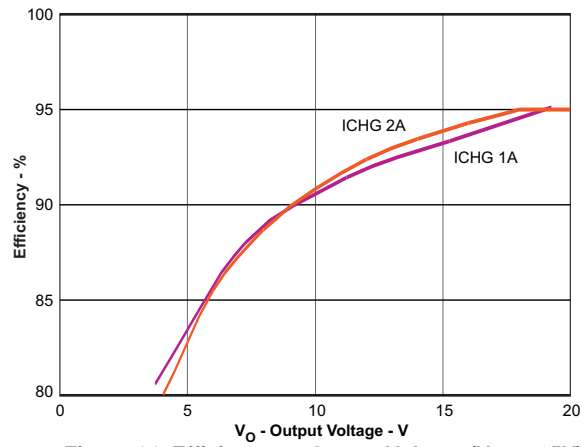V_{CC} = 25V, bq24650 Application Circuit, T_A = 25°C unless otherwise noted

Figure 14. Efficiency vs Output Voltage (V_{CC} = 25V)

Product Folder Link(s): *bq24650*

TEXAS INSTRUMENTS

PIN FUNCTIONS

| PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VCC	P	IC power positive supply. Place a 1-μF ceramic capacitor from VCC to GND and place it as close as possible to IC. Place a 10-Ω resistor from input side to VCC pin to filter the noise.
2	MPPSET	I	Input voltage set point. Use a voltage divider from input source to GND to set voltage on MPPSET to 1.2V. To disable charge, pull MPPSET below 75mV.
3	STAT1	O	Open drain charge status output to indicate various charger operation. Connect to the cathode of LED with 10kΩ to the pull-up rail. LOW or LED light up indicates charge in progress. Otherwise stays HI or LED stays off. When any fault condition occurs, both STAT1 and STAT2 are HI, or both LEDs are off.
4	TS	I	Temperature qualification voltage input. Connect to a negative temperature coefficient thermistor. Program the hot and cold temperature window with a resistor divider from VREF to TS to GND. A 103AT-2 thermister is recommended.
5	STAT2	O	Open drain charge status output to indicate various charger operation. Connect to the cathode of LED with 10kΩ to the pull-up rail. LOW or LED light up indicates charge is complete. Otherwise, stays HI or LED stays off. When any fault condition occurs, both STAT1 and STAT2 are HI, or both LEDs are off.
6	VREF	P	3.3V reference voltage output. Place a 1-μF ceramic capacitor from VREF to GND pin close to the IC. This voltage could be used for programming voltage on TS and the pull-up rail of STAT1 and STAT2.
7	TERM_EN	I	Charge termination enable. Pull TERM_EN to GND to disable charge termination. Pull TERM_EN to VREF to allow charge termination. TERM_EN must be terminated and cannot be left floating.
8	VFB	I	Charge voltage analog feedback adjustment. Connect the output of a resistor divider powered from the battery terminals to this node to adjust the output battery voltage regulation.
9	SRN	I	Charge current sense resistor, negative input. A 0.1-μF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. An optional 0.1-μF ceramic capacitor is placed from SRN to GND for common-mode filtering.
10	SRP	P/I	Charge current sense resistor, positive input. A 0.1-μF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1-μF ceramic capacitor is placed from SRP to GND for common-mode filtering.
11	GND	P	Power ground. Ground connection for high-current power converter node. On PCB layout, connect directly to source of low-side power MOSFET, to ground connection of input and output capacitors of the charger. Only connect to GND through the thermal pad underneath the IC.
12	REGN	P	PWM low-side driver positive 6V supply output. Connect a 1-μF ceramic capacitor from REGN to GND, close to the IC. Use to drive low-side driver and high-side driver bootstrap Schottky diode from REGN to BTST.
13	LODRV	O	PWM low-side driver output. Connect to the gate of the low-side N-channel power MOSFET with a short trace.
14	PH	P	Switching node, charge current output inductor connection. Connect the 0.1-μF bootstrap capacitor from PH to BTST.
15	HIDRV	O	PWM high-side driver output. Connect to the gate of the high-side N-channel power MOSFET with a short trace.
16	BTST	P	PWM high-side driver positive supply. Connect the 0.1-uF bootstrap capacitor from PH to BTST.
Thermal Pad			Exposed pad beneath the IC. The thermal pad must always be soldered to the board and have the vias on the thermal pad plane star-connecting to GND and ground plane for high-current power converter. It also serves as a thermal pad to dissipate heat.

BLOCK DIAGRAM
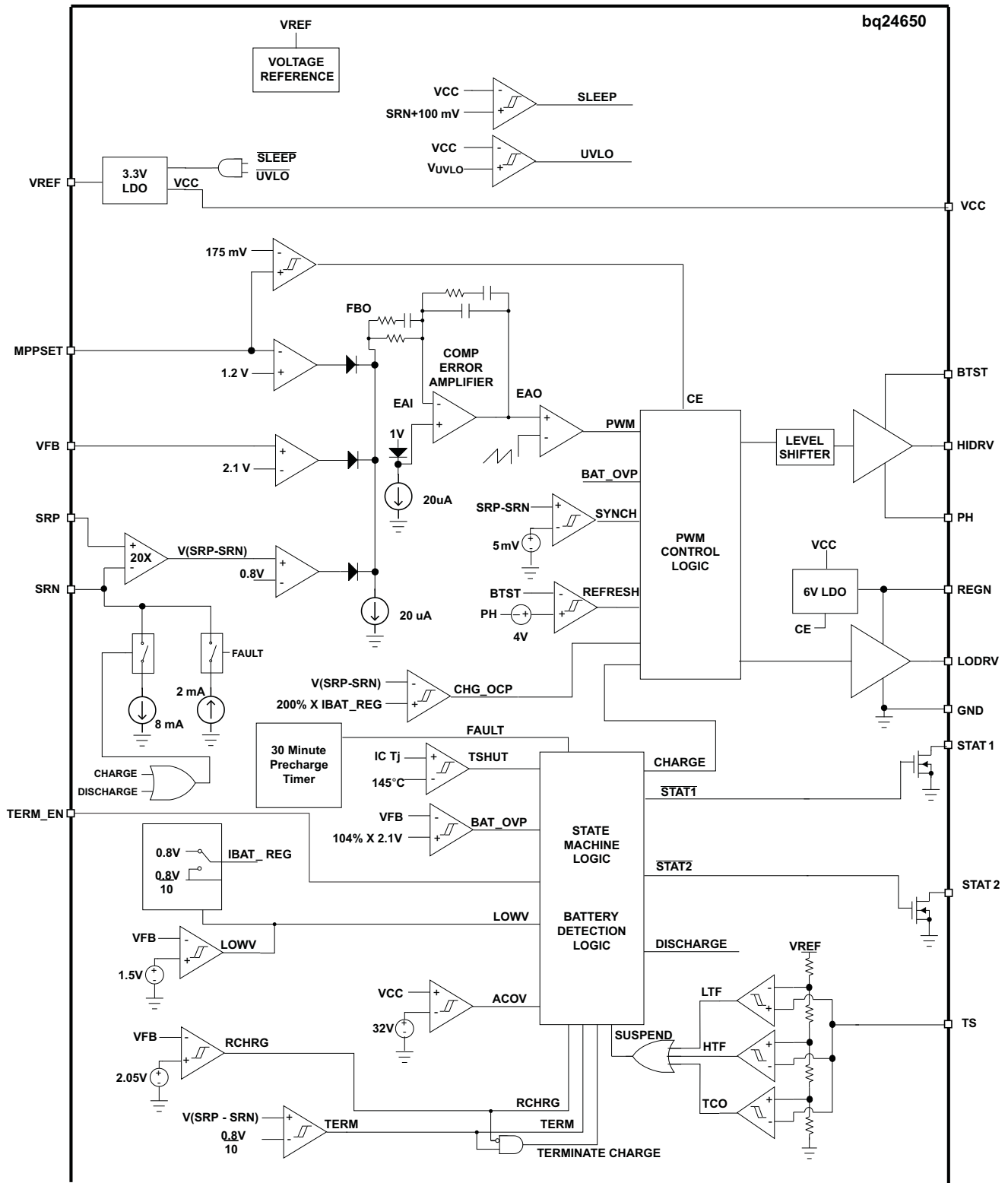
Figure 15. Functional Block Diagram
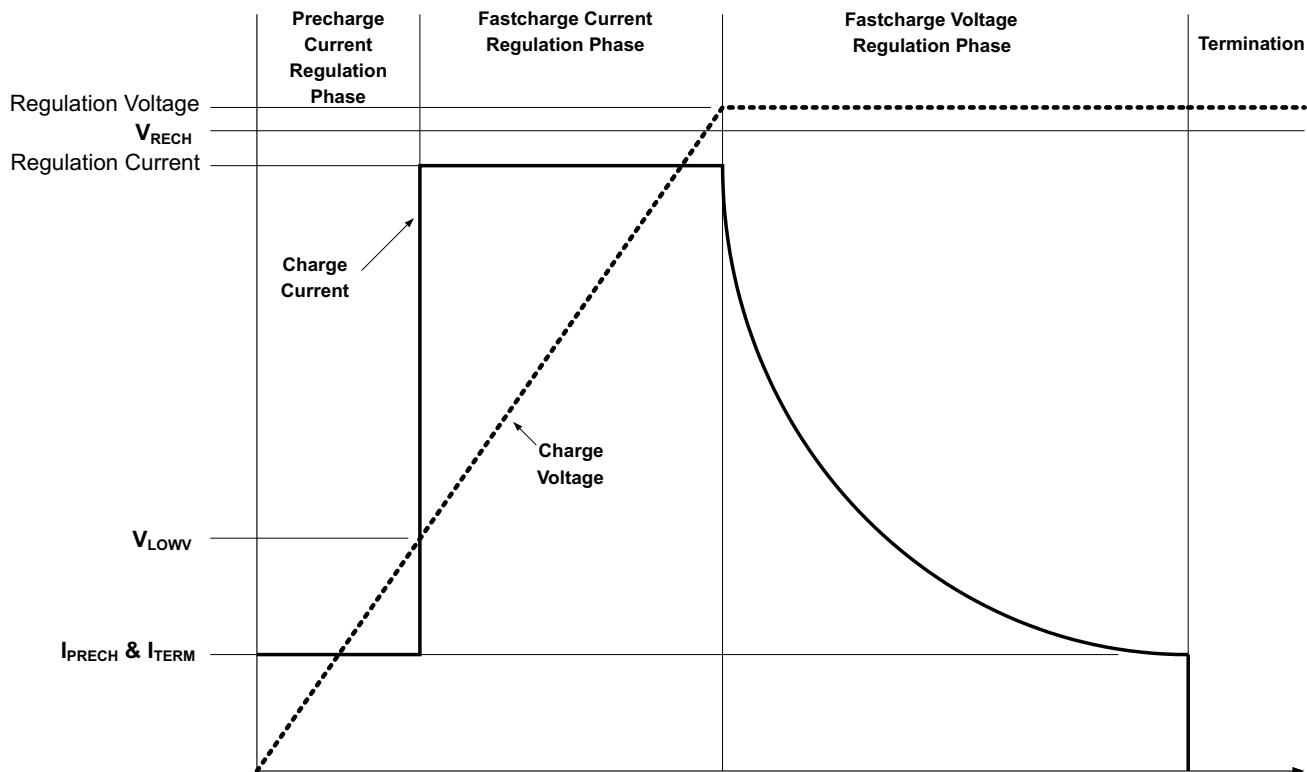
DETAILED DESCRIPTION

Figure 16. Typical Charging Profile

BATTERY VOLTAGE REGULATION

The bq24650 uses a high accuracy voltage regulator for the charging voltage. The charge voltage is programmed via a resistor divider from the battery to ground, with the midpoint tied to the VFB pin. The voltage at the VFB pin is regulated to 2.1V, giving the following equation for the regulation voltage:

$$V_{BAT} = 2.1 \text{ V} \times \left[1 + \frac{R2}{R1} \right]$$

(1)

where R2 is connected from VFB to the battery and R1 is connected from VFB to GND.

Li-Ion, LiFePO4, and sealed lead acid are widely used battery chemistries. Most commercial Li-ion cells can now be charged to 4.2V/cell. A LiFePO4 battery allows a much higher charge and discharge rate, but the energy density is lower. The typical cell voltage is 3.6V. The charge profile of both Li-Ion and LiFePO4 is preconditioning, constant current, and constant voltage. For maximum cycle life, the end-of-charge voltage threshold could be lowered to 4.1V/cell.

Although it's energy density is much lower than Li-based chemistry, lead acid is still popular due to its low manufacturing cost and high discharge rates. The typical voltage limit is from 2.3V to 2.45V. After the battery has been fully charged, a float charge is required to compensate for the self-discharge. The float charge limit is 100mV-200mV below the constant voltage limit.

INPUT VOLTAGE REGULATION

A solar panel has a unique point on the V-I or V-P curve, called the Maximum Power Point (MPP), at which the entire photovoltaic (PV) system operates with maximum efficiency and produces its maximum output power. The constant voltage algorithm is the simplest Maximum Power Point Tracking (MPPT) method. The bq24650 automatically reduces charge current so the maximum power point is maintained for maximum efficiency.

If the solar panel or other input source cannot provide the total power of the system and bq24650 charger, the input voltage drops. Once the voltage sensed on the MPPSET pin drops below 1.2V, the charger maintains the input voltage by reducing the charge current. If the MPPSET pin voltage is forced below 1.2V, the bq24650 stays in the input voltage regulation loop while the output current is zero. The STAT1 pin is LOW and STAT2 pin is HIGH.

The voltage at the MPPSET pin is regulated to 1.2V, giving Equation 2 for the regulation voltage:

$$V_{MPPSET} = 1.2\ V \times \left[1 + \frac{R3}{R4}\right]$$

(2)

The MPPSET pin is also used as charge enable control. If the voltage on MPPSET is pulled down below 75mV, charge is disabled. Charge resumes if the voltage on MPPSET goes back above 175mV.

BATTERY CURRENT REGULATION

Battery current is sensed by resistor R_{SR} connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is fixed at 40mV. Thus, for a 20-mΩ sense resistor, the charging current is 2A. For charging current, refer to Equation 3:

$$I_{CHARGE} = \frac{40\ mV}{R_{SR}}$$

(3)

BATTERY PRECHARGE

On power-up, if the battery voltage is below the V_{LOWV} threshold, the bq24650 applies the precharge current to the battery. This feature is intended to revive deeply discharged cells. If the V_{LOWV} threshold is not reached within 30 minutes of initiating precharge, the charger turns off and a FAULT is indicated on the status pins.

The precharge current is determined as 1/10 of the fast charge current according to the following equation:

$$I_{PRECHARGE} = \frac{4\ mV}{R_{SR}}$$

(4)

CHARGE TERMINATION AND RECHARGE

The bq24650 monitors the charging current during the voltage regulation phase. Termination is detected while the voltage on the VFB pin is higher than the VRECH threshold and the charge current is less than the I_{TERM} threshold (1/10 of fast charge current), as calculated in Equation 5:

$$I_{TERM} = \frac{4\ mV}{R_{SR}}$$

(5)

A new charge cycle is initiated when one of the following conditions occurs:
- The battery voltage falls below the recharge threshold
- A power-on-reset (POR) event occurs
- MPPSET falls below 75mV to reset charge enable

The TERM_EN pin may be taken LOW to disable termination. If TERM_EN is pulled above 1.6V, the bq24650 allows termination.

POWER UP

The bq24650 uses a SLEEP comparator to determine the source of power on the VCC pin, since VCC can be supplied either from a battery or an adapter. If the VCC voltage is greater than the SRN voltage, and all other conditions are met for charging, the bq24650 then attempts to charge a battery (see **the Enabling and Disabling Charging** section). If SRN voltage is greater than VCC, indicating that a battery is the power source, the bq24650 enters low quiescent current (<15µA) SLEEP mode to minimize current drain from the battery.

If VCC is below the UVLO threshold, the device is disabled, and VREF LDO turns off.

ENABLE AND DISABLE CHARGING

The following conditions have to be valid before charging is enabled:

- Charge is allowed (MPPSET > 175mV)
- Device is not in Under-Voltage-Lock-Out (UVLO) mode and VCC is above the V_{CCLOWV} threshold
- Device is not in SLEEP mode (i.e. VCC > SRN)
- VCC voltage is lower than AC over-voltage threshold (VCC < VACOV)
- 30ms delay is complete after initial power-up
- REGN LDO and VREF LDO voltages are at correct levels
- Thermal Shut (TSHUT) is not valid
- TS fault is not detected

One of the following conditions stops on-going charging:

- Charge is disabled (MPPSET < 75mV)
- Adapter is removed, causing the device to enter V_{CCLOWV} or SLEEP mode
- Adapter voltage is less than 100mV above battery
- Adapter is over voltage
- REGN or VREF LDO voltage is not valid
- TSHUT IC temperature threshold is reached
- TS voltage goes out of range indicating the battery temperature is too hot or too cold

AUTOMATIC INTERNAL SOFT-START CHARGER CURRENT

The charger automatically soft-starts the charger regulation current every time the charger goes into fast-charge to ensure there is no overshoot or stress on the output capacitors or the power converter. The soft-start consists of stepping-up the charge regulation current into 8 evenly divided steps up to the programmed charge current. Each step lasts approximately 1.6ms, for a typical rise time of 13ms. No external components are needed for this function.

CONVERTER OPERATION

The synchronous buck PWM converter uses a fixed frequency voltage mode with feed-forward control scheme. A type III compensation network allows using ceramic capacitors at the output of the converter. The compensation input stage is connected internally between the feedback output (FBO) and the error amplifier input (EAI). The feedback compensation stage is connected between the error amplifier input (EAI) and error amplifier output (EAO). The LC output filter must be selected to give a resonant frequency of 12 kHz – 17 kHz for the bq24650, where resonant frequency, f_o, is given by:

$$f_o = \frac{1}{2\pi \sqrt{L_o C_o}}$$

(6)

An internal saw-tooth ramp is compared to the internal EAO error control signal to vary the duty-cycle of the converter. The ramp height is 7% of the input adapter voltage making it always directly proportional to the input adapter voltage. This cancels out any loop gain variation due to a change in input voltage and simplifies the loop compensation. The ramp is offset by 300mV in order to allow zero percent duty-cycle when the EAO signal is below the ramp. The EAO signal is also allowed to exceed the saw-tooth ramp signal in order to get a 100% duty-cycle PWM request. Internal gate drive logic allows achieving 99.98% duty-cycle while ensuring the N-channel upper device always has enough voltage to stay fully on. If the BTST pin to PH pin voltage falls below 4.2V for more than 3 cycles, then the high-side n-channel power MOSFET is turned off and the low-side n-channel power MOSFET is turned on to pull the PH node down and recharge the BTST capacitor. Then the high-side driver returns to 100% duty-cycle operation until the (BTST-PH) voltage is detected to fall low again due to leakage current discharging the BTST capacitor below 4.2 V, and the reset pulse is reissued.

The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature, simplifying output filter design and keeping it out of the audible noise region.

SYNCHRONOUS AND NON-SYNCHRONOUS OPERATION

The charger operates in synchronous mode when the SRP-SRN voltage is above 5mV (0.5-A inductor current for a 10-mΩ sense resistor). During synchronous mode, the internal gate drive logic ensures there is break-before-make complimentary switching to prevent shoot-through currents. During the 30ns dead time where both FETs are off, the body-diode of the low-side power MOSFET conducts the inductor current. Having the low-side FET turn on keeps power dissipation low, and allows safe charging at high currents. During synchronous mode the inductor current is always flowing and the converter operates in continuous conduction mode (CCM), creating a fixed two-pole system.

The charger operates in non-synchronous mode when the SRP-SRN voltage is below 5mV (0.5-A inductor current for a 10-mΩ sense resistor). In addition, the charger is forced into non-synchronous mode when battery voltage is lower than 2V or when the average SRP-SRN voltage is lower than 1.25mV.

During non-synchronous operation, the body-diode of the low-side MOSFET can conduct the positive inductor current after the low-side n-channel power MOSFET turns off. When the load current decreases and the inductor current drops to zero, the body diode is naturally turned off and the inductor current becomes discontinuous. This mode is called Discontinuous Conduction Mode (DCM). During DCM, the low-side n-channel power MOSFET turns on when the bootstrap capacitor voltage drops below 4.2V, then the low-side power MOSFET turns off and stays off until the beginning of the next cycle, where the high-side power MOSFET is turned on again. The low-side MOSFET on time is required to ensure the bootstrap capacitor is always recharged and able to keep the high-side power MOSFET on during the next cycle. This is important for battery chargers, where unlike regular dc-dc converters, there is a battery load that maintains a voltage and can both source and sink current. The low-side pulse pulls the PH node (connection between high and low-side MOSFETs) down, allowing the bootstrap capacitor to recharge up to the REGN LDO value. After the refresh pulse, the low-side MOSFET is kept off to prevent negative inductor current from occurring.

At very low currents during non-synchronous operation, there may be a small amount of negative inductor current during the recharge pulse. The charge should be low enough to be absorbed by the input capacitance. Whenever the converter goes into zero percent duty-cycle, the high-side MOSFET does not turn on, and the low-side MOSFET does not turn on (except for recharge pulse) either, and there is almost no discharge from the battery.

During DCM mode the loop response automatically changes and has a single pole system at which the pole is proportional to the load current, because the converter does not sink current, and only the load provides a current sink. This means at very low currents the loop response is slower, as there is less sinking current available to discharge the output voltage.

CYCLE-BY-CYCLE CHARGE UNDER CURRENT

In the bq24650, if the SRP-SRN voltage decreases below 5mV, the low side FET is turned off for the remainder of the switching cycle to prevent negative inductor current. During DCM, the low-side FET only turns on when the bootstrap capacitor voltage drops below 4.2V to provide refresh charge for the bootstrap capacitor. This is important to prevent negative inductor current from causing a boost effect in which the input voltage increases as power is transferred from the battery to the input capacitors and lead to an over-voltage stress on the VCC node and potentially cause damage to the system.

INPUT OVER-VOLTAGE PROTECTION (ACOV)

ACOV provides protection to prevent system damage due to high input voltage. Once the adapter voltage reaches the ACOV threshold, charge is disabled.

INPUT UNDER-VOLTAGE LOCK OUT (UVLO)

The system must have a minimum VCC voltage to allow proper operation. This VCC voltage could come from either input adapter or battery, since a conduction path exists from the battery to VCC through the high-side NMOS body diode. When VCC is below the UVLO threshold, all circuits on the IC, including VREF LDO, are disabled.

BATTERY OVER-VOLTAGE PROTECTION

The converter does not allow the high-side FET to turn on until the BAT voltage goes below 102% of the regulation voltage. This allows one-cycle response to an over-voltage condition – such as occurs when the load is removed or the battery is disconnected. A current sink from SRP to GND is on to discharge the stored energy on the output capacitors.

CYCLE-BY-CYCLE CHARGE OVER-CURRENT PROTECTION

The charger has a secondary cycle-to-cycle over-current protection. It monitors the charge current and prevents the current from exceeding 200% of the programmed charge current. The high-side gate drive turns off when over-current is detected and automatically resumes when the current falls below the over-current threshold.

THERMAL SHUTDOWN PROTECTION

The QFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junction temperatures low. As an added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the TSHUT threshold of 145°C. The charger stays off until the junction temperature falls below 130°C.

TEMPERATURE QUALIFICATION

The controller continuously monitors battery temperature by measuring the voltage between the TS pin and GND. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The controller compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the V_{LTF} to V_{HTF} thresholds. If battery temperature is outside of this range, the controller suspends charge and waits until the battery temperature is within the V_{LTF} to V_{HTF} range. During the charge cycle the battery temperature must be within the V_{LTF} to V_{TCO} thresholds. If battery temperature is outside of this range, the controller suspends charge and waits until the battery temperature is within the V_{LTF} to V_{HTF} range. The controller suspends charge by turning off the PWM charge FETs. Figure 17 summarizes the operation.
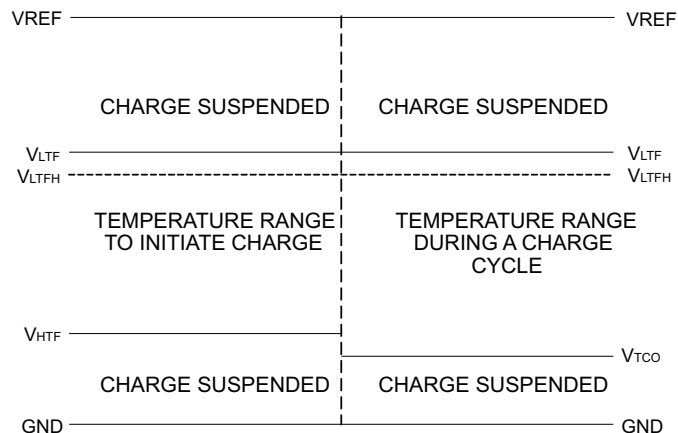

Figure 17. TS Pin, Thermistor Sense Thresholds

Assuming a 103AT NTC thermistor on the battery pack as shown in Figure 1, the values of RT1 and RT2 can be determined by using Equation 7 and Equation 8:

$$RT2 = \frac{V_{VREF} \times RTH_{COLD} \times RTH_{HOT} \times \left(\dfrac{1}{V_{LTF}} - \dfrac{1}{V_{TCO}} \right)}{RTH_{HOT} \times \left(\dfrac{V_{VREF}}{V_{TCO}} - 1 \right) - RTH_{COLD} \times \left(\dfrac{V_{VREF}}{V_{LTF}} - 1 \right)}$$

(7)

$$RT1 = \frac{\dfrac{V_{VREF}}{V_{LTF}} - 1}{\dfrac{1}{RT2} + \dfrac{1}{RTH_{COLD}}}$$
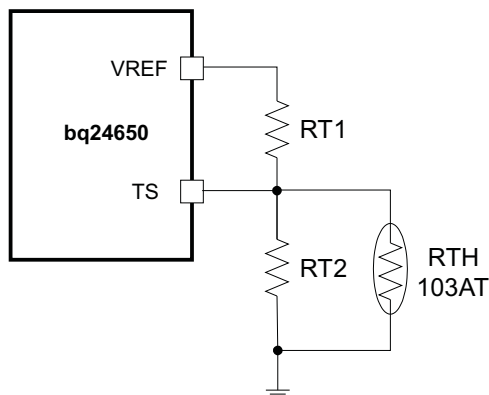
(8)

Figure 18. TS Resistor Network

CHARGE ENABLE

MPPSET is used to disable or enable the charge process. A voltage above 175mV on this pin enables charge, provided all other conditions for charge are met (see *the Enabling and Disabling Charge section*). A voltage below 75mV on this pin also resets all timers and fault conditions.

INDUCTOR, CAPACITOR, AND SENSE RESISTOR SELECTION GUIDELINES

The bq24650 provides internal loop compensation. With this scheme, the best stability occurs when the LC resonant frequency, f_o, is approximately 12kHz – 17kHz for the bq24650.

Table 1 provides a summary of typical LC components for various charge currents.

Table 1. Typical Inductor, Capacitor, and Sense Resistor Values as a Function of Charge Current

CHARGE CURRENT	0.5A	1A	2A	4A	8A	10A
Output inductor low	22 µH	15 µH	10 µH	6.8 µH	3.3 µH	3.3 µH
Output capacitor C_O	7 µF	10 µF	15 µF	20 µF	40 µF	40 µF
Sense resistor	80 mΩ	40 mΩ	20 mΩ	10 mΩ	5 mΩ	4 mΩ

CHARGE STATUS OUTPUTS

The open-drain STAT1 and STAT2 outputs indicate various charger operations as listed in Table 2. These status pins can be used to drive LEDs or communicate with the host processor. Note that OFF indicates that the open-drain transistor is turned off.

Table 2. STAT Pin Definition for bq24650

CHARGE STATE	STAT1	STAT2
Charge in progress	ON	OFF
Charge complete	OFF	ON
Charge suspend, over-voltage, sleep mode, battery absent	OFF	OFF

BATTERY DETECTION

For applications with removable battery packs, the bq24650 provides a battery absent detection scheme to reliably detect insertion or removal of battery packs.
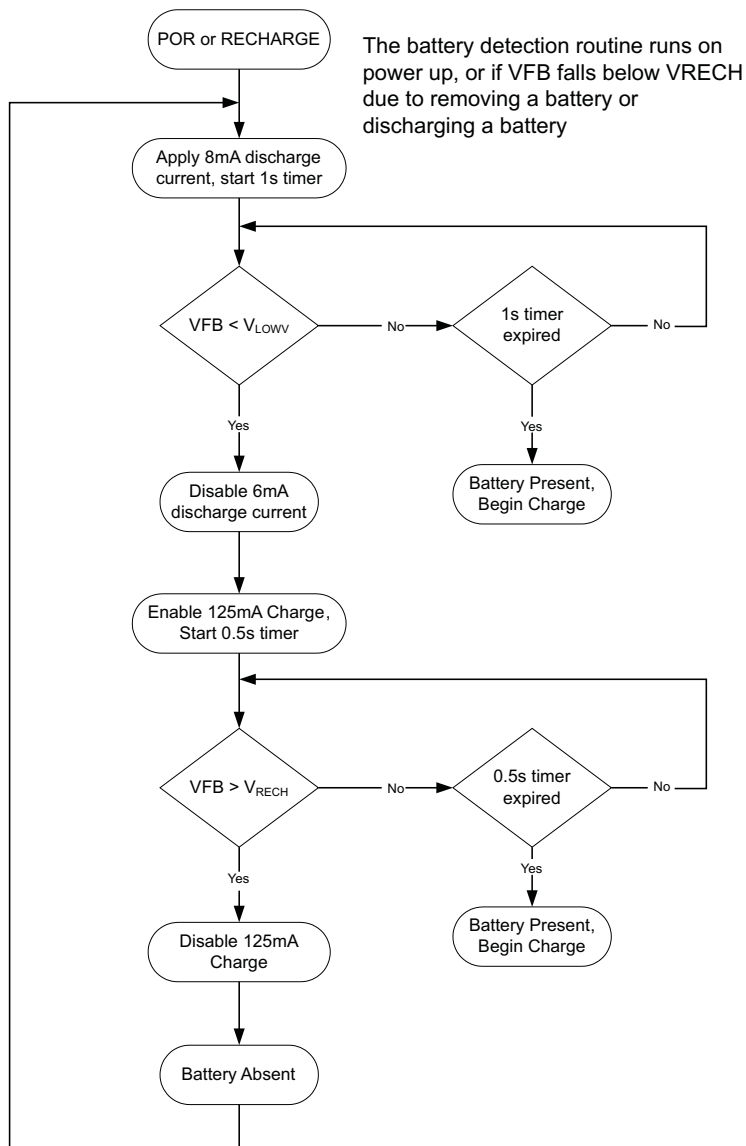

Figure 19. Battery Detection Flowchart

Once the device has powered up, a 6-mA discharge current is applied to the SRN terminal. If the battery voltage falls below the LOWV threshold within 1 second, the discharge source is turned off, and the charger is turned on at low charge current (125mA). If the battery voltage gets up above the recharge threshold within 500ms, there is no battery present and the cycle restarts. If either the 500ms or 1 second timer time out before the respective thresholds are hit, a battery is detected and a charge cycle is initiated.
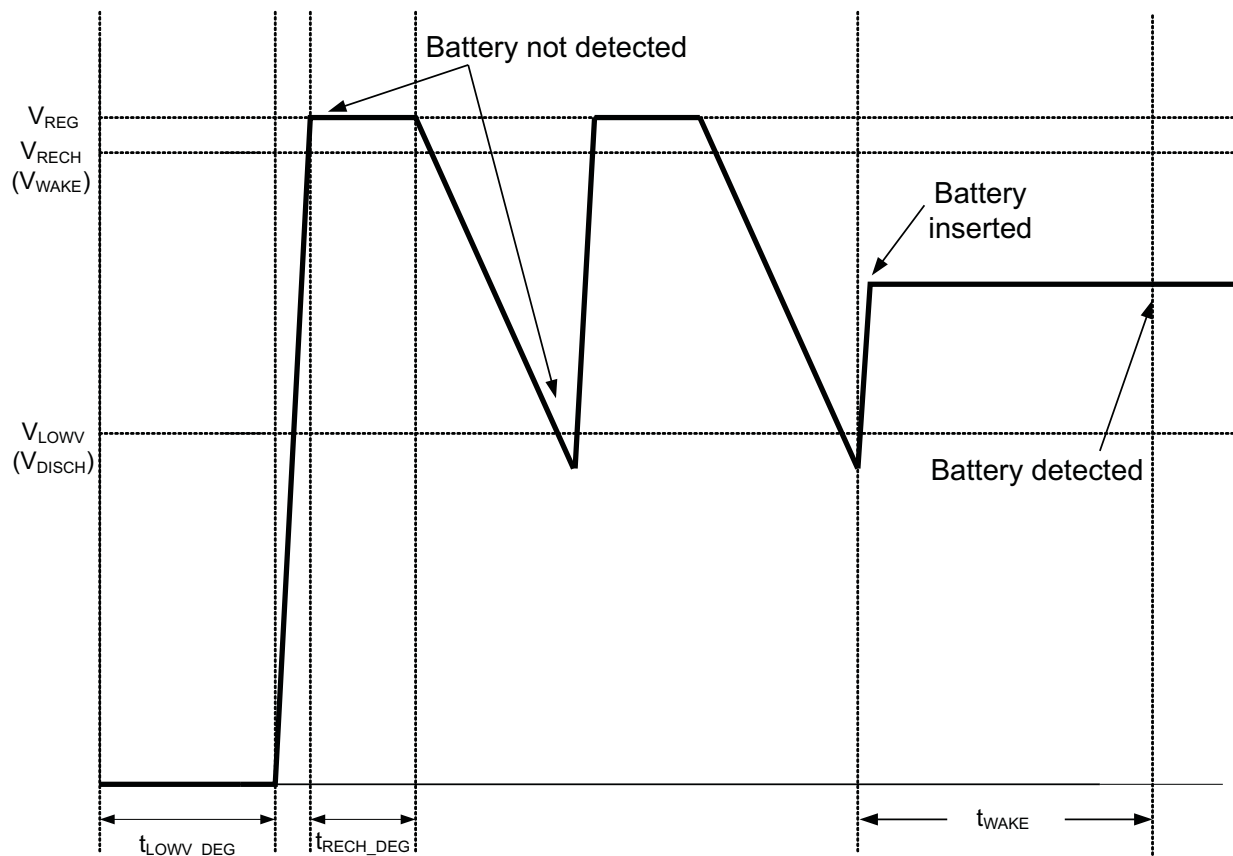
Product Folder Link(s): *bq24650*

Figure 20. Battery Detect Timing Diagram

Care must be taken that the total output capacitance at the battery node is not so large that the discharge current source cannot pull the V_{FB} voltage below the LOWV threshold during the 1 second discharge time. The maximum output capacitance can be calculated according to Equation 9:

$$C_{MAX} = \frac{I_{DISCH} \times t_{DISCH}}{0.5 \times \left[1 + \dfrac{R_2}{R_1}\right]}$$

(9)

Where C_{MAX} is the maximum output capacitance, I_{DISCH} is the discharge current, t_{DISCH} is the discharge time, and R_2 and R_1 are the voltage feedback resistors from the battery to the VFB pin. The 0.5 factor is the difference between the RECHARGE and the LOWV thresholds at the VFB pin.

Example

For a 3-cell Li+ charger, with $R_2 = 500k\Omega$, $R_1 = 100k\Omega$ (giving 12.6V for voltage regulation), $I_{DISCH} = 6mA$, $t_{DISCH} = 1$ second.

$$C_{MAX} = \frac{6 \text{ mA} \times 1 \text{ sec}}{0.5 \times \left[1 + \dfrac{500 \text{ k}\Omega}{100 \text{ k}\Omega}\right]} = 2000 \text{ µF}$$

(10)

Based on these calculations, no more than 2000 µF should be allowed on the battery node for proper operation of the battery detection circuit.

Component List for the Typical System Circuit in Figure 1

PART DESIGNATOR	QTY	DESCRIPTION
Q1, Q2	2	N-channel MOSFET, 40 V, 10 A, PowerPAK SO-8, Vishay-Siliconix, Si7288
D2	1	Diode, Dual Schottky, 30 V, 200 mA, SOT23, Fairchild, BAT54C
D3, D4	2	LED Diode, Green, 2.1V, 20mA, LTST-C190GKT
RSR	1	Sense Resistor, 20 mΩ, Vishay-Dale, WSL1206R0200DEA
L1	1	Inductor, 10 µH, 7A, Vishay-Dale IHLP-2525CZ
C6, C8	2	Capacitor, Ceramic, 10 µF, 35 V, 20%, X7R, 1210, Panasonic
C9	1	Capacitor, Ceramic, 4.7 µF, 35 V, 20%, X7R, 1210, Panasonic
C2, C3, C4	3	Capacitor, Ceramic, 1 µF, 35 V, 10%, X7R, 0805, Kemet
C5, C7	2	Capacitor, Ceramic, 0.1 µF, 35 V, 10%, X7R, 0805, Kemet
C1	1	Capacitor, Ceramic, 2.2 µF, 35V, 10%, X7R, 1210, Kemet
C10	1	Capacitor, Ceramic, 22 pF, 35V, 10%, X7R, 0603 Kemet
R1	1	Resistor, Chip, 100 kΩ, 1/16W, 0.5%, 0402
R2, R3	2	Resistor, Chip, 499 kΩ, 1/16W, 0.5%, 0402
R4	1	Resistor, Chip, 36 kΩ, 1/16W, 0.5%, 0402
R9	1	Resistor, Chip, 5.23 kΩ, 1/16W, 1%, 0402
R10	1	Resistor, Chip, 30.1 kΩ, 1/16W, 1%, 0402
R7, R8	2	Resistor, Chip, 10 kΩ, 1/16W, 5%, 0402
R6	1	Resistor, Chip, 10 Ω, 1/4W, 5%, 1206
R5	1	Resistor, Chip, 2 Ω, 1W, 5%, 2012
D1	1	Diode, Schottky Rectifier, 40V, 10A, PDS1040
Q3	1	N-Channel MOSFET, 60V, 115mA, SOT-23, 2N7002DICT

APPLICATION INFORMATION

INDUCTOR SELECTION

The bq24650 has a 600-kHz switching frequency to allow the use of small inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)I_{RIPPLE}$$

(11)

Inductor ripple current depends on input voltage (V_{IN}), duty cycle ($D = V_{OUT}/V_{IN}$), switching frequency (fs), and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{fs \times L}$$

(12)

The maximum inductor ripple current happens with $D = 0.5$ or close to 0.5. Usually inductor ripple is designed in the range of 20% to 40% of the maximum charging current as a trade-off between inductor size and efficiency for a practical design.

INPUT CAPACITOR

The input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)}$$

(13)

A low ESR ceramic capacitor such as X7R or X5R is preferred for the input decoupling capacitor and should be placed as close as possible to the drain of the high-side MOSFET and source of the low-side MOSFET. The voltage rating of the capacitor must be higher than the normal input voltage level. A 25V rating or higher capacitor is preferred for a 20V input voltage. A 20μF capacitance is suggested for a typical 3A to 4A charging current.

OUTPUT CAPACITOR

The output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current I_{COUT} is given as:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE}$$

(14)

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

(15)

At certain input/output voltages and switching frequencies, the voltage ripple can be reduced by increasing the output filter inductor and capacitor values.

The bq24650 has an internal loop compensator. To achieve good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 12 kHz and 17 kHz. The preferred ceramic capacitor has a 35V or higher rating, X7R or X5R.

Ceramic capacitors show a de-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high voltages and small capacitor packages. See the manufacturer's datasheet about performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to achieve the required value at the operating point.

POWER MOSFETS SELECTION

Two external N-channel MOSFETs are used for a synchronous switching battery charger. The gate drivers are internally integrated into the IC with 6V of gate drive voltage. 30V or higher voltage rating MOSFETs are preferred for 20V input voltage, and 40V or higher rating MOSFETs are preferred for 20V to 28V input voltage.

Figure-of-merit (FOM) is usually used for selecting a proper MOSFET based on a tradeoff between conduction loss and switching loss. For a top-side MOSFET, FOM is defined as the product of the MOSFET's on-resistance, $R_{DS(on)}$, and the gate-to-drain charge, Q_{GD}. For a bottom-side MOSFET, FOM is defined as the product of the MOSFET's on-resistance, $R_{DS(on)}$, and the total gate charge, Q_G.

$$FOM_{top} = R_{DS(on)} \times Q_{GD}; \; FOM_{bottom} = R_{DS(ON)} \times Q_G \tag{16}$$

The lower the FOM value, the lower the total power loss. Usually a lower $R_{DS(on)}$ has a higher cost with the same package size.

Top-side MOSFET loss includes conduction loss and switching loss. It is a function of duty cycle ($D = V_{OUT}/V_{IN}$), charging current (I_{CHG}), the MOSFET's on-resistance $R_{DS(on)}$, input voltage (V_{IN}), switching frequency (F), turn-on time (t_{on}) and turn-off time (t_{off}):

$$P_{top} = D \times I_{CHG}^2 \times R_{DS(ON)} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times (t_{on} + t_{off}) \times F \tag{17}$$

The first item represents the conduction loss. Usually MOSFET $R_{DS(ON)}$ increases by 50% with 100°C junction temperature rise. The second term represents switching loss. The MOSFET turn-on and turn-off times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}}; \; t_{off} = \frac{Q_{SW}}{I_{off}} \tag{18}$$

where Q_{SW} is the switching charge, I_{on} is the turn-on gate driving current, and I_{off} is the turn-off gate driving current. If the switching charge is not given in the MOSFET datasheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}):

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS} \tag{19}$$

The gate driving current total can be estimated by the REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{PLT}), total turn-on gate resistance (R_{on}), and turn-off gate resistance (R_{off}) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}}; \; I_{off} = \frac{V_{plt}}{R_{off}} \tag{20}$$

The conduction loss of the bottom-side MOSFET is calculated with the following equation when it operates in synchronous continuous conduction mode:

$$P_{bottom} = (1-D) \times I_{CHG}^2 \times R_{DS(ON)} \tag{21}$$

If the SRP-SRN voltage decreases below 5mV (the charger is also forced into non-synchronous mode when the average SRP-SRN voltage is lower than 1.25mV), the low-side FET is turned off for the remainder of the switching cycle to prevent negative inductor current.

As a result, all of the freewheeling current goes through the body diode of the bottom-side MOSFET. The maximum charging current in non-synchronous mode can be up to 0.9A (0.5A typ) for a 10-mΩ charging current sensing resistor, considering the IC tolerance. Choose a bottom-side MOSFET with either an internal Schottky or body diode capable of carrying the maximum non-synchronous mode charging current.

MOSFET gate driver power loss contributes to dominant losses on the controller IC, when the buck converter is switching. Choosing a MOSFET with a small Q_{g_total} reduces power loss to avoid thermal shutdown.

$$P_{ICLOSS\_Driver} = V_{IN} \times Q_{g\_total} \times f_s \tag{22}$$

Where Q_{g_total} is the total gate charge for both the upper and lower MOSFETs at 6V V_{REGN}.

INPUT FILTER DESIGN

During adapter hot plug-in, the parasitic inductance and the input capacitor from the adapter cable form a second order system. The voltage spike at the VCC pin may be beyond the IC maximum voltage rating and damage the IC. The input filter must be carefully designed and tested to prevent an over-voltage event on the VCC pin.

There are several methods to damping or limiting the over-voltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the over-voltage spike well below the IC maximum pin voltage rating. A high current capability TVS Zener diode can also limit the over-voltage level to an IC safe level. However, these two solutions may not be lowest cost or smallest size.

A cost effective and small size solution is shown in Figure 21. R1 and C1 are composed of a damping RC network to damp the hot plug-in oscillation. As a result, the over-voltage spike is limited to a safe level. D1 is used for reverse voltage protection for the VCC pin. C2 is the VCC pin decoupling capacitor and it should be placed as close as possible to the VCC pin. R2 and C2 form a damping RC network to further protect the IC from high dv/dt and high voltage spike. The C2 value should be less than the C1 value so R1 can dominant the equivalent ESR value to get enough damping effect for hot plug-in. R1 and R2 must be sized enough to handle in-rush current power loss according to the resistor manufacturer's datasheet. The filter component values always need to be verified with a real application.
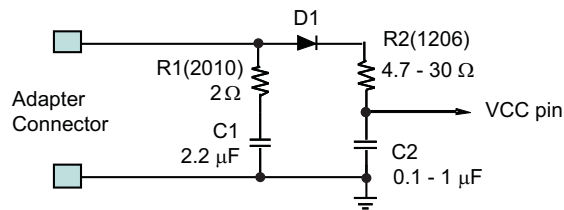

Figure 21. Input Filter

MPPT TEMPERATURE COMPENSATION

A typical solar panel comprises of alot of cells in a series connection, and each cell is a forward-biased p-n junction. So, the open-circuit voltage (V_{OC}) of a solar cell has a temperature coefficient that is similar to a common p-n diode, or about –2mV/°C. A crystalline solar panel specification always provides both open-circuit voltage V_{OC} and peak power point voltage V_{MP}. The difference between V_{OC} and V_{MP} can be approximated as fixed and temperature-independent, so the temperature coefficient for the peak power point is similar to that of V_{OC}. Normally, panel manufacturers specify the 25°C values for V_{OC} and V_{MP}, and the temperature coefficient for V_{OC}, as shown in the following figure.
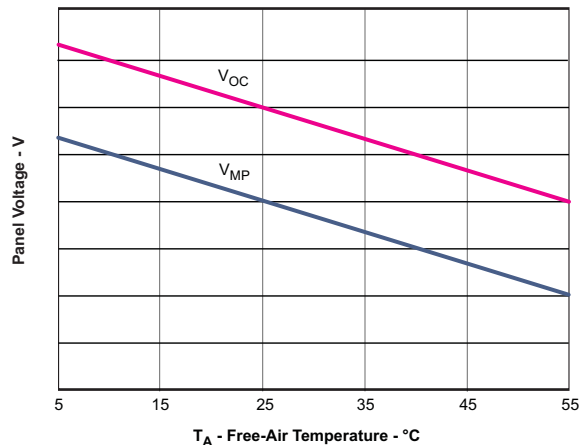
Figure 22. Solar Panel Output Voltage Temperature Characteristics

The bq24650 employs a feedback network to the MPPSET pin to program the input regulation voltage. Because the temperature characteristic for a typical solar panel V_{MP} voltage is almost linear, a simple solution for tracking this characteristic can be implemented by using an LM234 3-terminal current source, which can create an easily programmable, linear temperature dependent current to compensate the negative temperature coefficient of the solar panel output voltage.

Figure 23. Feedback Network

In the circuit shown in Figure 23, for the LM234 temperature sensor,
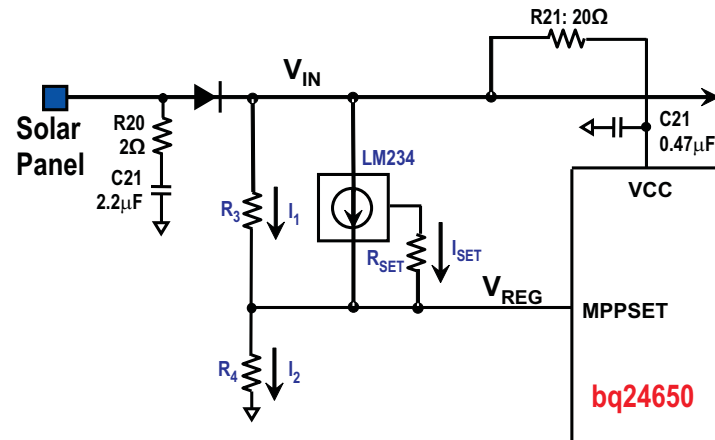
$$I_{SET} = \frac{227 \text{ μV/°K}}{R_{SET}} \times \text{Temp} \tag{23}$$

Thus,

$$I_{SET}(25°C) = \frac{0.0677V}{R_{SET}} \tag{24}$$

The current node equation is,

$$I_2 = \frac{V_{REG}}{R_4} = I_1 + I_{SET} = \frac{V_{IN} - V_{REG}}{R_3} + I_{SET} \tag{25}$$

To have a zero temperature coefficient on V_{REG},

$$\frac{dI_2}{dT} = \frac{d(V_{IN} - V_{REG})}{dT} \times \frac{1}{R_3} + \frac{dI_{SET}}{dT} = 0 \tag{26}$$

$$R_3 = \left(\frac{-dV_{IN}/dT}{dI_{SET}/dT}\right) = R_{SET} \times \frac{2mV \times \text{number of solar cells in series}}{227μV} \tag{27}$$

$$R_4 = \frac{V_{REG} \times R_3}{(V_{IN} + R_3 \times I_{SET}) - V_{REG}} = \frac{V_{MPPSET} \times R_3}{\left(V_{MP}(25°C) + R_3 \times \frac{0.0677V}{R_{SET}}\right) - V_{MPPSET}} \tag{28}$$

For example, given a common 18-cell solar panel that has the following specified characteristics:
   Open circuit voltage (V_{OC}) = 10.3V
   Maximum power voltage (V_{MP}) = 9V
   Open-circuit voltage temperature coefficient (V_{OC}) = −38mV/°C

Appling the following parameters into the equations of R_3 and R_4:

 1. Temperature coefficient for V_{MP} (same as that of V_{OC}) of −38mV/°C

 2. Peak power voltage of 9V

 3. MPPSET regulation voltage of 1.2V

And choosing R_{SET} = 1000Ω.

The resistor values are R_{SET} = 1kΩ, R_3 = 167.4kΩ, and R_4=10.6kΩ. Selecting standard 1% accuracy resistors and R_{SET} = 1kΩ, R_3 = 169kΩ, and R_4=10.7kΩ.

PCB LAYOUT

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize the high frequency current path loop (see Figure 24) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. The following is a PCB layout priority list for proper layout. Layout of the PCB according to this specific order is essential.

1. Place input capacitor as close as possible to the switching MOSFET supply and ground connections and use the shortest copper trace connection. These parts should be placed on the same layer of the PCB instead of on different layers and using vias to make this connection.
2. The IC should be placed close to the switching MOSFET gate terminals, and the gate drive signal traces kept short for a clean MOSFET drive. The IC can be placed on the other side of the PCB of the switching MOSFETs.
3. Place the inductor input terminal as close as possible to the switching MOSFET output terminal. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
4. The charging current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in the same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path (see Figure 25 for Kelvin connection for best current accuracy). Place decoupling capacitor on these traces next to the IC.
5. Place output capacitor next to the sensing resistor output and ground.
6. Output capacitor ground connections need to be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
7. Route analog ground separately from power ground and use a single ground connection to tie charger power ground to charger analog ground. Just beneath the IC use analog ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling. Connect analog ground to the GND pin. Use the thermal pad as a single ground connection point to connect analog ground and power ground together, or use a 0-Ω resistor to tie analog ground to power ground (thermal pad should tie to analog ground in this case). A star-connection under the thermal pad is highly recommended.
8. It is critical that the exposed thermal pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
9. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
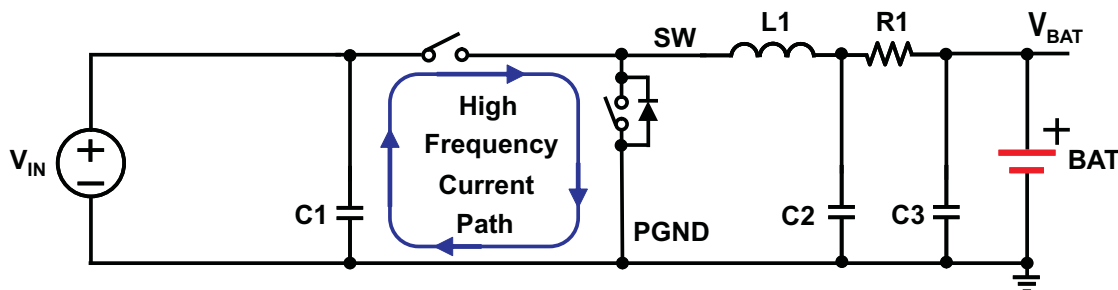10. The number and physical size of the vias should be enough for a given current path.

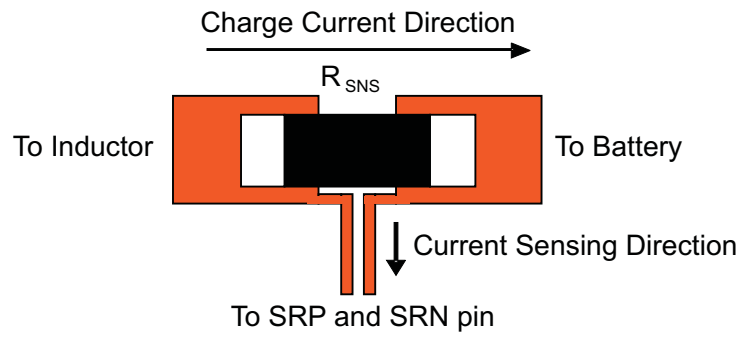**Figure 24. High Frequency Current Path**

Charge Current Direction

R_{SNS}

To Inductor

To Battery

Current Sensing Direction

To SRP and SRN pin

Figure 25. Sensing Resistor PCB Layout

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
BQ24650RVAR	ACTIVE	VQFN	RVA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
BQ24650RVAT	ACTIVE	VQFN	RVA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24650RVAR	VQFN	RVA	16	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
BQ24650RVAT	VQFN	RVA	16	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION
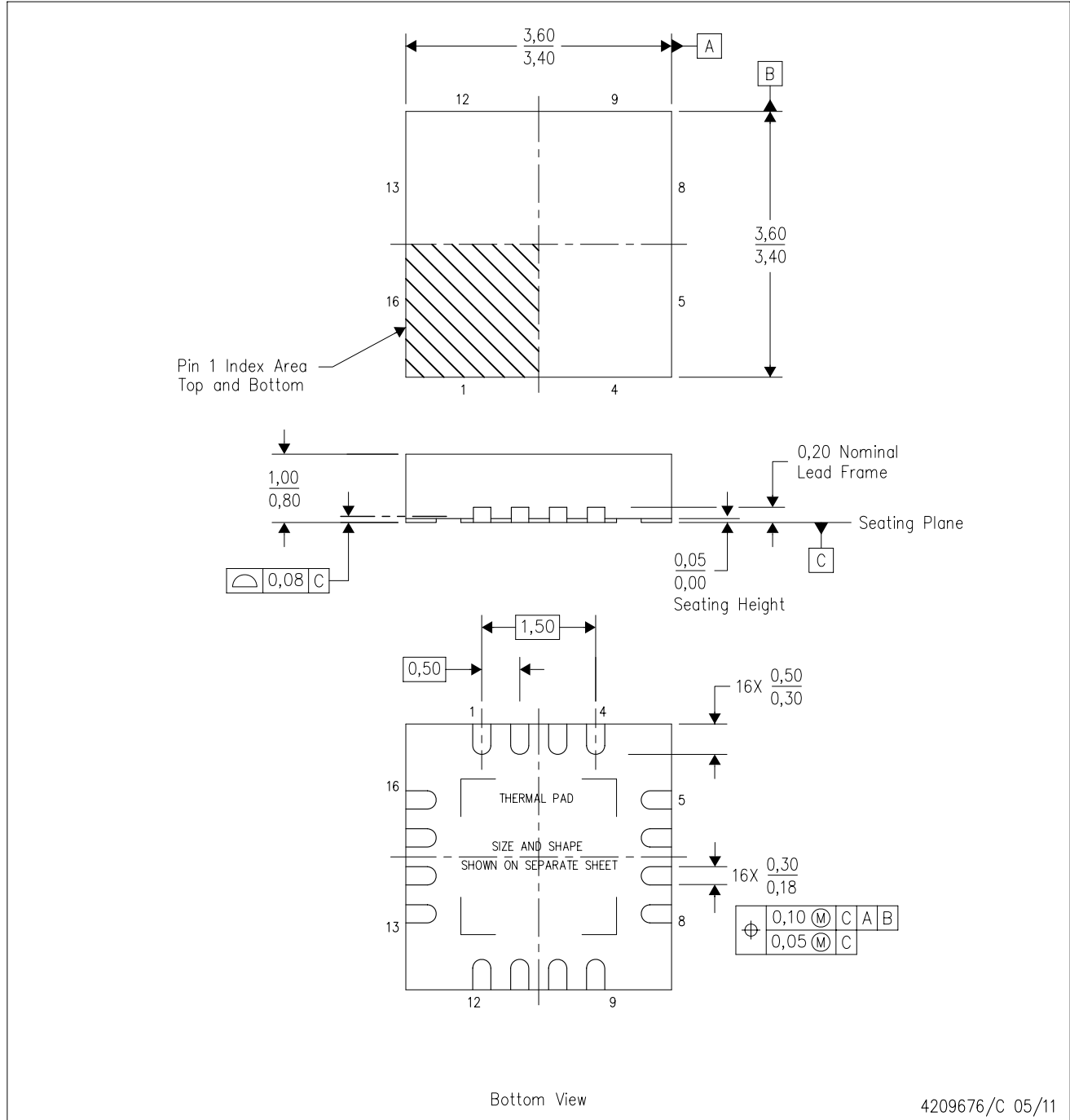
TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24650RVAR	VQFN	RVA	16	3000	346.0	346.0	29.0
BQ24650RVAT	VQFN	RVA	16	250	210.0	185.0	35.0

RVA (S−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

3,60 / 3,40   A
B

12   9

13   8

3,60 / 3,40

16   5

Pin 1 Index Area
Top and Bottom

1   4

1,00 / 0,80

0,20 Nominal
Lead Frame

Seating Plane

0,05 / 0,00
Seating Height

0,08 C

1,50

0,50

16X 0,50 / 0,30

1   4

16   5

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

16X 0,30 / 0,18

13   8

0,10 Ⓜ C A B
0,05 Ⓜ C

12   9

Bottom View

4209676/C 05/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No−Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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RVA (S−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
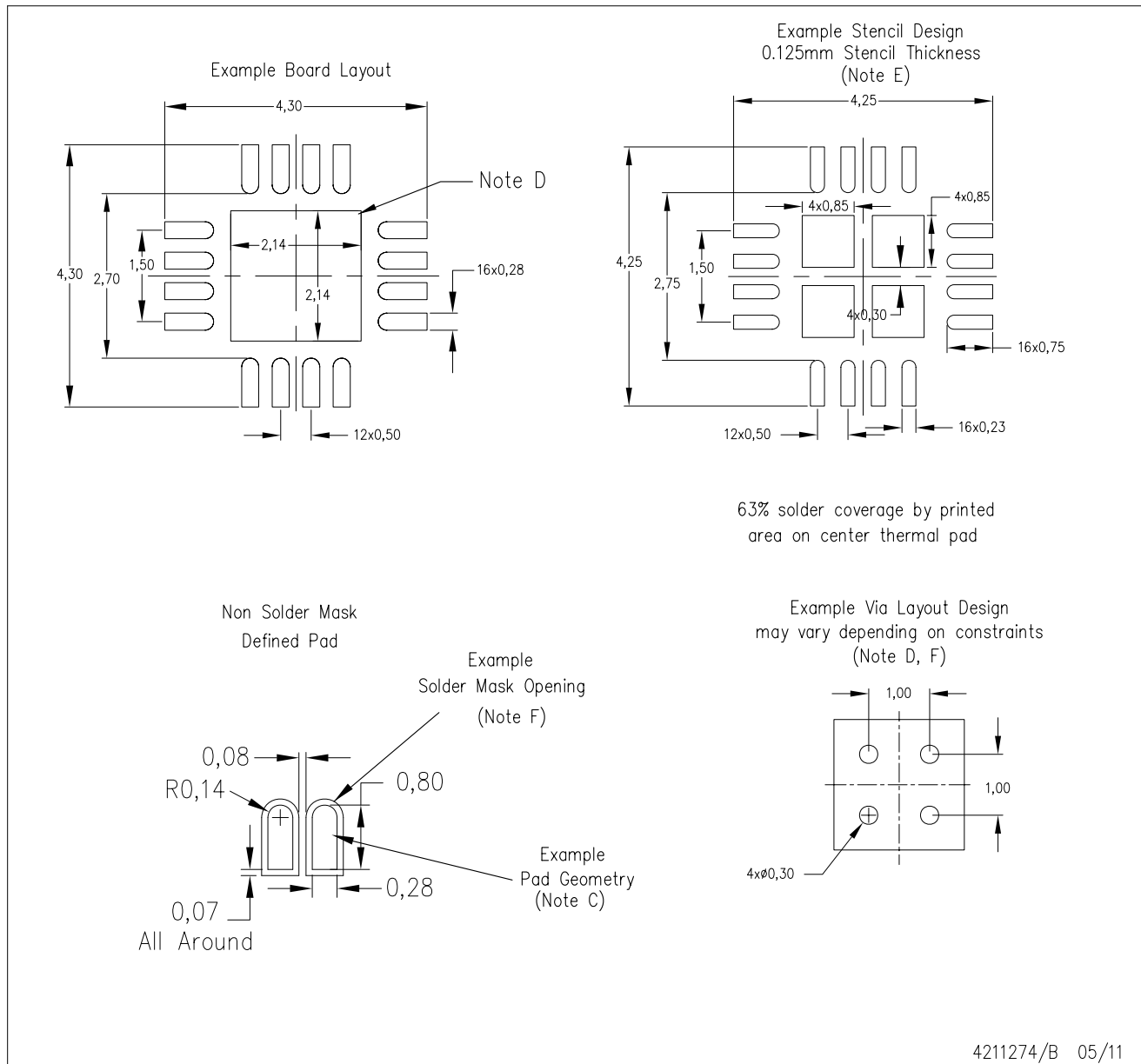

Bottom View

Exposed Thermal Pad Dimensions
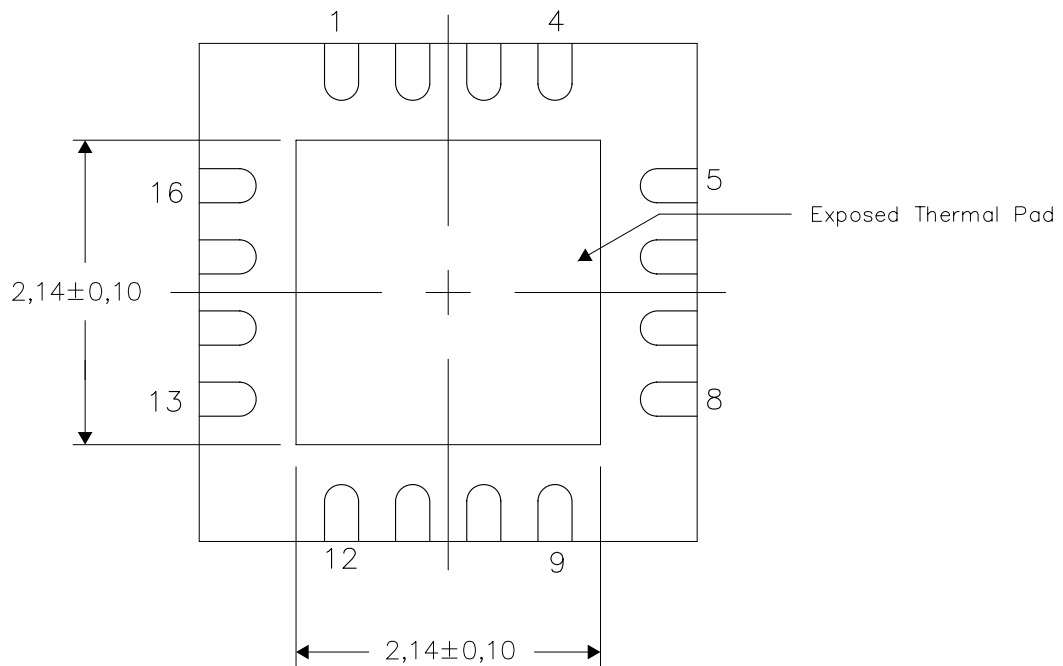
4209715/B   05/11

NOTE: All linear dimensions are in millimeters

RVA (S-PVQFN-N16)   PLASTIC QUAD FLATPACK NO-LEAD

Example Board Layout

Note D

4,30
4,30 2,70
1,50
2,14
2,14
16x0,28
12x0,50

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

4,25
4,25 2,75
1,50
4x0,85
4x0,85
4x0,30
16x0,75
12x0,50
16x0,23

63% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08
R0,14
0,80
0,28
0,07
All Around

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

1,00
1,00
4xø0,30

4211274/B 05/11

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC-7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack
            QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout.
            These documents are available at www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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