Arquitectura de Computadores Avançada

Grupo 1

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Parallel Encoder

$$G = \begin{Vmatrix} 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{Vmatrix}$$

X0 = M4

X1 = M4 ⊕ M1

X2 = M4 ⊕ M2

X3 = M4 ⊕ M1 ⊕ M2

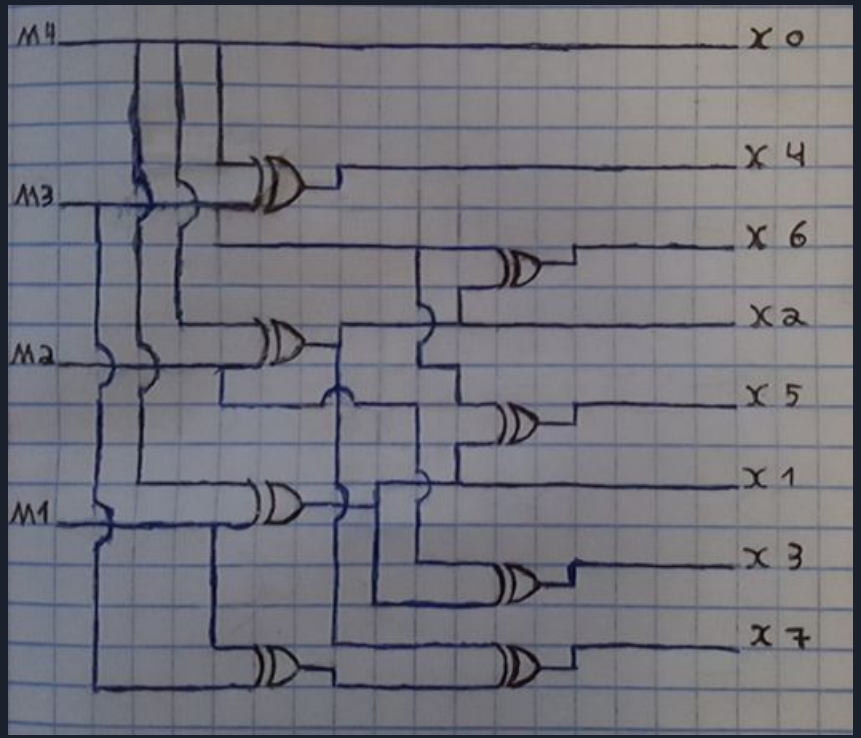
X4 = M4 ⊕ M3

X5 = M4 ⊕ M1 ⊕ M3

X6 = M4 ⊕ M2 ⊕ M3

X7 = M4 ⊕ M2 ⊕ M3 ⊕ M1

Parallel Encoder



Parallel Decoder

$C01 = X0 \oplus X1$
$C02 = X2 \oplus X3$
$C03 = X4 \oplus X5$
$C04 = X6 \oplus X7$

$C11 = X0 \oplus X2$
$C12 = X1 \oplus X3$
$C13 = X4 \oplus X6$
$C14 = X5 \oplus X7$

$C21 = X0 \oplus X4$
$C22 = X1 \oplus X5$
$C23 = X2 \oplus X6$
$C24 = X3 \oplus X7$

$M1 = C01 \bullet C02 \bullet (C03 + C04) + C03 \bullet C04 \bullet (C01 + C02)$
$M2 = C11 \bullet C12 \bullet (C13 + C14) + C13 \bullet C14 \bullet (C11 + C12)$
$M3 = C21 \bullet C22 \bullet (C23 + C24) + C23 \bullet C24 \bullet (C21 + C22)$

$\overline{Z1} = (C01 + C02 + (C03 \bullet C04)) \bullet (C03 + C04 + (C01 \bullet C02))$

$\overline{Z2} = (C11 + C12 + (C13 \bullet C14)) \bullet (C13 + C14 + (C11 \bullet C12))$

$V1 = C02 \oplus C03 \oplus C04$
$V2 = C12 \oplus C13 \oplus C14$
$Valid = V1 \bullet V2$

$D1 = M1 + Z1$
$D2 = M2 + Z2$

$M4 = \overline{D1 + D2} \bullet [C01 \oplus M1] \oplus X0$

Parallel Decoder