Politecnico di Torino
Circuit Theory

Switching behaviour of a Bistable circuit

Mattia Antonini.

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Abstract

Switching behaviour analysis of a Bistable circuit, circuit model, simulation by LTSpice.

1 Introduction

A **Bistable circuit** is an electronic circuit, usually an integrated circuit, whose output has two stable states to which it is directed by the input signal or signals. It is more usually known as a flip-flop. Binary states denote logic '1' and '0'. A Bistable circuit is implemented as in the following Fig. 1 and it is based on an negative-resistance converter.

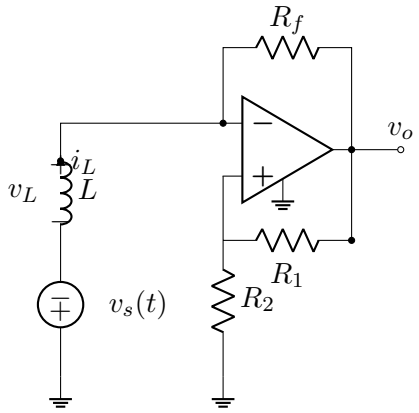

Figure 1: Bistable circuit based on OpAmp

2 Negative-resistance converter

A negative-resistance converter is shown here below in Fig. 2. Our task is to determine the driving-point characteristic of the Negative-resistance converter in the $i - v$ plane. We will analyze the behaviour of the Bistable circuit in the different regions of the driving-point characteristic. We will replace the OpAmp of Fig. 2 by three circuit models for each of the regions where the Bistable circuit can work: the Linear region, the +Saturation region, the -Saturation region and for each of them the transient will be analyzed in depth.

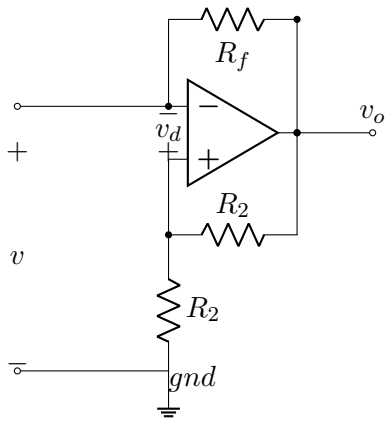

Figure 2: Negative-resistance converter

2.1 Linear region

The OpAmp working in the Linear region can be modeled as in the next Fig. 3. By inspection of

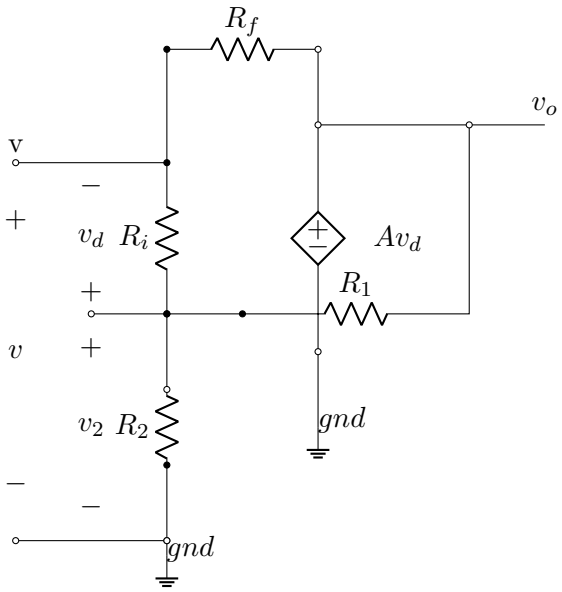

Figure 3: Negative-resistance converter: linear region

the equivalent circuit in Fig. 3 we note that R_1 and R_2 constitute a voltage divider so that

$$v_2 = \frac{R_2}{R_1 + R_2} v_0 = \beta v_0 \tag{1}$$

In the linear region $v_d = 0$ and so we can assume that $v = v_2$. Hence the previous equation (1) can be re-written as

$$v = \beta v_o \tag{2a}$$

$$v_o = \frac{v}{\beta} \tag{2b}$$

Applying KVL we obtain

$$v = R_f i + v_o \tag{3}$$

Substituting Equation (3) into Equation(2a), we obtain

$$i = -\left(\frac{R_1}{R_2}\right)\left(\frac{1}{R_f}\right) v \tag{4}$$

To determine the boundary of these segments substitute equation(2a) into the validating inequality

$$-E_{sat} \leq v_o \leq E_{sat} \tag{5}$$

Hence we get

$$-\beta E_{sat} \leq v \leq \beta E_{sat} \tag{6}$$

Equation(6) determines the range of validity for the input voltage v in the Linear region.
It is important to remark that in this region the slope of the $i-v$ line is negative with value $-\frac{R_1}{R_2 R_f}$.
Thus, we can claim that the resistance of the equivalent Norton circuit is

$$\frac{v}{i} = -\frac{R_2 R_f}{R_1} \tag{7}$$

The Bistable circuit in the Linear region can be modeled by the Norton equivalent circuit with a negative resistance, no source current, coupled to the inductor, show in Fig. 4.

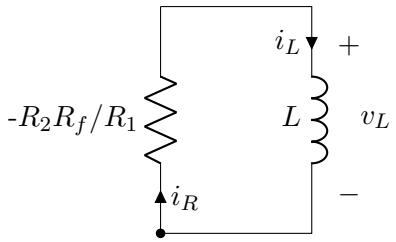

Figure 4: Norton equivalent circuit for the OpAmp in the 'Linear' region

2.2 + Saturation region

When the OpAmp is operating on the '+ Saturation' the output voltage is E_{sat}. Hence the controlled voltage source of the 'Linear' region can be replaced by a battery with value E_{sat}.

By inspection of the equivalent circuit in Fig. 5 and following the same procedure as above, we obtain

$$v = R_f i + E_{sat} \tag{8}$$

and so we get

$$i = \frac{v}{R_f} - \frac{E_{sat}}{R_f} \tag{9a}$$

$$v_o = E_{sat} \tag{9b}$$

To determine the range of v for which the previous two equations are valid, we solve for v_d by applying KVL around the closed node sequence of the output stage of the OpAmp

$$v_d = \frac{R_2}{R_1 + R_2} E_{sat} - v = \beta E_{sat} - v \tag{10}$$

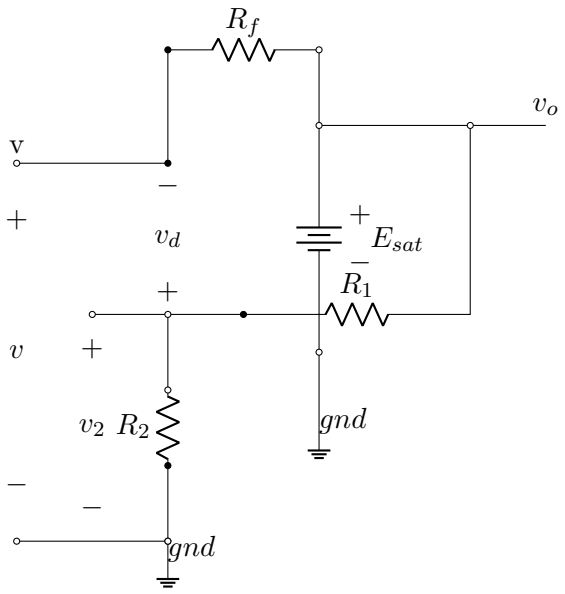

Figure 5: Bistable circuit: + Saturation region

The validating inequality for the '+ Saturation' region is

$$v_d > 0 \tag{11}$$

Hence we obtain

$$v < \beta E_{sat} \tag{12}$$

The Norton equivalent circuit for the '+ Saturation' region is shown here below in Fig. 6.

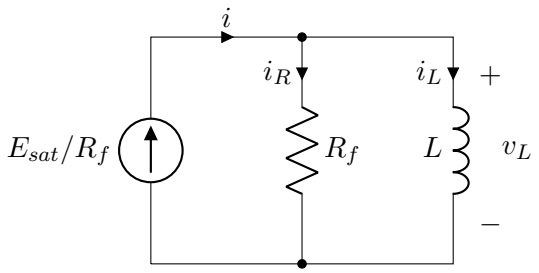

Figure 6: Norton equivalent circuit for the OpAmp in the '+ Saturation' region

2.3 - Saturation region

The OpAmp working in the '- Saturation' region can be modeled as in the following picture Fig. 7.

By inspection of this circuit in Fig. 7 and following the same procedure as above we obtain

$$v = R_f i - E_{sat} \tag{13}$$

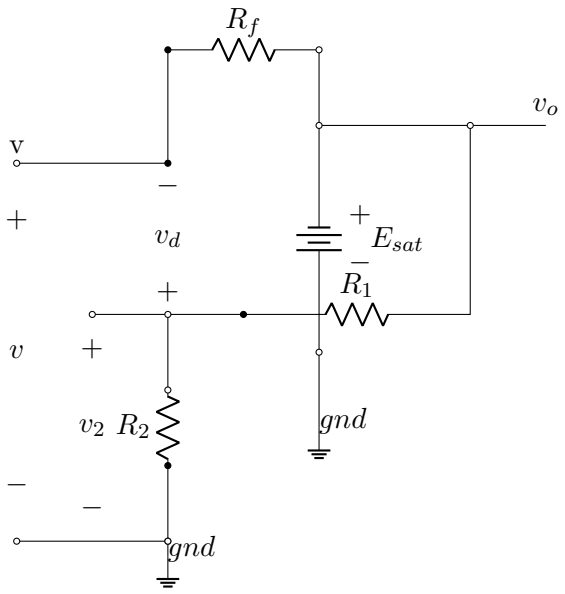

Figure 7: Bistable circuit: - Saturation region

that leads to

$$i = \frac{v}{R_f} + \frac{E_{sat}}{R_f} \tag{14a}$$

$$v_o = -E_{sat} \tag{14b}$$

$$v > -\beta Esat \tag{14c}$$

The Norton equivalent circuit is shown here below in Fig. 8.

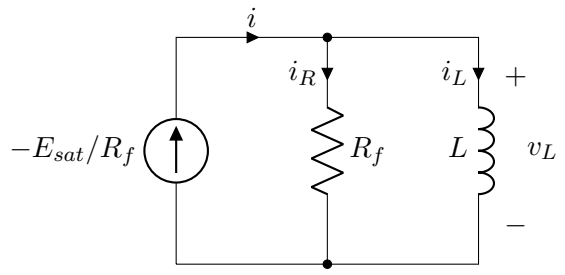

Figure 8: Norton equivalent circuit for the OpAmp in the '- Saturation' region

3 Circuit and driving-point characteristic

As we have explained previously, a Bistable circuit can be implemented by the circuit shown in Fig. 1. Further the driving-point characteristic obtained in the previous paragraphs is shown here below. Consider first the case where $v_s(t) = 0$ so that the inductor is directly connected across the circuit. Since $\frac{di(t)}{dt} = -v(t)/L$ and $L > 0$, it follows that $\frac{di(t)}{dt} > 0$ whenever $v < 0$ and $\frac{di(t)}{dt} < 0$ whenever $v > 0$.

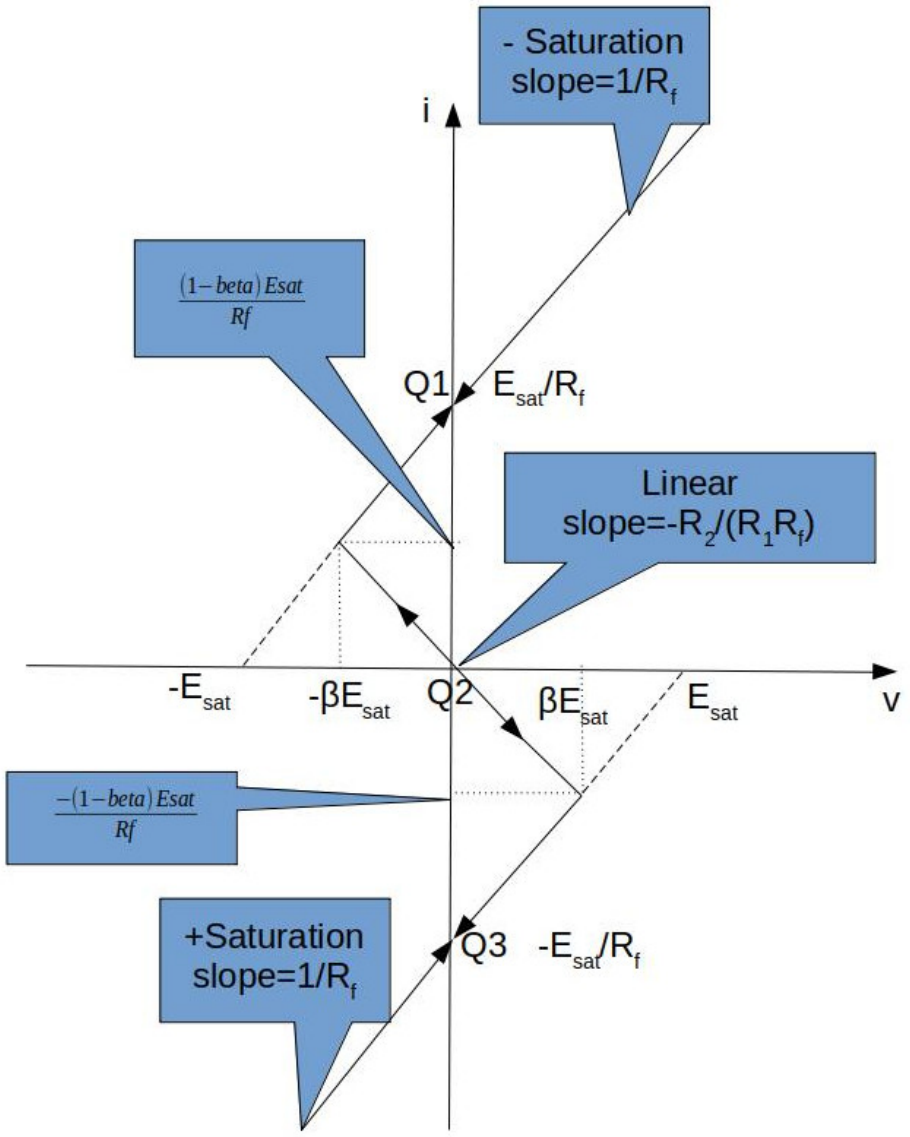

Figure 9: Bistable circuit: driving-point characteristic.

Hence, the current i decreases in the right half $v-i$ plane and increases in the left half $v-i$ plane, as depicted by the typical dynamic routes in Fig. 9.
Since the equilibrium state of a first order RL circuit is determined by replacing the inductor by a short circuit, i.e. $v = v_L = 0$, it follows that this circuit has three equilibrium points: Q_1, Q_2 and Q_3. These equilibrium points are the operating points of the associated resistive circuit obtained by short-circuiting the inductor L.
Since the dynamic route in Fig. 9 either tends to Q_1 or Q_3, but always diverges from Q_2, we say that the equilibrium point Q_2 is unstable. Hence even though the associated resistive circuit has three operating points, Q_2 can never be observed in practice (the slightest noise voltage will cause the dynamic route to diverge from Q_2, even if the circuit is operating initially at Q_2.
Whether Q_1 or Q_3 is actually observed depends on the initial condition. Such a circuit is said to be bistable.

Bistable circuits (flip-flops) are used extensively in digital computers, where the two stable equilibrium points correspond to the two binary states; say Q_1 denotes $'0'$ and Q_3 denotes $'1'$.
In order to perform logical operations, it is essential to switch from Q_1 to Q_3 and vice versa. This is done by using a small triggering signal. We will now show how the voltage source in Fig. 1 serves as a triggering signal.

4 Some helpful equations

As we have shown previously the Bistable circuit can be modeled as three RL circuits for each of the regions where it can work (Linear, +Saturation, -Saturation). In the following analysis it will be helpful to evaluate at what time t_k the current $i(t)$ through the inductor gets a specific value $i(t_k)$ knowing the initial time t_j, the current value $i(t_\infty)$ for $t \to +\infty$ (or for $t \to -\infty$). Hence the following formula will be used along the way.

$$t_k - t_j = \tau log\left(\frac{i(t_j) - i(t_\infty)}{i(t_k) - i(t_\infty)}\right) \tag{15}$$

This formula doesn't depend on whether τ is positive or negative. It will be used also for the linear region where the G_{eq} is negative ($-\frac{R_1}{R_2 R_f}$).
It will be useful also to compute the value of the current $i(t)$ at a specific time knowing the initial current value $i(t_0)$ and the current value $i(t_\infty)$ for $t \to +\infty$ (or for $t \to -\infty$).

$$i(t) = i(t_\infty) + [i(t_0) - i(t_\infty)]e^{\frac{-(t-t_0)}{\tau}} \tag{16}$$

which holds for all times t, i.e. $-\infty < t < +\infty$ and for τ positive or negative (in the Linear region). Depending on whether τ is positive or negative, the exponential waveform tends either to a constant or to ∞ as the time t tends to ∞. The switching analysis will start from a known stable point (Q_1 for instance) and then applying a voltage impulse to the inductor voltage in order to force a transient. Then the inductor current will move along the piecewise characteristic in the $i - v$ plane.

5 Switching analysis

Assume that the circuit first is working in Q_1. We know that this is a stable equilibrium point. A constant (negative) current i_L is flowing through the inductor L. The voltage across the inductor L is 0. The OpAmp is working in saturation (-Saturation region) and, thus, its output voltage is $v_o = -E_{sat}$.

$$v_o = -E_{sat} \tag{17a}$$

$$v = 0 \tag{17b}$$

$$v_d = v_2 - 0 = \frac{R_2}{R_1 + R_2} v_o = -\frac{R_2}{R_1 + R_2} E_{sat} < 0 \tag{17c}$$

$$i = \frac{v - v_o}{R_f} = \frac{0 - (-E_{sat})}{R_f} = \frac{E_{sat}}{R_f} \tag{17d}$$

The derivative of the current $\frac{di_L(t)}{dt}$ is '0'. The circuit will not move from this point unless a triggering signal will be applied by the voltage source $v_s(t)$ (see Fig. 1).
Let us at $t = t_1$ apply a square pulse of width $T = t_2 - t_1$ and amplitude E (see Fig. 10).

$$E_s(t) = E(u(t_1) - u(t_2)) \tag{17e}$$

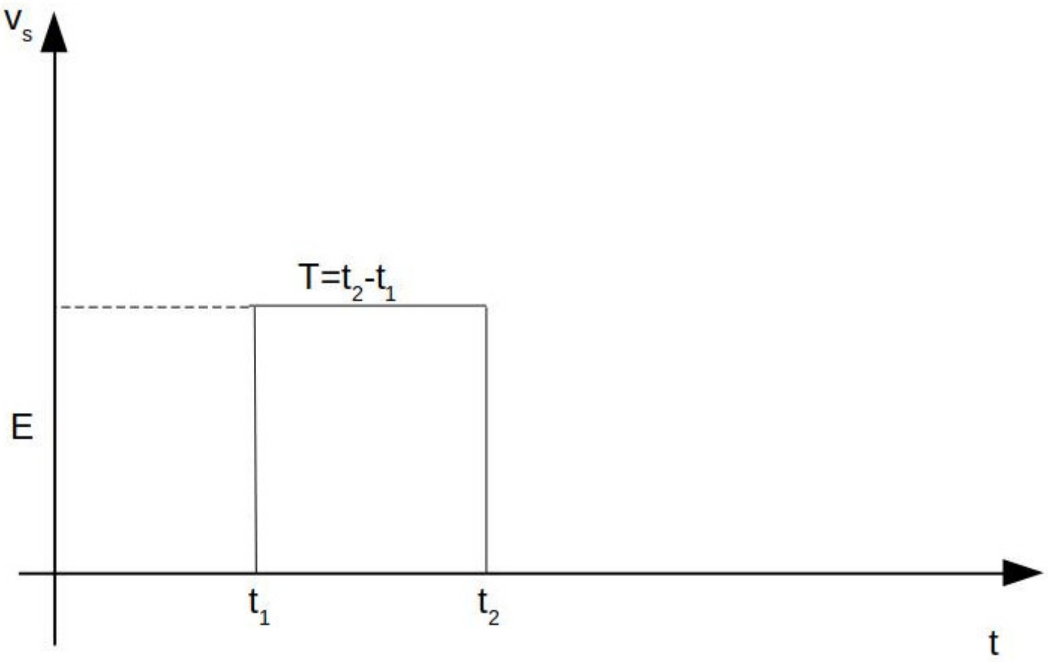

Figure 10: Triggering positive pulse.

During the time interval $t_1 \leq t \leq t_2$, $v_s(t)$ can be replaced by a battery E so that the inductor sees a translated driving-point characteristic as show in the following figure in broken line segments. Now the voltage across the inductor is greater than '0'. In other words the two pins across the inductor are at different voltages, the upper is still at 0 Volts, while the lower is at $-E$ Volts. The voltage across the inductor is

$$v_L = v = E \tag{18}$$

Let us denote the original and the translated piece wise-linear driving-point characteristics by Γ and $\Gamma^{'}$ respectively. See Fig. 11. The Γ holds over the time interval $t \leq t_1$ and $t \geq t_2$, whereas $\Gamma^{'}$ holds over the time interval $t_1 \leq t \leq t_2$. Since the inductor current cannot change instantaneously $i_L(t_1^-) = i_L(t_1^+)$, the dynamic route must jump horizontally from Q_1 to P_0 at time $t = t1$. The Γ driving-point characteristic has been horizontally translated of E Volts to the right. The circuit can be modeled taking its Norton equivalent circuit as shown in Fig. 12. The conductance is the slope of the driving-point characteristic (see Fig. 9). From P_0 the current i must subsequently decrease so long as $v \geq 0$ towards P_1 with slope $\frac{1}{R_f}$. In that region the Bistable circuit is in the '-Saturation' region as indicated in Fig. 11 and so it will modeled as a RL circuit described in Fig. 8 and ruled by the equations (14a). Hence, the input current $i(t)$ to the Bistable circuit will evolve as an decreasing exponential with time constant $\tau = \frac{L}{R}$.

$$i(t) = \frac{E - E_{sat}}{R_f} + [i(P_0) - \frac{E - E_{sat}]}{R_f} e^{\frac{-t}{\tau}} \tag{19}$$

We can claim that

$$i_{P_0}(E) = i(Q_1) = \frac{E_{sat}}{R_f} \tag{20a}$$

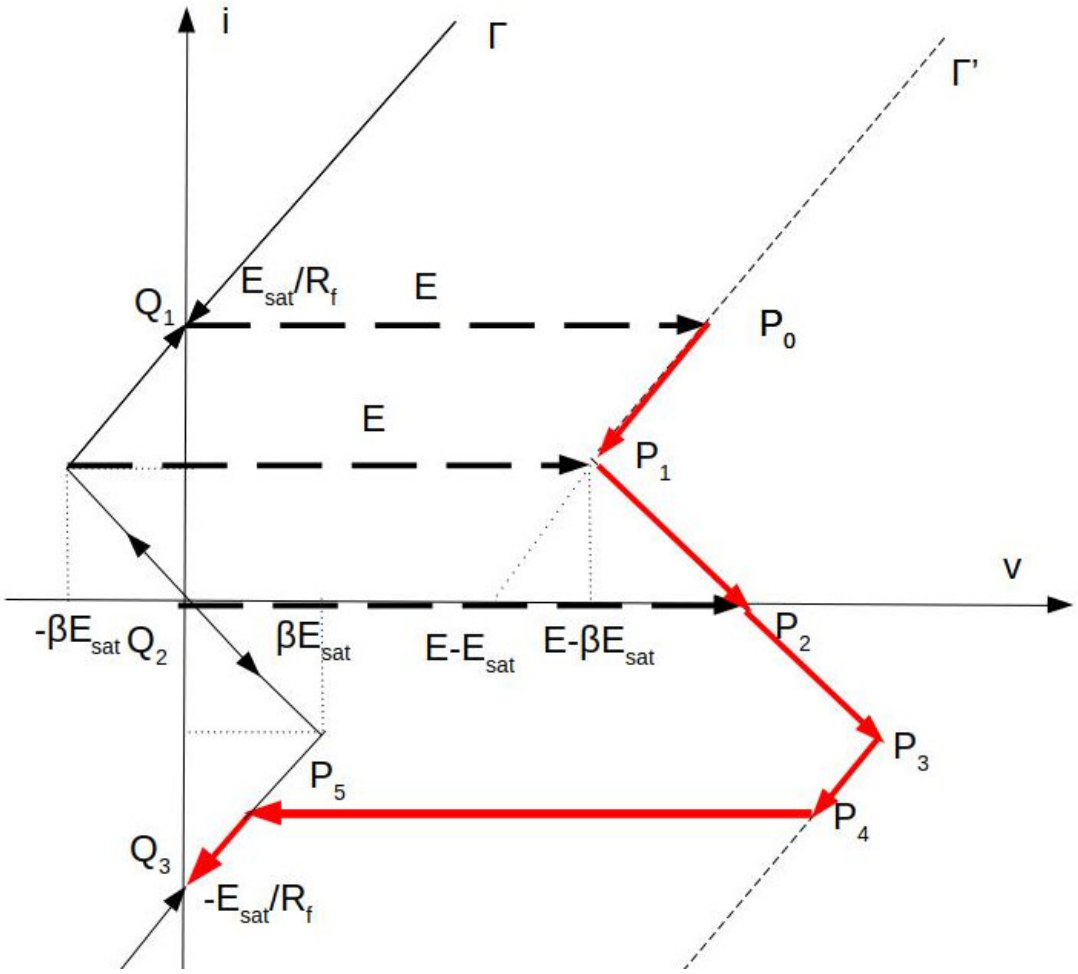

Figure 11: Translated 'driving-point' characteristic.

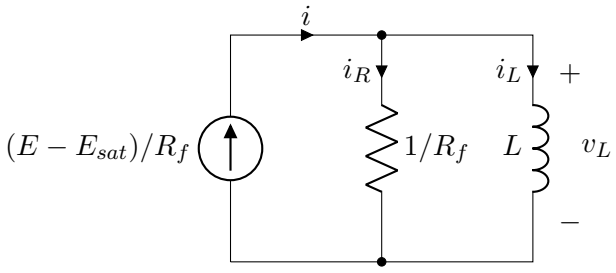

Figure 12: Norton equivalent circuit for the OpAmp in the shifted '- Saturation' region

$$i_{P_1}(E - \beta E_{sat}) = \frac{E_{sat}(1-\beta)}{R_f} \tag{20b}$$

$$i(t_\infty) = \frac{E - E_{sat}}{R_f} \tag{20c}$$

By the equation(15) after some manipulation we obtain:

$$t_{P_1} = t_{P_0} + \tau \log\left(\frac{E}{E - \beta E_{sat}}\right) \tag{20d}$$

The transient in the '- Saturation' region evolves from P_0 to P_1, but there the behaviour will be driven by the 'Linear' region (negative slope $-\frac{R_1}{R_2 R_f}$) where the Bistable circuit is ruled by the following equations and values:

$$i(t) = -\frac{R_1(v - E)}{R_2 R_f} \tag{21}$$

From the analysis in the '- saturation' region we know that

$$i(P_1) = \frac{E_{sat}(1 - \beta)}{R_f} \tag{22a}$$

$$v(P_1) = E + \beta E_{sat} \tag{22b}$$

$$i(P_3) = -i(P_1) = -\frac{E_{sat}(1 - \beta)}{R_f} \tag{22c}$$

In the 'Linear' region the time constant of the circuit has a negative value and can be expressed as

$$\tau_{lin} = \frac{L}{R_{eq}} = -\frac{R_1 L}{R_2 R_f} \tag{23}$$

In the 'Linear' region the Bistable circuit is modeled by the following Norton equivalent circuit (see Fig. 13). Because of the negative time constant τ the RL circuit is unstable and exponentially

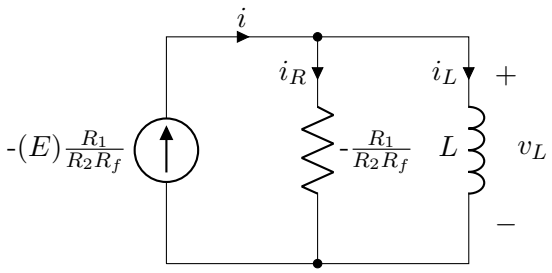

Figure 13: Norton equivalent circuit for the OpAmp in the shifted 'Linear' region

growing when t tends to ∞. The $i(t)$ function is stable when t tends to $-\infty$. The current value tends to current generator i_{eq} value $-E\frac{R1}{R_2 R_f}$ when $t \to \infty$. In the 'Linear' region the current $i(t)$ evolves according to the following exponential expression valid for $t_{P_1} < t < t_{P_3}$:

$$i(t) = (i(P_1) - i_{eq})e^{-\frac{t - t(P_1)}{\tau_{lin}}} \tag{24a}$$

$$t_{P_3} = t_{P_1} + \tau_{lin} log(\frac{i(P_1) - i(t_{-\infty})}{i_{P_3} - i(t_{-\infty})}) \tag{24b}$$

$$v(P_3) = E + E_{sat} \tag{24c}$$

In the point P_3 the behaviour of the circuit changes once more. From P_3 to P_4 the circuit works in the '+ Saturation' state. It can be modeled by the following Norton equivalent circuit shown in

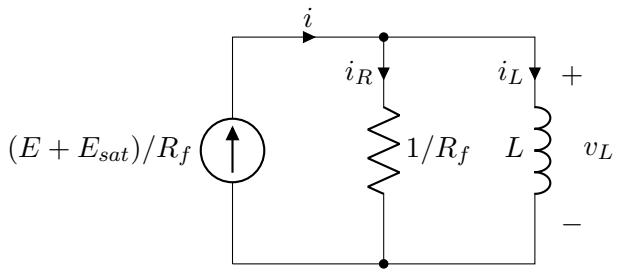

Figure 14: Norton equivalent circuit for the OpAmp in the shifted '+ Saturation' region

Fig. 14. The time constant is positive with value $\tau = \frac{L}{R_f}$. The time evaluation of the current $i(t)$ is ruled by the following expression from P_3 and beyond:

$$i(t) = \left(i(P_3) - \frac{E + E_{sat}}{R_f} \right) e^{-\frac{t - t(P_3)}{\tau}} + \frac{E + E_{sat}}{R_f} \tag{25}$$

This is a stable exponentially growing evolution that tends to the value $\frac{E+E_{sat}}{R_f}$ for $t \to \infty$.
Assume now that the t_2 occurs during this phase and so the voltage source $v_s(t)$ goes to 0. At time $t = t_2$ the driving-point characteristic Γ' switches back to Γ and the dynamic route must jump horizontally from P_4 to P_5 at $t = t_2^+$. Then, from P_5 to Q_3 the dynamic route will move along the initial driving-point characteristic until it reaches the stable point Q_3. In Q_3 the voltage $v = 0$ and also the derivative of the current through the inductor $\frac{di_L}{dt}$. Hence, the Bistable circuit will not move out from Q_3. It has been forced to change its steady state.
To trigger from Q_3, back to Q_1, simply apply a similar triggering pulse of opposite polarity, as shown in Fig.(15). The resulting dynamic route is shown in the following figure. The Bistable circuit behaviour from Q_3 to Q_1 will be based on the same concepts described in the previous section, only the direction of the dynamic route will be the opposite.

6 LTspice simulations

6.1 Schematic

The schematic entry used in LTSpice to simulate the Bistable behaviour is show in Fig. 16

6.2 Initial Conditions

In order to force the circuit to start from the stable point Q_1 specific initial conditions were required for the inductor current $i_L = -\frac{E_{sat}}{R_f}$, the input voltage ($v = 0$) and output voltage $v_o = -E_{sat}$. The initial conditions have been specified by the *.ic* directive (see the appendix for all the netlist details).

```
.ic i(L1)=-1.5m v(n002)=-15 v(n001)=0
```

6.3 First simulation: pulse width $T = 0.415\ ms$

In the first simulation the pulse width has been set to a specific value in order to reproduce the behaviour shown in Fig. 11. In other words when the pulse goes to $0V$ the dynamic route jumps

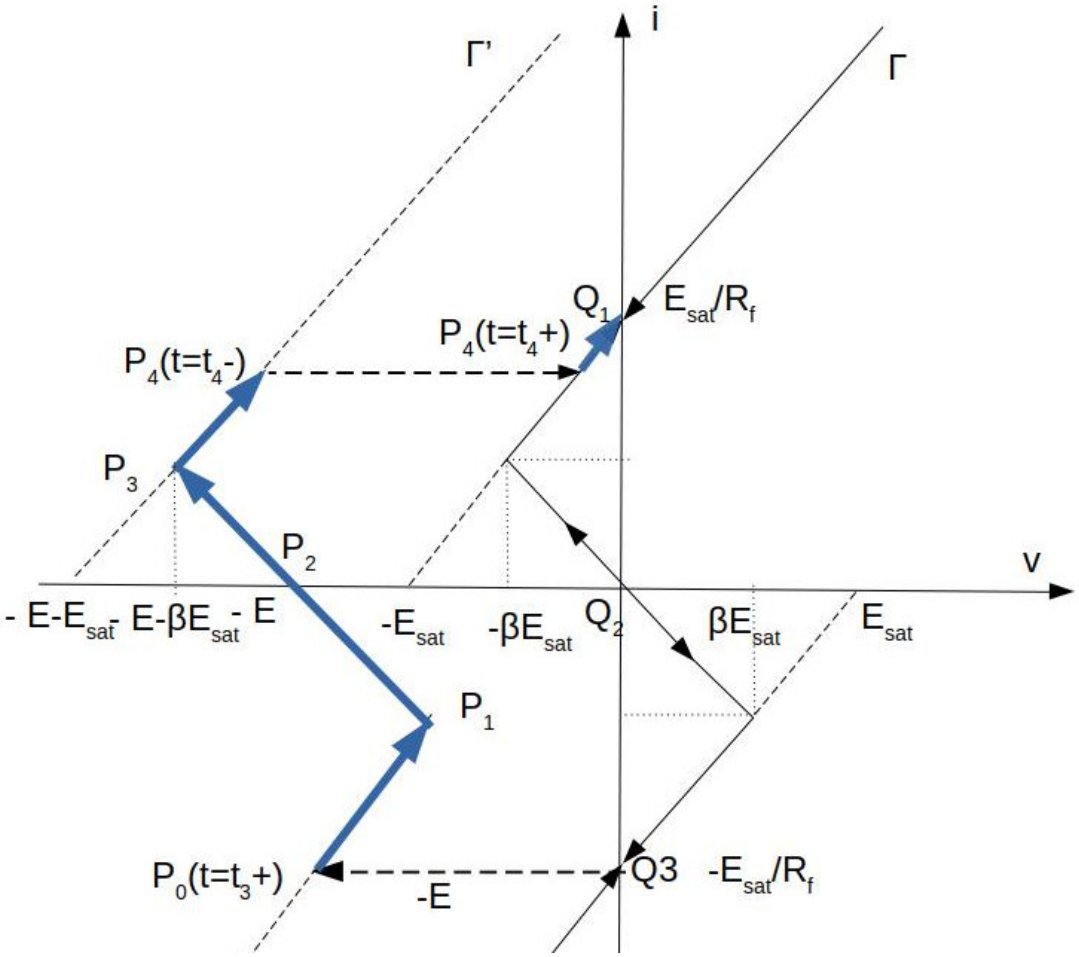

Figure 15: Triggering reset signal and translated 'driving-point' characteristic.

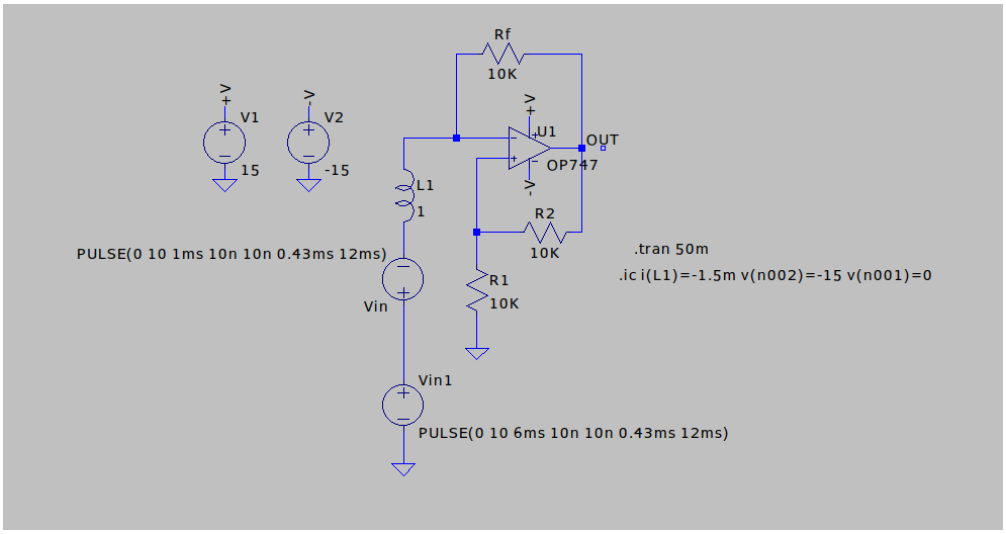

Figure 16: LTspice schematic used for simulation.

back and the point P_5 is still in the right side of the $i - v$ plane. Thus, the following transient from P_5 to Q_3 occurs as a growing exponential for i_L or a decreasing exponential for i. The SPICE syntax for a voltage source is

```
Vin1 N005 0 PULSE(0 10 6ms 10n 10n 0.415ms 12ms)
```

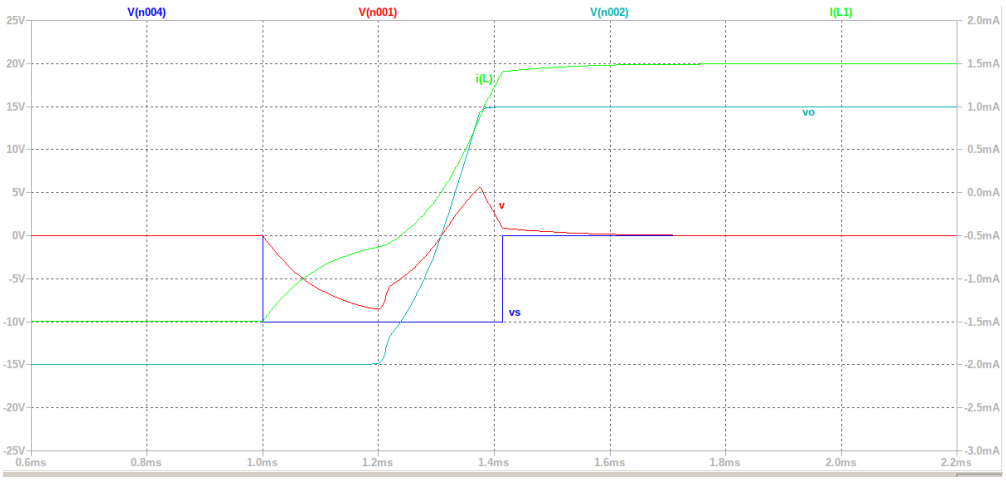

Figure 17: First simulation: $T = 0.415\ ms$, from Q_1 to Q_3.

As expected the inductor current i_L grows as an exponential with positive time constant in the phase ('- Saturation' region). In the 'Linear region' the current grows with a negative time constant. It would tends to $+\infty$ (unstable behaviour) but when the dynamic route enters the '+ Saturation' region the behaviour returns to be stable. It will grow exponentially, but it would tend to a finite value for $t \to +\infty$.
The output voltage (red line) jumps from $-E_{sat}$ (logical '0') to E_{sat} (logical '1').
The transition from Q_3 to Q_1 can be triggered by an opposite signal to the voltage source v_s as depicted in Fig. 18.

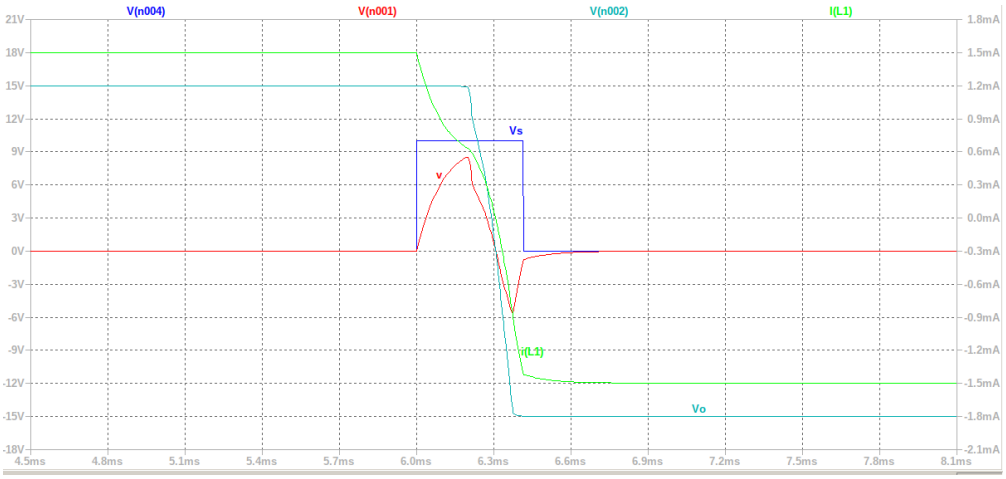

Figure 18: First simulation: T=0.415ms, from Q_3 to Q_1.

6.4 Second simulation, pulse width $T = 0.45\ ms$

In this second simulation we are going to increase the pulse width so that when the voltage source returns to 0 the dynamic route will jump in the left side of the $i - v$ plane and so the transient from $P5$ to $Q3$ will be different from the previous one.

```
Vin1 N005 0 PULSE(0 10 6ms 10n 10n 0.45ms 12ms)
```

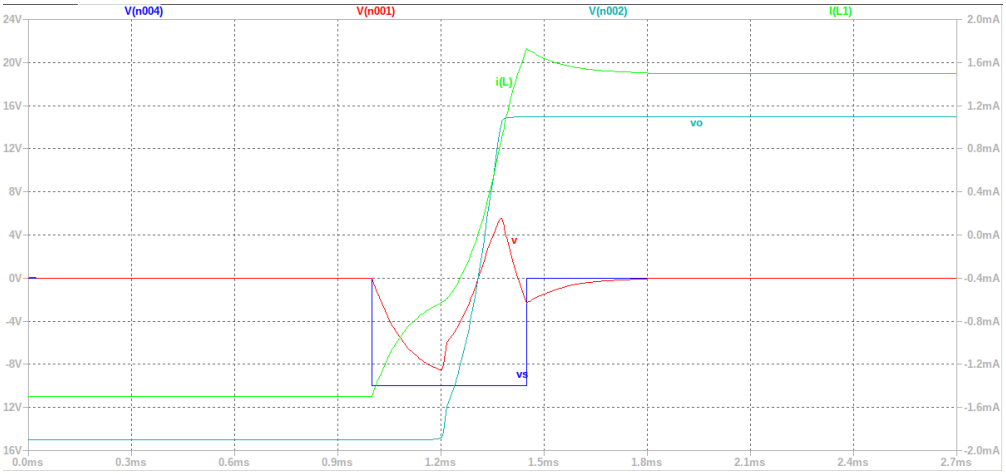

Figure 19: Second simulation: $T = 0.45\ ms$, from Q_1 to Q_3.

The different behaviour is evident at the end of the triggering pulse because the inductor current i_L has grown over the steady value and so it decreases a bit to reach the steady state.
In other words when the triggering pulse goes to 0 the point $P5$ will be in the left side of the $i - v$ plane. The output voltage (red line) will be forced to jump from the logical value 0 (Q_1) to the logical value 0 (Q_3). Fig. 20 shows the opposite transition from Q_3 to Q_1. The transient is the dual of the previous one.

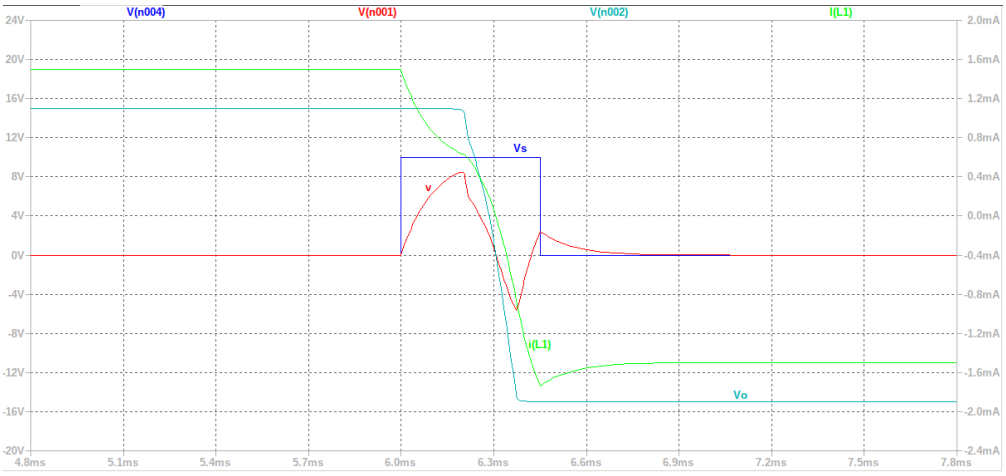

Figure 20: Second simulation: $T = 0.45\ ms$, from Q_3 to Q_1.

6.5 Third simulation, pulse width T too short, no transition

When the triggering pulse is too short the transition will not occur. The third simulation shows this (bad) behaviour. The triggering pulse width is just $0.1ms$. Hence when the triggering pulse return to 0 the dynamic route is still in the '- Saturation' region and so the dynamic route will jump back to the left side of the $i - v$ plane. The dynamic point will return back to Q_1 by a decreasing exponential. No transition takes place and the output voltage (red line) will remain at the logical value 0. In this case the dynamic route will move as in the following Fig. 21.

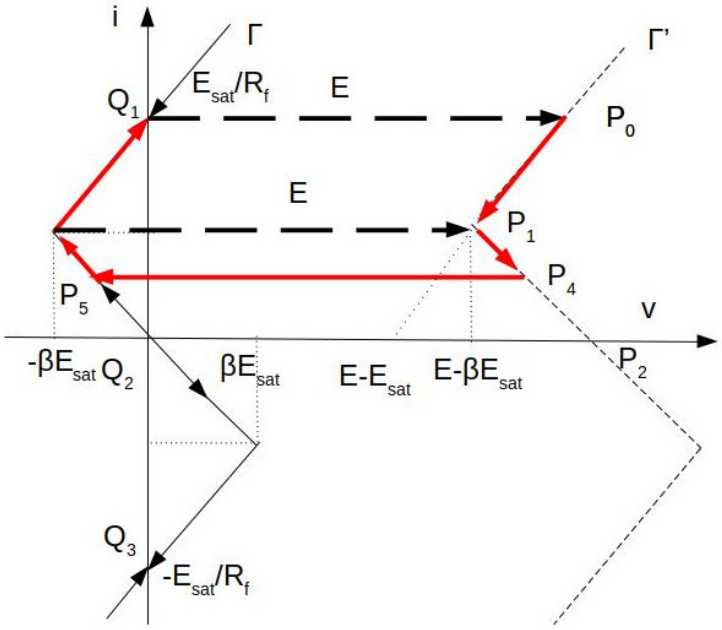

Figure 21: Third simulation: dynamic route, no transition.

The inductor transient current and voltages are depicted in Fig. 22.

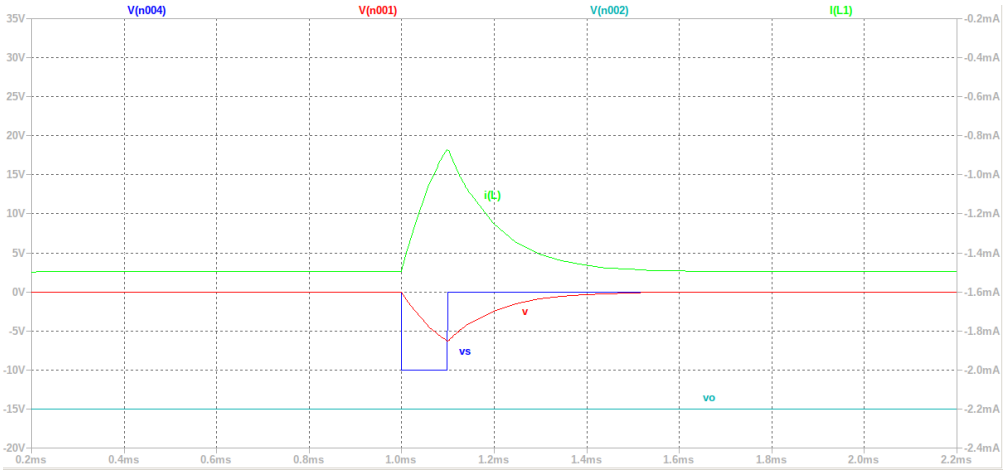

Figure 22: Third simulation: width too short $T = 0.1\ ms$, no transition.

6.6 Fourth simulation, pulse width $T = 0.415\ ms$, but pulse amplitude to small (2V), no transition

The transition will not occur whenever the pulse amplitude is too small. In the fourth simulation the amplitude has been set to $2V$.

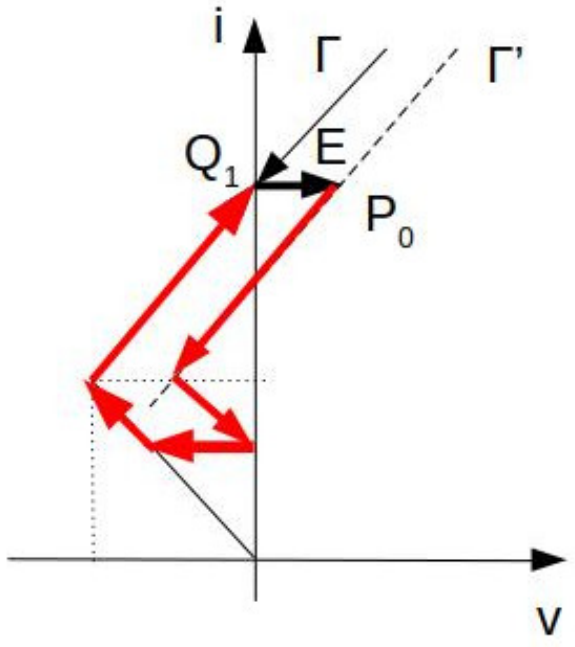

Figure 23: Fourth simulation: amplitude too short, no transition.

In this case, the breakpoint P_1 on Γ' is located in the left side of the plane. During this transient, the dynamic route will intercept the vertical axis and so the transient will stop in this point until the end of the triggering pulse. Then it will return to Γ back to Q_1 and no logical transition will occur. In order to have a transition the pulse amplitude must be:

$$E > \beta E_{sat} \tag{26}$$

or

$$E < -\beta E_{sat} \tag{27}$$

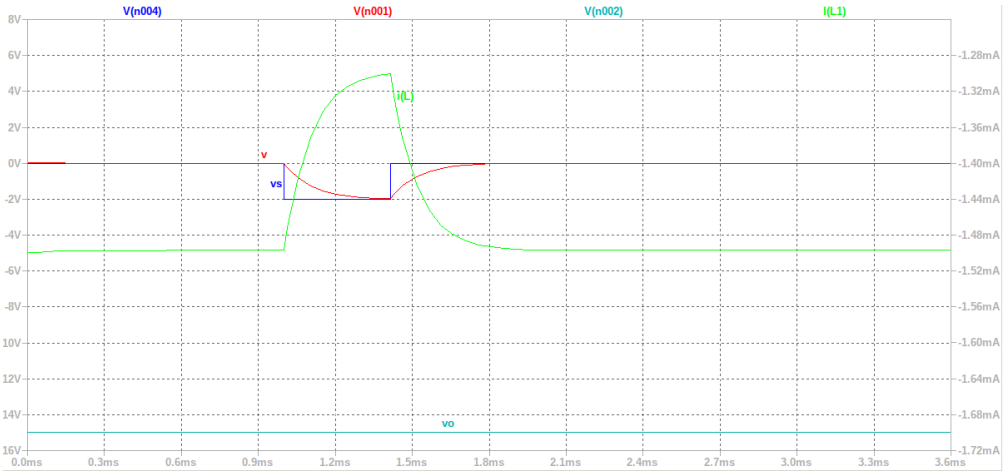

Figure 24: Fourth simulation: amplitude too short $(2V), T = 0.415\ ms$, no transition.

7 Conclusion

In the present short paper the switching behavior of a Bistable circuit has been analyzed. The Bistable circuit has been modeled by three different RL equivalent circuits. In other words the Bistable circuit has been described by a piecewise-linear driving-point characteristic.
Finally, some LTspice simulations have been done to dive into the transient behaviour of the circuit changing the triggering pulse width and amplitude. The SPICE netlist ha been provided.

References

Author, Leon O. Chua, Charles A. Desoer, Ernest S. Kuh, - Linear and Nonlinear Circuits (1987) (1), McGraw-Hill College.

Author, Simon Bramble, - LTspice Tutorial, (2).

A LTspice netlist: bistable circuit

```
V1 +V 0 15
Vin N005 N004 PULSE(0 10 1ms 10n 10n 0.415ms 12ms)
R1 N003 0 10K
R2 N002 N003 10K
XU1 N003 N001 +V -V N002 OP747
V2 -V 0 -15
L1 N001 N004 1
Rf N002 N001 10K
Vin1 N005 0 PULSE(0 10 6ms 10n 10n 0.415ms 12ms)
.tran 50m
.ic i(L1)=-1.5m v(n002)=-15 v(n001)=0
.lib ADI.lib
.backanno
.end
```