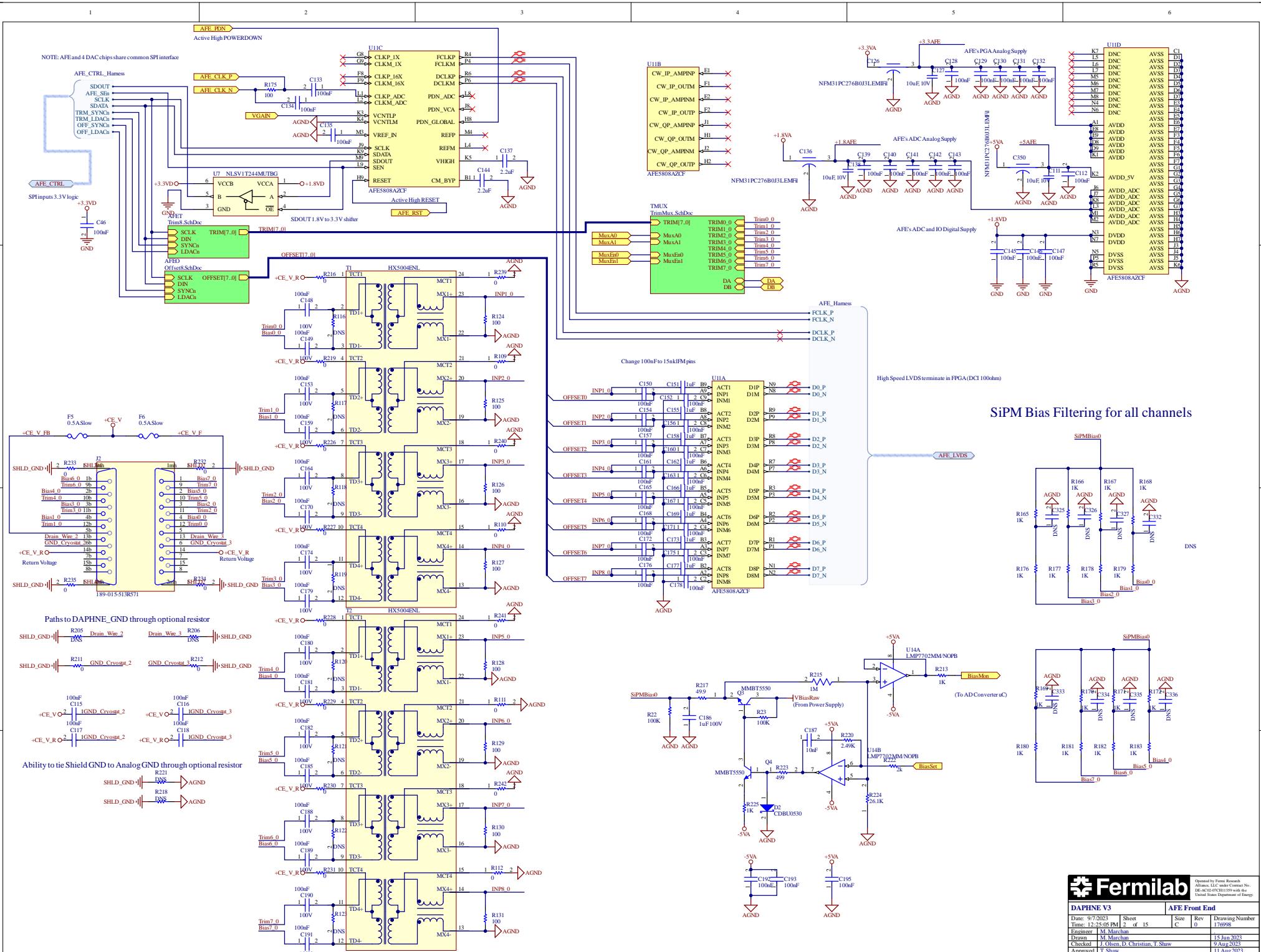


Pink ports represent ANALOG signals

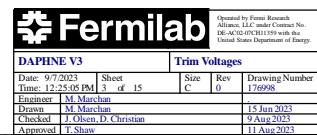
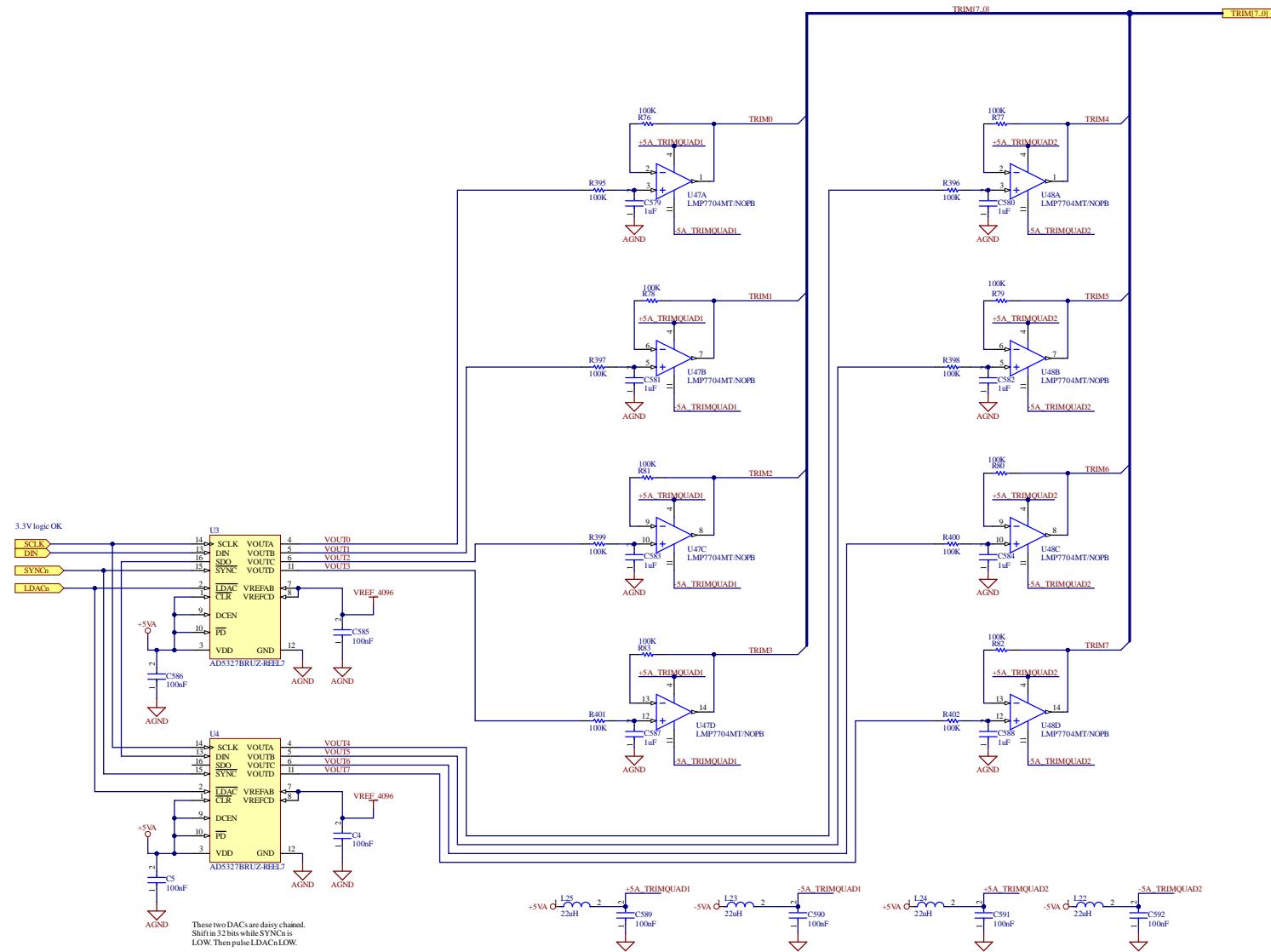


A

E

1

11



A

A

B

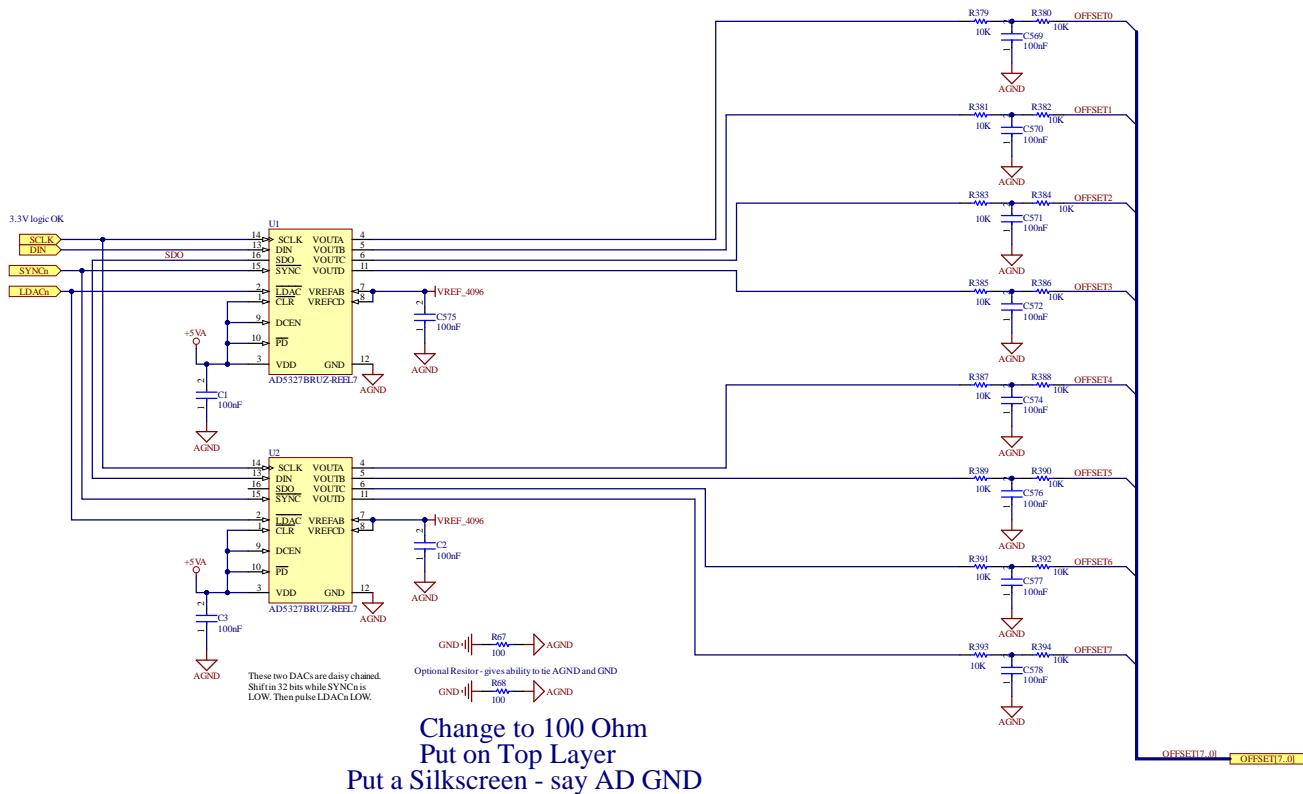
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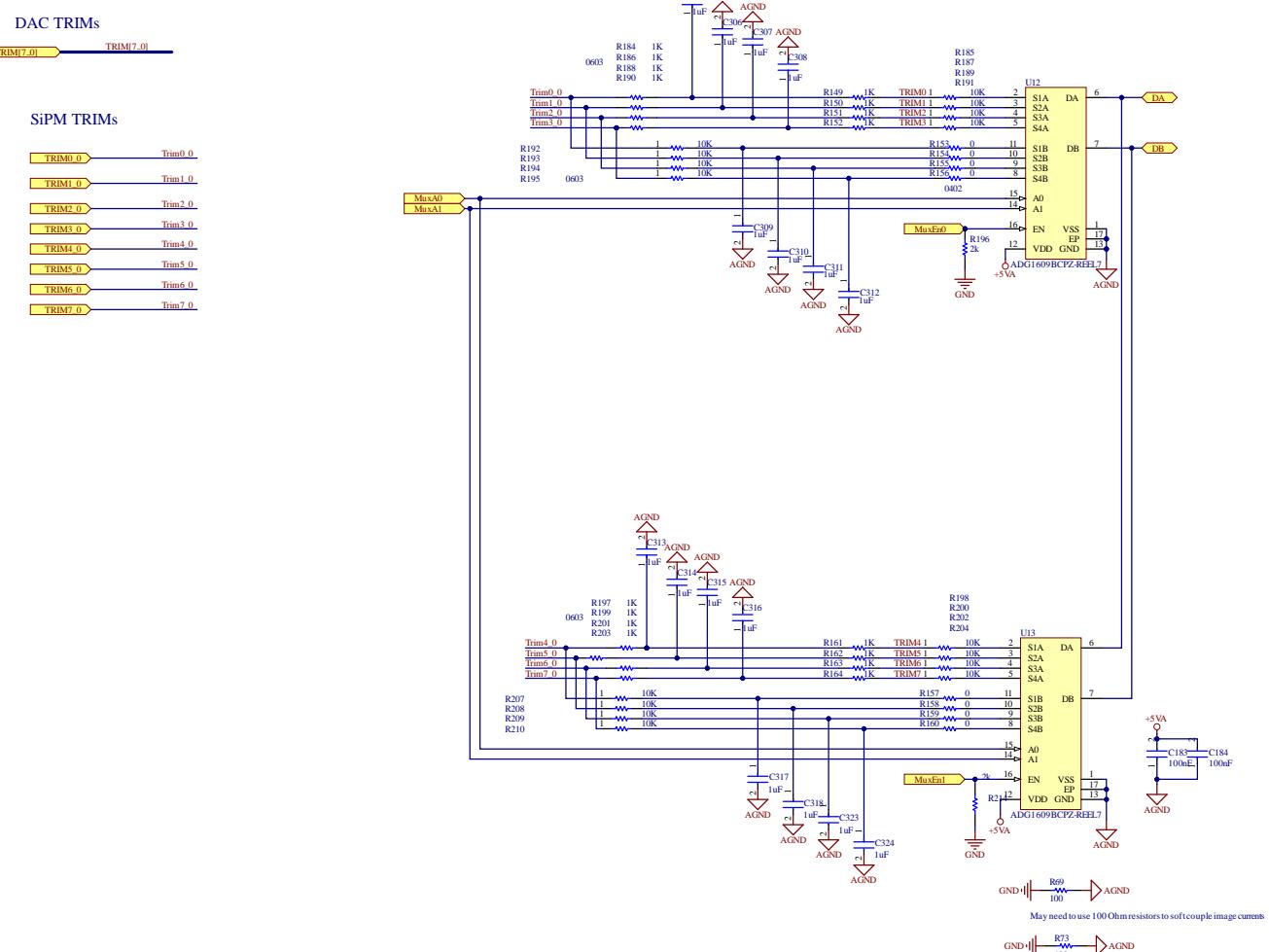
C

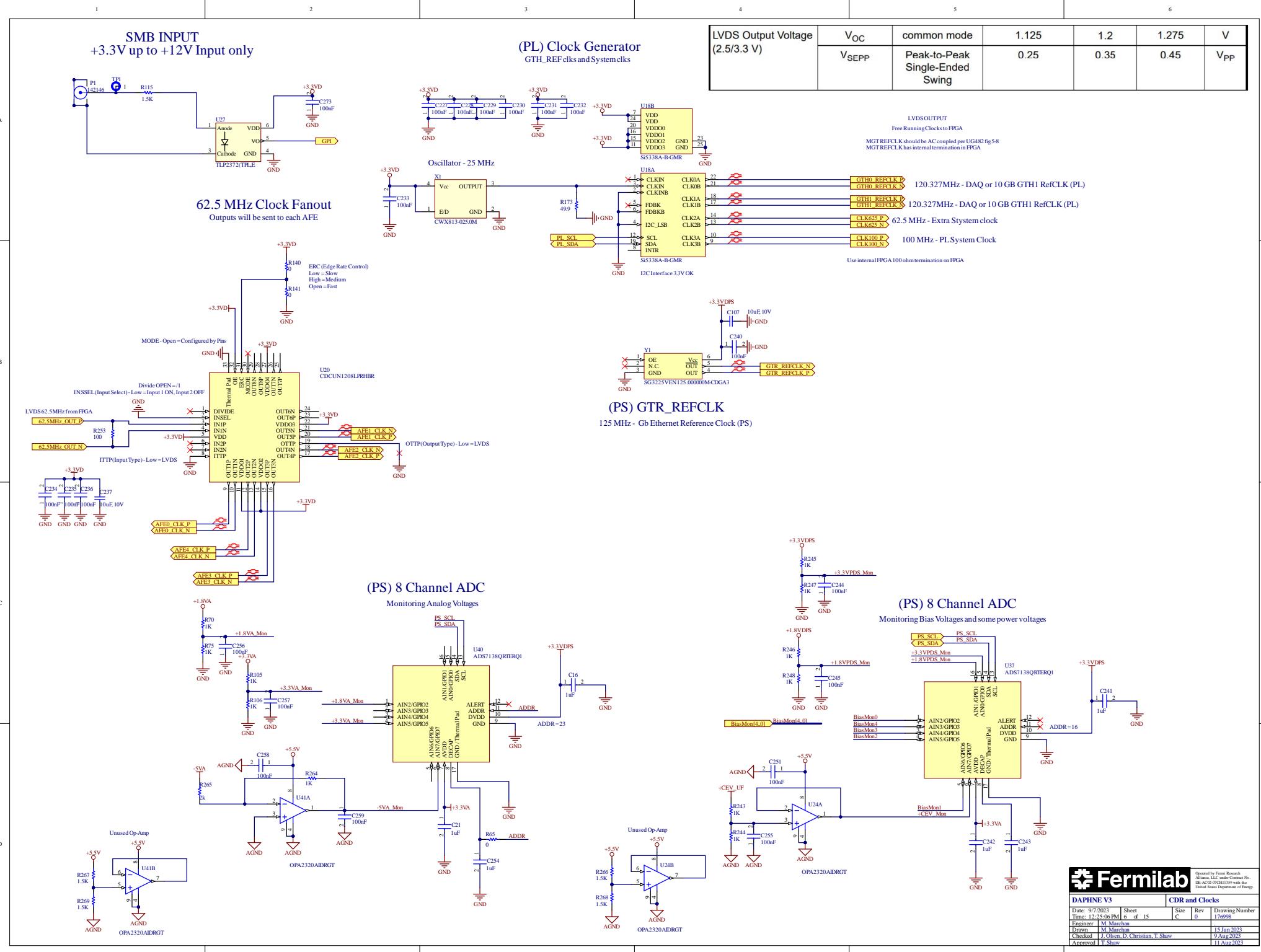
C

D

D







## Notes:

1. This device can also monitor internal temperature sensor, the DVDD pin (+3.3VD), and the AVDD pin (+5VA).

2. Use SPI command to start a conversion. Monitor the DRDYn pin or poll the status bits via SPI to determine when conversion is done.

3. Use SPI command to reset device if needed.

4. Hardware power down mode is not used.

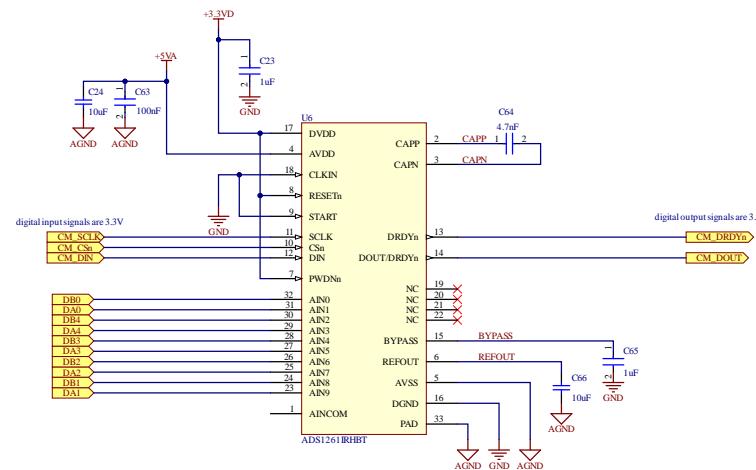
5. PGA gain range is up to 128. As gain increases the allowable differential input range decreases. See datasheet for details.

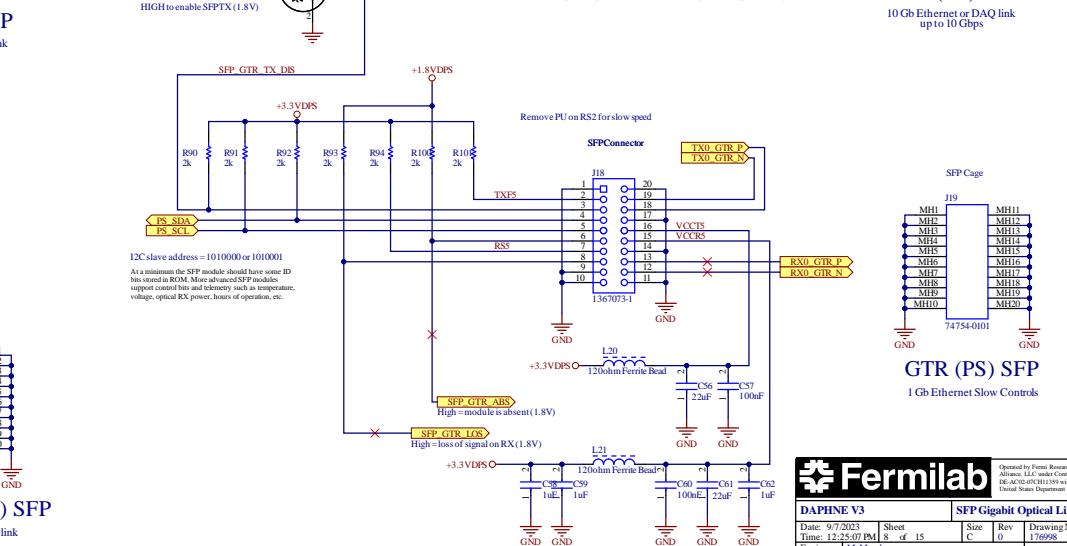
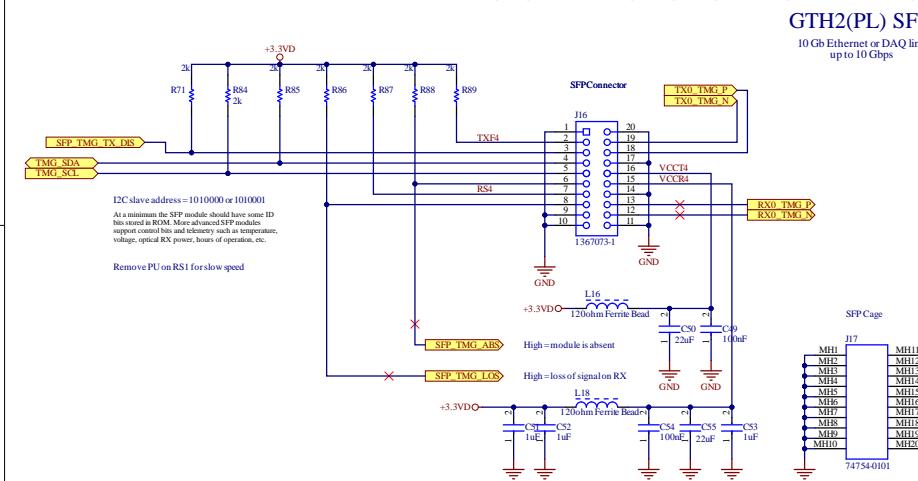
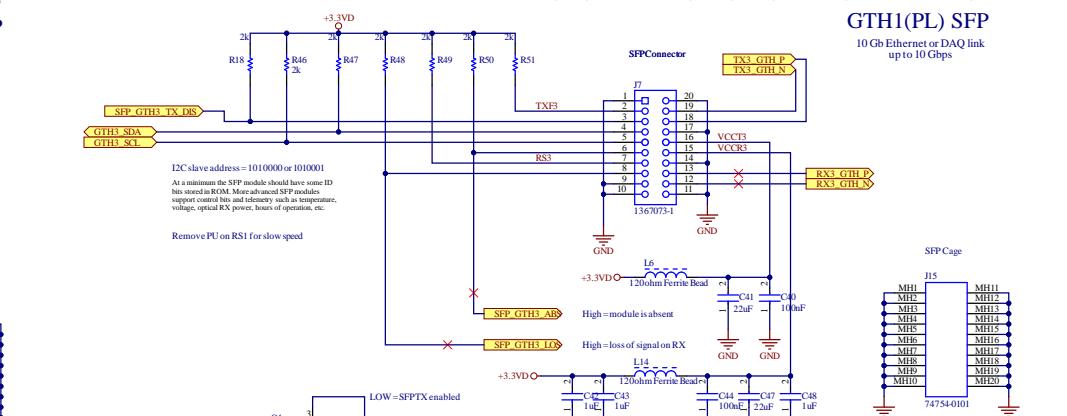
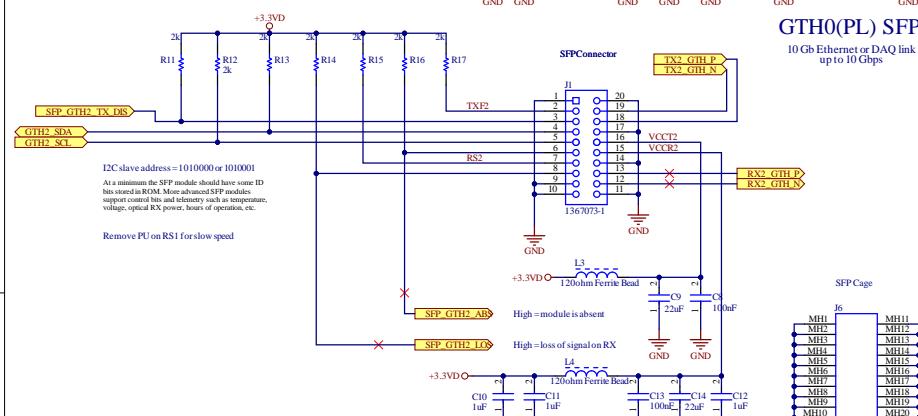
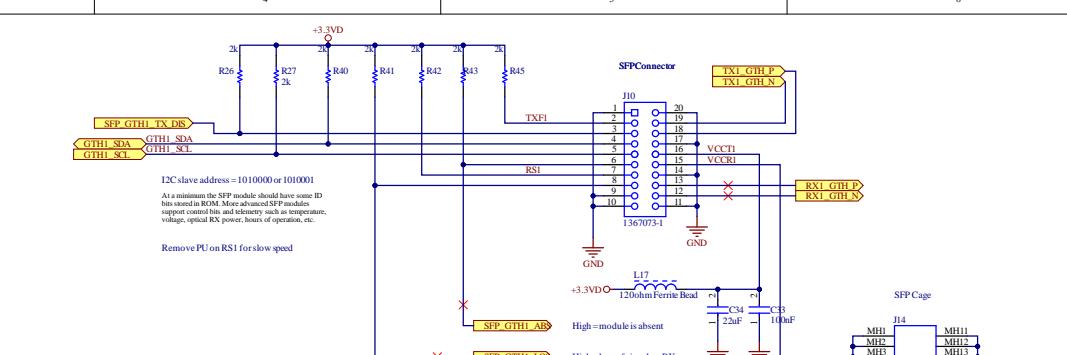
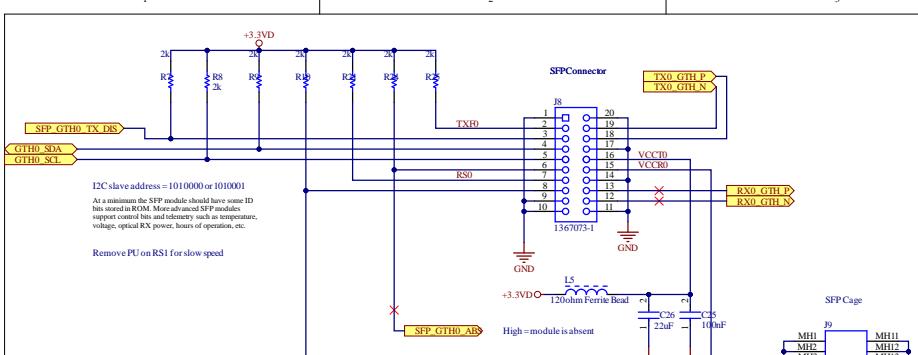
6. All analog inputs have an absolute voltage range of 0 to +5VA.

7. All SPI signals are 3.3V logic.

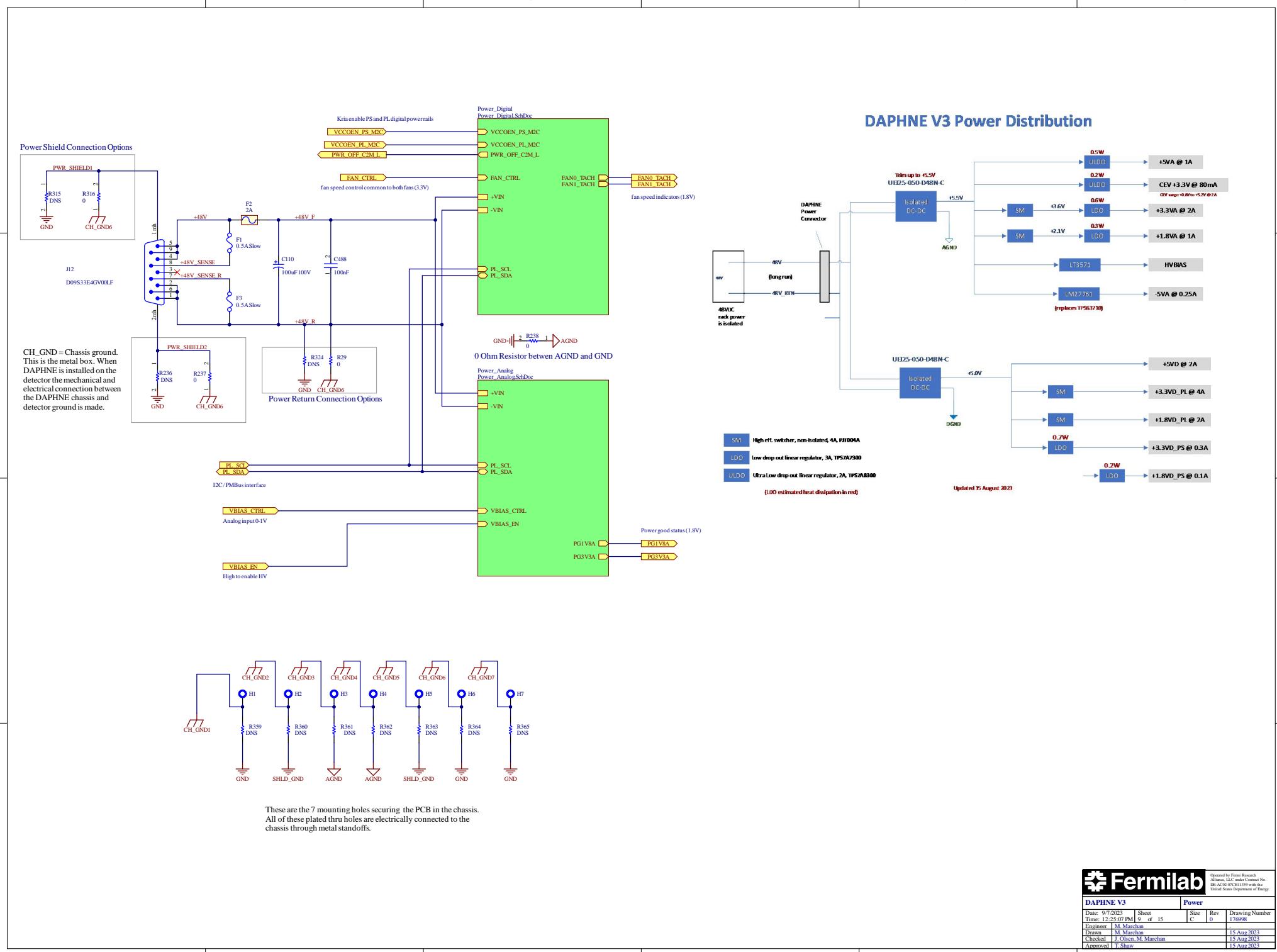
8. This device supports 5 differential inputs, one per AFE block.

9. Use internal voltage reference and internal clock generator.





<b>Fermilab</b>	
Operated by Fermi National Accelerator Laboratory, Batavia, Illinois, under Contract No. DE-AC02-07CH11359 with the United States Department of Energy.	
DAPHE V3	SFP Gigabit Optical Links
Date: 9/7/2023	Sheet: 8 of 15
Time: 12:25:07 PM	Size: C_0
Engineer: M. Marchan	Rev: 0
Drawn: M. Marchan	Drawing Number: 176998
Checked:	
Approved:	
T. Shaw	11 Aug 2023

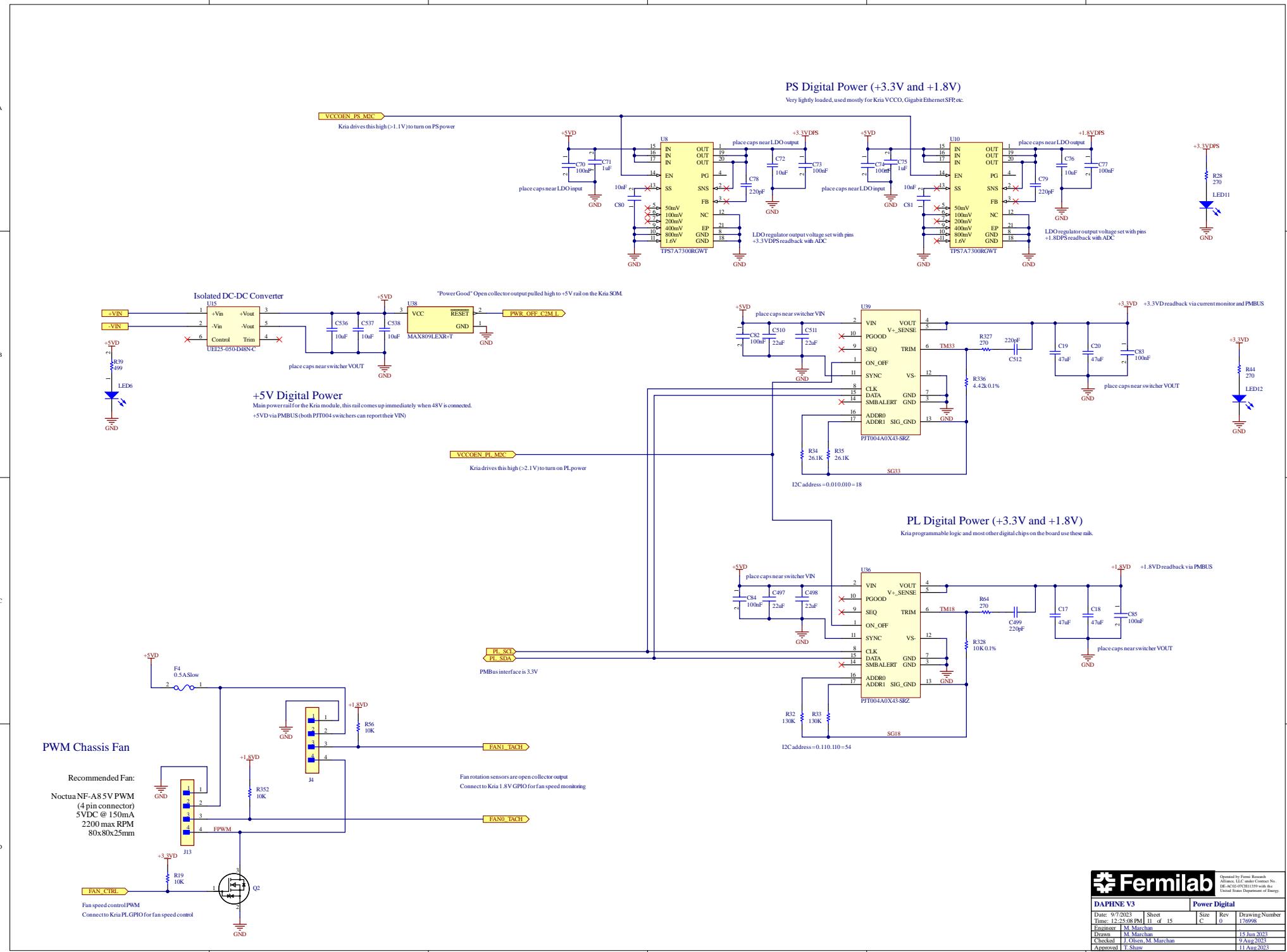


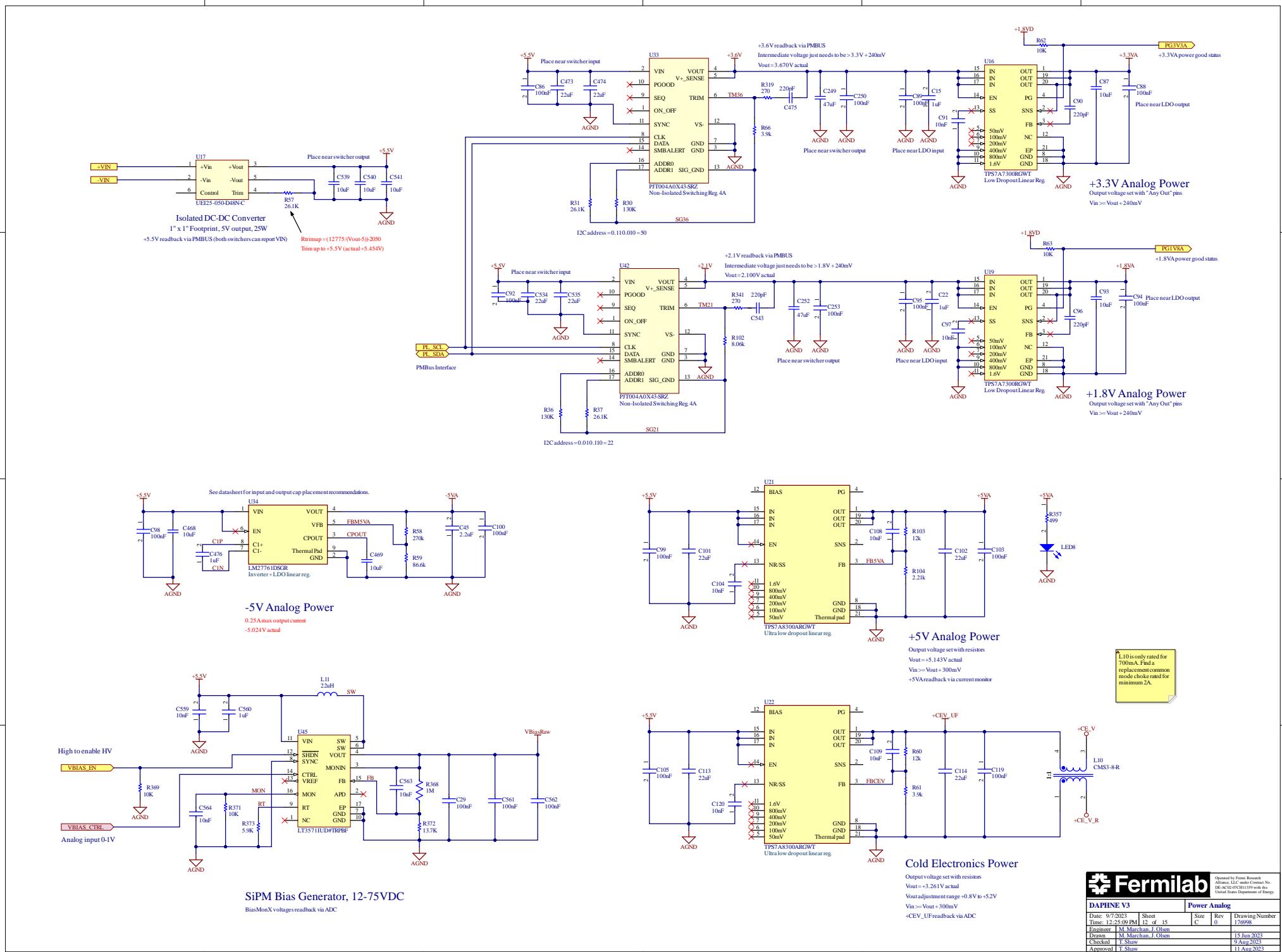
A

Detailed description of the schematic:

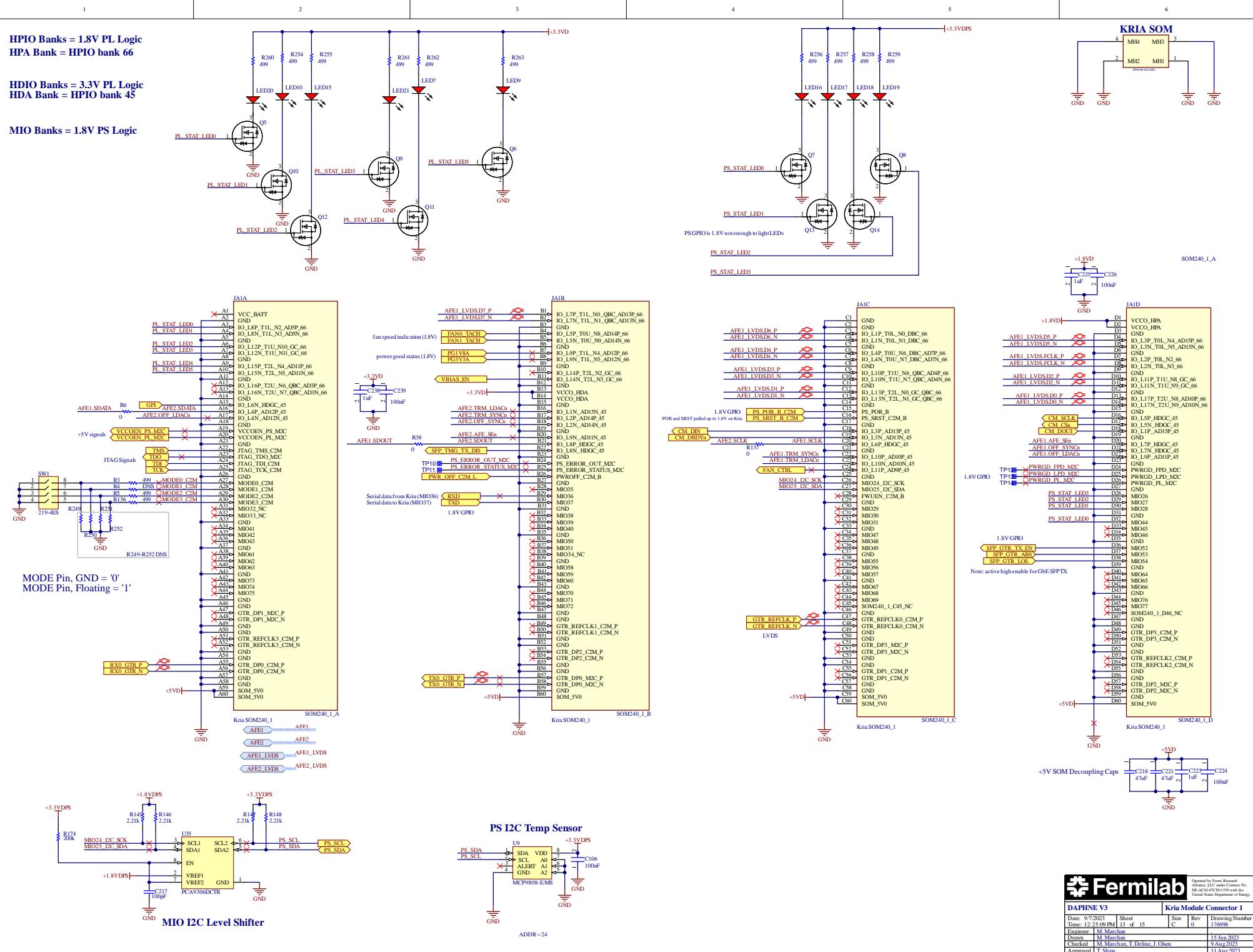
- DAC Section:** Three AD5327BRUZ-REF7 DACs are shown. Each DAC has its own reference voltage source (VREFAB and VREFCD) and a 100nF bypass capacitor. The DACs are controlled by SCLK, DIN, SDO, SYNC, and LDACn pins.
- Op-Amp Section:** The outputs of the DACs are connected to a series of operational amplifiers (op-amps) labeled VGAIN0 through VGAIN4. These op-amps have feedback resistors (R403, R404, R405, R406, R409, R410, R411, R412, R416, R417) and capacitors (C593, C594, C602, C604, C619). The outputs of the op-amps are labeled VGAIN[4..0].
- Reference Voltage Generation:** A central block labeled "BIAS SETT4..0" provides buffered reference voltages (VREF\_4096) to the DACs. A "VBIAS CTRL" block is also shown.
- Powering:** The circuit is powered by +5VA supplies and ground connections. A note at the bottom states: "These three DACs are daisy chained. Shift in 48 bits while SYNCn is LOW. Then pulse LDACn LOW."

	<b>Fermilab</b>	Operated by Fermi Research Alliance, LLC for the U.S. Department of Energy DE-AC02-07CH11359
<b>DAPHNE V3</b>		<b>DAC and Ref Voltages</b>
Date: 9/7/2023	Sheet 10 of 15	Size C Rev 0 Drawing Number 176998
Engineer: M. Marchan	Last Update: 15 Jun 2023	
Reviewed: J. Olsen	Checked: D. Christian 9 Aug 2023	
Approved: T. Shan	11 Aug 2023	



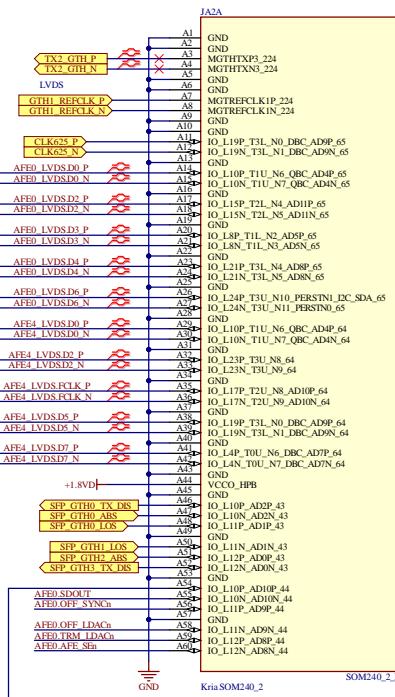


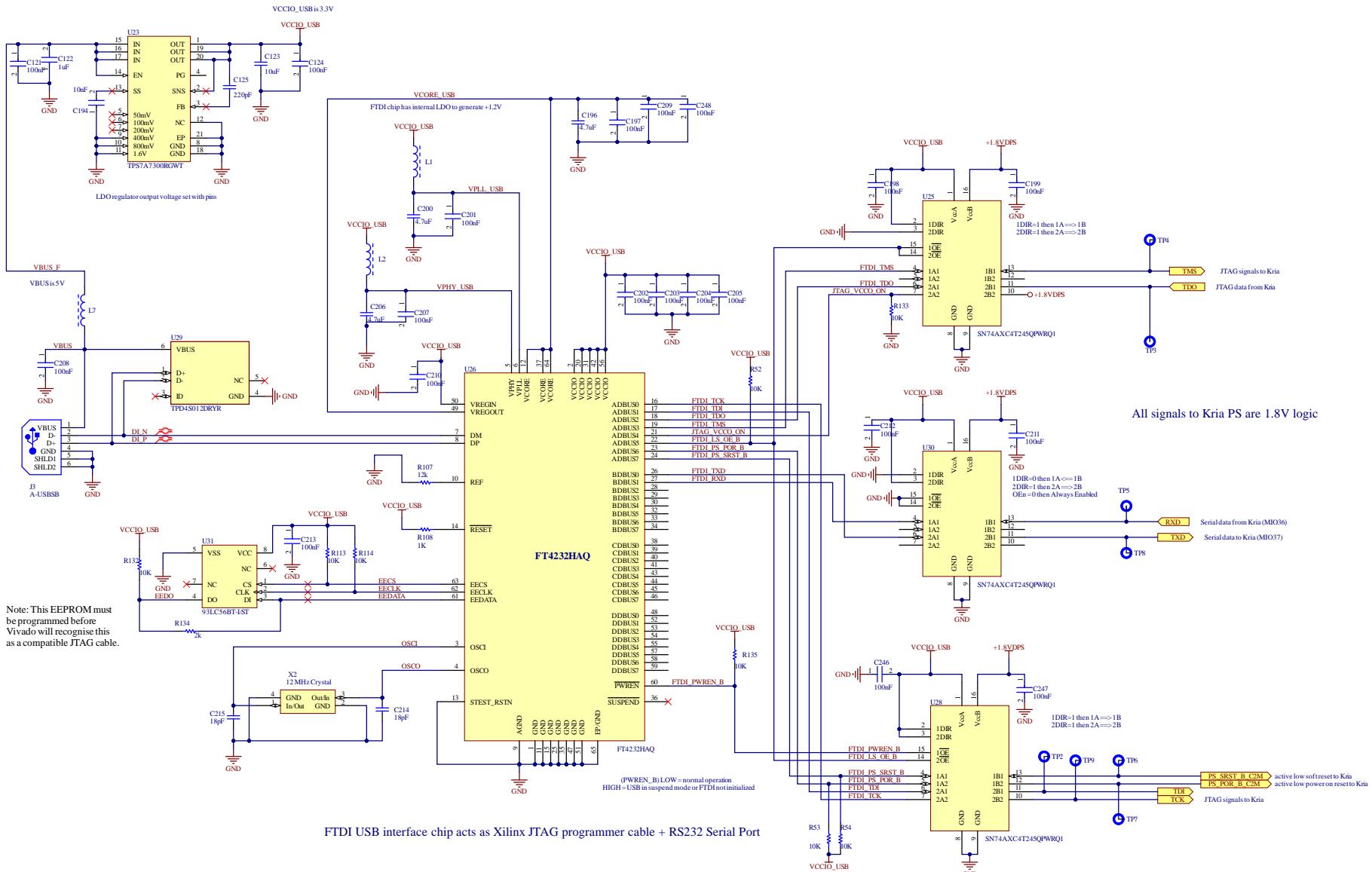
<b>Fermilab</b>	
Operated by Fermi Research Alliance, Inc.	DE-AC02-07CH11359 with the United States Department of Energy
<b>DAPHNE V3</b>	<b>Power Analog</b>
Date: 9/7/2023	Sheet: 12 of 15
Time: 12:25:09 PM	Size: C
Engineer: M. Marchan, J. Olsen	Rev: 0
Drawn: M. Marchan, J. Olsen	Drawing Number: 176998
Checked: M. Marchan, J. Olsen	
Approved: T. Shaw	



HPIO Banks = 1.8V PL Logic  
HPB Bank = HPIO bank 65  
HPC Bank = HPIO bank 64

HDIO Banks = 3.3V PL Logic  
HDB Bank = HPIO bank 43  
HDC Bank = HPIO bank 44

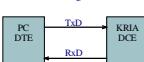




All signals from Kria PS are 1.8V logic

## RS-232 Naming Convention

ITAG\_VCCO\_ON goes high when Krig\_RS\_VCCO is ON



	<b>Fermilab</b>	Operated by Fermi Research Alliance, LLC under Contract No. DE-AC02-07CH11359 with the United States Department of Energy.
<b>DAPHNE V3</b>		<b>USB ITAG Interface</b>
Date: 9/7/2023	Sheet 15 of 15	Size C
Engineer: M. Marchan		Rev 1
Drawn by: M. Marchan		15 Jun 2023
Checked by: M. Marchan, T. DeLine		
Approved by: T. Shewchuk		11 Jun 2023