STEP-MX02 Hardware Manual

STEP FPGA

STEP 2017/2/14

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1. Introduction

The STEP-MXO2 development board presents a robust, portable and easy-to-learn hardware design platform built around the Lattice MachXO2 4000HC FPGA.

This board currently features the MachXO2-4000HC FPGA which offers embedded Flash technology for instanton, non-volatile operation in a single chip. Numerous system functions are included, such as two PLLs and 10 Kbits of embedded RAM plus hardened implementations of I2C, and user Flash memory.

The STEP MXO2 FPGA development board includes hardware such as on-board JTAG Programmer, 7-Segment Displays, LEDs, GPIOs and much more. By leveraging all of these capabilities, the STEP MXO2 FPGA development board is the perfect solution for learning FPGA, evaluating and prototyping the true potential of the MXO2 FPGA.

2. Package Contents

Figure 1 shows a photograph of the STEP-MXO2 package.



Figure 1 The STEP MXO2 Package contents

The STEP MXO2 package includes: 1.The STEP MXO2 FPGA Development Board 2.Product Packing Box 3.Quick Start Manual

3. Layout and Components

3.1 Development Board Layout

This section presents the features and design characteristics of the board.

A photograph of the board is shown in Figure 2 and Figure 3. It depicts the layout of the board and indicates the location of the connectors and key components.

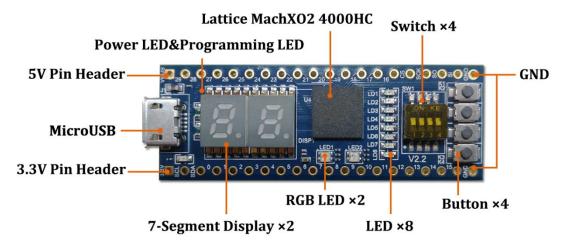


Figure 2 Development Board (top view)

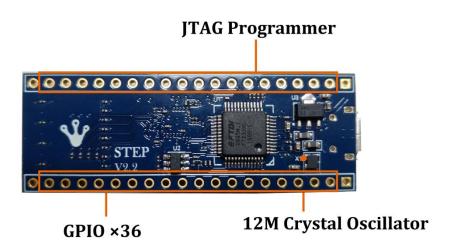


Figure 3 Development Board (bottom view)

This board has many features that allow users to implement a wide range of designed circuits, from simple circuits to various creative projects.

3.2 FPGA Device

Version	MachXO2 4000HC		
Series	MachXO2		
Density LUTs	4320		
EBR SRAM(Kbits)	10		
Dist. SRAM(Kbits)	34		
User Flash Memory(Kbits)	96		
PLL	2		
DDR/DDR2/LPDDR	VEC		
Memory Support	YES		

3.3 Programming and Configuration

· On-Board JTAG Programmer(Normal Micro-USB connector)

3.4 Connecters

· 36 GPIO Header

3.5 Display

- · 7-Segment Display ×2
- · User LEDs ×8
- · RGB LEDs ×2

3.6 Buttons and Switches

- · Buttons ×4
- \cdot Switches $\times 4$

3.7 Power

 \cdot 5V DC input from Micro-USB.

4. Block Diagram of Board

Figure 4 gives the block diagram of the board. To provide maximum flexibility for the user, all connections are made through the MachXO2 4000HC FPGA device. Thus, the user can configure the FPGA to implement any system design.

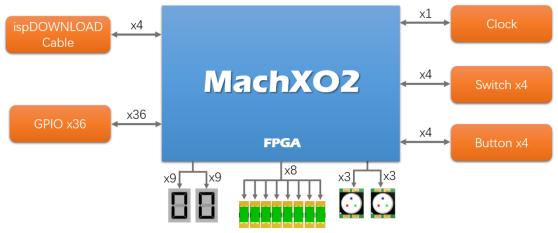


Figure 4 Board Block Diagram

5. Pins Assignments

STEP	FPGA	STEP	FPGA	Digital	FPGA	12M	FPGA PINs
PINs	PINs	PINs	PINs	Display1	PINs	CLOCK	
3.3V		VBUS		SEG-A1	A10	PCLK	C1
SCL	С8	GPI029	E12	SEG-B1	C11	LED	FPGA PINs
SDA	B8	GPI028	F12	SEG-C1	F2	LED1	N13
GPI00	E3	GPIO27	G12	SEG-D1	E1	LED2	M12
GPIO1	F3	GPIO26	F13	SEG-E1	E2	LED3	P12
GPIO2	G3	GPIO25	F14	SEG-F1	A9	LED4	M11
GPIO3	Н3	GPIO24	G13	SEG-G1	В9	LED5	P11
GPI04	J2	GPIO23	G14	SEG-DP1	F1	LED6	N10
GPI05	J3	GPIO22	H12	SEG-DIG1	С9	LED7	N9
GPI06	К2	GPIO21	J13	Digital	FPGA	LED8	Р9
GPIO7	К3	GPIO20	J14	Display2	PINs	Switch	FPGA PINs
GPI08	L3	GPIO19	K12	SEG-A2	C12	SW1	М7
GPI09	N5	GPIO18	K14	SEG-B2	B14	SW2	М8
GPIO10	P6	GPIO17	K13	SEG-C2	J1	SW3	М9
GPIO11	N6	GPIO16	J12	SEG-D2	114	CVALA	M10
	140	GPIUIO	J12	SEG-DZ	Н1	SW4	M10
GPIO12	P7	CS	P3	SEG-E2	H2	Sw4 Button	FPGA PINs
GPIO12 GPIO13							
	P7	CS	P3	SEG-E2	Н2	Button	FPGA PINs
GPI013	P7 N7	CS SCK	P3 M4	SEG-E2 SEG-F2	H2 B12	Button KEY1	FPGA PINs L14
GPI013 GPI014	P7 N7 P8	CS SCK SO	P3 M4 N4	SEG-E2 SEG-F2 SEG-G2	H2 B12 A11	Button KEY1 KEY2	FPGA PINS L14 M13
GPI013 GPI014 GPI015	P7 N7 P8	CS SCK SO SI	P3 M4 N4	SEG-E2 SEG-F2 SEG-G2 SEG-DP2	H2 B12 A11 K1	Button KEY1 KEY2 KEY3	FPGA PINS L14 M13 M14

6. Version

Version number	Date	Comments
1.0	2017/2/14	Initial Revision