

Bruno Valinoti November 26th to December 7th, 2018, Trieste









Outline

Introduction

Reconfigurable Virtual Instrument

Zynq-7000 PL-PS Commblock Interface





Accessing the CommBlock from PC

- Standardize packets
- Hardware reusability
- Communication protocols
- Multiplatform and multivendor software





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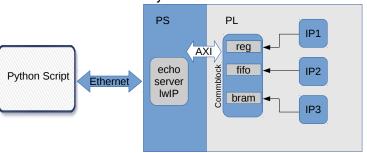
Zynq-7000 PL-PS Commblock Interface





RVI System

In this lab we will see a system like this







PC to PS communication method

- Protocol definition
 Ethernet, PCIe, USB, etc...
- Package standard
 Standardization of the way the data is build inside the packets
- Basic functionalities Read data, move data between the different hardware resources, write data, general resets, etc..





Read from CommBlock

Read basic function

$$\mathbf{x}$$
_read < $addr > [-r][< output format >]$

- Not limited to CommBlock
- Read from general memory resources

$$x_read_mem < addr > < N > < inc > [-r][< output format >]$$

Where address is in hexadecimal format as 0x0001, **N** the number of words, **inc** the increment after each word read.





Write to CommBlock

Write basic function

- Not limited to CommBlock
- Write from general memory resources

$$x_write_mem < addr >< N >< inc > [-r][< inputfile >]$$





Commands format

COMMAND_TYPE COMMAND_SPECIFIC DATA





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CommBlock

```
comblock 0
  + S00 AXI
  + S01 AXI
  + S02_AXI
  reg0_i[31:0]
  reg1_i[31:0]
  reg2_i[31:0]
                         reg0 o[31:0] -
reg3_i[31:0]
                         reg1_o[31:0] -
reg4_i[31:0]
                         reg2_o[31:0] =
reg5_i[31:0]
                         reg3_o[31:0] =
reg6_i[31:0]
                         reg4_o[31:0] -

    reg7 i[31:0]

                         rea5 of31:01 -
reg8_i[31:0]
                         reg6_o[31:0]
reg9 i[31:0]
                         reg7 o[31:0] -
- ram clk i
                         reg8 o[31:0] -
- ram we i
                         rea9 o[31:0] -

    ram addr if15:01

                     ram data of31:01 -

    ram data i[31:0]

                            fifo full o
fifo clk i
                           fifo afull o
- fifo clear i
                       fifo overflow o
fifo_we_i
                      fifo data o[15:0] -

    fifo data (15:0)

                         fifo empty o
fifo_re_i
                        fifo_aempty_o -

 s00 axi aclk

                      fifo underflow o

 s00 axi aresetn

 s01 axi aclk

 s01_axi_aresetn

- s02 axi aclk

 s02 axi aresetn
```

comblock v1.0 (Pre-Production)

- 3 AXI interfaces
- Set of registers for read only or write only
- ▶ Two FIFOs
- A true dual port memory





INTI-CMNB-FPGA

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Thanks!