



WELCOME to the

Joint ICTP-IAEA School on Systems-on-Chip based on FPGA for Scientific Instrumentation and Reconfigurable Computing

20 November – 01 December, 2023

ICTP Organizers

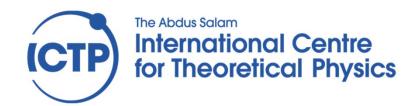
Maria Liz CRESPO

Andres CICUTTIN

IAEA Organizers

Kalliopi KANAKI

Mladen BOGOBAC



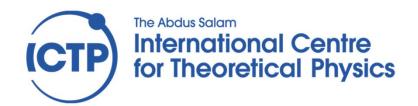


SCHOOL PROGRAMME

- The School is held at the ICTP AGH:
 - Informatics Lab and Kastler Lecture Hall (first week)
 - Informatics Lab and Giambiagi Lecture Hall (second week)
- School website: https://indico.ictp.it/event/10225/

Detailed schedule can be consulted at the school website

School's email (secretariat): smr3891@ictp.it



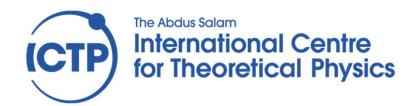


SCHOOL PROGRAMME

• Typical daily timetable (9:00 – 18:30):

Timetable	
9:00 - 10:00	lectures
10:00 - 10:30	coffee-break
10:30 - 12:30	lectures
12:30 - 14:00	lunch
14:00 - 16:00	lectures / lab activities
16:00 - 16:30	coffee-break
16:30 - 18:30	lab activities

• Wednesday, 22 November 2023, 19:00: Welcome Reception (AGH)





PARTICIPANTS

Requests for participation: 207 applicants from 48 different countries

Selected: 44 participants from 26 different countries

Algeria Guatemala Peru

Argentina Honduras Romania

Bangladesh India Russia

Brazil Indonesia Sudan

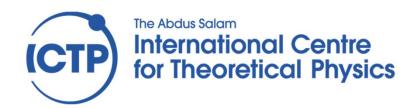
Cameroon Iran Tunisia

Colombia Malaysia Turkey

Cuba Mexico Uruguay

Ecuador Nigeria Venezuela

El Salvador Pakistan





FACULTY

SISTERNA Cristian (Argentina)

RINCON CALLE Fernando (Spain)

RONGEN Heinz (Germany)

VALCARENGHI Luca (Italy)

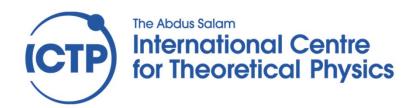
CASTOLDI Piero (Italy)

DUPONT DE DINECHIN Florent (France)

REAZ Mamun Bin Ibne (Bangladesh)

HALL-WILTON Richard John (Sweden)

JOVALEKIC Nikola (Netherlands)





FACULTY

BALLINA ESCOBAR Maynor (Guatemala)

FLORIAN SAMAYOA Werner (Guatemala)

GARCIA ORDOÑEZ Luis (Guatemala)

MOLINA Romina (Argentina)

MORALES ARGUETA Ivan (Guatemala)

SILVA Agustin (Argentina)

VALINOTI Bruno (Argentina)





Topics

FPGA and System-on-Chip (SoC) technology

SoC Architecture and Design Methodology

C for Embedded Systems

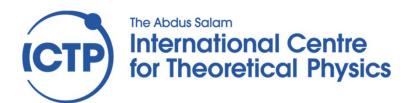
VHDL (Hardware Description Language)

High Level Synthesis (HLS)

Real Time Operating System (FreeRTOS)

The FloPoCo arithmetic core generator

Reconfigurable Virtual Instrumentation (RVI) based on SoC-FPGA





Topics

FPGA for Accelerating Machine Learning Algorithms

Programmable Hardware Acceleration in Communications Networks

Handling High Data Rates in Data Acquisition Systems

Semiconductor and Quantum Detectors Developments

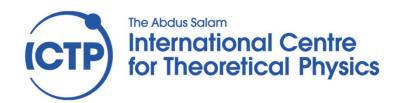
Digital Pulse Processing Techniques for Detectors

HyperFPGA: Experimental Infrastructure for Reconfigurable Supercomputing

Agent-based Reinforcement Learning for Quantum Computing

The Open Standard RISC-V Architecture

Academic Writing Strategy for Impacted Journal





Lab Activities

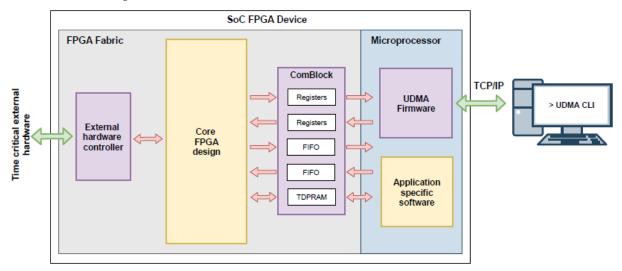
- Virtual Machines (VM) in a Cloud Instance
- Vivado IDE 2022.2 (Xilinx)
- ZedBoard: Xilinx Zynq-7000 All-Programmable SoC
- GitLab link (guides for lab activities):
 https://gitlab.com/ictp-mlab/smr-3891/-/wikis/home
- Lab Tutors will assist you during the lab activities





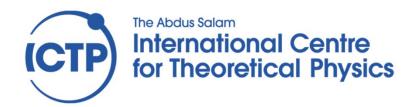
Lab Activities

SoC-FPGA Development Framework:



Projects:

- Pulse Acquisition and Detector Characterization (SiPM)
- Digital Pulse Processing (DPP) for Isotope Identification
- DPP for X-ray Photon Detection and Energy Measurement





Recommendations:

- 1) Be on time
- 2) Attend at least 90% of the lectures + labs to receive the Diploma
- 3) Feel free to ask questions!





WHAT ABOUT YOU?

NAME

COUNTRY

UNIVERSITY / INSTITUTE

AREA OF RESEARCH

INTEREST IN THE SCHOOL