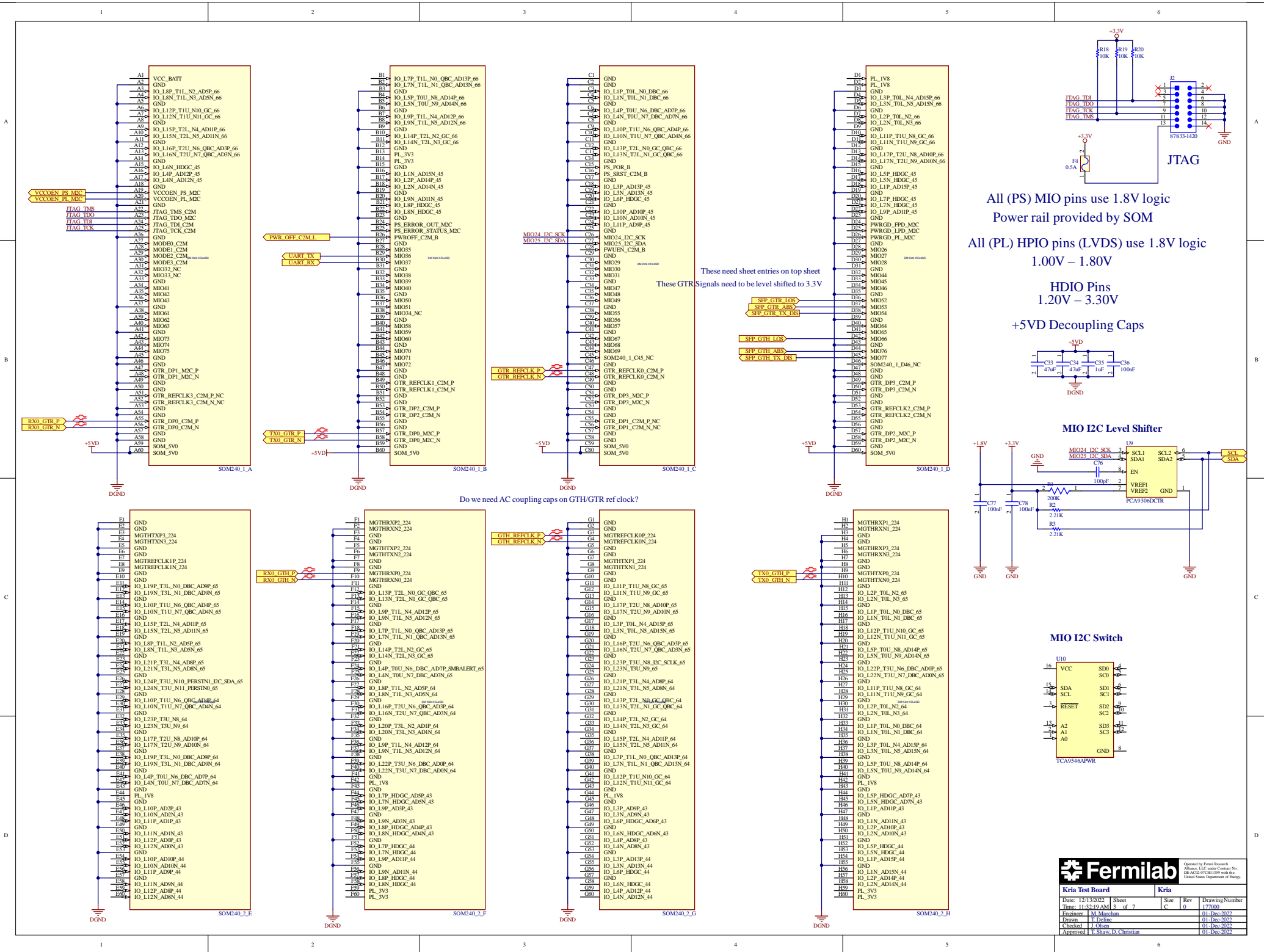


If possible, use regulators with I2C (PMBus) interface and tie it to the Kria
Maybe OK to use LDO to make +1.8V from the +3.3V rail
Do we need any other power rails? +2.5V?

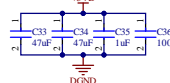


All (PS) MIO pins use 1.8V logic
Power rail provided by SOM

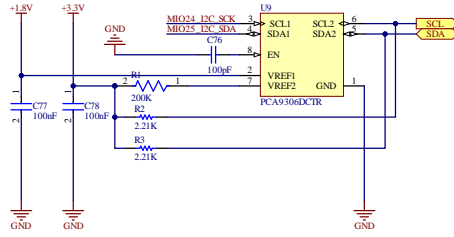
All (PL) HPIO pins (LVDS) use 1.8V logic
1.00V – 1.80V

HDIO Pins
1.20V – 3.30V

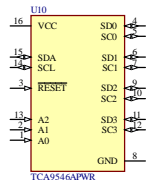
+5VDD Decoupling Caps



MIO I2C Level Shifter

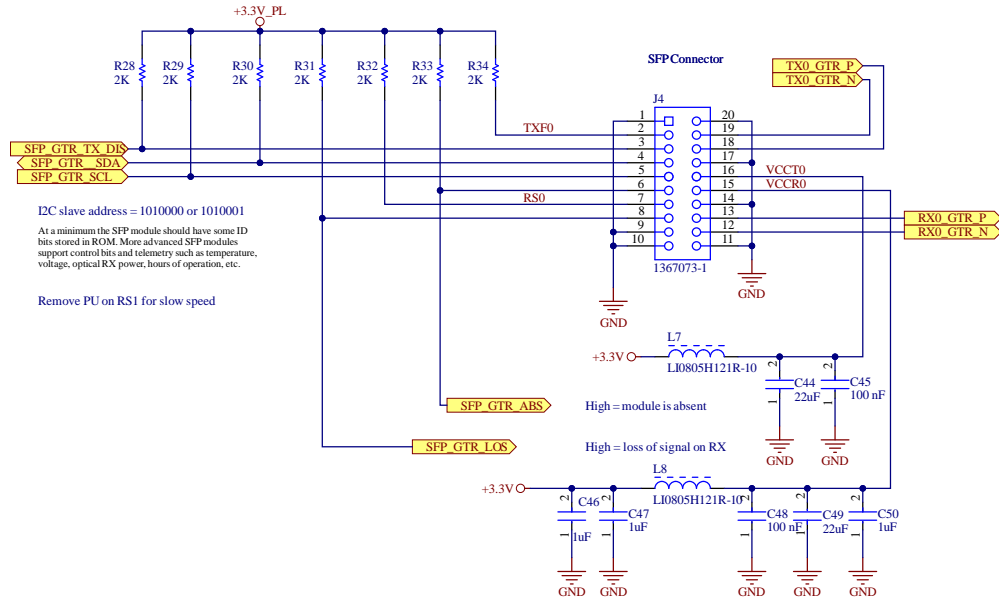


MIO I2C Switch

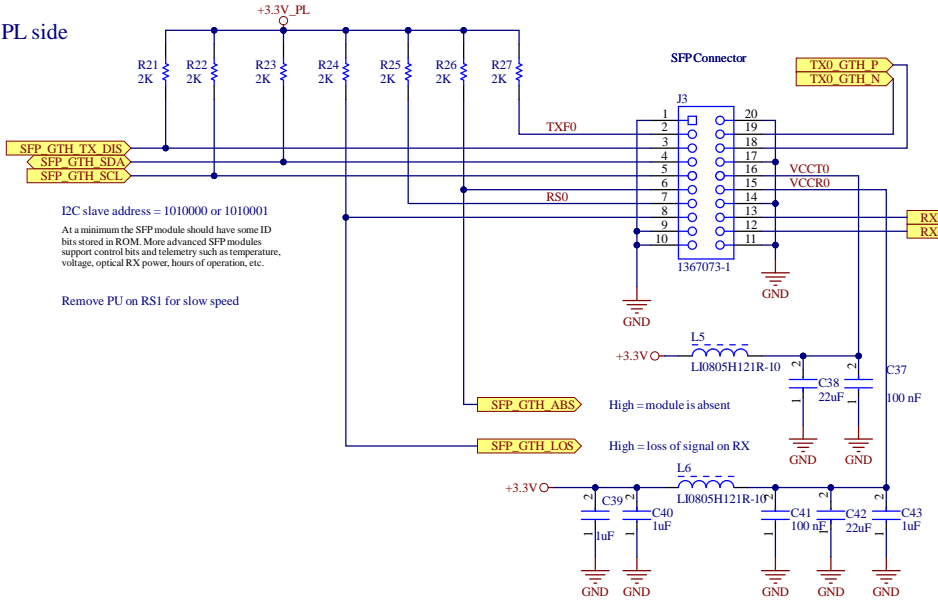


Kria Test Board		Kria	
Date: 12/13/2022	Sheet: 3 of 7	Size: 177000	Rev: 01-Dec-2022
Engineer: M. Marchant			01-Dec-2022
Drawn: T. Dillman			01-Dec-2022
Checked: T. Dillman			01-Dec-2022
Approved: T. Shaw, D. Christian			01-Dec-2022

If we want to keep the PL and PS sides separate we will need separate I2C bus on the PS side and on the PL side



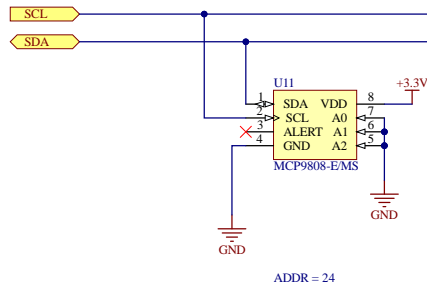
GTR (PS) SFP
1 Gb Ethernet Slow Controls



GTH (PL) SFP
10 Gb Ethernet or DAQ link
up to 10 Gbps

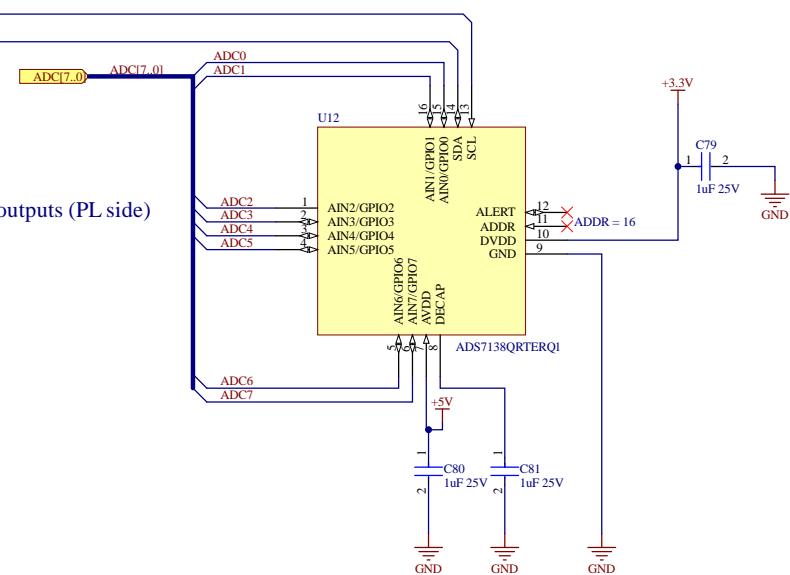
Kria Test Board				SFP			
Date:	12/13/2022	Sheet	4 of 7	Size	B	Rev	0
Time:	11:32:20 AM					Drawing Number	177000
Engineer	M. Marchan						01-Dec-2022
Drawn	T. Deline						01-Dec-2022
Checked	J. Olsen						01-Dec-2022
Approved	T. Shaw, D. Christian						01-Dec-2022


I2C Temperature Sensor



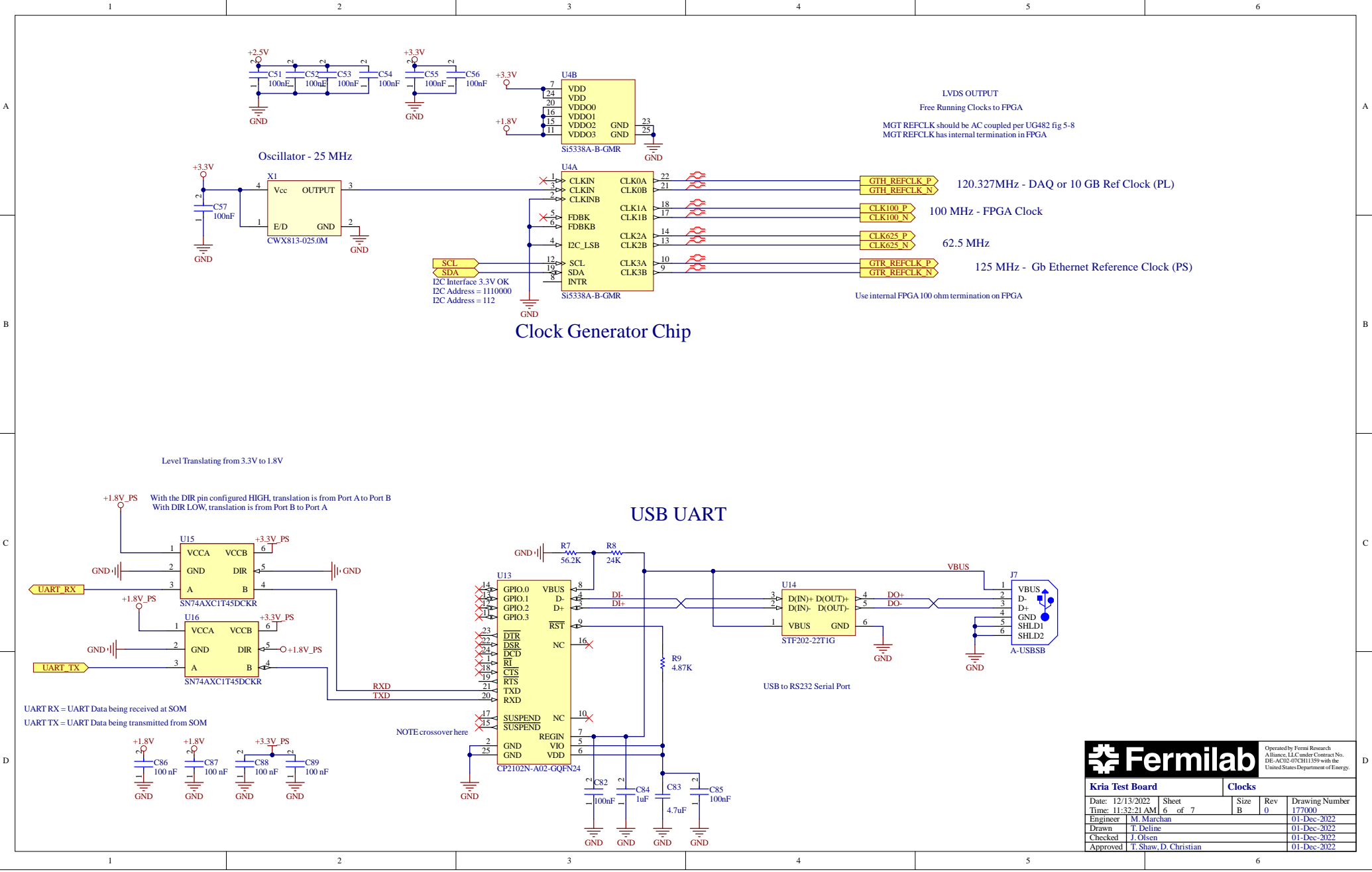
ADC inputs (PS side) will receive DAC outputs (PL side)


I2C 8 channel ADC



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Kria Test Board				Sensor			
Date:	12/13/2022	Sheet		Size	Rev	Drawing Number	
Time:	11:32:21 AM	5 of 7		B	0	177000	
Engineer	M. Marchan					01-Dec-2022	
Drawn	T. Deline					01-Dec-2022	
Checked	J. Olsen					01-Dec-2022	
Approved	T. Shaw, D. Christian					01-Dec-2022	

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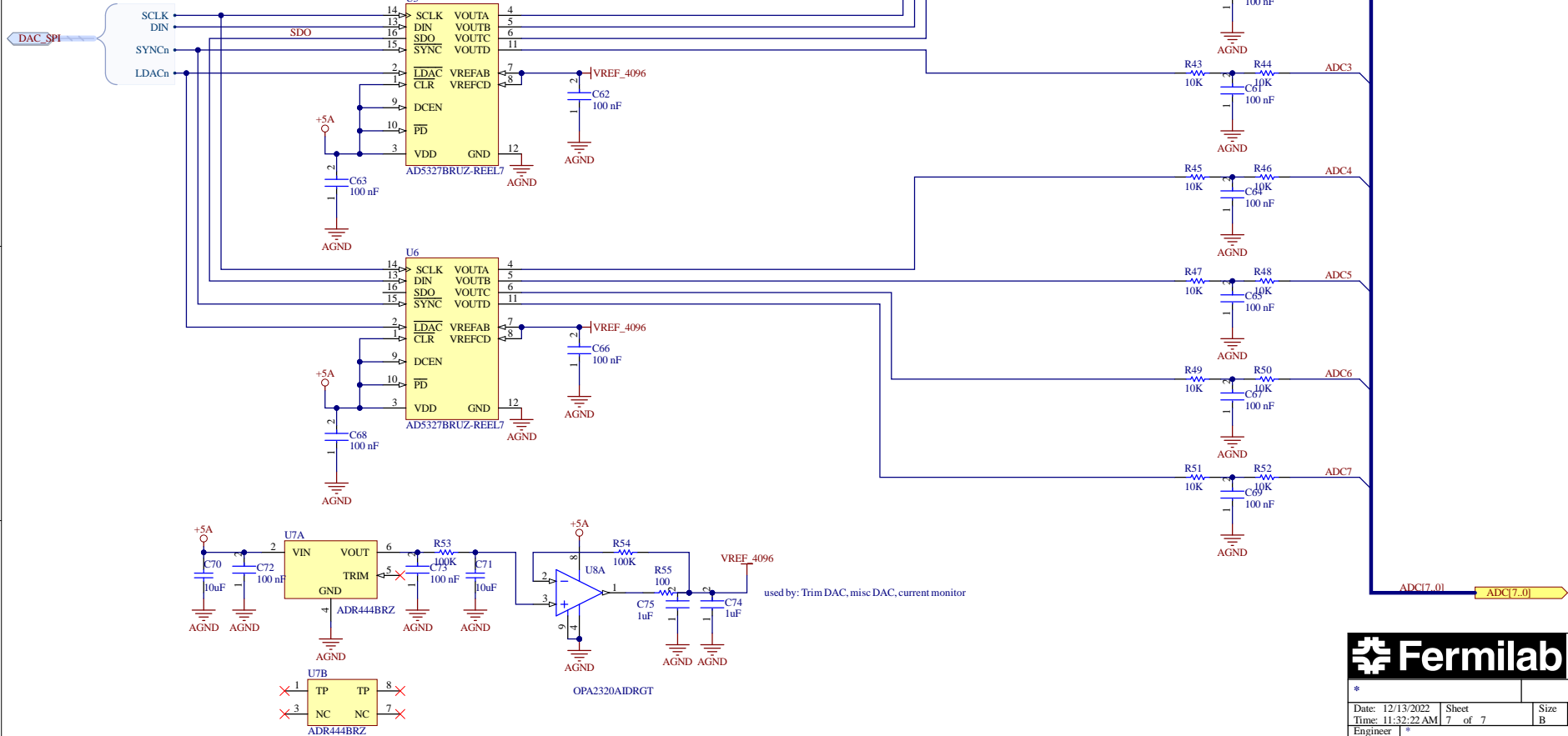


Operated by Fermi Research Alliance, LLC under Contract No. DE-AC02-07CH11339 with the United States Department of Energy.

Kria Test Board			Clocks	
Date: 12/13/2022	Sheet 6 of 7	Size B	Rev 0	Drawing Number 177000
Engineer	M. Marchan			01-Dec-2022
Drawn	T. Define			01-Dec-2022
Checked	J. Olsen			01-Dec-2022
Approved	T. Shaw, D. Christian			01-Dec-2022

These two DACs are daisy chained.
Shift in 32 bits while SYNCn is
LOW. Then pulse LDACn LOW.

3.3V logic OK
DAC_Harness



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Date: 12/13/2022	Sheet 7 of 7	Size B	Rev *	Drawing Number *
Engineer *				
Drawn *				
Checked *				
Approved *				

