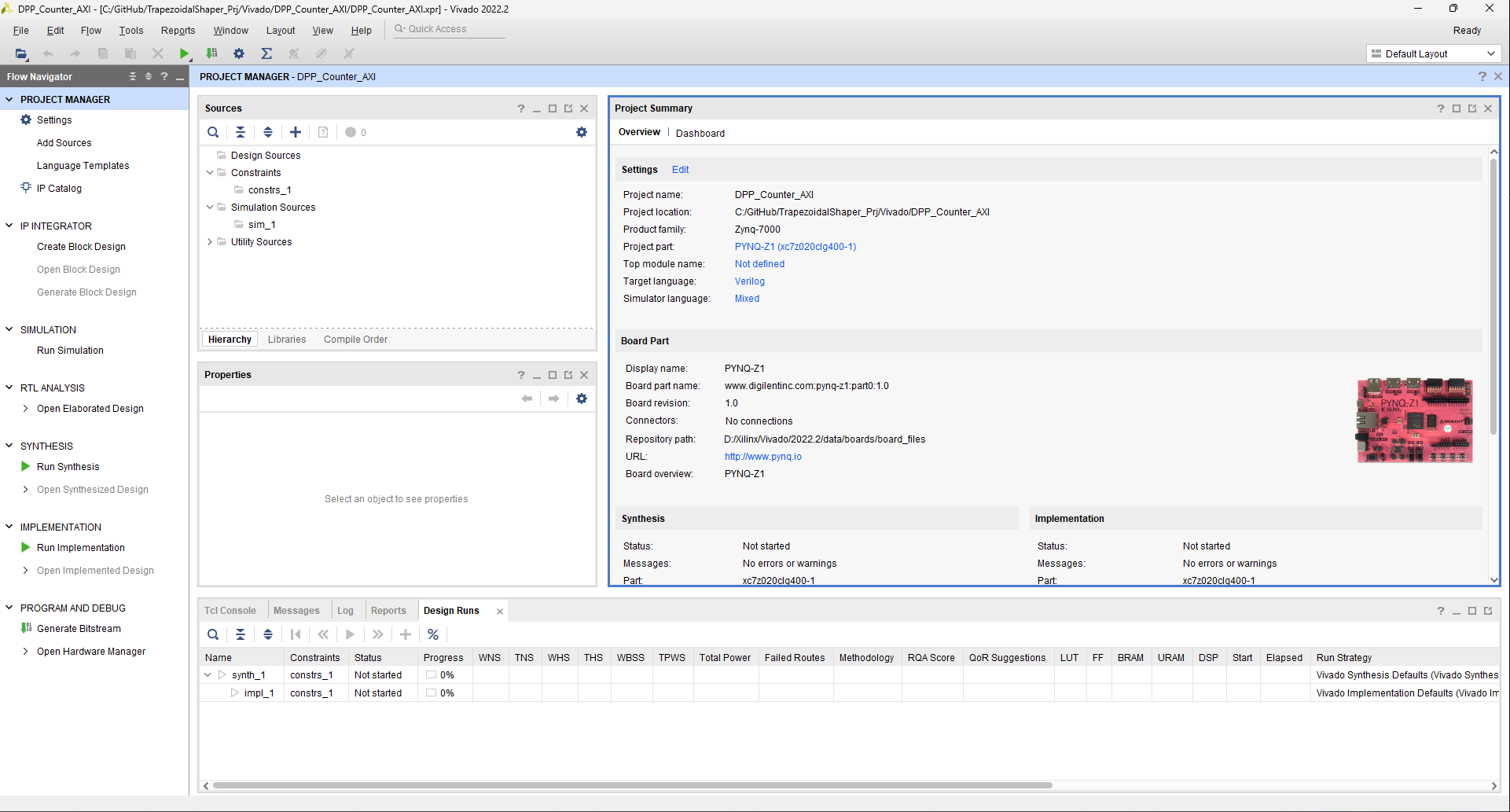
Se crea el proyecto



Se verifica que el lenguaje sea VHDL

Interfaz de usuario gráfica, Aplicación

Descripción generada automáticamente

Now you need to create a block design to add the different modules to the project

Interfaz de usuario gráfica, Aplicación

Descripción generada automáticamente

Also, create a constrain file with the follow code

## This file is a general .xdc for the PYNQ-Z1 board Rev. C

## To use it in a project:

## - uncomment the lines corresponding to used pins

## - rename the used ports (in each line, after get\_ports) according to the top level signal names in the project

## Clock signal 125 MHz

#set\_property -dict { PACKAGE\_PIN H16 IOSTANDARD LVCMOS33 } [get\_ports { sysclk }]; #IO\_L13P\_T2\_MRCC\_35 Sch=sysclk

#create\_clock -add -name sys\_clk\_pin -period 8.00 -waveform {0 4} [get\_ports { sysclk }];

##Switches

#set\_property -dict { PACKAGE\_PIN M20 IOSTANDARD LVCMOS33 } [get\_ports { sw[0] }]; #IO\_L7N\_T1\_AD2N\_35 Sch=sw[0]

#set\_property -dict { PACKAGE\_PIN M19 IOSTANDARD LVCMOS33 } [get\_ports { sw[1] }]; #IO\_L7P\_T1\_AD2P\_35 Sch=sw[1]

##RGB LEDs

#set\_property -dict { PACKAGE\_PIN L15 IOSTANDARD LVCMOS33 } [get\_ports { led\_0[4] }]; #IO\_L22N\_T3\_AD7N\_35 Sch=led4\_b

#set\_property -dict { PACKAGE\_PIN G17 IOSTANDARD LVCMOS33 } [get\_ports { led\_0[5] }]; #IO\_L16P\_T2\_35 Sch=led4\_g

#set\_property -dict { PACKAGE\_PIN N15 IOSTANDARD LVCMOS33 } [get\_ports { led\_0[6] }]; #IO\_L21P\_T3\_DQS\_AD14P\_35 Sch=led4\_r

#set\_property -dict { PACKAGE\_PIN G14 IOSTANDARD LVCMOS33 } [get\_ports { led\_0[7] }]; #IO\_0\_35 Sch=led5\_b

#set\_property -dict { PACKAGE\_PIN L14 IOSTANDARD LVCMOS33 } [get\_ports { led\_rst\_0 }]; #IO\_L22P\_T3\_AD7P\_35 Sch=led5\_g

#set\_property -dict { PACKAGE\_PIN M15 IOSTANDARD LVCMOS33 } [get\_ports { led\_1 }]; #IO\_L23N\_T3\_35 Sch=led5\_r

##LEDs

#set\_property -dict { PACKAGE\_PIN R14 IOSTANDARD LVCMOS33 } [get\_ports { led\_0[0] }]; #IO\_L6N\_T0\_VREF\_34 Sch=led[0]

#set\_property -dict { PACKAGE\_PIN P14 IOSTANDARD LVCMOS33 } [get\_ports { led\_0[1] }]; #IO\_L6P\_T0\_34 Sch=led[1]

#set\_property -dict { PACKAGE\_PIN N16 IOSTANDARD LVCMOS33 } [get\_ports { led\_0[2] }]; #IO\_L21N\_T3\_DQS\_AD14N\_35 Sch=led[2]

#set\_property -dict { PACKAGE\_PIN M14 IOSTANDARD LVCMOS33 } [get\_ports { led\_0[3] }]; #IO\_L23P\_T3\_35 Sch=led[3]

##Buttons

#set\_property -dict { PACKAGE\_PIN D19 IOSTANDARD LVCMOS33 } [get\_ports { in\_sig\_0 }]; #IO\_L4P\_T0\_35 Sch=btn[0]

#set\_property CLOCK\_DEDICATED\_ROUTE FALSE [get\_nets { in\_sig\_0\_IBUF }];

#set\_property -dict { PACKAGE\_PIN D20 IOSTANDARD LVCMOS33 } [get\_ports { fifo\_en\_0 }]; #IO\_L4N\_T0\_35 Sch=btn[1]

#set\_property -dict { PACKAGE\_PIN L20 IOSTANDARD LVCMOS33 } [get\_ports { btn[2] }]; #IO\_L9N\_T1\_DQS\_AD3N\_35 Sch=btn[2]

#set\_property -dict { PACKAGE\_PIN L19 IOSTANDARD LVCMOS33 } [get\_ports { btn[3] }]; #IO\_L9P\_T1\_DQS\_AD3P\_35 Sch=btn[3]

##Pmod Header JA

#set\_property -dict { PACKAGE\_PIN Y18 IOSTANDARD LVCMOS33 } [get\_ports { ja[0] }]; #IO\_L17P\_T2\_34 Sch=ja\_p[1]

#set\_property -dict { PACKAGE\_PIN Y19 IOSTANDARD LVCMOS33 } [get\_ports { ja[1] }]; #IO\_L17N\_T2\_34 Sch=ja\_n[1]

#set\_property -dict { PACKAGE\_PIN Y16 IOSTANDARD LVCMOS33 } [get\_ports { ja[2] }]; #IO\_L7P\_T1\_34 Sch=ja\_p[2]

#set\_property -dict { PACKAGE\_PIN Y17 IOSTANDARD LVCMOS33 } [get\_ports { ja[3] }]; #IO\_L7N\_T1\_34 Sch=ja\_n[2]

#set\_property -dict { PACKAGE\_PIN U18 IOSTANDARD LVCMOS33 } [get\_ports { ja[4] }]; #IO\_L12P\_T1\_MRCC\_34 Sch=ja\_p[3]

#set\_property -dict { PACKAGE\_PIN U19 IOSTANDARD LVCMOS33 } [get\_ports { ja[5] }]; #IO\_L12N\_T1\_MRCC\_34 Sch=ja\_n[3]

#set\_property -dict { PACKAGE\_PIN W18 IOSTANDARD LVCMOS33 } [get\_ports { ja[6] }]; #IO\_L22P\_T3\_34 Sch=ja\_p[4]

#set\_property -dict { PACKAGE\_PIN W19 IOSTANDARD LVCMOS33 } [get\_ports { ja[7] }]; #IO\_L22N\_T3\_34 Sch=ja\_n[4]

##Pmod Header JB

#set\_property -dict { PACKAGE\_PIN W14 IOSTANDARD LVCMOS33 } [get\_ports { jb[0] }]; #IO\_L8P\_T1\_34 Sch=jb\_p[1]

#set\_property -dict { PACKAGE\_PIN Y14 IOSTANDARD LVCMOS33 } [get\_ports { jb[1] }]; #IO\_L8N\_T1\_34 Sch=jb\_n[1]

#set\_property -dict { PACKAGE\_PIN T11 IOSTANDARD LVCMOS33 } [get\_ports { jb[2] }]; #IO\_L1P\_T0\_34 Sch=jb\_p[2]

#set\_property -dict { PACKAGE\_PIN T10 IOSTANDARD LVCMOS33 } [get\_ports { jb[3] }]; #IO\_L1N\_T0\_34 Sch=jb\_n[2]

#set\_property -dict { PACKAGE\_PIN V16 IOSTANDARD LVCMOS33 } [get\_ports { jb[4] }]; #IO\_L18P\_T2\_34 Sch=jb\_p[3]

#set\_property -dict { PACKAGE\_PIN W16 IOSTANDARD LVCMOS33 } [get\_ports { jb[5] }]; #IO\_L18N\_T2\_34 Sch=jb\_n[3]

#set\_property -dict { PACKAGE\_PIN V12 IOSTANDARD LVCMOS33 } [get\_ports { jb[6] }]; #IO\_L4P\_T0\_34 Sch=jb\_p[4]

#set\_property -dict { PACKAGE\_PIN W13 IOSTANDARD LVCMOS33 } [get\_ports { jb[7] }]; #IO\_L4N\_T0\_34 Sch=jb\_n[4]

##Audio Out

#set\_property -dict { PACKAGE\_PIN R18 IOSTANDARD LVCMOS33 } [get\_ports { aud\_pwm }]; #IO\_L20N\_T3\_34 Sch=aud\_pwm

#set\_property -dict { PACKAGE\_PIN T17 IOSTANDARD LVCMOS33 } [get\_ports { aud\_sd }]; #IO\_L20P\_T3\_34 Sch=aud\_sd

##Mic input

#set\_property -dict { PACKAGE\_PIN F17 IOSTANDARD LVCMOS33 } [get\_ports { m\_clk }]; #IO\_L6N\_T0\_VREF\_35 Sch=m\_clk

#set\_property -dict { PACKAGE\_PIN G18 IOSTANDARD LVCMOS33 } [get\_ports { m\_data }]; #IO\_L16N\_T2\_35 Sch=m\_data

##ChipKit Single Ended Analog Inputs

##NOTE: The ck\_an\_p pins can be used as single ended analog inputs with voltages from 0-3.3V (Chipkit Analog pins A0-A5).

## These signals should only be connected to the XADC core. When using these pins as digital I/O, use pins ck\_io[14-19].

set\_property -dict { PACKAGE\_PIN D18 IOSTANDARD LVCMOS33 } [get\_ports { Vaux1\_0\_v\_n }]; #IO\_L3N\_T0\_DQS\_AD1N\_35 Sch=ck\_an\_n[0]

set\_property -dict { PACKAGE\_PIN E17 IOSTANDARD LVCMOS33 } [get\_ports { Vaux1\_0\_v\_p }]; #IO\_L3P\_T0\_DQS\_AD1P\_35 Sch=ck\_an\_p[0]

#set\_property -dict { PACKAGE\_PIN E19 IOSTANDARD LVCMOS33 } [get\_ports { Vaux9\_0\_v\_n }]; #IO\_L5N\_T0\_AD9N\_35 Sch=ck\_an\_n[1]

#set\_property -dict { PACKAGE\_PIN E18 IOSTANDARD LVCMOS33 } [get\_ports { Vaux9\_0\_v\_p }]; #IO\_L5P\_T0\_AD9P\_35 Sch=ck\_an\_p[1]

#set\_property -dict { PACKAGE\_PIN J14 IOSTANDARD LVCMOS33 } [get\_ports { Vaux6\_0\_v\_n }]; #IO\_L20N\_T3\_AD6N\_35 Sch=ck\_an\_n[2]

#set\_property -dict { PACKAGE\_PIN K14 IOSTANDARD LVCMOS33 } [get\_ports { Vaux6\_0\_v\_p }]; #IO\_L20P\_T3\_AD6P\_35 Sch=ck\_an\_p[2]

#set\_property -dict { PACKAGE\_PIN J16 IOSTANDARD LVCMOS33 } [get\_ports { Vaux15\_0\_v\_n }]; #IO\_L24N\_T3\_AD15N\_35 Sch=ck\_an\_n[3]

#set\_property -dict { PACKAGE\_PIN K16 IOSTANDARD LVCMOS33 } [get\_ports { Vaux15\_0\_v\_p }]; #IO\_L24P\_T3\_AD15P\_35 Sch=ck\_an\_p[3]

#set\_property -dict { PACKAGE\_PIN H20 IOSTANDARD LVCMOS33 } [get\_ports { ck\_an\_n[4] }]; #IO\_L17N\_T2\_AD5N\_35 Sch=ck\_an\_n[4]

#set\_property -dict { PACKAGE\_PIN J20 IOSTANDARD LVCMOS33 } [get\_ports { ck\_an\_p[4] }]; #IO\_L17P\_T2\_AD5P\_35 Sch=ck\_an\_p[4]

#set\_property -dict { PACKAGE\_PIN G20 IOSTANDARD LVCMOS33 } [get\_ports { ck\_an\_n[5] }]; #IO\_L18N\_T2\_AD13N\_35 Sch=ck\_an\_n[5]

#set\_property -dict { PACKAGE\_PIN G19 IOSTANDARD LVCMOS33 } [get\_ports { ck\_an\_p[5] }]; #IO\_L18P\_T2\_AD13P\_35 Sch=ck\_an\_p[5]

##ChipKit Digital I/O Low

#set\_property -dict { PACKAGE\_PIN T14 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[0] }]; #IO\_L5P\_T0\_34 Sch=ck\_io[0]

#set\_property -dict { PACKAGE\_PIN U12 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[1] }]; #IO\_L2N\_T0\_34 Sch=ck\_io[1]

#set\_property -dict { PACKAGE\_PIN U13 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[2] }]; #IO\_L3P\_T0\_DQS\_PUDC\_B\_34 Sch=ck\_io[2]

#set\_property -dict { PACKAGE\_PIN V13 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[3] }]; #IO\_L3N\_T0\_DQS\_34 Sch=ck\_io[3]

#set\_property -dict { PACKAGE\_PIN V15 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[4] }]; #IO\_L10P\_T1\_34 Sch=ck\_io[4]

#set\_property -dict { PACKAGE\_PIN T15 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[5] }]; #IO\_L5N\_T0\_34 Sch=ck\_io[5]

#set\_property -dict { PACKAGE\_PIN R16 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[6] }]; #IO\_L19P\_T3\_34 Sch=ck\_io[6]

#set\_property -dict { PACKAGE\_PIN U17 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[7] }]; #IO\_L9N\_T1\_DQS\_34 Sch=ck\_io[7]

#set\_property -dict { PACKAGE\_PIN V17 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[8] }]; #IO\_L21P\_T3\_DQS\_34 Sch=ck\_io[8]

#set\_property -dict { PACKAGE\_PIN V18 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[9] }]; #IO\_L21N\_T3\_DQS\_34 Sch=ck\_io[9]

#set\_property -dict { PACKAGE\_PIN T16 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[10] }]; #IO\_L9P\_T1\_DQS\_34 Sch=ck\_io[10]

#set\_property -dict { PACKAGE\_PIN R17 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[11] }]; #IO\_L19N\_T3\_VREF\_34 Sch=ck\_io[11]

#set\_property -dict { PACKAGE\_PIN P18 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[12] }]; #IO\_L23N\_T3\_34 Sch=ck\_io[12]

#set\_property -dict { PACKAGE\_PIN N17 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[13] }]; #IO\_L23P\_T3\_34 Sch=ck\_io[13]

##ChipKit Digital I/O On Outer Analog Header

##NOTE: These pins should be used when using the analog header signals A0-A5 as digital I/O (Chipkit digital pins 14-19)

#set\_property -dict { PACKAGE\_PIN Y11 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[14] }]; #IO\_L18N\_T2\_13 Sch=ck\_a[0]

#set\_property -dict { PACKAGE\_PIN Y12 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[15] }]; #IO\_L20P\_T3\_13 Sch=ck\_a[1]

#set\_property -dict { PACKAGE\_PIN W11 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[16] }]; #IO\_L18P\_T2\_13 Sch=ck\_a[2]

#set\_property -dict { PACKAGE\_PIN V11 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[17] }]; #IO\_L21P\_T3\_DQS\_13 Sch=ck\_a[3]

#set\_property -dict { PACKAGE\_PIN T5 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[18] }]; #IO\_L19P\_T3\_13 Sch=ck\_a[4]

#set\_property -dict { PACKAGE\_PIN U10 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[19] }]; #IO\_L12N\_T1\_MRCC\_13 Sch=ck\_a[5]

##ChipKit Digital I/O On Inner Analog Header

##NOTE: These pins will need to be connected to the XADC core when used as differential analog inputs (Chipkit analog pins A6-A11)

#set\_property -dict { PACKAGE\_PIN B20 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[20] }]; #IO\_L1N\_T0\_AD0N\_35 Sch=ad\_n[0]

#set\_property -dict { PACKAGE\_PIN C20 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[21] }]; #IO\_L1P\_T0\_AD0P\_35 Sch=ad\_p[0]

#set\_property -dict { PACKAGE\_PIN F20 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[22] }]; #IO\_L15N\_T2\_DQS\_AD12N\_35 Sch=ad\_n[12]

#set\_property -dict { PACKAGE\_PIN F19 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[23] }]; #IO\_L15P\_T2\_DQS\_AD12P\_35 Sch=ad\_p[12]

#set\_property -dict { PACKAGE\_PIN A20 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[24] }]; #IO\_L2N\_T0\_AD8N\_35 Sch=ad\_n[8]

#set\_property -dict { PACKAGE\_PIN B19 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[25] }]; #IO\_L2P\_T0\_AD8P\_35 Sch=ad\_p[8]

##ChipKit Digital I/O High

#set\_property -dict { PACKAGE\_PIN U5 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[26] }]; #IO\_L19N\_T3\_VREF\_13 Sch=ck\_io[26]

#set\_property -dict { PACKAGE\_PIN V5 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[27] }]; #IO\_L6N\_T0\_VREF\_13 Sch=ck\_io[27]

#set\_property -dict { PACKAGE\_PIN V6 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[28] }]; #IO\_L22P\_T3\_13 Sch=ck\_io[28]

#set\_property -dict { PACKAGE\_PIN U7 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[29] }]; #IO\_L11P\_T1\_SRCC\_13 Sch=ck\_io[29]

#set\_property -dict { PACKAGE\_PIN V7 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[30] }]; #IO\_L11N\_T1\_SRCC\_13 Sch=ck\_io[30]

#set\_property -dict { PACKAGE\_PIN U8 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[31] }]; #IO\_L17N\_T2\_13 Sch=ck\_io[31]

#set\_property -dict { PACKAGE\_PIN V8 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[32] }]; #IO\_L15P\_T2\_DQS\_13 Sch=ck\_io[32]

#set\_property -dict { PACKAGE\_PIN V10 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[33] }]; #IO\_L21N\_T3\_DQS\_13 Sch=ck\_io[33]

#set\_property -dict { PACKAGE\_PIN W10 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[34] }]; #IO\_L16P\_T2\_13 Sch=ck\_io[34]

#set\_property -dict { PACKAGE\_PIN W6 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[35] }]; #IO\_L22N\_T3\_13 Sch=ck\_io[35]

#set\_property -dict { PACKAGE\_PIN Y6 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[36] }]; #IO\_L13N\_T2\_MRCC\_13 Sch=ck\_io[36]

#set\_property -dict { PACKAGE\_PIN Y7 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[37] }]; #IO\_L13P\_T2\_MRCC\_13 Sch=ck\_io[37]

#set\_property -dict { PACKAGE\_PIN W8 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[38] }]; #IO\_L15N\_T2\_DQS\_13 Sch=ck\_io[38]

#set\_property -dict { PACKAGE\_PIN Y8 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[39] }]; #IO\_L14N\_T2\_SRCC\_13 Sch=ck\_io[39]

#set\_property -dict { PACKAGE\_PIN W9 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[40] }]; #IO\_L16N\_T2\_13 Sch=ck\_io[40]

#set\_property -dict { PACKAGE\_PIN Y9 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[41] }]; #IO\_L14P\_T2\_SRCC\_13 Sch=ck\_io[41]

#set\_property -dict { PACKAGE\_PIN Y13 IOSTANDARD LVCMOS33 } [get\_ports { ck\_io[42] }]; #IO\_L20N\_T3\_13 Sch=ck\_ioa

## ChipKit SPI

#set\_property -dict { PACKAGE\_PIN W15 IOSTANDARD LVCMOS33 } [get\_ports { ck\_miso }]; #IO\_L10N\_T1\_34 Sch=ck\_miso

#set\_property -dict { PACKAGE\_PIN T12 IOSTANDARD LVCMOS33 } [get\_ports { ck\_mosi }]; #IO\_L2P\_T0\_34 Sch=ck\_mosi

#set\_property -dict { PACKAGE\_PIN H15 IOSTANDARD LVCMOS33 } [get\_ports { ck\_sck }]; #IO\_L19P\_T3\_35 Sch=ck\_sck

#set\_property -dict { PACKAGE\_PIN F16 IOSTANDARD LVCMOS33 } [get\_ports { ck\_ss }]; #IO\_L6P\_T0\_35 Sch=ck\_ss

## ChipKit I2C

#set\_property -dict { PACKAGE\_PIN P16 IOSTANDARD LVCMOS33 } [get\_ports { ck\_scl }]; #IO\_L24N\_T3\_34 Sch=ck\_scl

#set\_property -dict { PACKAGE\_PIN P15 IOSTANDARD LVCMOS33 } [get\_ports { ck\_sda }]; #IO\_L24P\_T3\_34 Sch=ck\_sda

##HDMI Rx

#set\_property -dict { PACKAGE\_PIN H17 IOSTANDARD LVCMOS33 } [get\_ports { hdmi\_rx\_cec }]; #IO\_L13N\_T2\_MRCC\_35 Sch=hdmi\_rx\_cec

#set\_property -dict { PACKAGE\_PIN P19 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_rx\_clk\_n }]; #IO\_L13N\_T2\_MRCC\_34 Sch=hdmi\_rx\_clk\_n

#set\_property -dict { PACKAGE\_PIN N18 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_rx\_clk\_p }]; #IO\_L13P\_T2\_MRCC\_34 Sch=hdmi\_rx\_clk\_p

#set\_property -dict { PACKAGE\_PIN W20 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_rx\_d\_n[0] }]; #IO\_L16N\_T2\_34 Sch=hdmi\_rx\_d\_n[0]

#set\_property -dict { PACKAGE\_PIN V20 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_rx\_d\_p[0] }]; #IO\_L16P\_T2\_34 Sch=hdmi\_rx\_d\_p[0]

#set\_property -dict { PACKAGE\_PIN U20 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_rx\_d\_n[1] }]; #IO\_L15N\_T2\_DQS\_34 Sch=hdmi\_rx\_d\_n[1]

#set\_property -dict { PACKAGE\_PIN T20 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_rx\_d\_p[1] }]; #IO\_L15P\_T2\_DQS\_34 Sch=hdmi\_rx\_d\_p[1]

#set\_property -dict { PACKAGE\_PIN P20 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_rx\_d\_n[2] }]; #IO\_L14N\_T2\_SRCC\_34 Sch=hdmi\_rx\_d\_n[2]

#set\_property -dict { PACKAGE\_PIN N20 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_rx\_d\_p[2] }]; #IO\_L14P\_T2\_SRCC\_34 Sch=hdmi\_rx\_d\_p[2]

#set\_property -dict { PACKAGE\_PIN T19 IOSTANDARD LVCMOS33 } [get\_ports { hdmi\_rx\_hpd }]; #IO\_25\_34 Sch=hdmi\_rx\_hpd

#set\_property -dict { PACKAGE\_PIN U14 IOSTANDARD LVCMOS33 } [get\_ports { hdmi\_rx\_scl }]; #IO\_L11P\_T1\_SRCC\_34 Sch=hdmi\_rx\_scl

#set\_property -dict { PACKAGE\_PIN U15 IOSTANDARD LVCMOS33 } [get\_ports { hdmi\_rx\_sda }]; #IO\_L11N\_T1\_SRCC\_34 Sch=hdmi\_rx\_sda

##HDMI Tx

#set\_property -dict { PACKAGE\_PIN G15 IOSTANDARD LVCMOS33 } [get\_ports { hdmi\_tx\_cec }]; #IO\_L19N\_T3\_VREF\_35 Sch=hdmi\_tx\_cec

#set\_property -dict { PACKAGE\_PIN L17 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_tx\_clk\_n }]; #IO\_L11N\_T1\_SRCC\_35 Sch=hdmi\_tx\_clk\_n

#set\_property -dict { PACKAGE\_PIN L16 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_tx\_clk\_p }]; #IO\_L11P\_T1\_SRCC\_35 Sch=hdmi\_tx\_clk\_p

#set\_property -dict { PACKAGE\_PIN K18 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_tx\_d\_n[0] }]; #IO\_L12N\_T1\_MRCC\_35 Sch=hdmi\_tx\_d\_n[0]

#set\_property -dict { PACKAGE\_PIN K17 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_tx\_d\_p[0] }]; #IO\_L12P\_T1\_MRCC\_35 Sch=hdmi\_tx\_d\_p[0]

#set\_property -dict { PACKAGE\_PIN J19 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_tx\_d\_n[1] }]; #IO\_L10N\_T1\_AD11N\_35 Sch=hdmi\_tx\_d\_n[1]

#set\_property -dict { PACKAGE\_PIN K19 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_tx\_d\_p[1] }]; #IO\_L10P\_T1\_AD11P\_35 Sch=hdmi\_tx\_d\_p[1]

#set\_property -dict { PACKAGE\_PIN H18 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_tx\_d\_n[2] }]; #IO\_L14N\_T2\_AD4N\_SRCC\_35 Sch=hdmi\_tx\_d\_n[2]

#set\_property -dict { PACKAGE\_PIN J18 IOSTANDARD TMDS\_33 } [get\_ports { hdmi\_tx\_d\_p[2] }]; #IO\_L14P\_T2\_AD4P\_SRCC\_35 Sch=hdmi\_tx\_d\_p[2]

#set\_property -dict { PACKAGE\_PIN R19 IOSTANDARD LVCMOS33 } [get\_ports { hdmi\_tx\_hpdn }]; #IO\_0\_34 Sch=hdmi\_tx\_hpdn

#set\_property -dict { PACKAGE\_PIN M17 IOSTANDARD LVCMOS33 } [get\_ports { hdmi\_tx\_scl }]; #IO\_L8P\_T1\_AD10P\_35 Sch=hdmi\_tx\_scl

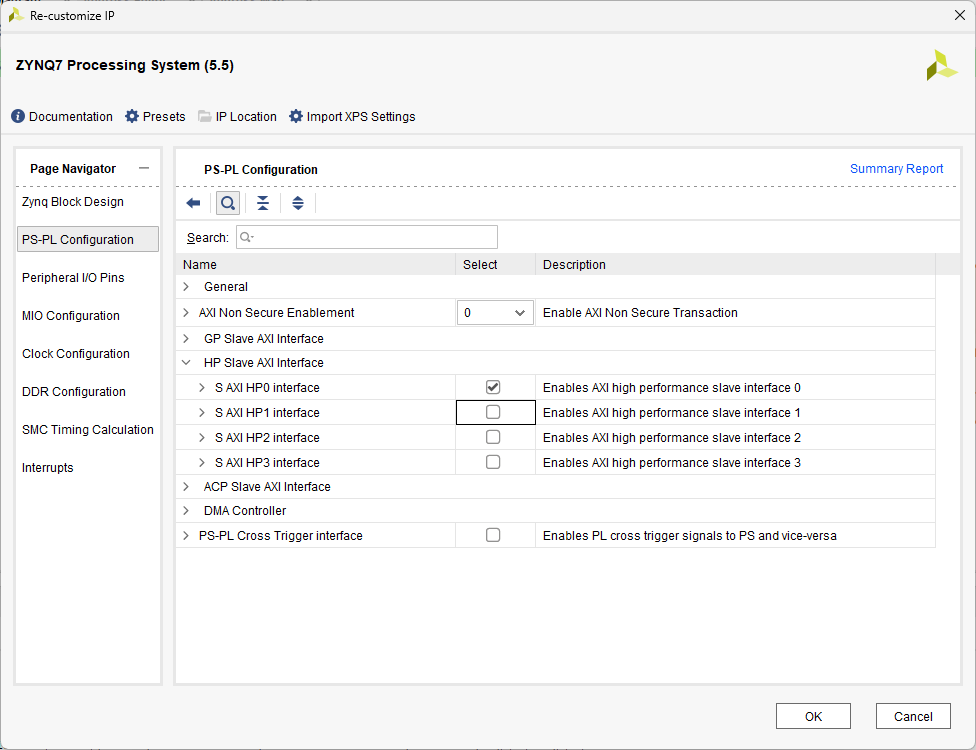
#set\_property -dict { PACKAGE\_PIN M18 IOSTANDARD LVCMOS33 } [get\_ports { hdmi\_tx\_sda }]; #IO\_L8N\_T1\_AD10N\_35 Sch=hdmi\_tx\_sda

##Crypto SDA

#set\_property -dict { PACKAGE\_PIN J15 IOSTANDARD LVCMOS33 } [get\_ports { crypto\_sda }]; #IO\_25\_35 Sch=crypto\_sda

Add the zynq processor, run the block automation and double click to modify the block,

Just add S AXI HP0 interface to add Slave axi stream support



Also add XADC module, double click on it, and apply the next modifications

Interfaz de usuario gráfica, Aplicación

Descripción generada automáticamente

Interfaz de usuario gráfica, Aplicación

Descripción generada automáticamente

Interfaz de usuario gráfica

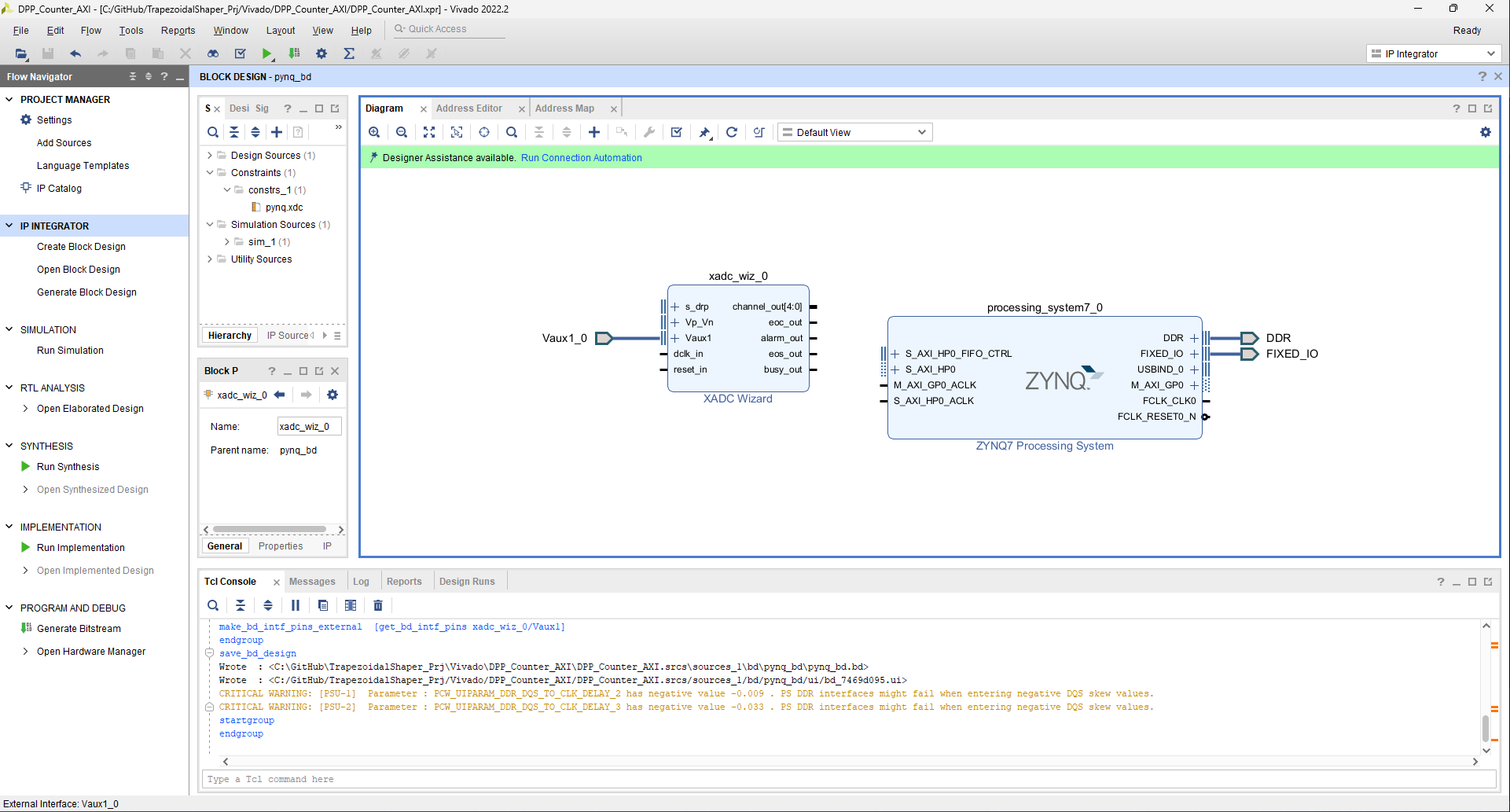
Descripción generada automáticamente

Interfaz de usuario gráfica, Texto, Aplicación

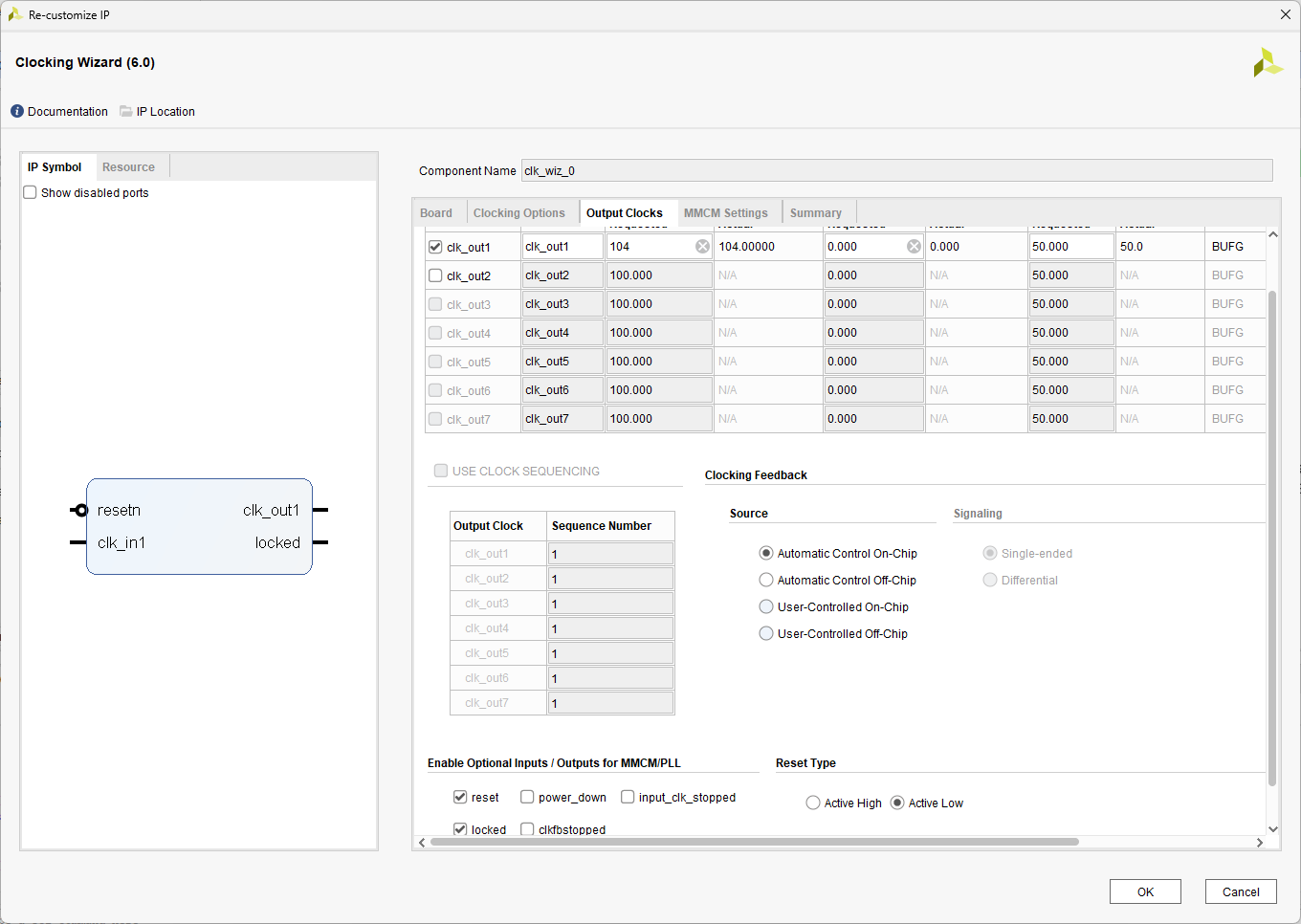
Descripción generada automáticamente

Then make external the Vaux1 bus, it will connect externally with the pins in the constrain file defined as Vaux1\_0

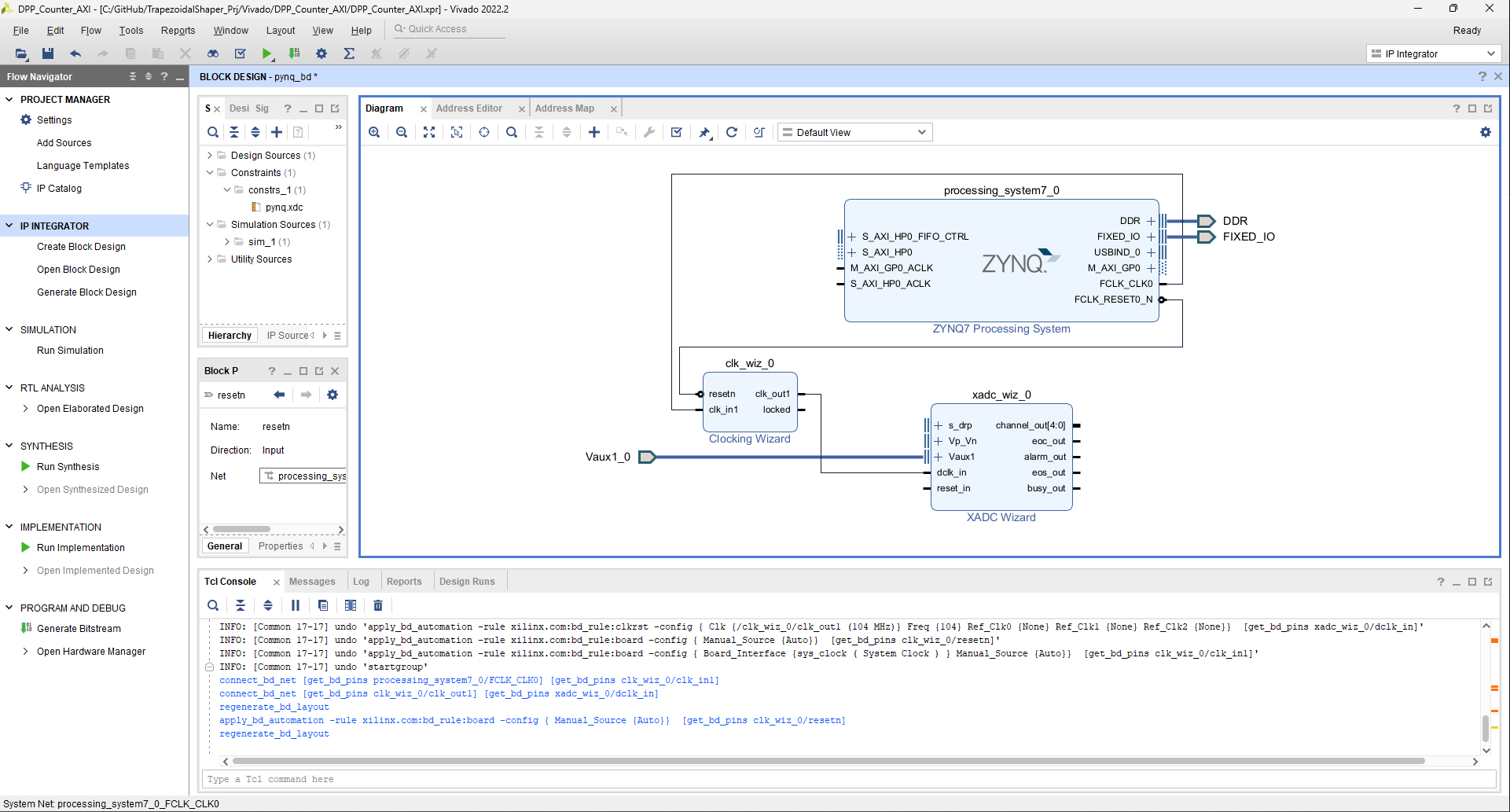
Until this point it looks like this



Add a clock wizard block aand configurate the outpuyt to 104 MHz and Reset as active low



Make the connections as follow



%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Now create the XADC buffer block

----------------------------------------------------------------------------------

-- Company: Universidad de Antioquia

-- Engineer: Fabian Castano

-- Description: This modules convert the 16 bits data from XADC in

-- 32 bits data, also syncronize with clock

----------------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

-- Entity creation

entity xadc\_buffer is

Port ( adc\_clk : in std\_logic;

adc\_rst : in std\_logic;

adc\_in : in std\_logic\_vector (15 downto 0);

adc\_out : out std\_logic\_vector (31 downto 0)

);

end xadc\_buffer;

architecture Behavioral of xadc\_buffer is

signal buf\_xadc : std\_logic\_vector (31 downto 0);

begin

BUFFER\_PROCESS: process (adc\_clk, adc\_rst)

begin

if (adc\_rst = '0') then

buf\_xadc <= X"00000000";

else

if rising\_edge(adc\_clk) then

buf\_xadc <= X"0000" & adc\_in;

end if;

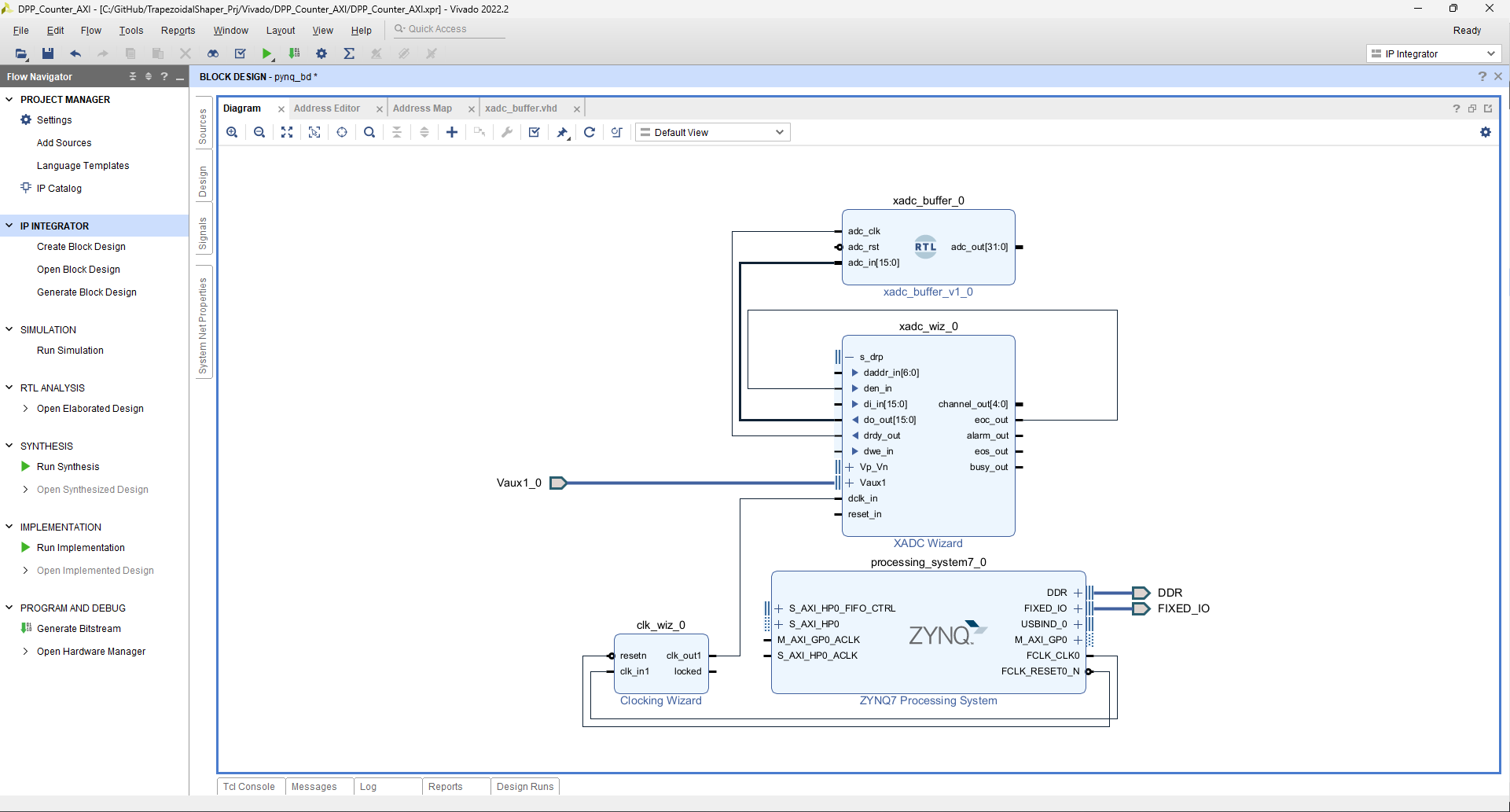
end if;

end process;

adc\_out <= buf\_xadc;

end Behavioral;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%



Add an constant to handled XADC addres. (17 for Vaux1 channel)

Interfaz de usuario gráfica, Aplicación

Descripción generada automáticamente