

Algorithm FEAS

Given a synchronous circuit G and a desired clock period c , this algorithm produces a retiming r of G such that G_r is a synchronous circuit with clock period $\Phi(G_r) \leq c$, if such a retiming exists.

1. For each vertex $v \in V$, set $r(v) \leftarrow 0$.
2. Repeat the following $|V| - 1$ times.
 - A. Compute graph G_r with the existing values for r .
 - B. Run Algorithm CP on the graph G_r to determine $\Delta(v) \forall v \in V$.
 - C. For each v such that $\Delta(v) > c$, set $r(v) \leftarrow r(v) + 1$.
3. Run Algorithm CP on the circuit G_r . If we have $\Phi(G_r) > c$, then no feasible retiming exists. Otherwise, r is the desired retiming.

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Complexity

- Time complexity: $\mathcal{O}(VE)$.
 - It may be wrong due to the possibly wrong time complexity of CP.
- Space complexity: $\mathcal{O}(V + E)$.