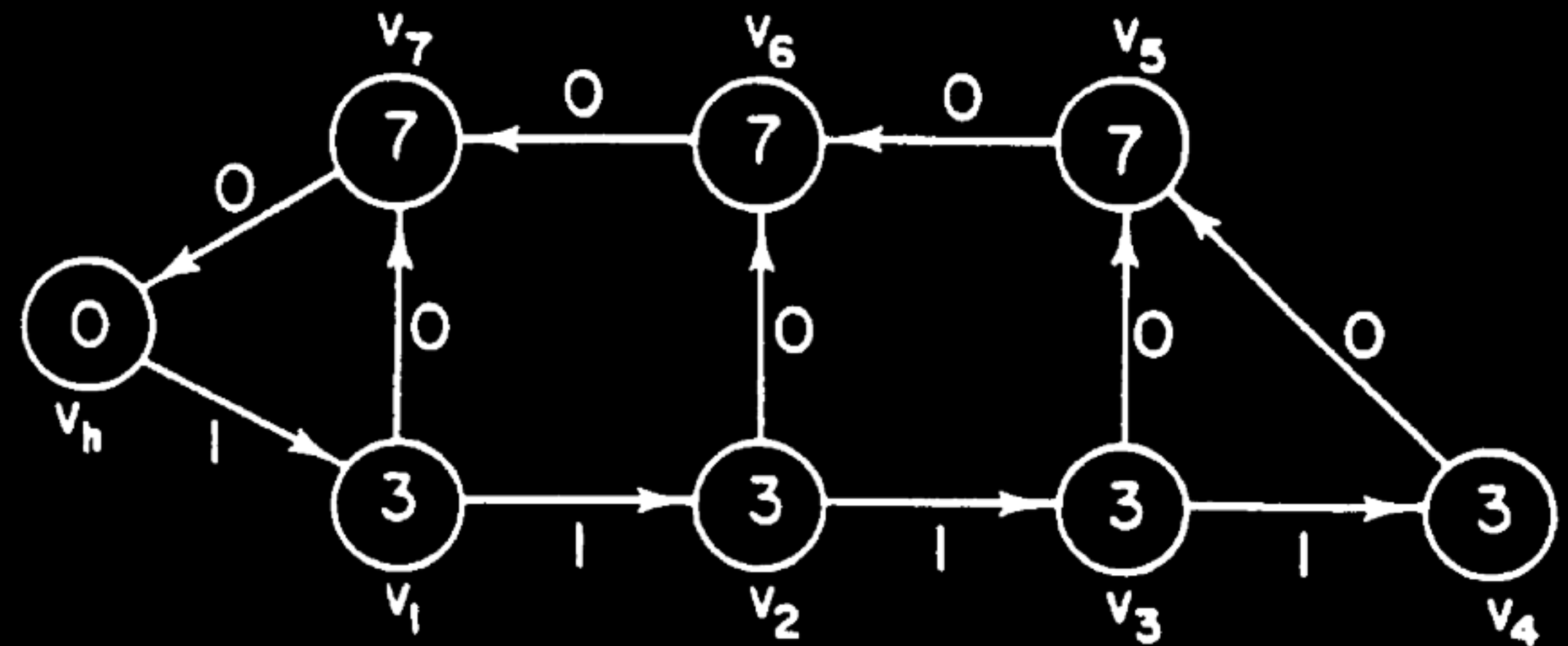


# The problem

The goal is to optimize clocked circuits by relocating registers so as to reduce combinational rippling, while maintaining the functional behavior of the circuit.

We model a circuit as a finite, vertex-weighted, edge-weighted, directed multigraph

$$G = \langle V, E, d, w \rangle.$$



# The problem

- The vertices  $V$  of the graph model the functional elements of the circuit.
- Each vertex  $v \in V$  is weighted with its numerical propagation delay  $d(v)$ .

