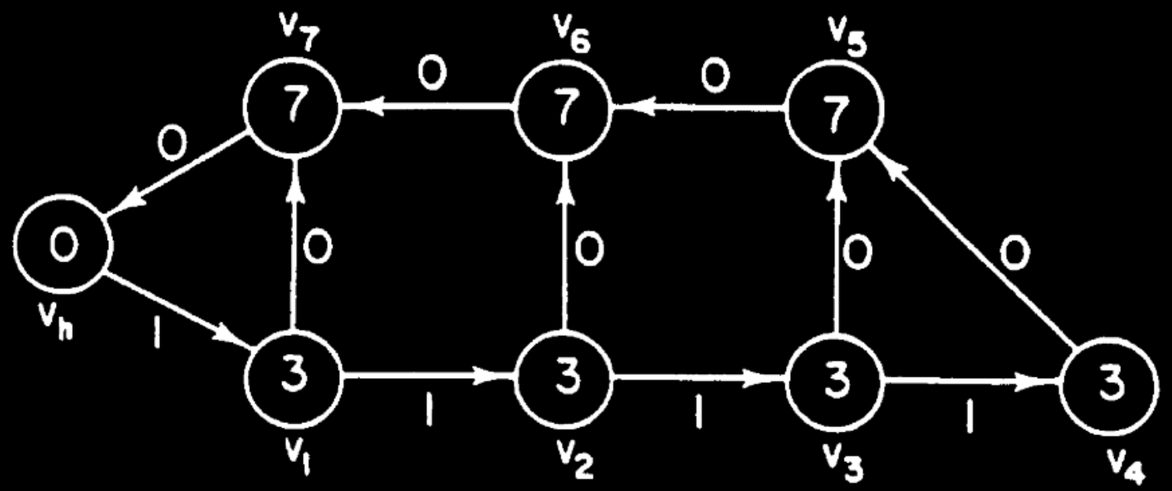
The problem

For any synchronous circuit G, we define the (minimum feasible) *clock period*.

$$\Phi(G) = \max\{d(p) : w(p) = 0\}$$

$$w(p) = \sum_{i=0}^{k-1} w(e_i) \qquad d(p) = \sum_{i=0}^{k-1} d(v_i)$$



The problem

A *retiming* of a circuit $G = \langle V, E, d, w \rangle$ is a function $r : V \mapsto \mathbb{Z}$ that transforms G into $G_r = \langle V, E, d, w_r \rangle$, where

$$w_r(e) = w(e) + r(v) - r(u).$$