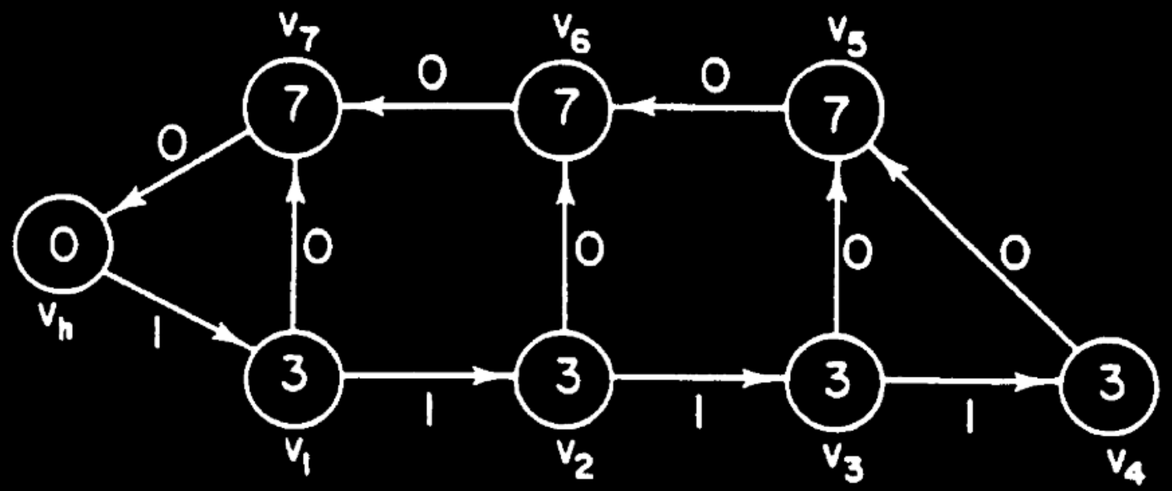
The problem

- The directed edges E of the graph model the interconnections between functional elements.
- Each edge $e \in E$ connects an output of some functional element to an input of some functional element and is weighted with a register count $w(e)$.



The problem

We define a *synchronous circuit* as a circuit that satisfies the following conditions

- $d(v) \geq 0 \quad \forall v \in V$
- $w(e) \geq 0 \quad \forall e \in E$
- In any directed cycle of the graph, there is some edge with strictly positive register count.