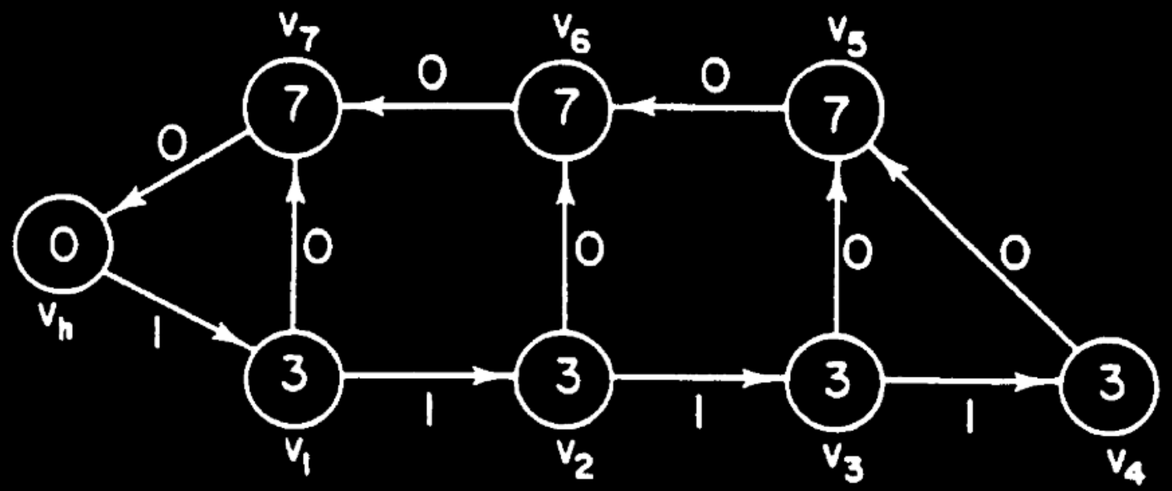
The problem

We define a *synchronous circuit* as a circuit that satisfies the following conditions

- $d(v) \geq 0 \quad \forall v \in V$
- $w(e) \geq 0 \quad \forall e \in E$
- In any directed cycle of the graph, there is some edge with strictly positive register count.



The problem

For any synchronous circuit G, we define the (minimum feasible) *clock period*.

$$\Phi(G) = \max\{d(p) : w(p) = 0\}$$

$$w(p) = \sum_{i=0}^{k-1} w(e_i) \qquad d(p) = \sum_{i=0}^{k-1} d(v_i)$$