

Algorithm FEAS

Complexity

- Time complexity: $\mathcal{O}(VE)$.
 - It may be wrong due to the possibly wrong time complexity of CP.
- Space complexity: $\mathcal{O}(V + E)$.

Algorithm OPT2

Given a synchronous circuit G , determine a retiming r such that $\Phi(G_r)$ is as small as possible.

1. Compute W and D using Algorithm WD.
2. Sort the elements in the range of D .
3. Binary search among the elements $D(u, v)$ for the minimum achievable clock period. To test whether each potential clock period c is feasible, apply Algorithm FEAS.
4. For the minimum achievable clock period found in Step 3, use the values for the $r(v)$ found by Algorithm FEAS as the optimal retiming.