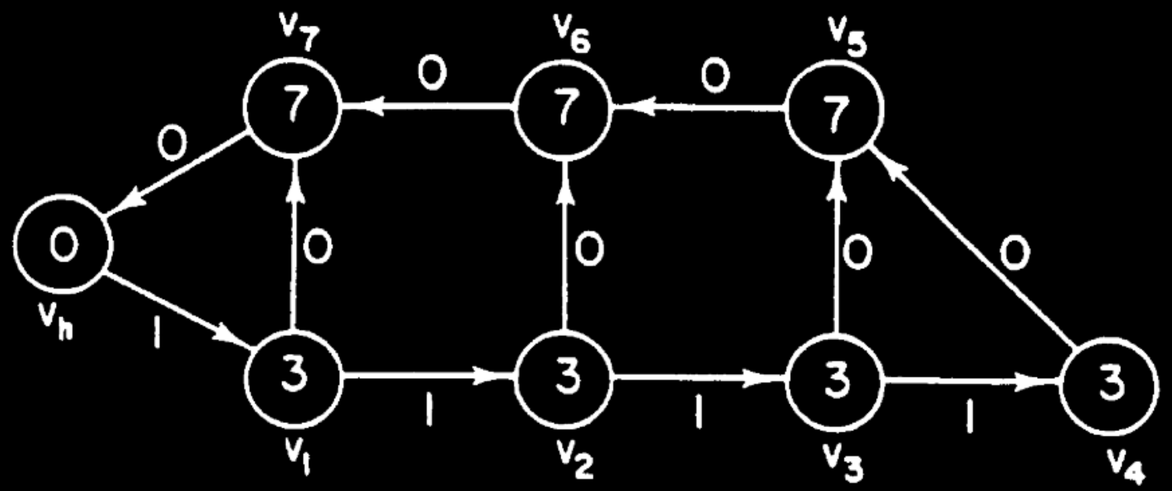
The problem

- The vertices V of the graph model the functional elements of the circuit.
- Each vertex $v \in V$ is weighted with its numerical propagation delay $d(v)$.



The problem

- The directed edges E of the graph model the interconnections between functional elements.
- Each edge $e \in E$ connects an output of some functional element to an input of some functional element and is weighted with a register count $w(e)$.