| Project | Rev. | Description | Release Date | Approved by |
|---|---|---|---|---|
| FBKD1701 | A | initial release | 2017.07.06 | DL, MAO |

1 IPC CLASSIFICATION:
BOARD TYPE:3
PERFORMANCE CLASS:2
COMPLEXITY LEVEL:B

2 FABRICATE BOARDS IN ACCORDANCE WITH IPC-6012B, CLASS 2.
FINISHED BOARDS MUST MEET QUALITY CONFORMANCE TESTING AND INSPECTION AS SPECIFIED.
REPORT SHOULD BE GIVEN TO CUSTOMER
BY-PRODUCTS MUST NOT MEET OR EXCEED A DECOMPOSITION TEMPERATURE OF 340 DEGREES CELCIUS.
T-288 OF > 3 MINUTES
ABILITY TO SURVIVE 6 PASS 246 DEGREES CELCIUS ASSEMBLY SITUATION.

3 MATERIAL IN ACCORDANCE WITH IPC-4101, LAMINATED SHEET.
FLAME RESISTANT (MEETING UL 94V-0) TG RATING:170°C MINIMUM.
MATERIAL MUST MEET RoHS AND WEEE REQUIREMENT.
MATERIAL SHALL BE SPECIFIED FOR LEAD FREE ASSEMBLY.
MATERIAL SHALL MEET OR EXCEED A DECOMPOSITION TEMPERATURE OF 340 DEGREES CELCIUS.
T-288 OF > 3 MINUTES
ABILITY TO SURVIVE 6 PASS 246 DEGREES CELCIUS ASSEMBLY SITUATION.

4 MATERIAL IN ACCORDANCE WITH IPC-4101, PREPREG (B-STAGE).
FLAME RESISTANT (MEETING UL 94V-0) TG RATING:170°C MINIMUM
MATERIAL MUST MEET RoHS AND WEEE REQUIREMENT.
MATERIAL SHALL BE SPECIFIED FOR LEAD FREE ASSEMBLY.
MATERIAL SHALL MEET OR EXCEED A DECOMPOSITION TEMPERATURE OF 340 DEGREES CELCIUS.
T-288 OF > 3 MINUTES
ABILITY TO SURVIVE 6 PASS 246 DEGREES CELCIUS ASSEMBLY SITUATION.

5 BOARD FABRICATOR SHALL APPLY DATE CODE, FABRICATOR'S TYPE DESIGNATION, 94V-0 AND UL MARKING TO PRIMARY AND/OR SECONDARY SIDE WHERE INDICATED. MARKING TO BE COPPER ETCHED. THE DATE CODE FORMAT SHALL BE WEEK-YEAR (I.E. 3898 WOULD INDICATE THE 38th WEEK OF YEAR 2008).

6 PRINTED CIRCUIT BOARDS SHALL EXHIBIT IONIC CONTAMINATION OF INNER LAYERS AFTER TREATMENT PRIOR TO LAMINATION AS PER IPC 6012B PARA. 3.9.3 AND SHALL BE LESS THAN 2.0µGRAM/square cm AS PER IPC-TM-650 METHOD 2.3.25 REV B.

7 CONSTRUCTION TO BE SMOBC, USING LIQUID PHOTOIMAGEABLE (LPI) SOLDER MASK MATERIAL. SOLDER MASK MATERIAL TO BE LIGHT GREEN IN COLOR, APPLIED TO
EXTERNAL LAYER WHERE INDICATED IN THE LAYER STACKUP IN ACCORDANCE WITH IPC-SM-840C CLASS T.
SOLDER MASK SHALL BE TYPE LPI, TYPE B IN CLASSIFICATION AND PERFORMANCE SPECIFICATION OF IPC-SM-840C.
SOLDER MASK SHALL MEET THE CURE REQUIREMENTS OF IPC-TM-650 METHOD 2.3.23. USE APPROPRIATE SOLDER MASK ARTWORK FOR EACH SIDE OF BOARD. PUNCTURING OF TENTED OR PLUGGED HOLES, IF ANY, IS NOT PERMISSIBLE.

8 PRINTED CIRCUIT BOARDS SHALL EXHIBIT IONIC CONTAMINATION LESS THAN AN EQUIVALENT OF 1.56 µGRAM/square cm OF NaCl AS PER IPC-6012B PARAGRAPH 3.9.1 WHEN MEASURED IN ACCORDANCE WITH IPC TM-650 METHOD 2.3.25 REV B. MEASUREMENTS SHALL BE MADE IMMEDIATELY PRIOR TO THE APPLICATION OF SOLDER MASK.

9 SOLDER MASK MISREGISTRATION SHALL NOT EXCEED +/-100µm.
MASK MATERIAL IS PERMITTED ON VIAS (ANNG).
MANUFACTURER CAN ADJUST SOLDERMASK OPENING EXCEPT FOR BGA PADS.
BGA PADS ARE ALREADY ADJUST FOR MISREGISTRATION AND SHALL NOT BE MODIFIED.
SOLDER MASK ON DAT PADS SHALL NOT BE PERMITTED.
EXPOSED ADJACENT TRACE SHALL NOT BE PERMITTED.
SOLDER MASK THICKNESS: 17µm MINIMUM, 50µm MAXIMUM

10 DRILL BOARDS USING DRILL DATA, DRILL PATTERN AND HOLE SCHEDULE. HOLE LOCATIONS MAY VARY WITHIN 75µm (RADIAL ERROR) MAX. ABOUT TRUE POSITION.

11 PLATING THICKNESS SHALL MEET THE REQUIREMENTS SPECIFIED IN IPC-6012B, TABLE 3-2.
COPPER CLASS 2 — 25µm MINIMUM AVERAGE. (NO SINGLE MEASUREMENT LESS THAN 18µm).
AG CLASS 2 — SOLDERABLE
PCB'S SHALL MEET THE REQUIREMENT OF ACCEPTANCE FOR SOLDERABILITY AS INDICATED IN IPC-A-600G, CLASS 2.

12 A MINIMUM OF 12 µm POSITIVE ETCHBACK SHALL BE MADE ON PCB FOR INNER LAYER CONTACT IF NOTE 1 REQUIRE A PERFORMANCE CLASS 3 OR 3A

13 MINIMUM ANNULAR RING AS PER PC CLASS IN NOTE 1.

14 ALL EXPOSED SURFACE LANDS AND LINES SHALL BE PLATED AS PER NOTE 11.

15 FINISHED LINES WIDTHS TOLERANCES ARE:
+/-25µm INNER LAYERS.
+/-50µ FOR CONDUCTOR WIDTH LESS OR EQUAL THAN 0.250mm ON OUTER LAYERS.
+/-50um FOR CONDUCTOR WIDTH LARGER THAN 0.250mm ON OUTER LAYERS.

16 N/A

17 DIMENSION ARE AFTER ETCHING AND PLATING, AND ARE BASIC UNLESS OTHERWISE INDICATED.

18 BOW AND TWIST SHALL NOT EXCEED 0.75% AS PER IPC-6012B, ASSESSED IN ACCORDANCE WITH IPC-TM-650, METHOD 2.4.22.

19 ALL ARTWORK OR DATA MAY BE ADJUSTED BY THE PCB FABRICATOR TO COMPENSATE FOR MANUFACTURING PROCESS TOLERANCES. CUSTOMER SHOULD BE NOTIFIED OF MODIFICATIONS AND GERBER OF SUCH MODIFICATIONS SHOULD BE SENT TO THE PCB DESIGNER FOR REVIEW AND APPROBATION.

20 DRAWINGS BASED ON IPC-2615.

21 UNLESS OTHERWISE SPECIFIED, HOLE FABRICATION ALLOWANCE : ±75µm.

22 IF APPLICABLE:
FOR EDGE-FIT CONNECTORS.
SPECIFICATIONS ARE:
DRILLED HOLE DIAMETER: 0.77mm ±0.72
FINISHED HOLE DIAMETER: 0.77mm ±0.72
FINISH (Note 11): 0.77mm - 0.77mm
FINISH (Note 11): 0.77 MM

23 SILKSCREEN MATERIAL SHALL BE PERMANENT NON-CONDUCTIVE, NON-CORROSIVE AND WHITE IN COLOR. THE SILKSCREEN SHALL SHOW NO DISCOLORATION IF IT HAS TO BE CURED. SILKSCREEN SHALL MEET THE ADHESION REQUIREMENTS OF IPC-TM-650, METHOD 2.4.1.1. SILKSCREEN SHALL MEET REQUIREMENTS OF IPC-TM-650, METHOD 2.3.4.

24 DESIGN DATA SHALL BE MODIFIED TO ENSURE THAT SILKSCREEN DOES NOT ENCROACH OVER CONDUCTOR PATTERN FEATURES. IN MOST CASES, THIS SHALL BE ACCOMPLISHED BY TRIMMING BACK SILKSCREEN DATA TO THE SOLDER RESIST DATA.

25 ELECTRICAL TEST REQUIREMENTS:
MAXIMUM CONTINUITY RESISTANCE: 50 Ω ≤ 18.0 @ 200 C
MINIMUM ISOLATION RESISTANCE: 50 Ω ≥ 5.18M Ω @ 180V MIN.
REPORT SHALL BE GIVEN TO CUSTOMER
AND SENT AT DCC_CADINUTAQ.COM

26 MICROSECTIONS REQUIREMENTS:
REPORT SHALL BE GIVEN TO CUSTOMER
AND SENT AT DCC_CADINUTAQ.COM

27 IF APPLICABLE: FILLED VIAS MATERIAL SHALL BE SIMILAR TO FICTER'S HOLE FILL PF2795 OR TATFO THP-100DX1 VF(non-conductive).

28 IF GERBER_DB IS PRESENT IN THE GERBER FILES OR LAYER "ATTENTION" IN ODB++, MANUFACTURER SHALL CHECK IT FOR SPECIAL ATTENTION ON CRITICAL FOOTPRINTS.

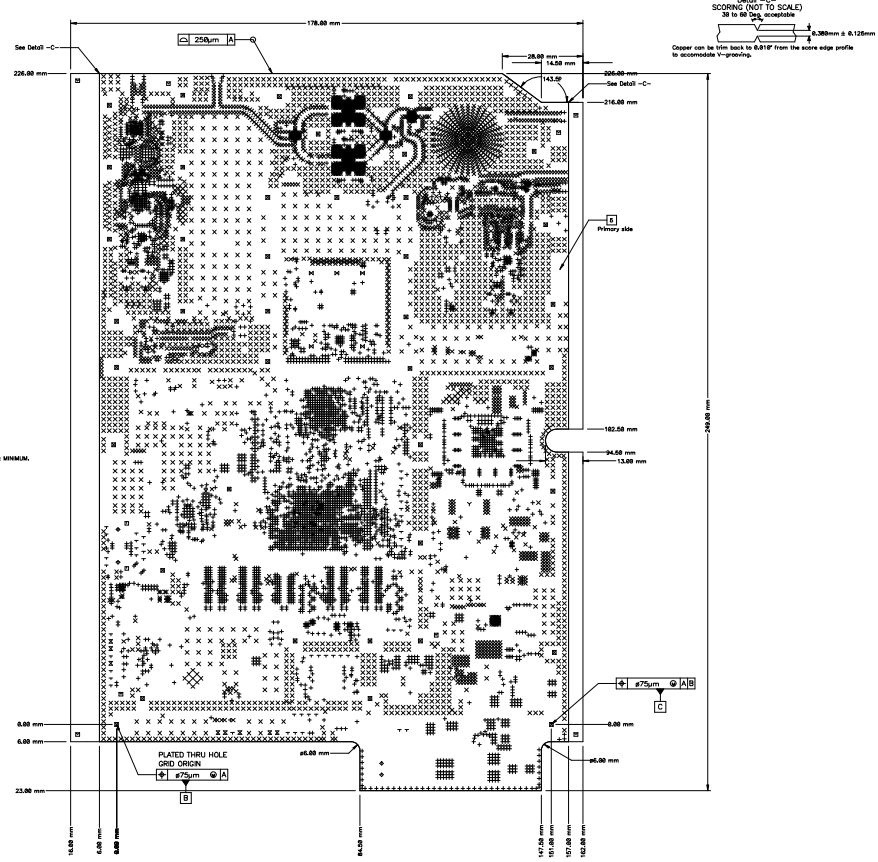
29 UNUSED PADS CAN BE REMOVED ON INTERNAL LAYERS

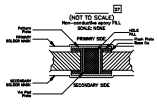
30 HOLE BREAKOUT IS ACCEPTABLE ON SAME NET.

31 ON OUTER LAYERS, BASE COPPER FOIL CAN BE 1/3oz TO ASSIST WITH ETCHING. FINAL COPPER WEIGHT SHOULD BE EQUIVALENT TO 0.5oz MINIMUM.

OTHER MANUFACTURER RELATED NOTES: FLAT-WRAPfm can be used if needed.

ACCEPTED SHORTED NETS :
GNDD GNDD1 GNDD2 NET00027




LAYERS STACK UP
FINISH PLATING: 31
SCALE: NONE

MULTILAYER CONSTRUCTION:

| | | | |
|---|---|---|---|
| TOP | TOP SLK | TOP SLK (White) 22 24 | |
| | TOP MSK | TOP MASK NO SWELL (LPI - Mat or Semi-Mat finish) 7 8 9 | |
| PRIMARY SIDE | FOIL | LAYER #1 Copper (0.5oz.) ----------(See DETAIL -B-) | |
| MEGTRON 6 R-5670 | PREPREG 0.097mm ** | | |
| | | LAYER #2 Copper Plane Negative View (0.5oz.) | |
| MEGTRON 6 R-5775 | CORE 0.152mm ** | | |
| | | LAYER #3 Copper Plane Negative View (0.5oz.) | |
| MEGTRON 6 R-5670 | PREPREG 0.152mm ** | | |
| | | LAYER #4 Copper (0.5oz.) ----------(See DETAIL -C-) | |
| MEGTRON 6 R-5775 | CORE 0.152mm ** | | |
| | | LAYER #5 Copper Plane Negative View (0.5oz.) | |
| MEGTRON 6 R-5670 | PREPREG 0.240mm ** | | |
| | | LAYER #6 Copper Plane Negative View (0.5oz.) | |
| MEGTRON 6 R-5775 | CORE 0.152mm ** | | |
| | | LAYER #7 Copper Plane Negative View (0.5oz.) | |
| MEGTRON 6 R-5670 | PREPREG 0.152mm ** | | |
| | | LAYER #8 Copper (0.5oz.) ----------(See DETAIL -C-) | |
| MEGTRON 6 R-5775 | CORE 0.152mm ** | | |
| | | LAYER #9 Copper Plane Negative View (0.5oz.) | |
| MEGTRON 6 R-5670 | PREPREG 0.097mm ** | | |
| SECONDARY SIDE | FOIL | LAYER #10 Copper (0.5oz.) ----------(See DETAIL -B-) | |
| BOTTOM | BOTTOM MSK | BOTTOM MASK NO SWELL (LPI - Mat or Semi-Mat finish) 7 8 9 | |
| | BOTTOM SLK | BOTTOM SLK (White) 22 24 | |

OVERALL THICKNESS AFTER PLATING 1.59mm ±10%

** ---> Manufacturer shall use the specified material.

Manufacturer may modify gerber to obtain required impedance for the traces with the following specifications:

Detail -B- (External Layer)
50 ± 5Ω, Ctrl. Imp.: W Trace = 1.081mm (Reference Plane 5 and Plane 6) (Cu-planar 0.258mm with adjacent copper. Traces without Soldermask on them.) <<IMPORTANT>> Contact customer for approval before modifing the 1.081mm traces or 0.258mm coplanars.
50 ± 5Ω, Ctrl. Imp.: W Trace = 0.508mm (Reference Plane 3) (Cu-planar 0.258mm with adjacent copper. Traces without Soldermask on them.) <<IMPORTANT>> Contact customer for approval before modifing the 0.508mm traces or 0.258mm coplanars.
50 ± 10Ω, Ctrl. Imp.: W Trace = 0.203mm
68.5 ± 10Ω, Ctrl. Imp.: W Trace = 0.2999mm
70 ± 5Ω, Ctrl. Imp.: W Trace = 0.216mm (Reference Plane 3) (Cu-planar 0.193mm with adjacent copper. Traces without Soldermask on them.) <<IMPORTANT>> Contact customer for approval before modifing the 0.216mm traces or 0.193mm coplanars.
100 ± 10Ω, Diff. Ctrl. Imp.: W Trace = 0.168mm (Edge to Edge spacing = 0.422mm)
100 ± 10Ω, Diff. Ctrl. Imp.: W Trace = 0.081mm

Detail -C- (Internal Layer)
50 ± 10Ω, Ctrl. Imp.: W Trace = 0.168mm
68.5 ± 10Ω, Ctrl. Imp.: W Trace = 0.081mm
100 ± 10Ω, Diff. Ctrl. Imp.: W Trace = 0.152mm (Edge to Edge spacing = 0.122mm)
100 ± 10Ω, Diff. Ctrl. Imp.: W Trace = 0.152mm (Edge to Edge spacing = 0.549mm)

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UNLESS OTHERWISE SPECIFIED
DIMENSIONS AND TOLERANCES
ARE IN MILLIMETERS AND
APPLY TO THE FINISHED PART
TOLERANCE ON:
1 PLACE DEC. ± 0.2 | 2 PLACE DEC. ± 0.08 | ANGLES ± 1/2°

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| | | | |
|---|---|---|---|
| Title | DC-2G | | |
| Project | FBKD1701 | Cust. P/N | 690-487-A |
| Date | 2017.07.06 | Drawn by | AL |
| CAD File | 690-487-A.pcb | Engineer | DL, MAO |
| Layer | BOARD SPECIFICATION (Use suffix or Set_Spec layer in ODB++ if applicable.) | | |

Finished hole size table

| Hole Dia (mm) | Symbol | Quantity | Plated | Range (mm) |
|---|---|---|---|---|
| 0.200 | + | 5856 | Yes | 0.200 - 0.275 See DETAIL -K- |
| 0.250 | × | 6497 | Yes | 0.000 - 0.525 See DETAIL -K- |
| 1.000 | ⊠ | 44 | Yes | 0.925 - 1.075 |
| 1.000 | Y | 2 | No | 0.950 - 1.050 |
| 1.016 | ⊠ | 5 | Yes | 0.950 - 1.108 |
| 1.400 | ⊠ | 5 | Yes | 1.325 - 1.475 |
| 1.651 | ⊡ | 2 | Yes | 1.575 - 1.725 |
| 1.780 | ⊕ | 2 | Yes | 1.780 - 2.858 |
| 3.175 | ⊠ | 8 | No | 3.175 - 3.250 |
| 3.251 | ⊕ | 2 | No | 3.208 - 3.308 |
| 3.780 | ⊠ | 40 | Yes | 3.625 - 3.775 |