CN8100-GBCv2

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REVISION HISTORY

REV	DESCRIPTION	DATE
1.0	initial version	2017-12-12
1.1	1.modfiy ethernet swith to KSZ9897R 2. modify clk distribution to microsemi solution 3. add power supply(1.2V,2.5V) for KSZ9897R	2018-1-18
1.1.1	1. change ddr4 to DDR4 SO-DIMM 2.update reset squence and spi flash,delete boot nand 3.add TPM ,modify SPI connection	2018-3-12 2018-3-13
1.1.2	1. updated the packages of many part 2. add IDT PTP module 3. modify uart,iic etc. 4. add power monitor,temp sensor etc	2018-3-14
1.1.3	1. delete the LT8640 and ORING power switch, page30 2. add power block diagram page5 3.connect tiva_syncconn_gpio1 to U82 4.modify some error of offpage connector name 5.add isolation between SDR and TIVA/SOC 6.add function block diagram page4	2018-3-29
1.1.4	1.update the iic device of tiva in blockdiagram and circult,page3 2.modify PTP connection accord IDT recommendations.page49 3.add OCT power control switch and 2pin header at page30. 4.add two eeprom for TIVA saving ID,inventory. page45 5.update the pcb_footprint of all components 6. remove LT8640 at page30	2018-3-30
1.1.5	1.Modify some part's pin name to generate list rightlly(U9,U86,U22-U25) 2.reannotate the part's reference 3. Don't place R178 4.update uSD connector 5.Add MTGHOLE at page52. 6.modified schemaitc accoard the excel review list v1.6, 7.update table content 8.modify ethsw to KSZ9897S,,add R769page 20,21 add SGMII path from ethsw to octeon.dlm1 ,page20 through out PME signal to TIVA,page20 through out IBA signal to TIVA,page20 9.delete TRXFE power ,page35, As will powering RF through separate cable from power board T 10,change R312 TO 150K 11. modify the errors according the review list ver0.17 12. modifiy KSZ9897S to KSZ9567S,Add syncE option. page20 13. modify errors on ksz9897s base MicroChip's review, page20 14, add syncE option ,page49.	2018-4-11
1.1.6	1.add series resistor,R777~R780, at page40 2.Modifiy some resistor to DNP, at page51 3. modify some component's footprint,and part-number 4.modify JTB1 pin2,pin3 to V12P0, JTB1 pin5,pin4 to GND,page30 5.Modify S1 same as S2, Modify RJ45/J10/JTAG pcb_foorprint. 6.delete the no-used connection to Rsvd-pin on mini-pcie.page28,page29 7.modify BT1 same with BT2	2018-4-20
1.1.7	1.update power block,page4 2. add 12V backup related circult (LTC4419), page30, 3.add super cap for tiva/tpm/ir, page54 4.add IR sensor, 5.delete T2,J27, modify ethsw port1,port2 connect to FX18-40s-0.8sh . 6.add U89, page53, 7. modify OCT strapping resistor, connect PLL configuration to U89,page53 8,connect BOOT method configer to U89 page53	2018-4-23
1.1.8	1.add USB hub 2.add 0ohm resistor(package=25120 for DVT test) 3.modify J13,J15 pcb footprint 4.Delete D13~D15,C485,C486,C488 5.change J2 package 6,add J32,Buzzer circult add led:D34,D35,D36,D39,D40,D41,D42,D43,D44,D45 7,Add MH2,MH3 8.modify default boot method to SPI 9.modify J3M2 PCB Footprint with mount ing hole 10.add c908,c909	2018-4-27
1.1.9	1. add U92 ,U93,U94,C910~C912 2.add JP2,R908 3.bring back U38,U39 related circuit for TRXFE_12V at page35	2018-5-4
1.1.10	1.add R909,R910,R911,R912,R913,R914,R915,R916,R917 2.modify MH16 pcb footprint, 3.modify some error net	2018-5-7
1.1.11	1.Change R796.1 to GND, setting core clock defult 1.5G(Since the CPU max speed is1.5Ghz)	2018-5-9

REV	DESCRIPTION	DATE
1.2	1. Remove V5P0_EN,V3P3_EN from TIVA to U33,U28 respectively, 2.delete R767,R916, Place R339 3.Delete R910 ,Connect R368 to V3P3 4.Delete net: SATA0_LED_N,SATA1_LED_N, 5.add R918,R919 0ohm 6.Connect TIVA PP0,PP1 to J31 as UART IF 7,Connect TIVA_FE_RESET_OUT to TIVA PM2 8.Connect TIVA_USER_LED1/2 to IO expander 9.use TIVA PD0/PD1 as IIC7,connect to LED board, add R920,R921 2.2k 10.Add U96,U97 11. Add U95 related circult for IIC isolation	2018-5-11
1.2.1	1.modify T1 connection order for easily layout 2.modify U59~U62 pin order for easily layout 3.add jtag chain,R925~R937 0ohm for jtag chain 4.add D46,D47 ESD protection diode	2018-5-15
1.2.2	1.Add TRXFE_DET net for BB board present detection 2.add TIVA waken function page42	2018-5-17
1.2.3	1.add EBMP feature at page8, add U100,J33	2018-5-25
2.0	1.change R407 to 10K 2. Modify U28 part Number to MP2951-0067-Z 3.change U97,U97 to DNP 4.Modify msata rx lane polarity	2018-7-14
2.1	1.modify C325,C326 to DNP 2.Modify X2 part number	2018-7-18

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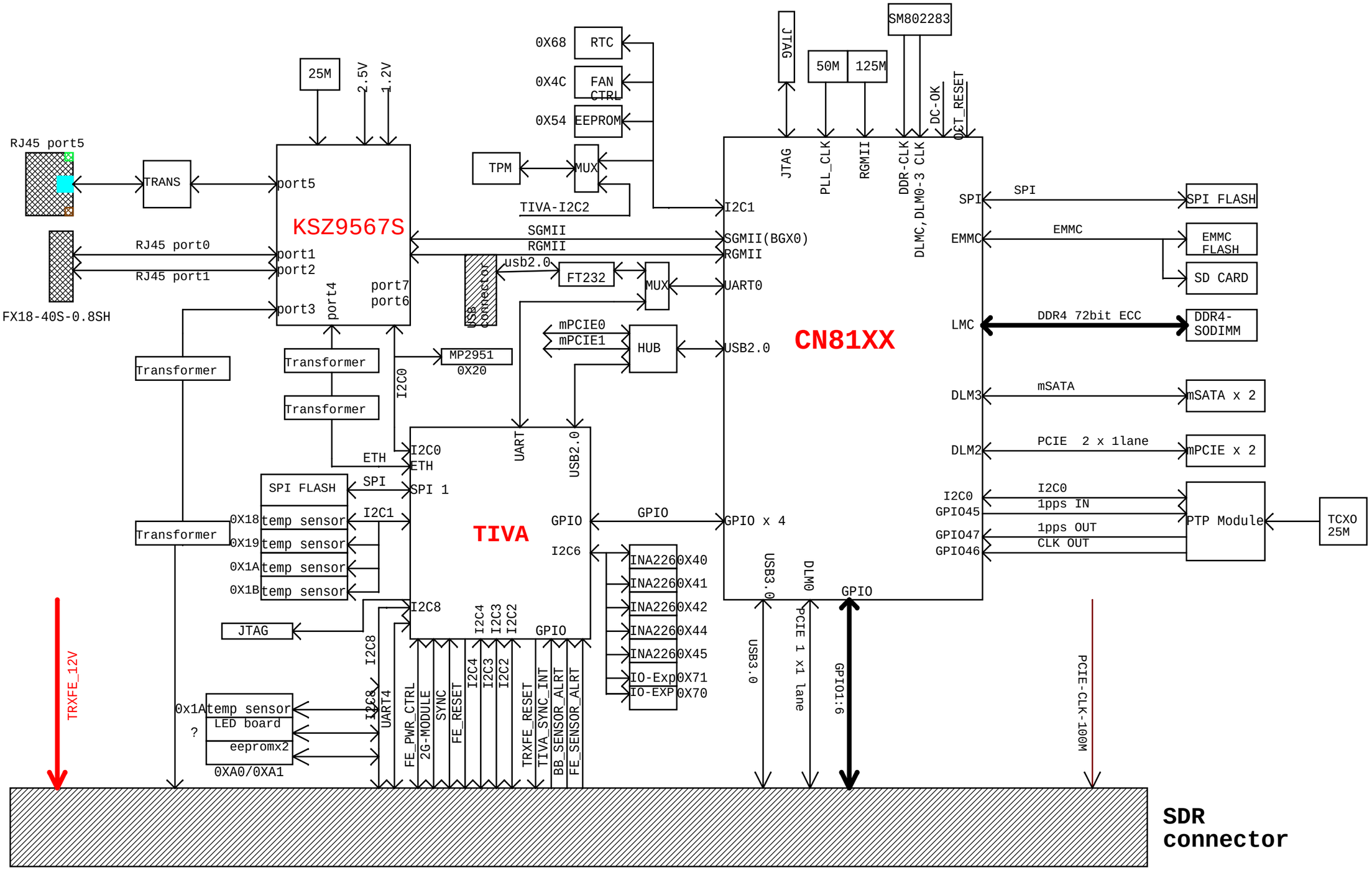

ICD TEST CONNECTOR

Need confirm and discuss

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Title	FUNCTIONAL BLOCK DIAGRAM	
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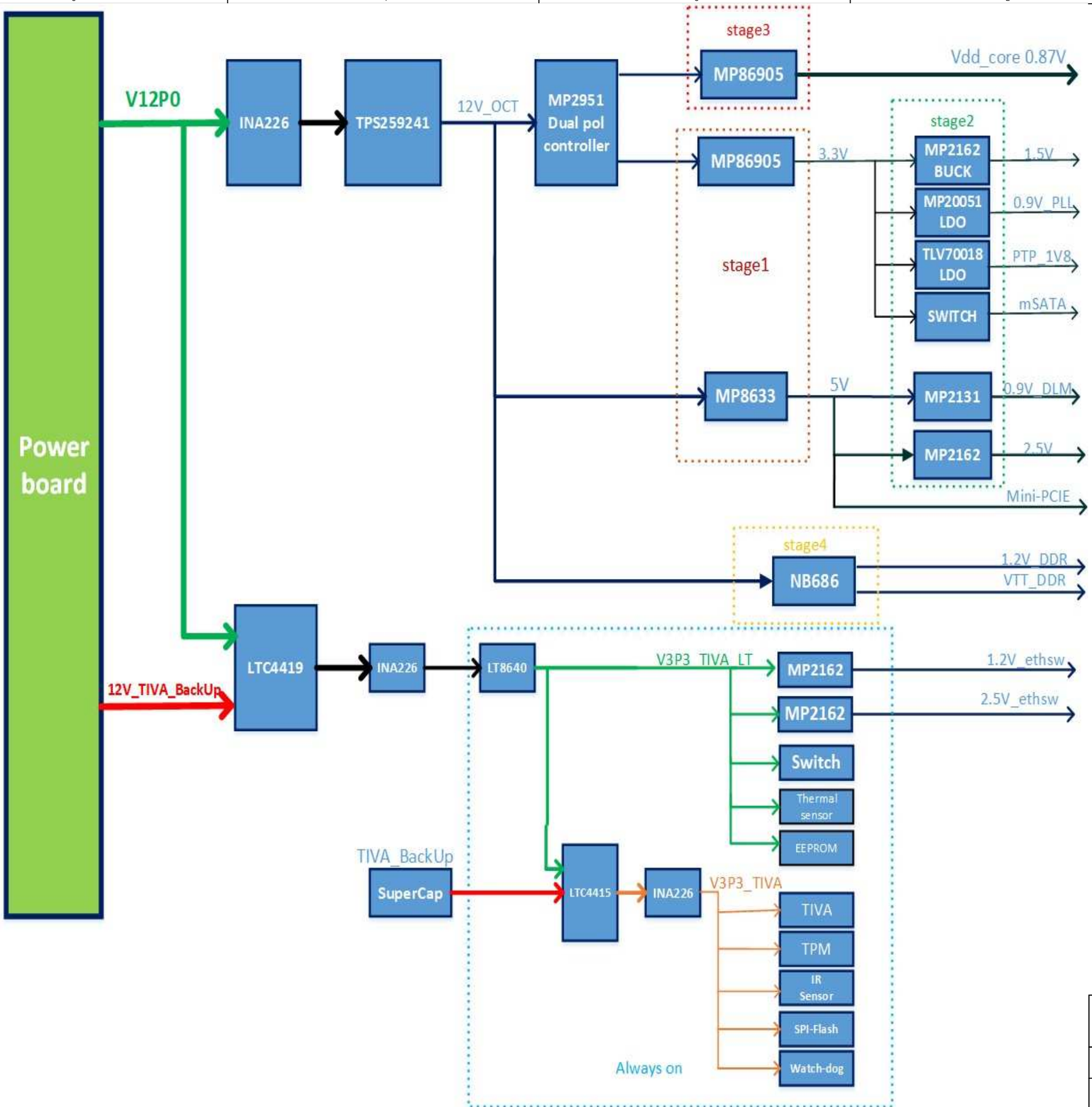

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Title	POWER DIAGRAMS	
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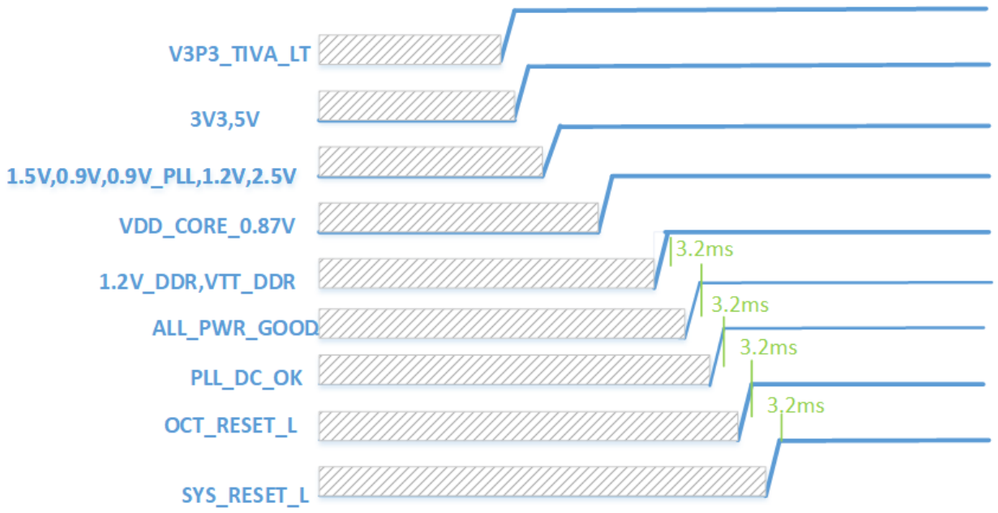

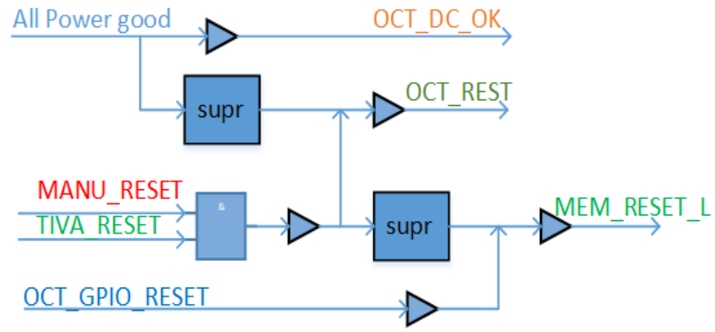

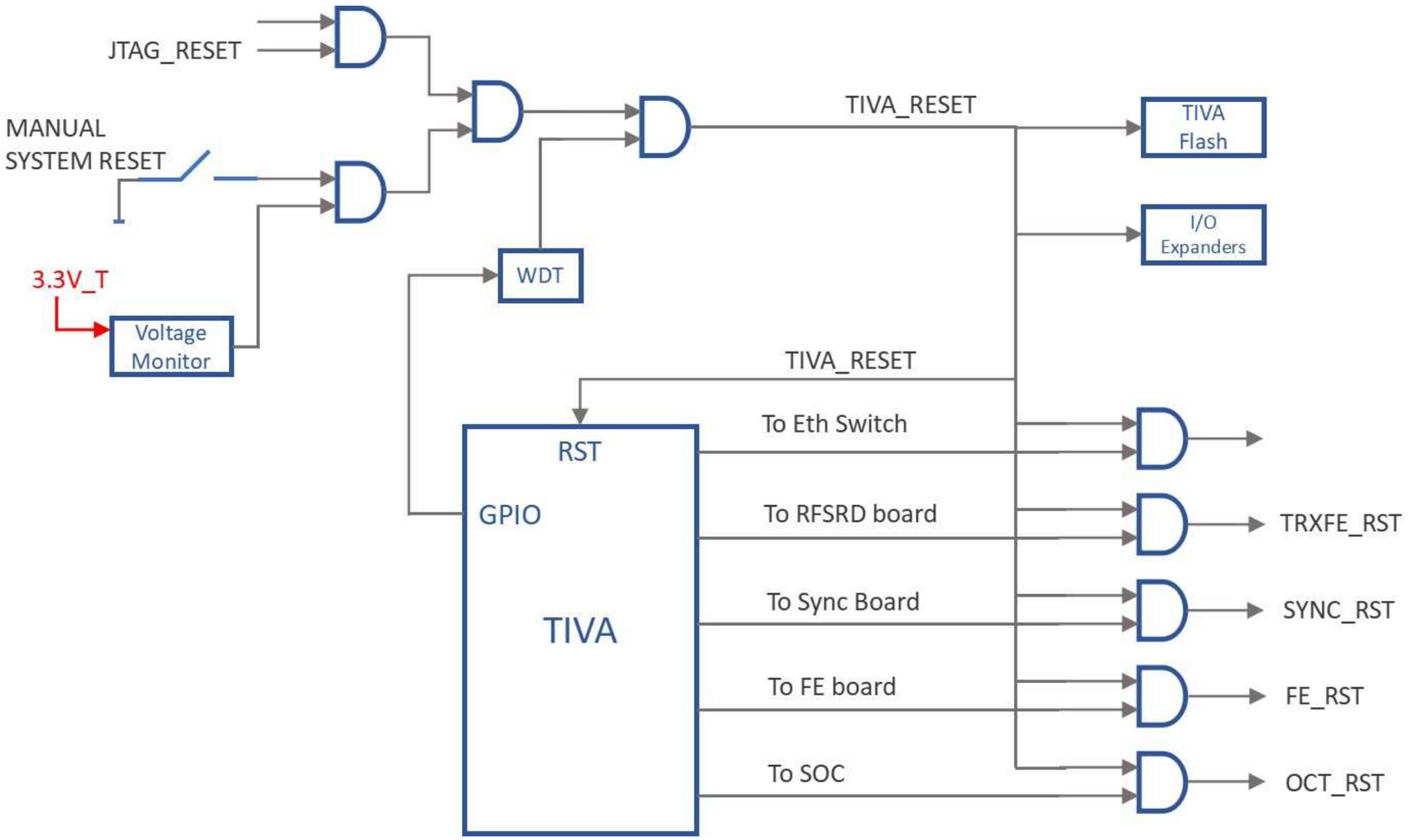

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Title	POWER UP SEQUENCE BLOCK	
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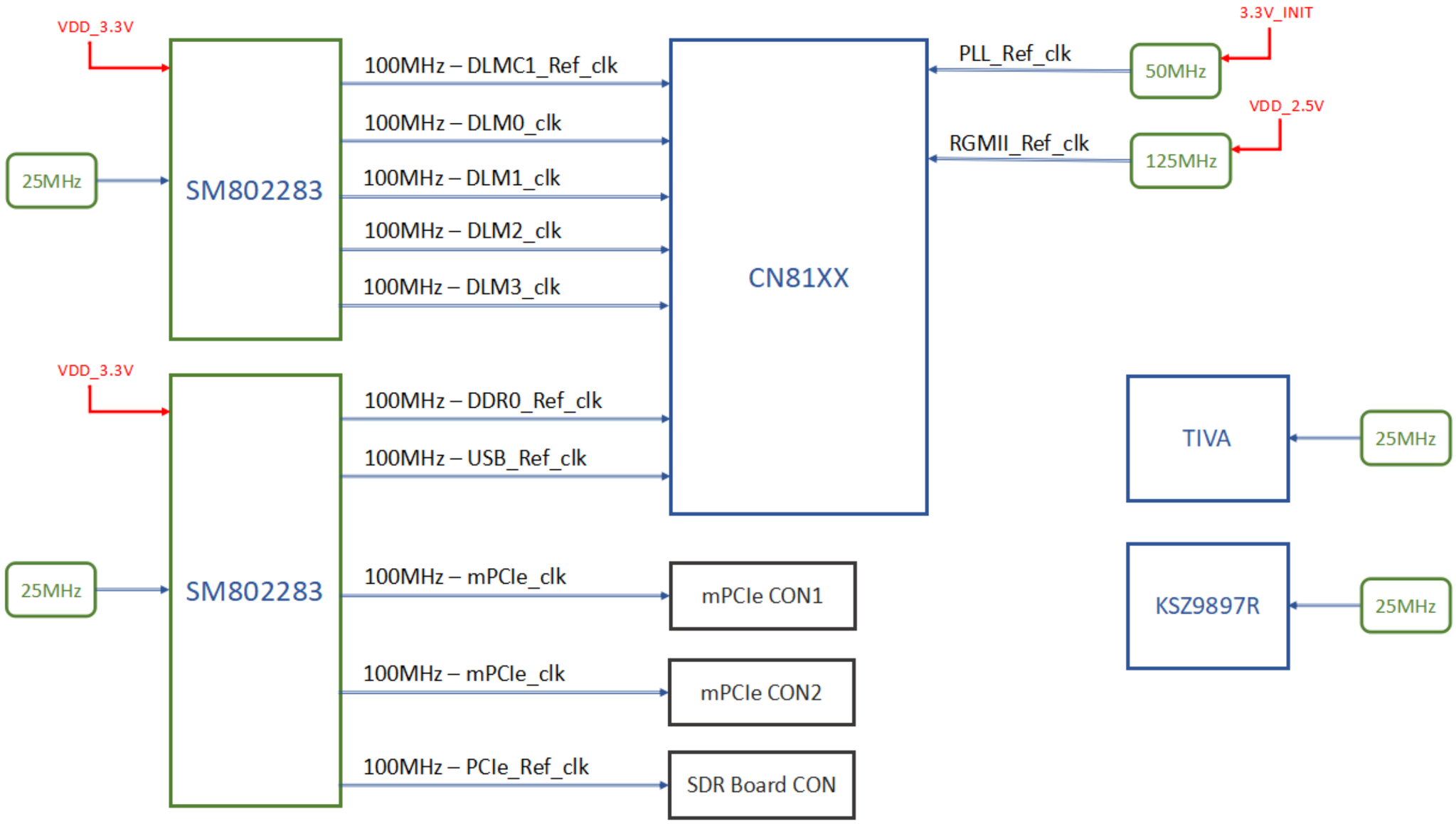

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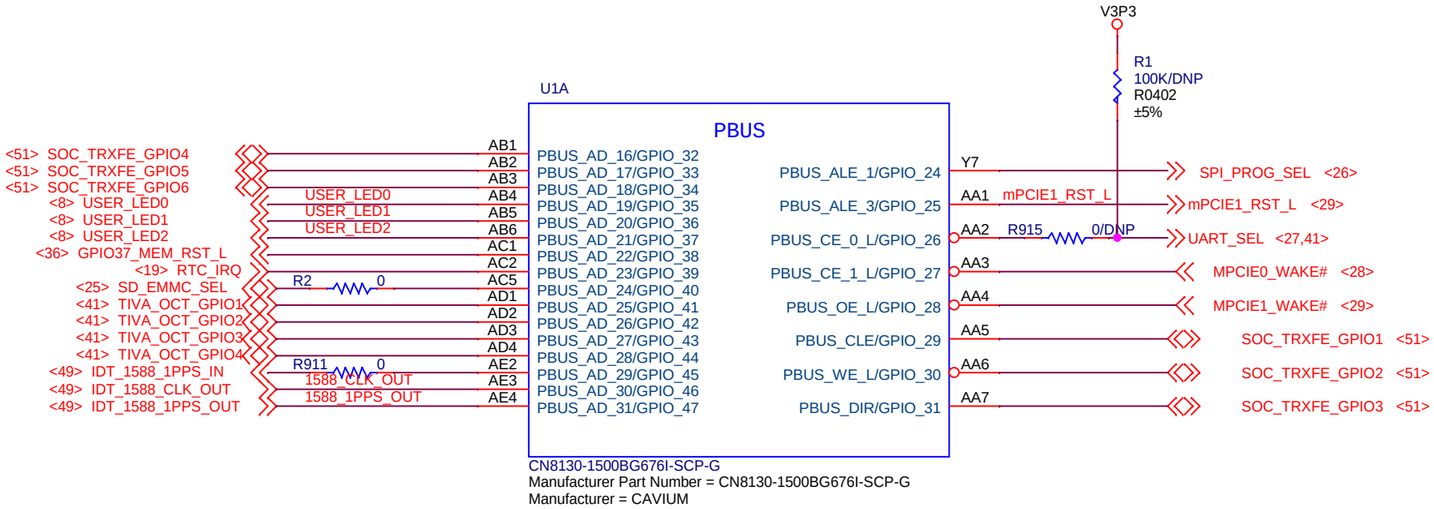

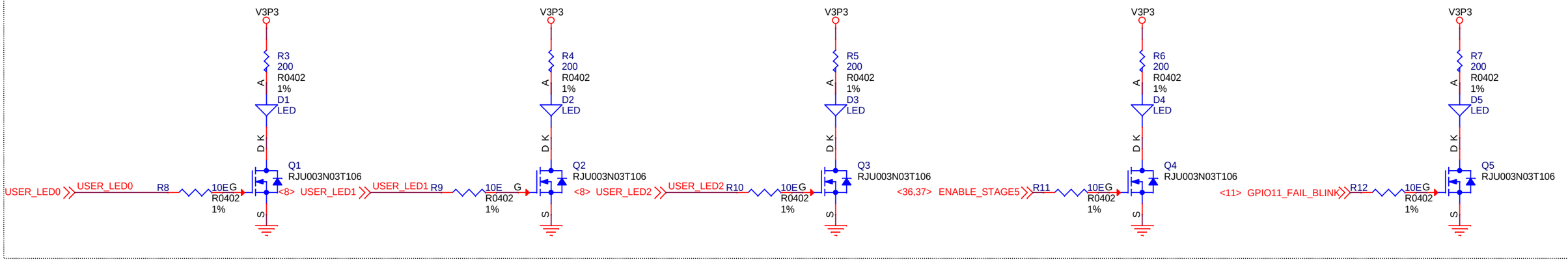

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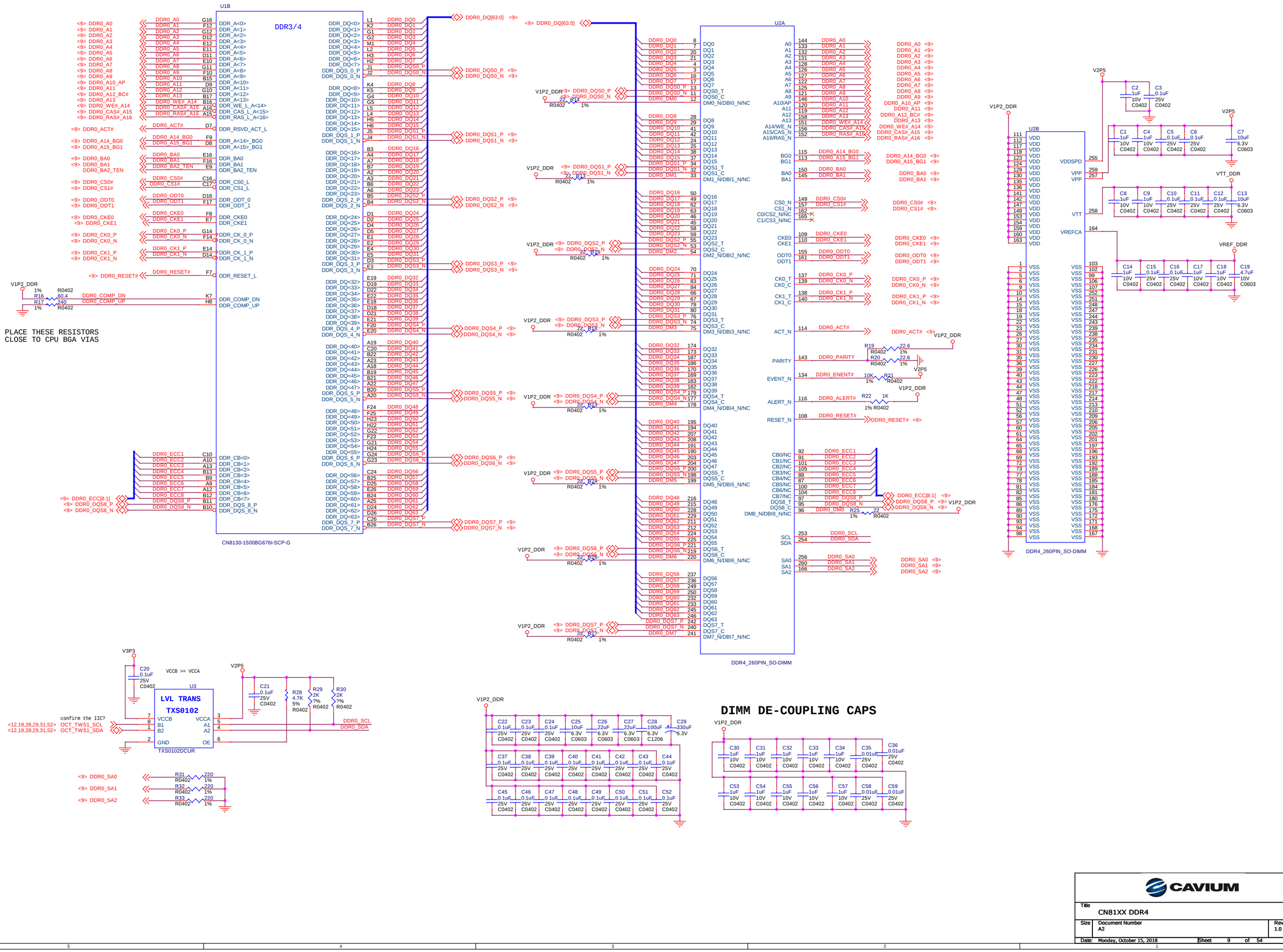

Title	CN81XX DDR4
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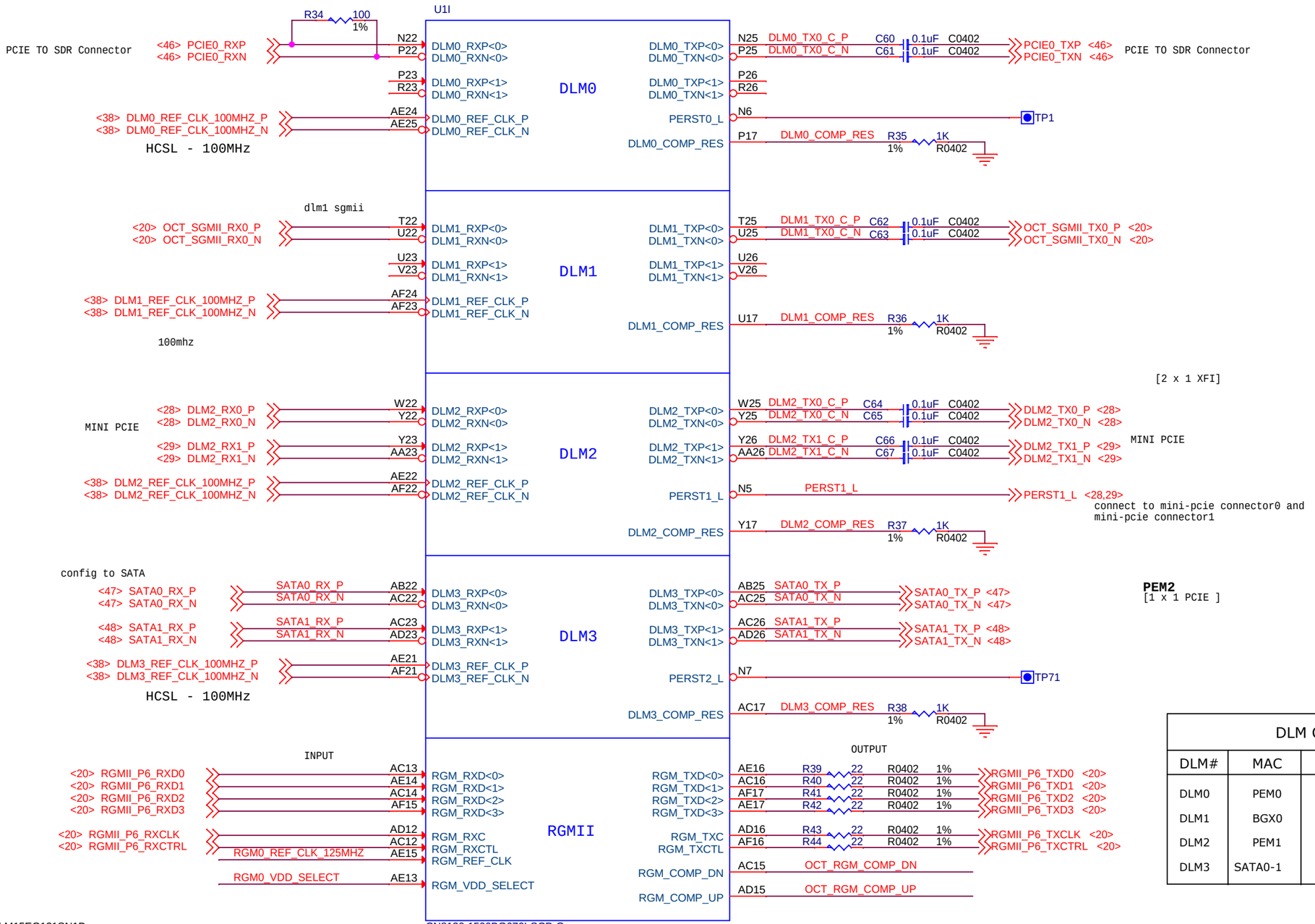

DLM Configuration		
DLM#	MAC	OCT IOT/ROUTER Gateway
DLM0	PEM0	1x1 PCIe
DLM1	BGX0	1x1 SGMII
DLM2	PEM1	2x1 PCIE
DLM3	SATA0-1	2X1 SATA

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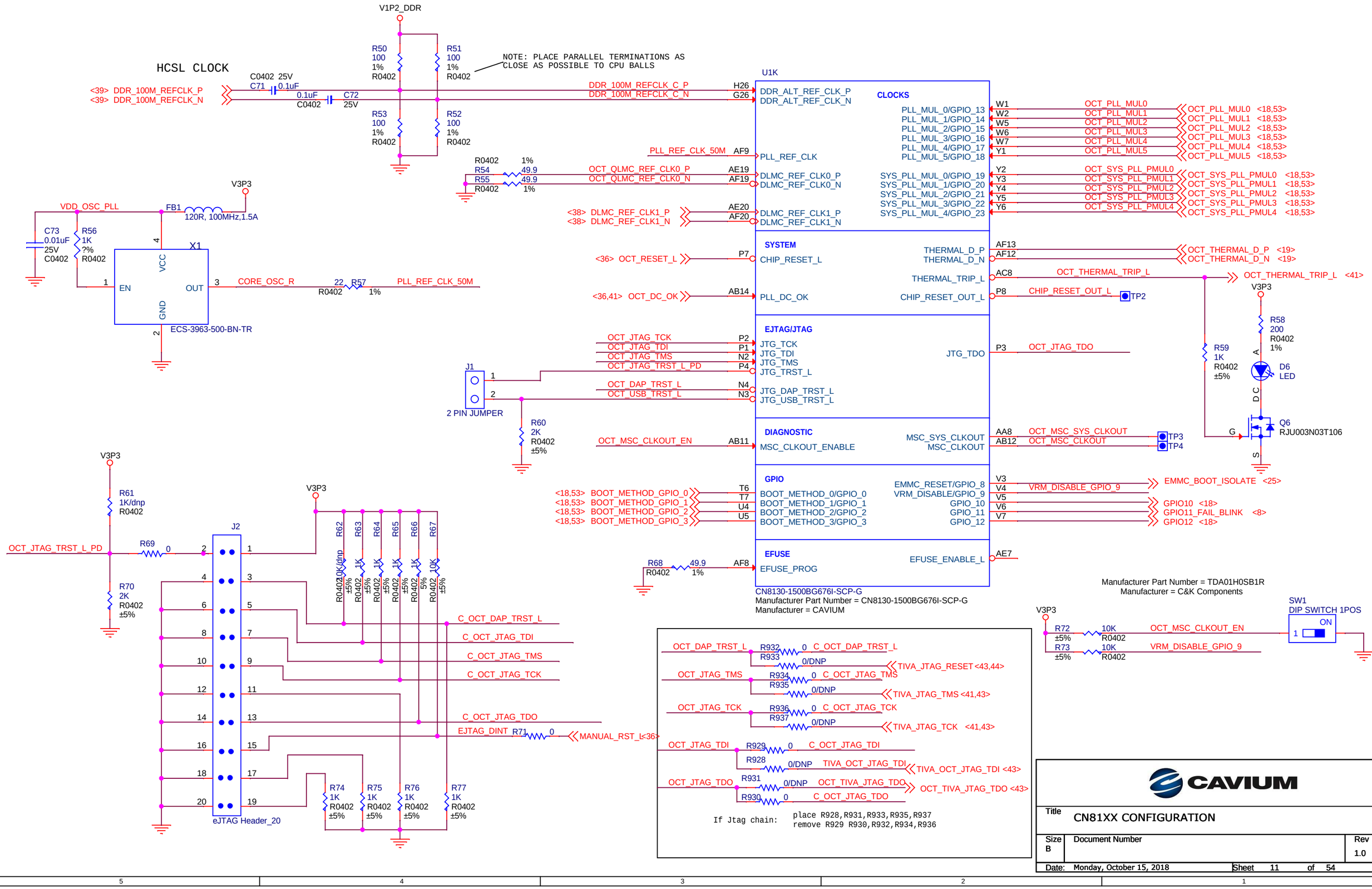
HCSL CLOCK
V1P2_DDR
R50 100 1% R0402
R51 100 1% R0402
R53 100 1% R0402
R52 100 1% R0402
NOTE: PLACE PARALLEL TERMINATIONS AS CLOSE AS POSSIBLE TO CPU BALLS
C0402 25V
C71 0.1uF
0.1uF C0402
C72 25V
<39> DDR_100M_REFCLK_P
<39> DDR_100M_REFCLK_N
DDR_100M_REFCLK_C_P
DDR_100M_REFCLK_C_N
H26
G26
U1K
DDR_ALT_REF_CLK_P
DDR_ALT_REF_CLK_N
CLOCKS
PLL_MUL_0/GPIO_13
PLL_MUL_1/GPIO_14
PLL_MUL_2/GPIO_15
PLL_MUL_3/GPIO_16
PLL_MUL_4/GPIO_17
PLL_MUL_5/GPIO_18
W1 OCT_PLL_MUL0
W2 OCT_PLL_MUL1
W5 OCT_PLL_MUL2
W6 OCT_PLL_MUL3
W7 OCT_PLL_MUL4
Y1 OCT_PLL_MUL5
OCT_PLL_MUL0 <18,53>
OCT_PLL_MUL1 <18,53>
OCT_PLL_MUL2 <18,53>
OCT_PLL_MUL3 <18,53>
OCT_PLL_MUL4 <18,53>
OCT_PLL_MUL5 <18,53>
PLL_REF_CLK_50M
AF9
PLL_REF_CLK
R0402 1%
R54 49.9
R55 49.9
R0402 1%
OCT_QLMC_REF_CLK0_P
OCT_QLMC_REF_CLK0_N
AE19
AF19
DLMC_REF_CLK0_P
DLMC_REF_CLK0_N
SYS_PLL_MUL_0/GPIO_19
SYS_PLL_MUL_1/GPIO_20
SYS_PLL_MUL_2/GPIO_21
SYS_PLL_MUL_3/GPIO_22
SYS_PLL_MUL_4/GPIO_23
Y2 OCT_SYS_PLL_PMUL0
Y3 OCT_SYS_PLL_PMUL1
Y4 OCT_SYS_PLL_PMUL2
Y5 OCT_SYS_PLL_PMUL3
Y6 OCT_SYS_PLL_PMUL4
OCT_SYS_PLL_PMUL0 <18,53>
OCT_SYS_PLL_PMUL1 <18,53>
OCT_SYS_PLL_PMUL2 <18,53>
OCT_SYS_PLL_PMUL3 <18,53>
OCT_SYS_PLL_PMUL4 <18,53>
<38> DLMC_REF_CLK1_P
<38> DLMC_REF_CLK1_N
AE20
AF20
DLMC_REF_CLK1_P
DLMC_REF_CLK1_N
V3P3
VDD_OSC_PLL
FB1
120R, 100MHz,1.5A
C73 0.01uF 25V C0402
R56 1K ?% R0402
X1
VCC
EN
OUT
GND
CORE_OSC_R
22 R57 R0402 1%
PLL_REF_CLK_50M
ECS-3963-500-BN-TR
SYSTEM
<36> OCT_RESET_L
P7
CHIP_RESET_L
THERMAL_D_P
THERMAL_D_N
AF13
AF12
OCT_THERMAL_D_P <19>
OCT_THERMAL_D_N <19>
THERMAL_TRIP_L
AC8
OCT_THERMAL_TRIP_L
OCT_THERMAL_TRIP_L <41>
<36,41> OCT_DC_OK
AB14
PLL_DC_OK
CHIP_RESET_OUT_L
P8
CHIP_RESET_OUT_L
TP2
EJTAG/JTAG
OCT_JTAG_TCK
OCT_JTAG_TDI
OCT_JTAG_TMS
OCT_JTAG_TRST_L_PD
P2
P1
N2
P4
JTG_TCK
JTG_TDI
JTG_TMS
JTG_TRST_L
JTG_TDO
P3
OCT_JTAG_TDO
J1
2 PIN JUMPER
OCT_DAP_TRST_L
OCT_USB_TRST_L
N4
N3
JTG_DAP_TRST_L
JTG_USB_TRST_L
R60 2K R0402 ±5%
DIAGNOSTIC
OCT_MSC_CLKOUT_EN
AB11
MSC_CLKOUT_ENABLE
MSC_SYS_CLKOUT
MSC_CLKOUT
AA8 OCT_MSC_SYS_CLKOUT
AB12 OCT_MSC_CLKOUT
TP3
TP4
GPIO
<18,53> BOOT_METHOD_GPIO_0
<18,53> BOOT_METHOD_GPIO_1
<18,53> BOOT_METHOD_GPIO_2
<18,53> BOOT_METHOD_GPIO_3
T6
T7
U4
U5
BOOT_METHOD_0/GPIO_0
BOOT_METHOD_1/GPIO_1
BOOT_METHOD_2/GPIO_2
BOOT_METHOD_3/GPIO_3
EMMC_RESET/GPIO_8
VRM_DISABLE/GPIO_9
GPIO_10
GPIO_11
GPIO_12
V3 EMMC_BOOT_ISOLATE <25>
V4 VRM_DISABLE_GPIO_9
V5 GPIO10 <18>
V6 GPIO11_FAIL_BLINK <8>
V7 GPIO12 <18>
EFUSE
R68 49.9 R0402 1%
AF8
EFUSE_PROG
EFUSE_ENABLE_L
AE7
CN8130-1500BG676I-SCP-G
Manufacturer Part Number = CN8130-1500BG676I-SCP-G
Manufacturer = CAVIUM
R58 200 R0402 1%
R59 1K R0402 ±5%
D6 LED
Q6 RJU003N03T106
G
D
S
A
C
Manufacturer Part Number = TDA01H0SB1R
Manufacturer = C&K Components
SW1
DIP SWITCH 1POS
ON
R72 10K ±5% R0402
R73 10K ±5% R0402
OCT_MSC_CLKOUT_EN
VRM_DISABLE_GPIO_9
R61 1K/dnp R0402
R69 0
R70 2K R0402 ±5%
OCT_JTAG_TRST_L_PD
J2
eJTAG Header_20
R62 10K/dnp R0402 ±5%
R63 1K R0402 ±5%
R64 1K R0402 ±5%
R65 1K R0402 ±5%
R66 1K R0402 5%
R67 10K R0402 ±5%
C_OCT_DAP_TRST_L
C_OCT_JTAG_TDI
C_OCT_JTAG_TMS
C_OCT_JTAG_TCK
C_OCT_JTAG_TDO
EJTAG_DINT
R71 0
MANUAL_RST_L<36>
R74 1K R0402 ±5%
R75 1K R0402 ±5%
R76 1K R0402 ±5%
R77 1K R0402 ±5%
OCT_DAP_TRST_L
R932 0 C_OCT_DAP_TRST_L
R933 0/DNP
TIVA_JTAG_RESET <43,44>
OCT_JTAG_TMS
R934 0 C_OCT_JTAG_TMS
R935 0/DNP
TIVA_JTAG_TMS <41,43>
OCT_JTAG_TCK
R936 0 C_OCT_JTAG_TCK
R937 0/DNP
TIVA_JTAG_TCK <41,43>
OCT_JTAG_TDI
R929 0 C_OCT_JTAG_TDI
R928 0/DNP
TIVA_OCT_JTAG_TDI
TIVA_OCT_JTAG_TDI <43>
OCT_JTAG_TDO
R931 0/DNP
OCT_TIVA_JTAG_TDO
OCT_TIVA_JTAG_TDO <43>
R930 0 C_OCT_JTAG_TDO
If Jtag chain:
place R928,R931,R933,R935,R937
remove R929 R930,R932,R934,R936
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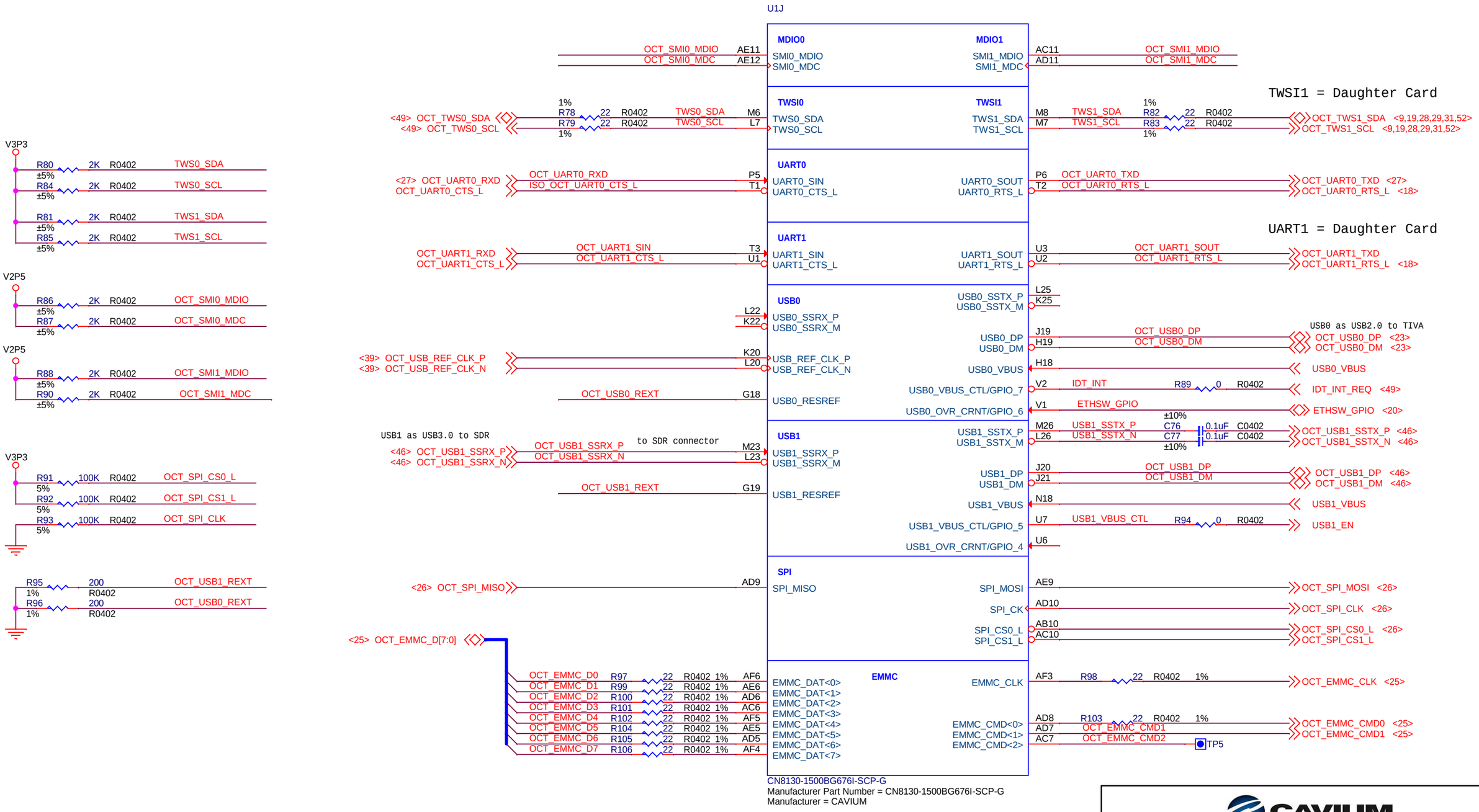
U1J
MDIO0
SMI0_MDIO
SMI0_MDC
OCT_SMI0_MDIO AE11
OCT_SMI0_MDC AE12
MDIO1
SMI1_MDIO
SMI1_MDC
AC11 OCT_SMI1_MDIO
AD11 OCT_SMI1_MDC
TWSI1 = Daughter Card
TWSI0
TWS0_SDA
TWS0_SCL
<49> OCT_TWS0_SDA
<49> OCT_TWS0_SCL
R78 22 R0402 TWS0_SDA M6
R79 22 R0402 TWS0_SCL L7
1%
TWSI1
TWS1_SDA
TWS1_SCL
M8 TWS1_SDA R82 22 R0402
M7 TWS1_SCL R83 22 R0402
OCT_TWS1_SDA <9,19,28,29,31,52>
OCT_TWS1_SCL <9,19,28,29,31,52>
UART0
UART0_SIN
UART0_CTS_L
UART0_SOUT
UART0_RTS_L
<27> OCT_UART0_RXD
OCT_UART0_CTS_L
OCT_UART0_RXD
ISO_OCT_UART0_CTS_L
P5
T1
P6 OCT_UART0_TXD
T2 OCT_UART0_RTS_L
OCT_UART0_TXD <27>
OCT_UART0_RTS_L <18>
UART1 = Daughter Card
UART1
UART1_SIN
UART1_CTS_L
UART1_SOUT
UART1_RTS_L
OCT_UART1_RXD
OCT_UART1_CTS_L
OCT_UART1_SIN
OCT_UART1_CTS_L
T3
U1
U3 OCT_UART1_SOUT
U2 OCT_UART1_RTS_L
OCT_UART1_TXD
OCT_UART1_RTS_L <18>
USB0
USB0_SSRX_P
USB0_SSRX_M
USB0_SSTX_P
USB0_SSTX_M
L22
K22
L25
K25
USB0 as USB2.0 to TIVA
USB0_DP
USB0_DM
J19 OCT_USB0_DP
H19 OCT_USB0_DM
OCT_USB0_DP <23>
OCT_USB0_DM <23>
<39> OCT_USB_REF_CLK_P
<39> OCT_USB_REF_CLK_N
K20
L20
USB_REF_CLK_P
USB_REF_CLK_N
USB0_VBUS
H18
USB0_VBUS
OCT_USB0_REXT
G18
USB0_RESREF
USB0_VBUS_CTL/GPIO_7
V2 IDT_INT R89 0 R0402
IDT_INT_REQ <49>
USB0_OVR_CRNT/GPIO_6
V1 ETHSW_GPIO
ETHSW_GPIO <20>
USB1 as USB3.0 to SDR
USB1
USB1_SSRX_P
USB1_SSRX_M
USB1_SSTX_P
USB1_SSTX_M
<46> OCT_USB1_SSRX_P
<46> OCT_USB1_SSRX_N
OCT_USB1_SSRX_P
OCT_USB1_SSRX_N
to SDR connector
M23
L23
M26 USB1_SSTX_P C76 0.1uF C0402
L26 USB1_SSTX_N C77 0.1uF C0402
±10%
OCT_USB1_SSTX_P <46>
OCT_USB1_SSTX_N <46>
OCT_USB1_REXT
G19
USB1_RESREF
USB1_DP
USB1_DM
J20 OCT_USB1_DP
J21 OCT_USB1_DM
OCT_USB1_DP <46>
OCT_USB1_DM <46>
USB1_VBUS
N18
USB1_VBUS
USB1_VBUS_CTL/GPIO_5
U7 USB1_VBUS_CTL R94 0 R0402
USB1_EN
USB1_OVR_CRNT/GPIO_4
U6
SPI
SPI_MISO
SPI_MOSI
SPI_CK
SPI_CS0_L
SPI_CS1_L
<26> OCT_SPI_MISO
AD9
AE9 OCT_SPI_MOSI <26>
AD10 OCT_SPI_CLK <26>
AB10 OCT_SPI_CS0_L <26>
AC10 OCT_SPI_CS1_L
<25> OCT_EMMC_D[7:0]
EMMC
EMMC_DAT<0>
EMMC_DAT<1>
EMMC_DAT<2>
EMMC_DAT<3>
EMMC_DAT<4>
EMMC_DAT<5>
EMMC_DAT<6>
EMMC_DAT<7>
EMMC_CLK
EMMC_CMD<0>
EMMC_CMD<1>
EMMC_CMD<2>
OCT_EMMC_D0 R97 22 R0402 1% AF6
OCT_EMMC_D1 R99 22 R0402 1% AE6
OCT_EMMC_D2 R100 22 R0402 1% AD6
OCT_EMMC_D3 R101 22 R0402 1% AC6
OCT_EMMC_D4 R102 22 R0402 1% AF5
OCT_EMMC_D5 R104 22 R0402 1% AE5
OCT_EMMC_D6 R105 22 R0402 1% AD5
OCT_EMMC_D7 R106 22 R0402 1% AF4
AF3 R98 22 R0402 1%
OCT_EMMC_CLK <25>
AD8 R103 22 R0402 1%
AD7 OCT_EMMC_CMD1
AC7 OCT_EMMC_CMD2
TP5
OCT_EMMC_CMD0 <25>
OCT_EMMC_CMD1 <25>
V3P3
R80 2K R0402 ±5% TWS0_SDA
R84 2K R0402 ±5% TWS0_SCL
R81 2K R0402 ±5% TWS1_SDA
R85 2K R0402 ±5% TWS1_SCL
V2P5
R86 2K R0402 ±5% OCT_SMI0_MDIO
R87 2K R0402 ±5% OCT_SMI0_MDC
V2P5
R88 2K R0402 ±5% OCT_SMI1_MDIO
R90 2K R0402 ±5% OCT_SMI1_MDC
V3P3
R91 100K R0402 5% OCT_SPI_CS0_L
R92 100K R0402 5% OCT_SPI_CS1_L
R93 100K R0402 5% OCT_SPI_CLK
R95 200 R0402 1% OCT_USB1_REXT
R96 200 R0402 1% OCT_USB0_REXT
CN8130-1500BG676I-SCP-G
Manufacturer Part Number = CN8130-1500BG676I-SCP-G
Manufacturer = CAVIUM
CAVIUM
Title
CN81XX MISCELLANEOUS I/O
Size B
Document Number <Doc>
Rev 1.0
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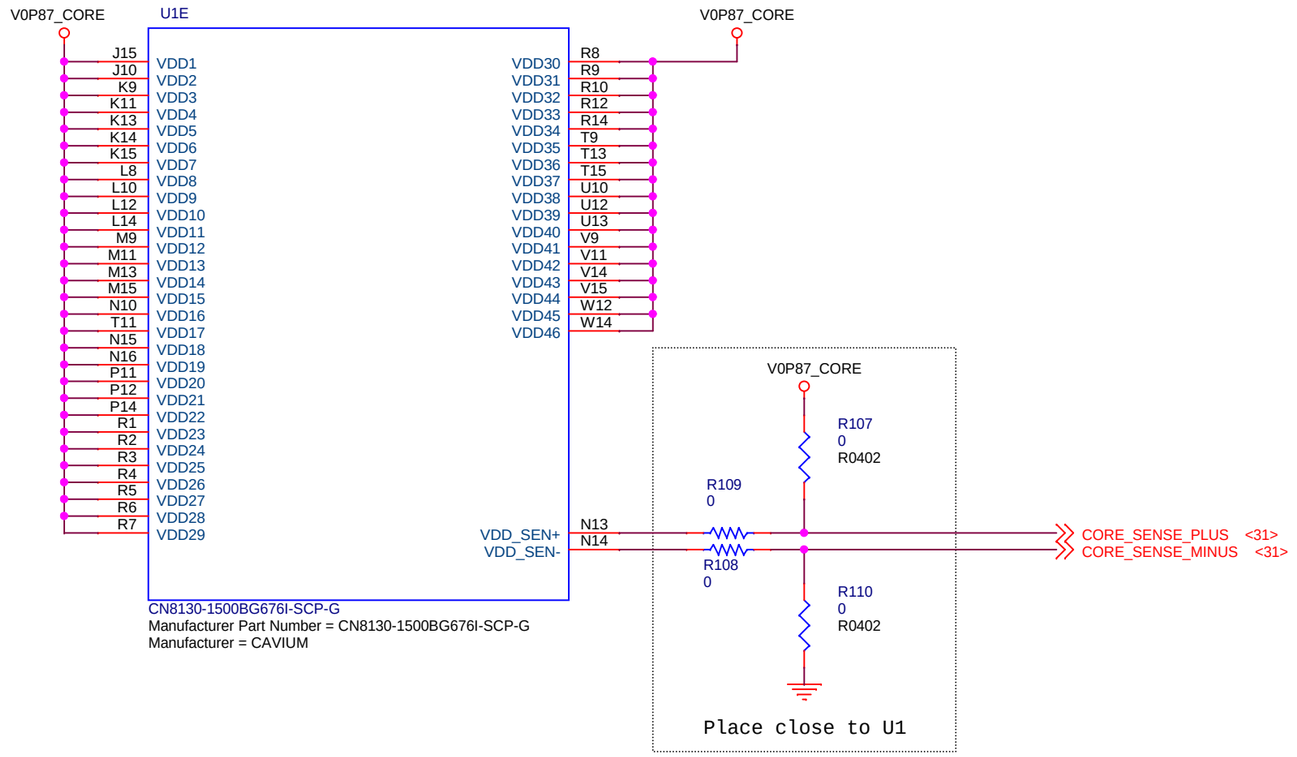

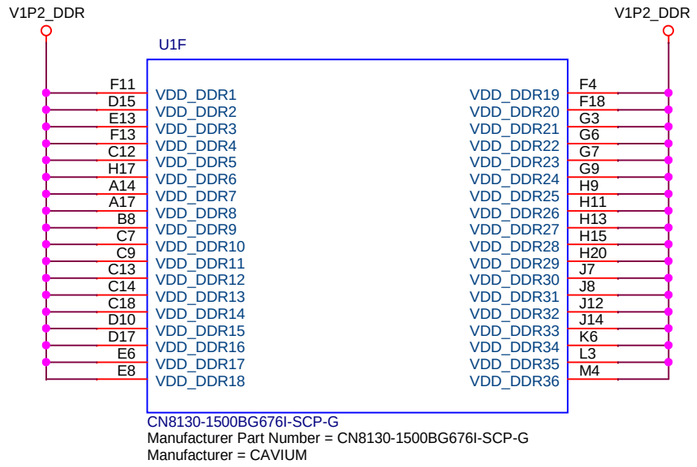

CAVIUM

Title
CN81XX CORE VDD

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Supply Voltage for the On-Chip PLLs

SMI_VDD_SELECT & IO_VDD_SELECT

Selects VDD level for SMI/MDIO:
3.3V = NC
2.5V = 1K pull-up to VDD

U1G

V0P87_CORE — R111 1K ?% R0402 — AB13 SMI_VDD_SELECT
V0P87_CORE — R112 1K R0402 — AE8 IO_VDD_SELECT
AF1 NC

F15 RSVD1
G15 RSVD2
B1 RSVD3
J18 RSVD4
N17 RSVD5
P18 RSVD6
R17 RSVD7
R18 RSVD8
U18 RSVD9
V17 RSVD10
V18 RSVD11
W16 RSVD12
Y18 RSVD13
AA9 RSVD14
AA10 RSVD15
AA12 RSVD16
AA13 RSVD17
AA17 RSVD18
AA18 RSVD19
AB7 RSVD20
AB8 RSVD21

CN8130-1500BG676I-SCP-G
Manufacturer Part Number = CN8130-1500BG676I-SCP-G
Manufacturer = CAVIUM

VDD_SMI AA11 — FLTR_OCT_SMI_VDD2P5V — C78 0.1uF 25V (Place close to the device) — Place close to the filter: C79 0.1uF 25V, C80 1uF 4V, C81 10uF 6.3V, L2 120R,100MHz,2A L0402, C82 0.1uF 25V — V2P5
Manufacturer Part Number = BLM15PX121SN1D
Manufacturer = MURATA

VDD_IO1 N8
VDD_IO2 T5
VDD_IO3 U8
VDD_IO4 W4
VDD_IO5 Y11
VDD_IO6 Y13
VDD_IO7 AB9
VDD_IO8 AC4
R113 0 R0402 jmpr — 3V3_SENSE_P <31>
FLTR_OCT_VDD_IO — C83 0.1uF 25V, C84 0.1uF 25V, C85 0.1uF 25V, C86 0.1uF 25V, C87 1uF 4V, C88 1uF 4V, C89 1uF 4V, C90 1uF 4V (Place close to the device)
L3 120R,100MHz,2A — V3P3
Manufacturer Part Number = BLM15PX121SN1D
Manufacturer = MURATA

DDR_PLL_VDD H16 — FLTR_OCT_DDR0_PLL_VDD_0P9V — C91 0.1uF C0402 25V (Place close to the device) — Place close to the filter: C92 0.1uF 25V, C93 1uF 4V, C94 10uF C0603 6.3V, L4 120R,100MHz,2A L0402, C95 0.1uF 25V — V0P9_PLL
Manufacturer Part Number = BLM15PX121SN1D
Manufacturer = MURATA

PLL_VDD AF10 — FLTR_OCT_PLL_VDD_0P9V — C96 0.1uF 25V (Place close to the device) — Place close to the filter: C97 0.1uF 25V, C98 1uF 4V, C99 10uF C0603 6.3V, L5 120R,100MHz,2A L0402, C100 0.1uF 25V — V0P9_PLL
Manufacturer Part Number = BLM15PX121SN1D
Manufacturer = MURATA

SYS_PLL_VDD AF11 — FLTR_OCT_SYS_PLL_VDD_0P9V — C101 0.1uF 25V (Place close to the device) — Place close to the filter: C102 0.1uF 25V, C103 1uF 4V, C104 10uF C0603 6.3V, L6 120R,100MHz,2A L0402, C105 0.1uF 25V — V0P9_PLL
Manufacturer Part Number = BLM15PX121SN1D
Manufacturer = MURATA

VDD_15_1 W10
VDD_15_2 AA14

VDD_EMMC1 W8
VDD_EMMC2 Y9
FLTR_OCT_VDD_1P5V — C106 0.1uF 25V, C107 1uF 4V (Place close to the device) — Place close to the filter: C108 0.1uF 25V, C109 1uF 4V, C110 10uF C0603 6.3V, L7 120R,100MHz,2A L0402, C111 0.1uF 25V — V1P5
Manufacturer Part Number = BLM15PX121SN1D
Manufacturer = MURATA

VDD_RGM1 AD17
VDD_RGM2 AB15
VDD_RGM3 AD13
FLTR_VDD_OCT_EMMC_3P3V — C112 0.1uF 25V, C113 1uF 4V (Place close to the device) — Place close to the filter: C114 0.1uF 25V, C115 1uF 4V, C116 10uF C0603 6.3V, L8 120R,100MHz,2A L0402, C117 0.1uF 25V — V3P3
Manufacturer Part Number = BLM15PX121SN1D
Manufacturer = MURATA

FLTR_VDD_OCT_RGM_2P5V — C118 0.1uF 25V, C119 0.1uF 25V, C120 1uF 4V (Place close to the device) — Place close to the filter: C121 0.1uF 25V, C122 1uF 4V, C123 10uF C0603 6.3V, L9 120R,100MHz,2A, C124 0.1uF 25V — V2P5
Manufacturer Part Number = BLM15PX121SN1D
Manufacturer = MURATA

CAVIUM

Title: CN81XX I/O & MISC VDD

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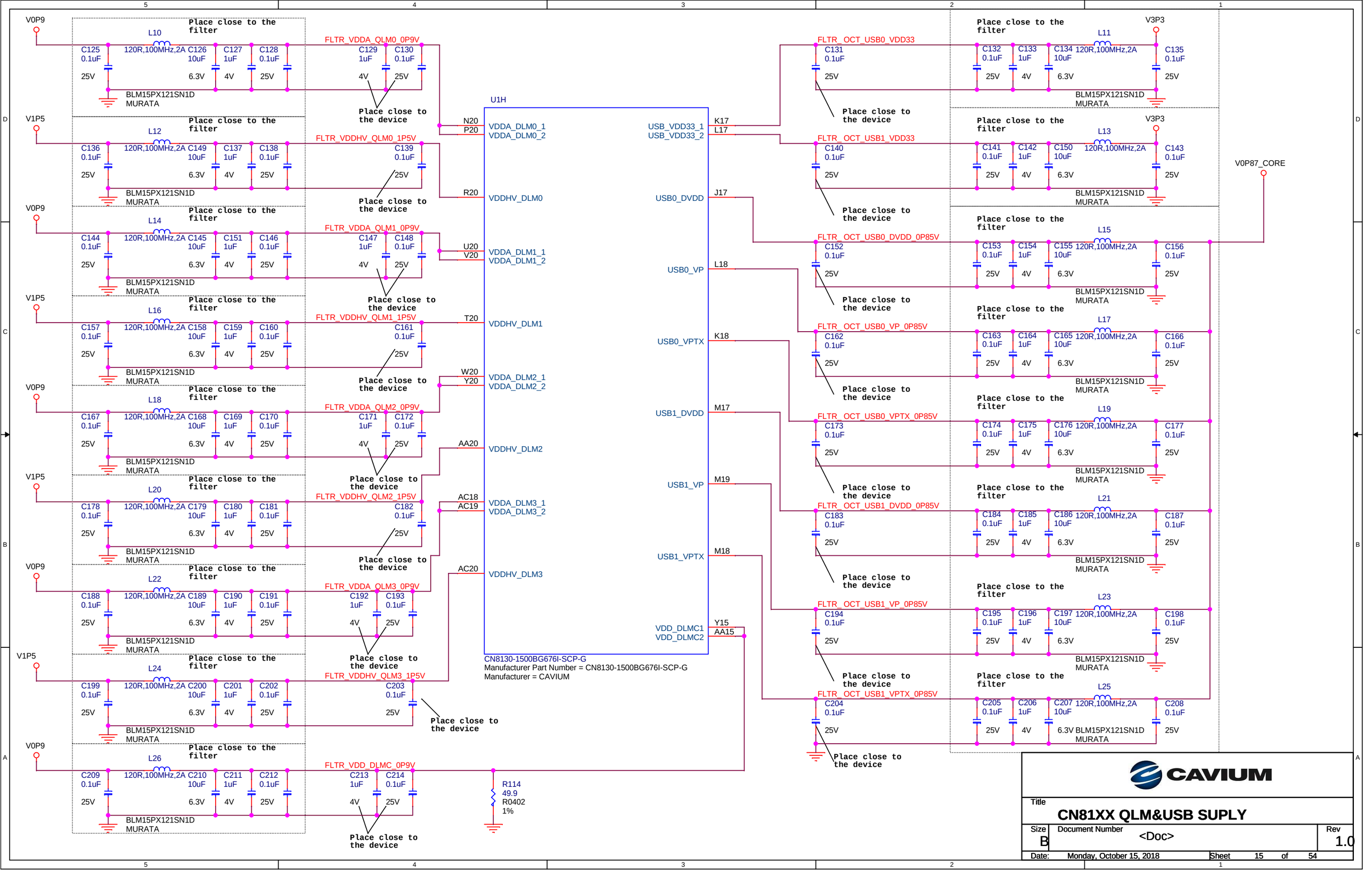
U1H
VDDA_DLM0_1
VDDA_DLM0_2
VDDHV_DLM0
VDDA_DLM1_1
VDDA_DLM1_2
VDDHV_DLM1
VDDA_DLM2_1
VDDA_DLM2_2
VDDHV_DLM2
VDDA_DLM3_1
VDDA_DLM3_2
VDDHV_DLM3
USB_VDD33_1
USB_VDD33_2
USB0_DVDD
USB0_VP
USB0_VPTX
USB1_DVDD
USB1_VP
USB1_VPTX
VDD_DLMC1
VDD_DLMC2
CN8130-1500BG676I-SCP-G
Manufacturer Part Number = CN8130-1500BG676I-SCP-G
Manufacturer = CAVIUM
V0P9
V1P5
V3P3
V0P87_CORE
BLM15PX121SN1D
MURATA
Place close to the filter
Place close to the device
R114
49.9
R0402
1%
CAVIUM
Title
CN81XX QLM&USB SUPLY
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1.0
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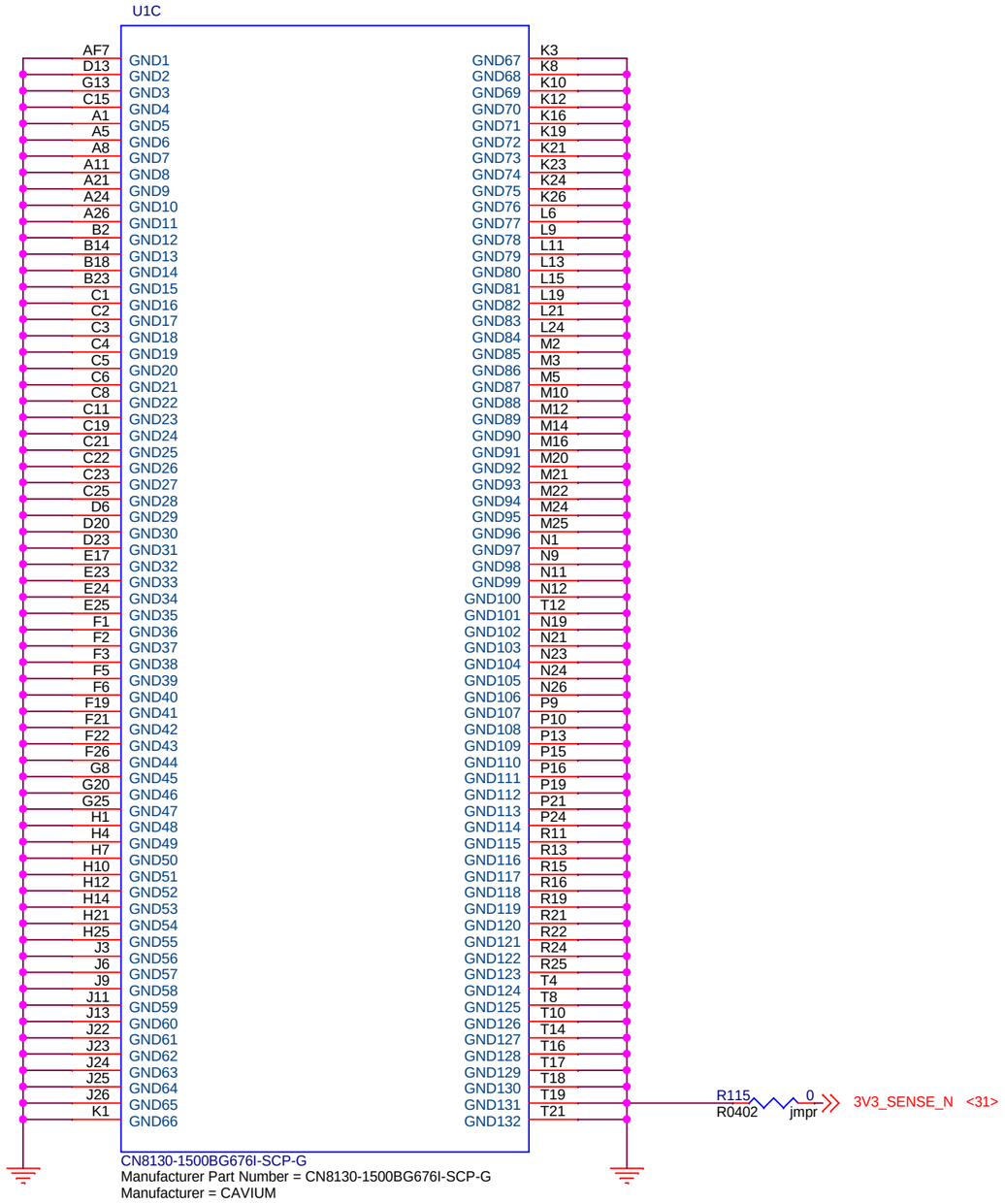

CAVIUM

Title
CN81XX GND

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B	<Doc>	1.0

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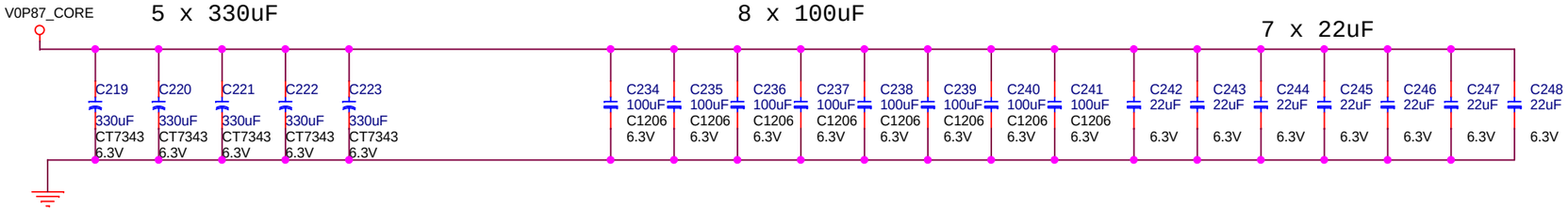
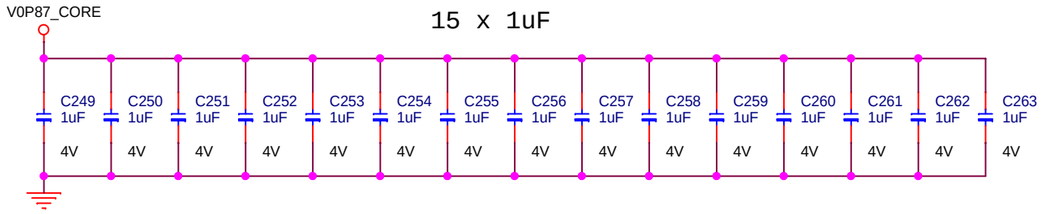
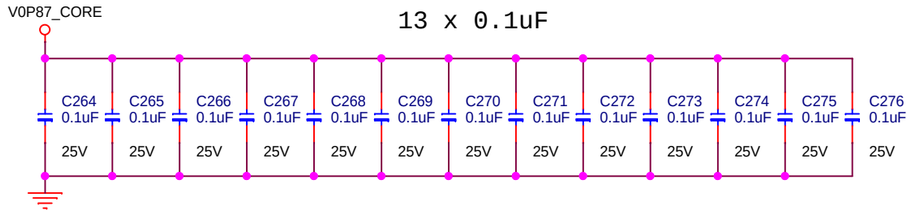
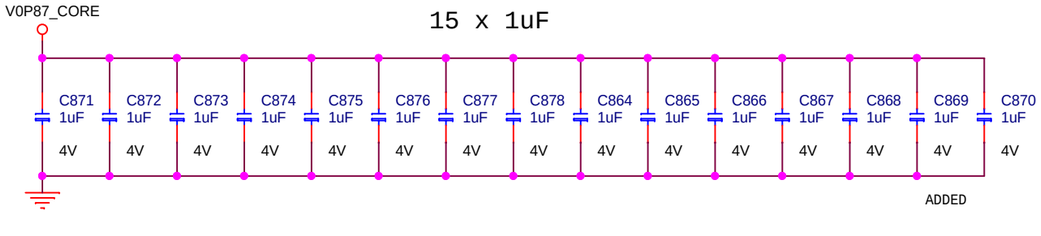
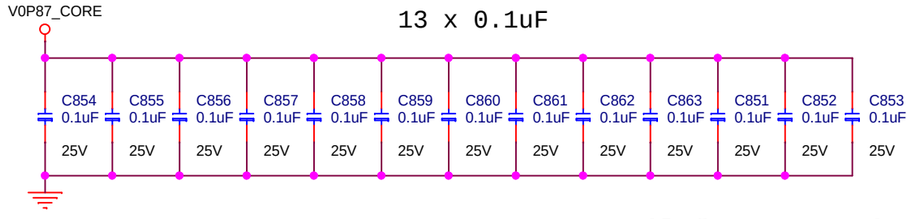
Delete C215~C218



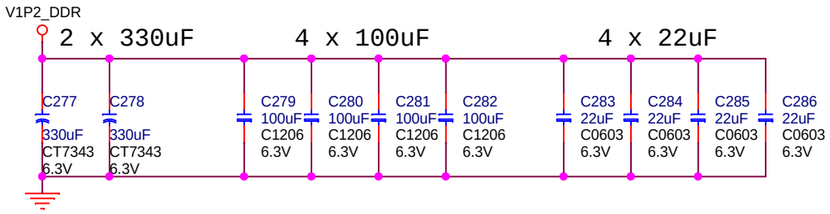


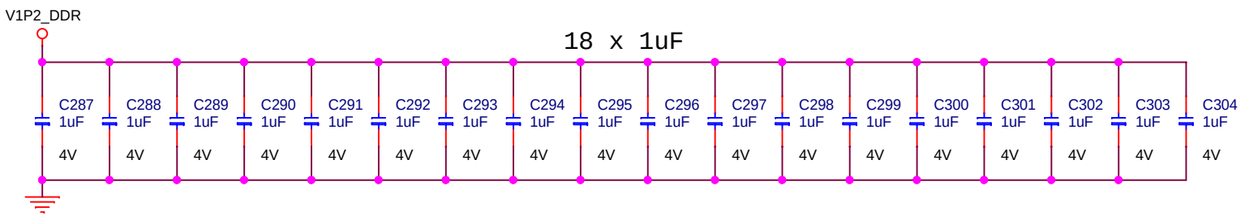


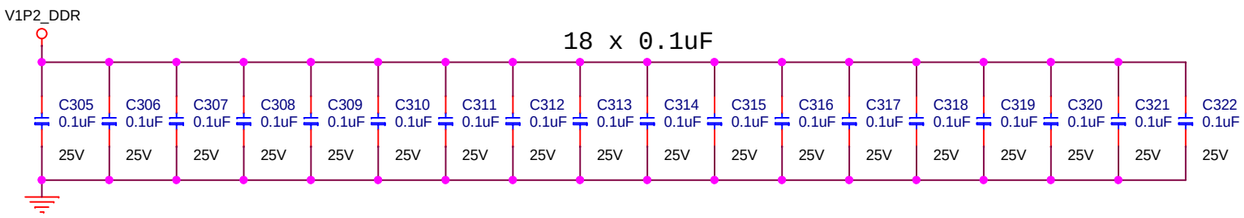




Layout Note: Use 10 mil for power vias







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CN81XX CORE & DR DECOUPLING

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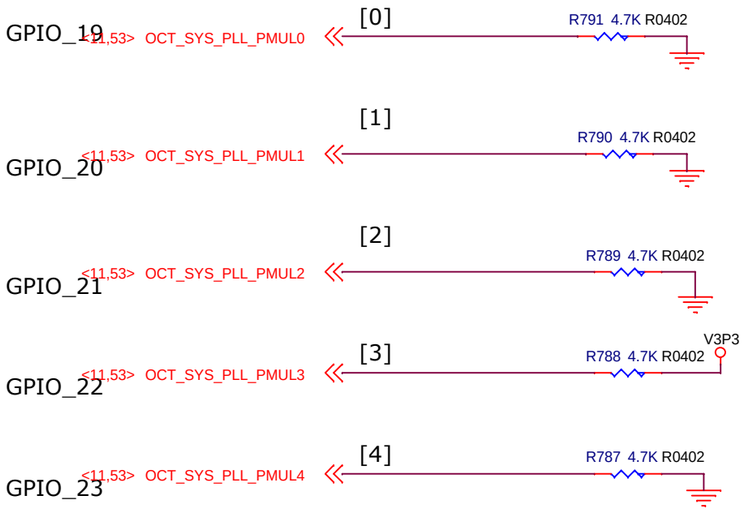
CN81xx Strapping

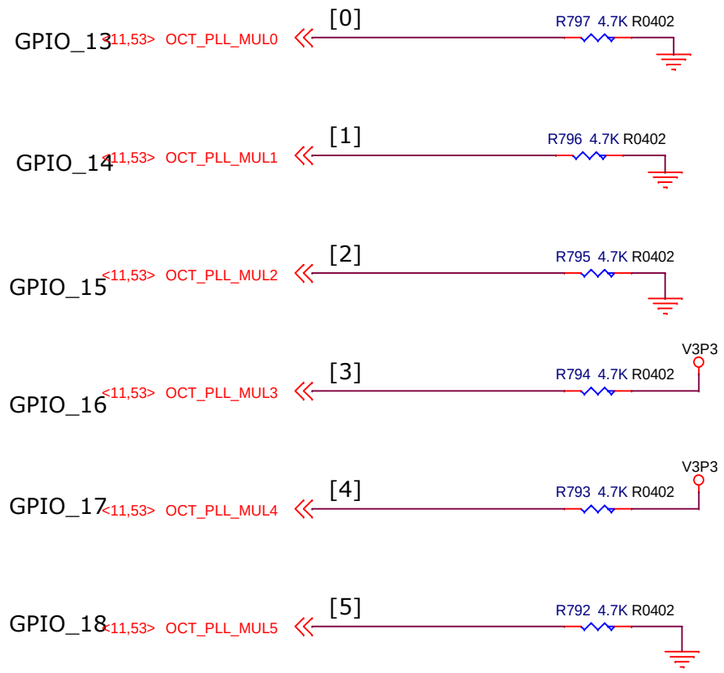
Coprocessor-clock (SCLK) PLL multiplier



Description :

0 0 0 0 1	= 350 MHz.
0 0 0 1 0	= 400 MHz.
0 0 0 1 1	= 450 MHz.
0 0 1 0 0	= 500 MHz
0 0 1 0 1	= 550 MHz.
0 0 1 1 0	= 600 MHz.
0 0 1 1 1	= 650 MHz.
0 1 0 0 0	**= 700 MHz. (DEFAULT)**

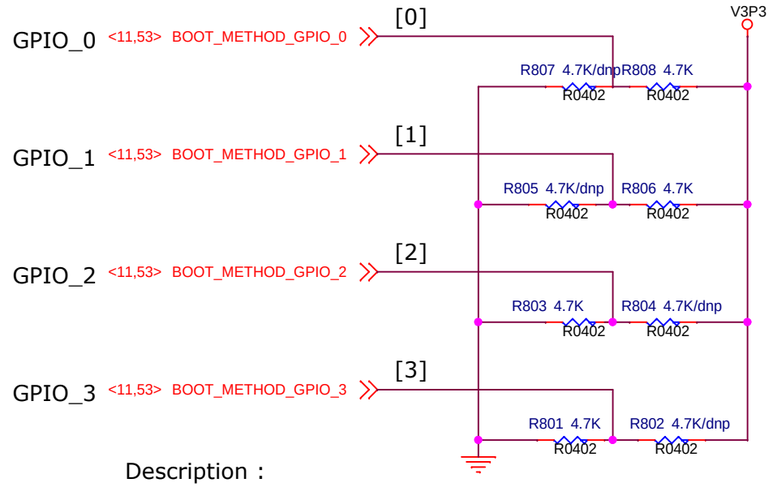
Core-clock (RCLK) PLL multiplier



Description :

0 0 0 0	0 1 1 0	= 600 MHz.
0 0 0 0	1 0 1 0	= 800 MHz.
0 0 0 0	1 1 1 0	= 1000 MHz.
0 0 0 1	0 0 1 0	= 1200 MHz.
0 0 0 1	0 1 1 0	= 1400 MHz.
0 0 0 1	1 0 0 0	**= 1500 MHz.(DEFAULT)**
0 0 0 1	**1 0 1 0**	**= 1600 MHz.**
0 0 0 1	1 1 1 0	= 1800 MHz.
0 0 1 0	0 0 1 0	= 2000 MHz.

RST Boot-strap Method Enumeration



Description :

0 0 1 0	= EMMC_SS
0 0 1 1	= EMMC_LS (Default boot from SD
0 1 0 1	**= SPI24**
0 1 1 0	= SPI32
1 0 0 0	= REMOTE
1 0 0 1	= CCPI0
1 0 1 0	= CCPI1
1 0 1 1	= CCPI2
1 1 0 0	= PCIE0
1 1 0 1	= PCIE2

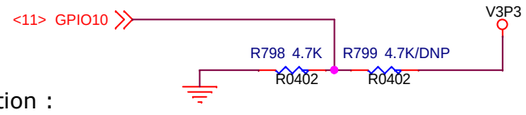
OCT_UART0_RTS_L = 1
OCT_UART1_RTS_L = 1
PLL SOURCE = PLL_REF_CLK

GPIO_12

During flash boot, reserved.
Post-boot, free for board use.

Trusted-mode

GPIO_10



Description :

0 = Non-trusted boot.

1 = Trusted boot.

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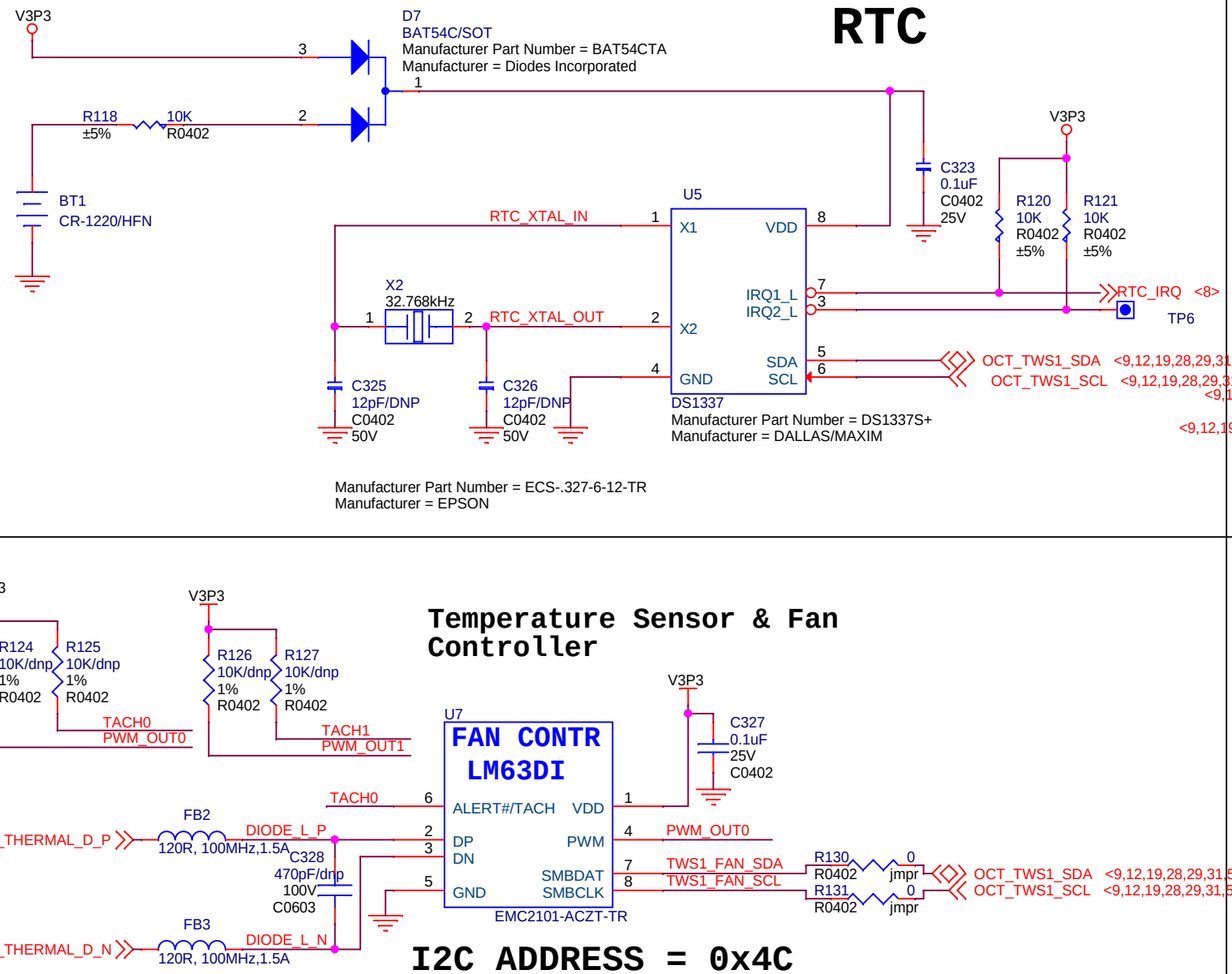
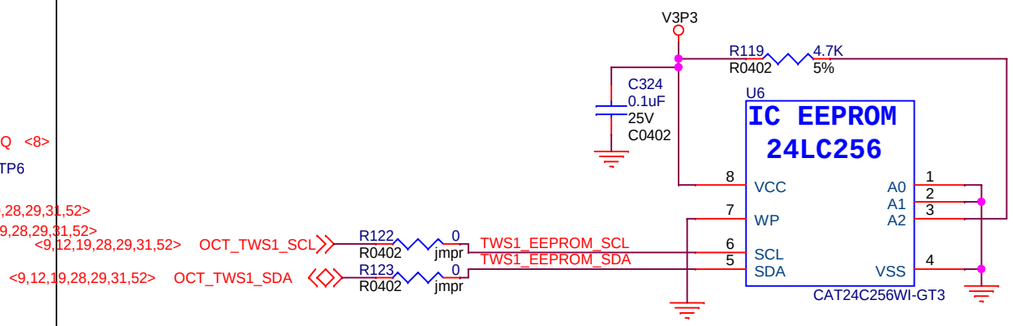
RTC



TLV EEPROM

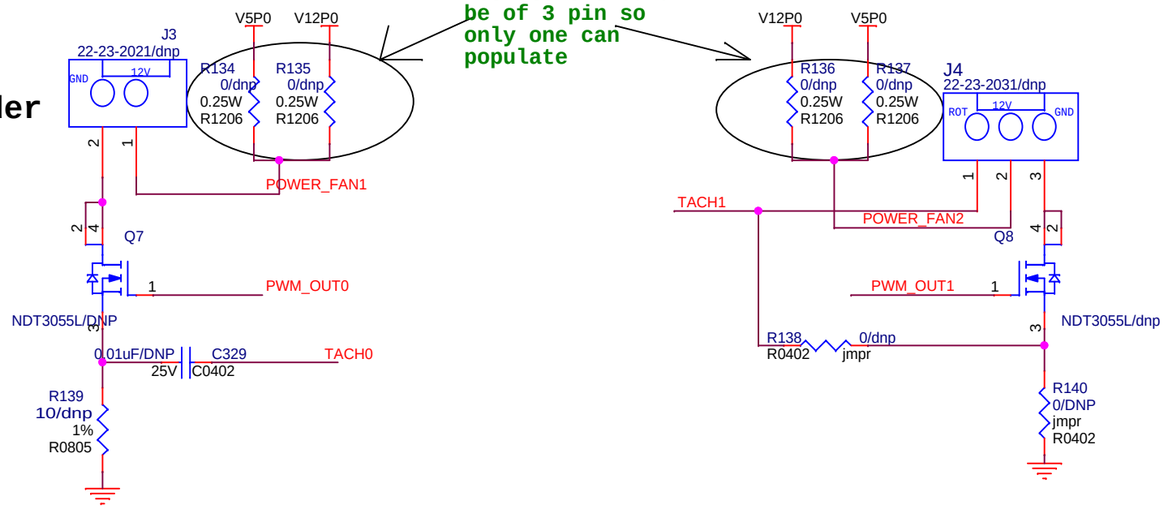
I2C ADDRESS = 0x54



Temperature Sensor & Fan Controller

I2C ADDRESS = 0x4C

BGA Fan Header



Layout Notes:
Resistors should be of 3 pin so only one can populate

Chassis Fan Header

CAVIUM

Title: RTC & THERMAL SENSORS

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PORT 6 RGMII MODE

RGMII TX length match:
RGMII_P6_TXD[0:3],TXCTRL,¡À20mil, TXCLK should 2.5inch longer than TXCTRL
RGMII RXlength match:
RGMII_P6_RXD[0:3],RXCTRL,RXCLK,should be ¡À20mil,

PORT 5-1 1000BASE-T DIFF

U9-1

<10> RGMII_P6_TXCLK — RGMII_P6_TXCLK — INPUT — 48 — TX_CLK6/REFCLKI6
<10> RGMII_P6_TXCTRL — RGMII_P6_TXCTRL — input — 49 — TX_EN6/TX_CTL6
50 — TX_ER6
51
<10> RGMII_P6_RXCLK — RGMII_P6_RXCLK — R0402R143 221% — output — 57 — COL6
<10> RGMII_P6_RXCTRL — RGMII_P6_RXCTRL — R0402R141 221% — output — 58 — RX_CLK6/REFCLKO6
59 — RX_DV6/CRS_DV6/RX_CTL6
60 — RX_ER6
CRS6

input

<10> RGMII_P6_TXD3 — RGMII_P6_TXD3 — 52 — TXD6_3
<10> RGMII_P6_TXD2 — RGMII_P6_TXD2 — 53 — TXD6_2
<10> RGMII_P6_TXD1 — RGMII_P6_TXD1 — 54 — TXD6_1
<10> RGMII_P6_TXD0 — RGMII_P6_TXD0 — 55 — TXD6_0

<10> RGMII_P6_RXD3 — RGMII_P6_RXD3 — R0402R144 221% — 62 — RXD6_3
<10> RGMII_P6_RXD2 — RGMII_P6_RXD2 — R0402R145 221% — 63 — RXD6_2
<10> RGMII_P6_RXD1 — RGMII_P6_RXD1 — R0402R146 221% — 64 — RXD6_1
<10> RGMII_P6_RXD0 — RGMII_P6_RXD0 — R0402R142 221% — 65 — RXD6_0

output

<10> OCT_SGMII_TX0_N — 78 — S_IN7M
<10> OCT_SGMII_TX0_P — 79 — S_IN7P

<10> OCT_SGMII_RX0_P — C845 0.1uF C0402 — 81 — S_OUT7P
<10> OCT_SGMII_RX0_N — C844 0.1uF C0402 — 82 — S_OUT7M

0: disable in-band management default

<53> ETHSW_TIVA_IBA — ETHSW_TIVA_IBA — 67 — IBA

V3P3_TIVA_LT

R148 10K R0402
R768 10K R0402
R147 10K R0402

R0402 R769 1% 191 — 76 — S_REXT
R0402 R149 1% 6.04K — 127 — ISET

<53> ETHSW_TIVA_PME_N — ETHSW_TIVA_PME_N — 93 — PME_N
<41> ETHSW_INT_TIVA — ETHSW_INT_TIVA — 94 — INTRP_N
<44> ETHSW_RESETN — ETHSW_RESETN — 96 — RESET_N

reset controlled by tiva

to IDT PLL
<49> ETHSW_SYNCLK_OUT — ETHSW_SYNCLK_OUT — R0402 R771 221% SYNCLK_OUT — 95 — SYNCLKO
90 — GPIO1
<12> ETHSW_GPIO — ETHSW_GPIO — R0402 R772 221% ETHSW_GPIO1
to 81xx GPIO

<31,41> TIVA_I2C0_SDA — TIVA_I2C0_SDA — 97 — SDO
98 — SDI/SDA/MDIO
<31,41> TIVA_I2C0_SCLK — TIVA_I2C0_SCLK — 100 — SCS_N
101 — SCL/MDC

125 — XO
126 — XI

<49> SYNCE_CLK from IDT pll — R773 22/DNP

108 — NC2
73 — NC3
74 — NC4

KSZ9567S

V3P3_TIVA_LT

R774 0
R775 0

X3
4 3
1 2
25MHZCRYSTAL

C331 12pF 1% 50V NPO
C330 12pF 1% 50V NPO

R150 1K R0402
LED3_1
LED4_1
R917 1K/dnp R0402
R151 1K R0402

TXRX1P_A 1 — P1_ETHSW_D0P — P1_ETHSW_D0P <22>
TXRX1M_A 2 — P1_ETHSW_D0N — P1_ETHSW_D0N <22>
TXRX1P_B 4 — P1_ETHSW_D1P — P1_ETHSW_D1P <22>
TXRX1M_B 5 — P1_ETHSW_D1N — P1_ETHSW_D1N <22>
TXRX1P_C 6 — P1_ETHSW_D2P — P1_ETHSW_D2P <22>
TXRX1M_C 7 — P1_ETHSW_D2N — P1_ETHSW_D2N <22>
TXRX1P_D 8 — P1_ETHSW_D3P — P1_ETHSW_D3P <22>
TXRX1M_D 9 — P1_ETHSW_D3N — P1_ETHSW_D3N <22>

PORT1 TO POWER BOARD

TXRX2P_A 12 — P2_ETHSW_D0P — P2_ETHSW_D0P <22>
TXRX2M_A 13 — P2_ETHSW_D0N — P2_ETHSW_D0N <22>
TXRX2P_B 15 — P2_ETHSW_D1P — P2_ETHSW_D1P <22>
TXRX2M_B 16 — P2_ETHSW_D1N — P2_ETHSW_D1N <22>
TXRX2P_C 17 — P2_ETHSW_D2P — P2_ETHSW_D2P <22>
TXRX2M_C 18 — P2_ETHSW_D2N — P2_ETHSW_D2N <22>
TXRX2P_D 20 — P2_ETHSW_D3P — P2_ETHSW_D3P <22>
TXRX2M_D 21 — P2_ETHSW_D3N — P2_ETHSW_D3N <22>

PORT2 TO POWER BOARD

TXRX3P_A 24 — P3_ETHSW_D0P — P3_ETHSW_D0P <24>
TXRX3M_A 25 — P3_ETHSW_D0N — P3_ETHSW_D0N <24>
TXRX3P_B 26 — P3_ETHSW_D1P — P3_ETHSW_D1P <24>
TXRX3M_B 27 — P3_ETHSW_D1N — P3_ETHSW_D1N <24>
TXRX3P_C 28 — P3_ETHSW_D2P — P3_ETHSW_D2P <24>
TXRX3M_C 29 — P3_ETHSW_D2N — P3_ETHSW_D2N <24>
TXRX3P_D 31 — P3_ETHSW_D3P — P3_ETHSW_D3P <24>
TXRX3M_D 32 — P3_ETHSW_D3N — P3_ETHSW_D3N <24>

PORT3 TO GBC CONNECTOR

TXRX4P_A 34 — ETHSW_TIVA_P0_TXP — ETHSW_TIVA_P0_TXP <40>
TXRX4M_A 35 — ETHSW_TIVA_P0_TXN — ETHSW_TIVA_P0_TXN <40>
TXRX4P_B 37 — TIVA_ETHSW_P0_RXP — TIVA_ETHSW_P0_RXP <40>
TXRX4M_B 38 — TIVA_ETHSW_P0_RXN — TIVA_ETHSW_P0_RXN <40>
TXRX4P_C 39
TXRX4M_C 40
TXRX4P_D 42
TXRX4M_D 43

PORT4 TO TIVA
TIVA only support 100M-BASE

TXRX5P_A 112 — P5_ETHSW_D0P — P5_ETHSW_D0P <22>
TXRX5M_A 113 — P5_ETHSW_D0N — P5_ETHSW_D0N <22>
TXRX5P_B 115 — P5_ETHSW_D1P — P5_ETHSW_D1P <22>
TXRX5M_B 116 — P5_ETHSW_D1N — P5_ETHSW_D1N <22>
TXRX5P_C 117 — P5_ETHSW_D2P — P5_ETHSW_D2P <22>
TXRX5M_C 118 — P5_ETHSW_D2N — P5_ETHSW_D2N <22>
TXRX5P_D 120 — P5_ETHSW_D3P — P5_ETHSW_D3P <22>
TXRX5M_D 121 — P5_ETHSW_D3N — P5_ETHSW_D3N <22>

PORT5 TO RJ46

LED1_1 106 — ETHSW_LED_Y1 — ETHSW_LED_Y1 <22>
LED1_0 105 — ETHSW_LED_G1 — ETHSW_LED_G1 <22>
LED2_1 92 — ETHSW_LED_Y2 — ETHSW_LED_Y2 <22>
LED2_0 91 — ETHSW_LED_G2 — ETHSW_LED_G2 <22>
LED3_1 89 — LED3_1
LED3_0 88
LED4_1 86 — LED4_1
LED4_0 85
LED5_1 103 — ETHSW_LED_Y5 — ETHSW_LED_Y5 <22>
LED5_0 102 — ETHSW_LED_G5 — ETHSW_LED_G5 <22>

PORT1 LED led1_1=1:Flow control: enable
PORT2 LED led2_1=1:normal link-up
auto-negotiation :enable

LED1_1/LED2_1/LED3_1
LED4_0/LED4_1/LED5_1 is IPU

LED4_1	LED3_1	Manage IF
0	0	MDIO
0	1	I2C default
1	X	SPI

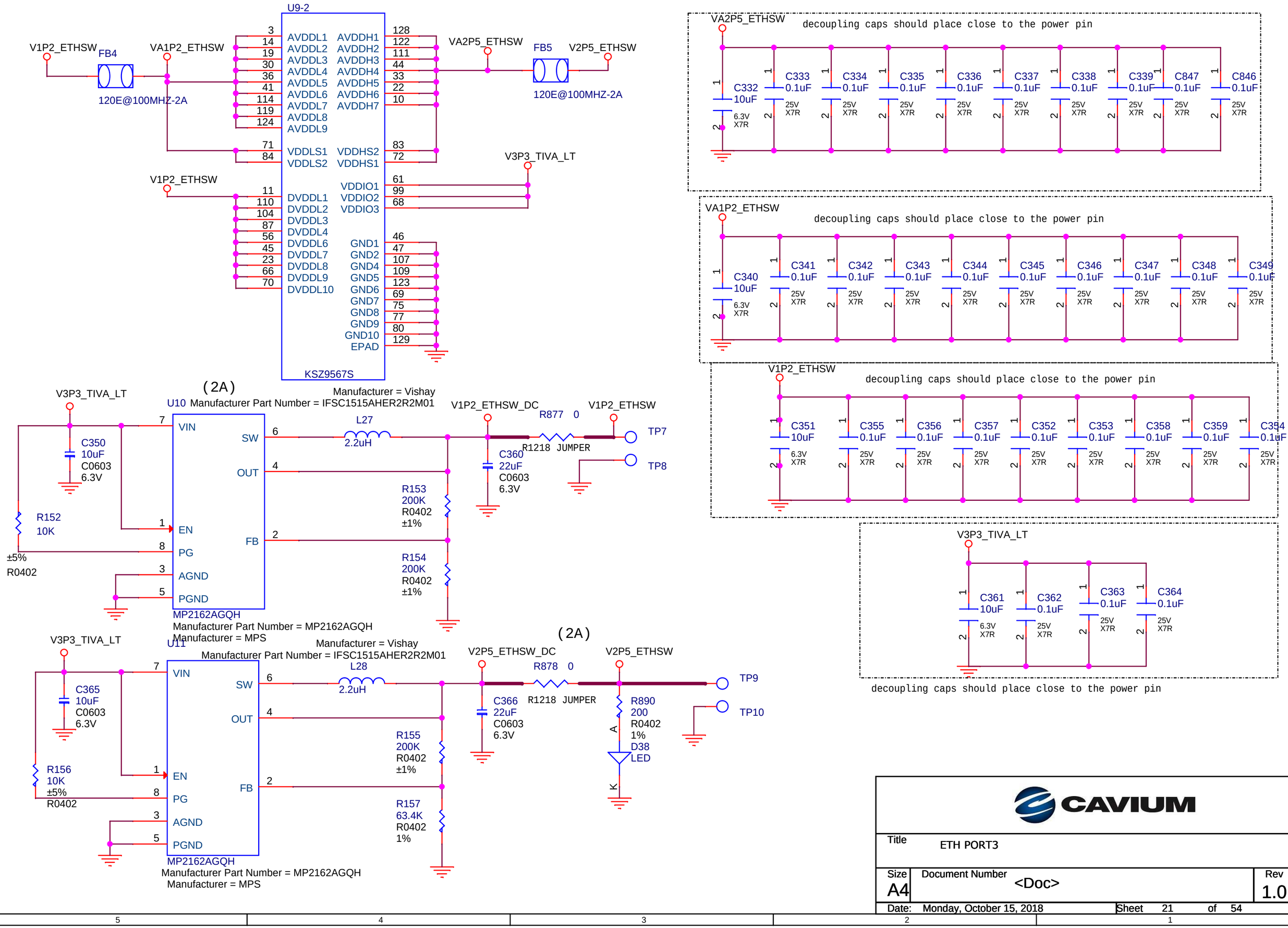
IIC ADDR: 0X5F

CAVIUM

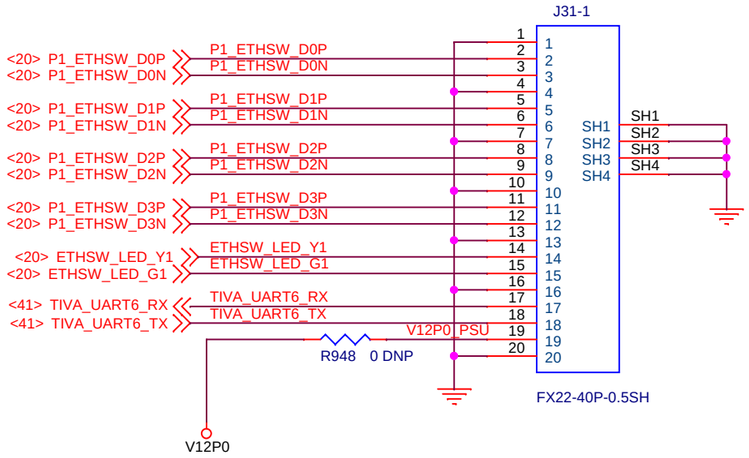
Title: ETHERNET SWITCH

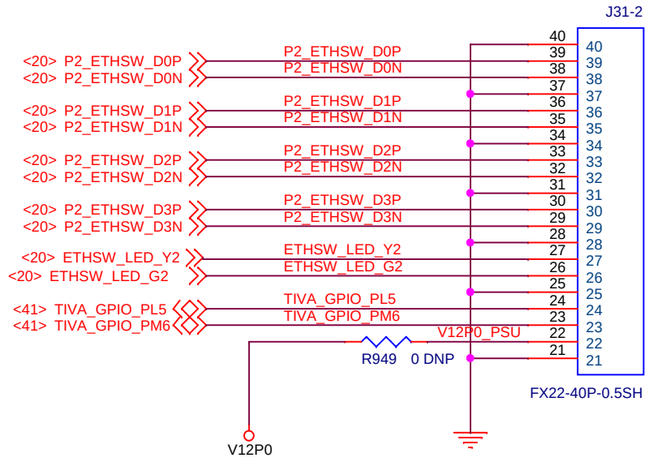
Size: Custom | Document Number: <Doc> | Rev: 1.0

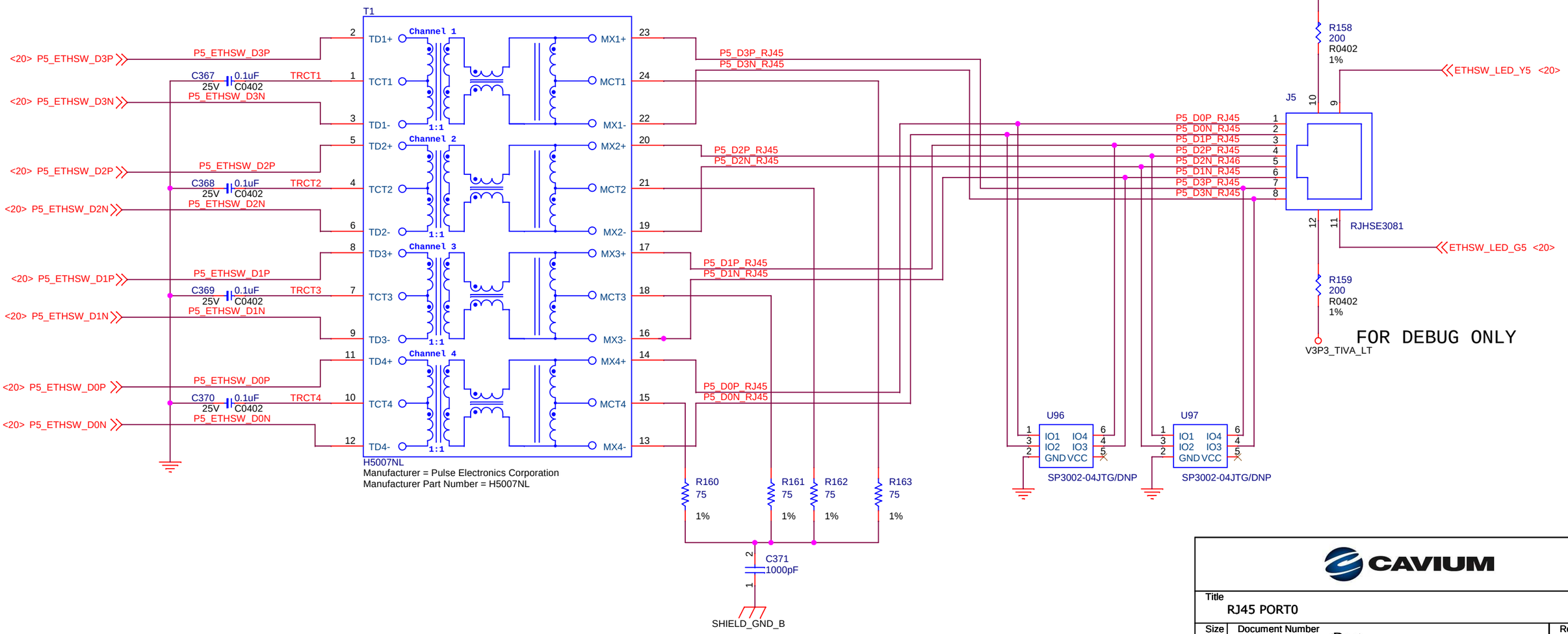
Date: Monday, October 15, 2018 | Sheet 20 of 54



Title	ETH PORT3	
Size A4	Document Number <Doc>	Rev 1.0
Date: Monday, October 15, 2018	Sheet 21 of 54	

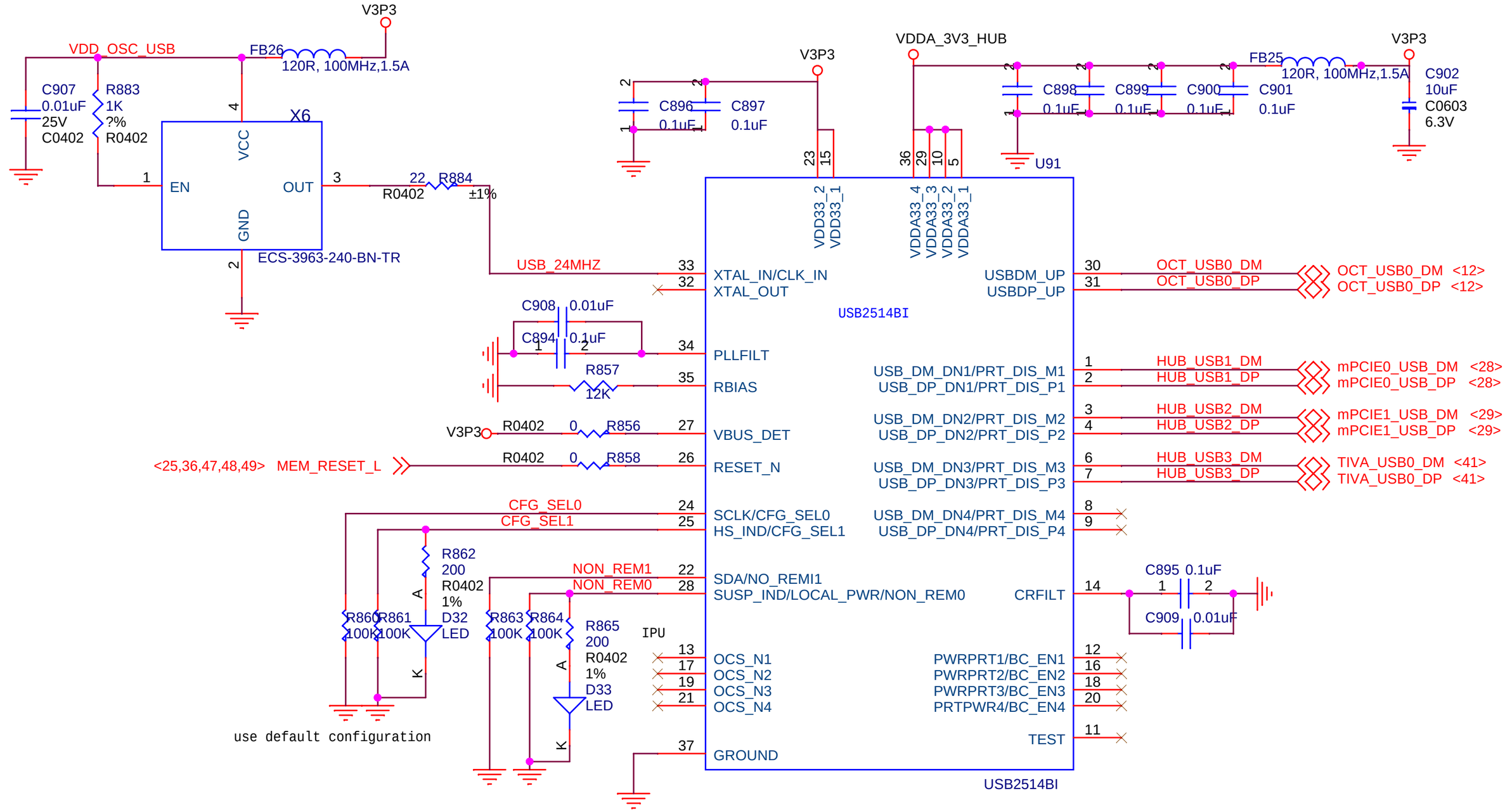






CAVIUM

Title: RJ45 PORT0		
Size: Custom	Document Number: <Doc>	Rev: 1.0
Date: Monday, October 15, 2018	Sheet 22 of 54	



CAVIUM

Title: USB2514BI-USB HUB		
Size: A	Document Number	Rev: 1.0
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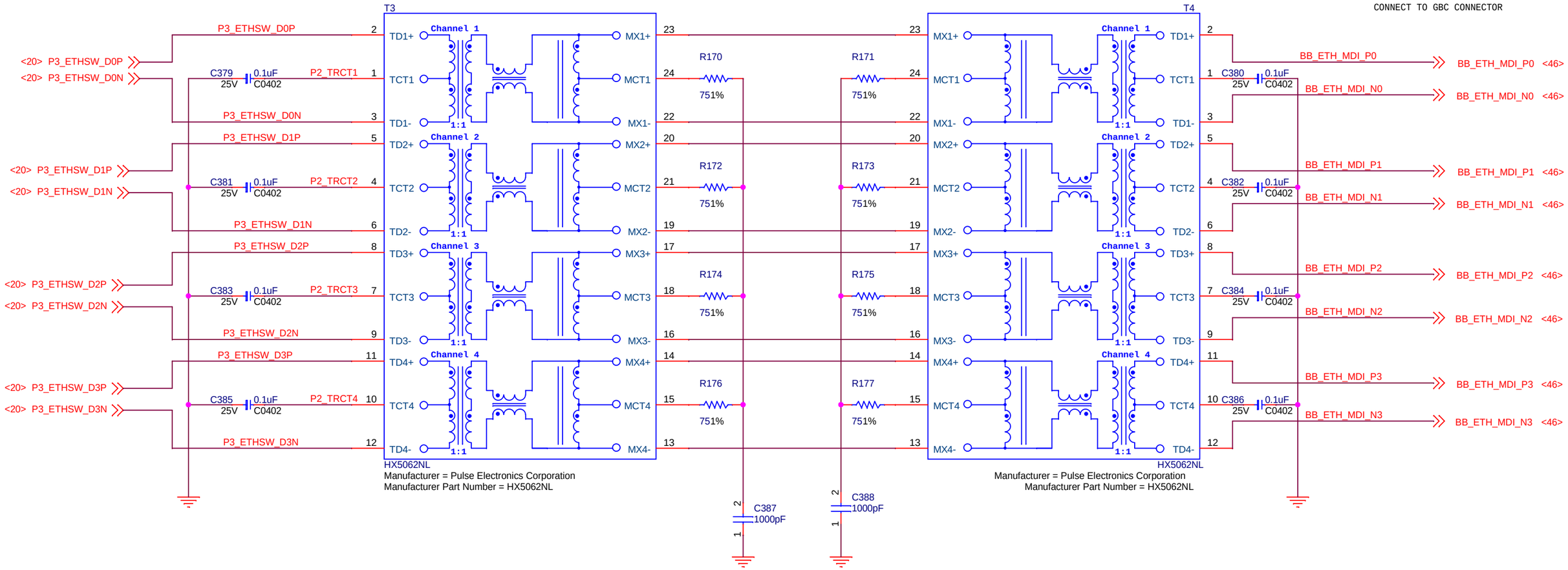
connect to port3



CAVIUM

Title: ETH PORT3 TO BB		
Size: B	Document Number: <Doc>	Rev: 1.0
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eMMC Flash

TP11
MMC_ISOLATE_L
<11> EMMC_BOOT_ISOLATE
R178 10K/DNP R0402
R179 10K R0402 ±5%
R181 10K R0402 ±5%
R180 1K/DNP R0402 ±5%
V3P3
V3P3_MMC
J6 2 PIN JUMPER
U12
S2_PMOS
G2_PMOS
D2_PMOS
D1_NMOS
G1_NMOS
S1_NMOS
AO6604
Manufacturer Part Number = AO6604
Manufacturer = Alpha & Omega Semiconductor

V5P0
C395 0.1uF C0402 25V
U13
R183 0
<12> OCT_EMMC_CMD0
<12> OCT_EMMC_CMD1
<8,25> SD_EMMC_SEL
R185 0
MMC_ISOLATE_L
SD_EMMC_SEL
R184 0
R186 0
MMC_SD_CMD
MMC_FL_CMD
MMC_FL_CMD
VCC
A
B
OE_L
EX
C
D
GND
Translate_Switch
Manufacturer Part Number = 7WBD383USG
Manufacturer = On Semi
R188 0DNP R0402
R190 0DNP R0402

V3P3
R189 10K R0402 ±5%
J7
SD_EMMC_SEL
<SD_EMMC_SEL <8,25>
R191 10K R0402 ±5%
3 PIN HEADER
HIGH => eMMC Flash Boot
LOW => SD Card Boot

V5P0
C401 0.1uF C0402 25V
C402 0.1uF C0402 25V
U15
SN74CBTD3861
VCC
<12> OCT_EMMC_CLK
<12> OCT_EMMC_D[7:0]
OCT_EMMC_D7
OCT_EMMC_D6
OCT_EMMC_D2
OCT_EMMC_D5
OCT_EMMC_D1
OCT_EMMC_D4
OCT_EMMC_D0
OCT_EMMC_D3
MMC_ISOLATE_L
OE
MMC_CLK
MMC_D7
MMC_D6
MMC_D2
MMC_D5
MMC_D1
MMC_D4
MMC_D0
MMC_D3
NC
GND
Manufacturer Part Number = SN74CBTD3861DW
Manufacturer = TI

V3P3_MMC
C408 10uF C0603 6.3V
C409 0.1uF C0402 25V
C410 0.1uF C0402 25V
J8
ASSY HDR
47571-0001
VDD
DAT0
DAT1
DAT2
CD/DAT3
CMD
CLOCK
VSS
MMC_D0
MMC_D1
MMC_D2
MMC_D3
MMC_SD_CMD
MMC_CLK
MICRO SD
0475710001

U14
MMC Memory
MTFC4GACAAAM
MMC_D0
MMC_D1
MMC_D2
MMC_D3
MMC_D4
MMC_D5
MMC_D6
MMC_D7
DAT0
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7
RFU_0
RFU_1
RFU_2
RFU_3
RFU_4
RFU_5
RFU_6
RFU_7
RFU_8
RFU_9
RFU_10
RFU_11
RFU_12
RFU_13
RFU_14
RFU_15
NC_0
NC_1
NC_2
NC_3
NC_4
NC_5
NC_6
NC_7
NC_8
NC_9
NC_10
NC_11
NC_12
NC_13
NC_14
NC_15
NC_16
NC_17
NC_18
NC_19
NC_20
NC_21
NC_22
NC_23
NC_24
NC_25
NC_26
NC_27
NC_28
NC_29
NC_30
NC_31
NC_32
NC_33
NC_34
NC_35
NC_36
NC_37
NC_38
NC_39
NC_40
NC_41
NC_42
NC_43
NC_44
NC_45
NC_46
NC_47
NC_48
NC_49
NC_50
NC_51
NC_52
NC_53
NC_54
NC_55
VCC_0
VCC_1
VCC_2
VCC_3
VCCQ_0
VCCQ_1
VCCQ_2
VCCQ_3
VCCQ_4
VSSQ_0
VSSQ_1
VSSQ_2
VSSQ_3
VSSQ_4
VSS_0
VSS_1
VSS_2
VSS_3
CLK
RST_N
CMD
VDDIM
NC_56
NC_57
NC_58
NC_59
NC_60
NC_61
NC_62
NC_63
NC_64
NC_65
NC_66
NC_67
NC_68
NC_69
NC_70
NC_71
NC_72
NC_73
NC_74
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NC_80
NC_81
NC_82
NC_83
NC_84
NC_85
NC_86
NC_87
NC_88
NC_89
NC_90
NC_91
NC_92
NC_93
NC_94
NC_95
NC_96
NC_97
NC_98
NC_99
NC_100
NC_101
NC_102
NC_103
NC_104
NC_105
NC_106
MTFC4GACAAAM-1M WT

V3P3
FB6 120R, 100MHz,1.5A
C391 0.1uF 25V C0402
C392 2.2uF 10V C0402
C393 0.1uF 25V C0402
C394 2.2uF 10V C0402
R182 0 R0402 jmpr
AGND_EMMC
VCCQ_MMC
C396 0.1uF 25V C0402
C389 0.1uF 25V C0402
C390 0.1uF 25V C0402
C397 0.1uF 25V C0402
C398 0.1uF 25V C0402
AGND_EMMC
R187 0 R0402 jmpr
MEM_RESET_L <23,36,47,48,49>
MMC_CLK
MMC_RST_L
MMC_FL_CMD
MMC_VDDIM
C399 0.1uF 25V C0402
C400 1uF 10V C0402

V3P3
C403 22uF 6.3V C0603
C404 0.1uF 25V C0402
C405 0.1uF 25V C0402
C406 0.1uF 25V C0402
C407 0.1uF 25V C0402

V3P3
R193 10K 1% R0402
R194 10K 1% R0402
R195 10K 1% R0402
R196 10K 1% R0402
R197 10K 1% R0402
R198 10K 1% R0402
R199 10K 1% R0402
R200 10K 1% R0402
R201 10K 1% R0402
R202 10K 1% R0402
R203 10K 1% R0402
MMC_CLK
MMC_D0
MMC_D1
MMC_D2
MMC_D3
MMC_D4
MMC_D5
MMC_D6
MMC_D7
MMC_FL_CMD
MMC_SD_CMD

CAVIUM

Title	BOOT EMMC/MMC	
Size: Custom	Document Number: <Doc>	Rev: 1.0
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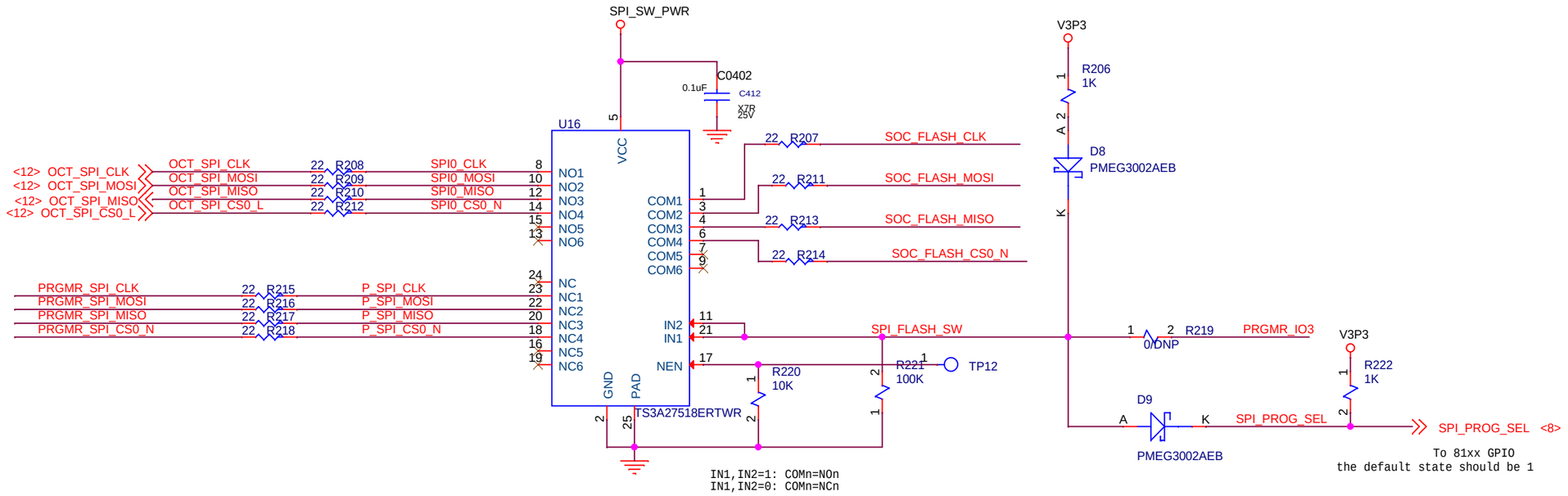

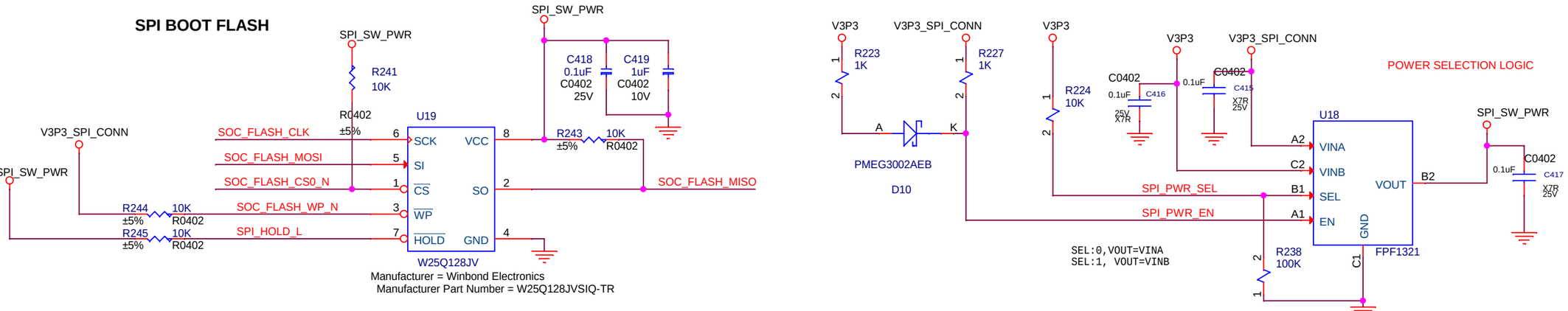

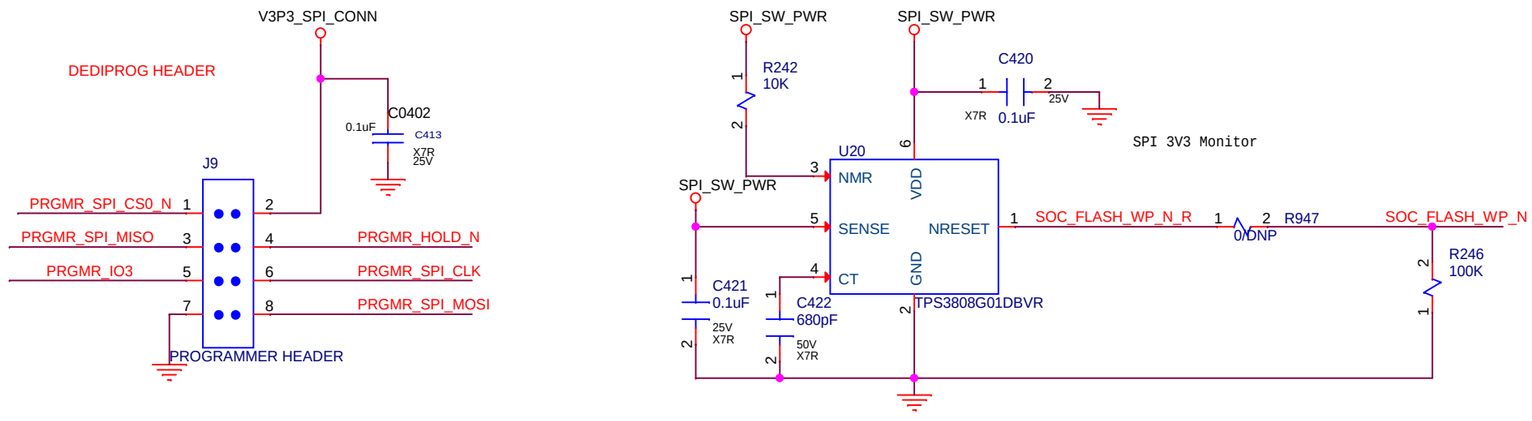

CAVIUM

Title
BOOT SPI FLASH & NAND FLASH

B

Size	Document Number	Rev
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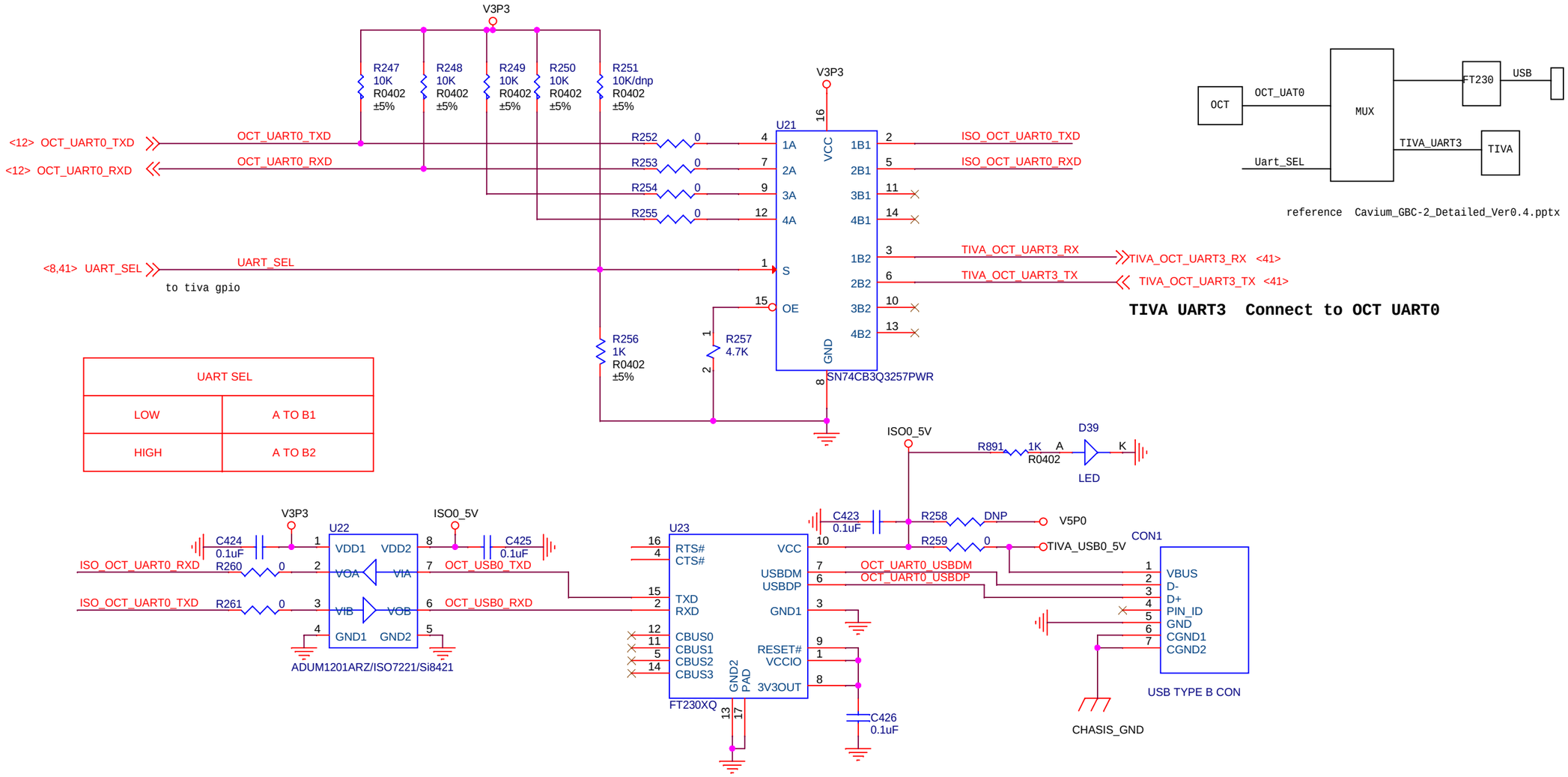
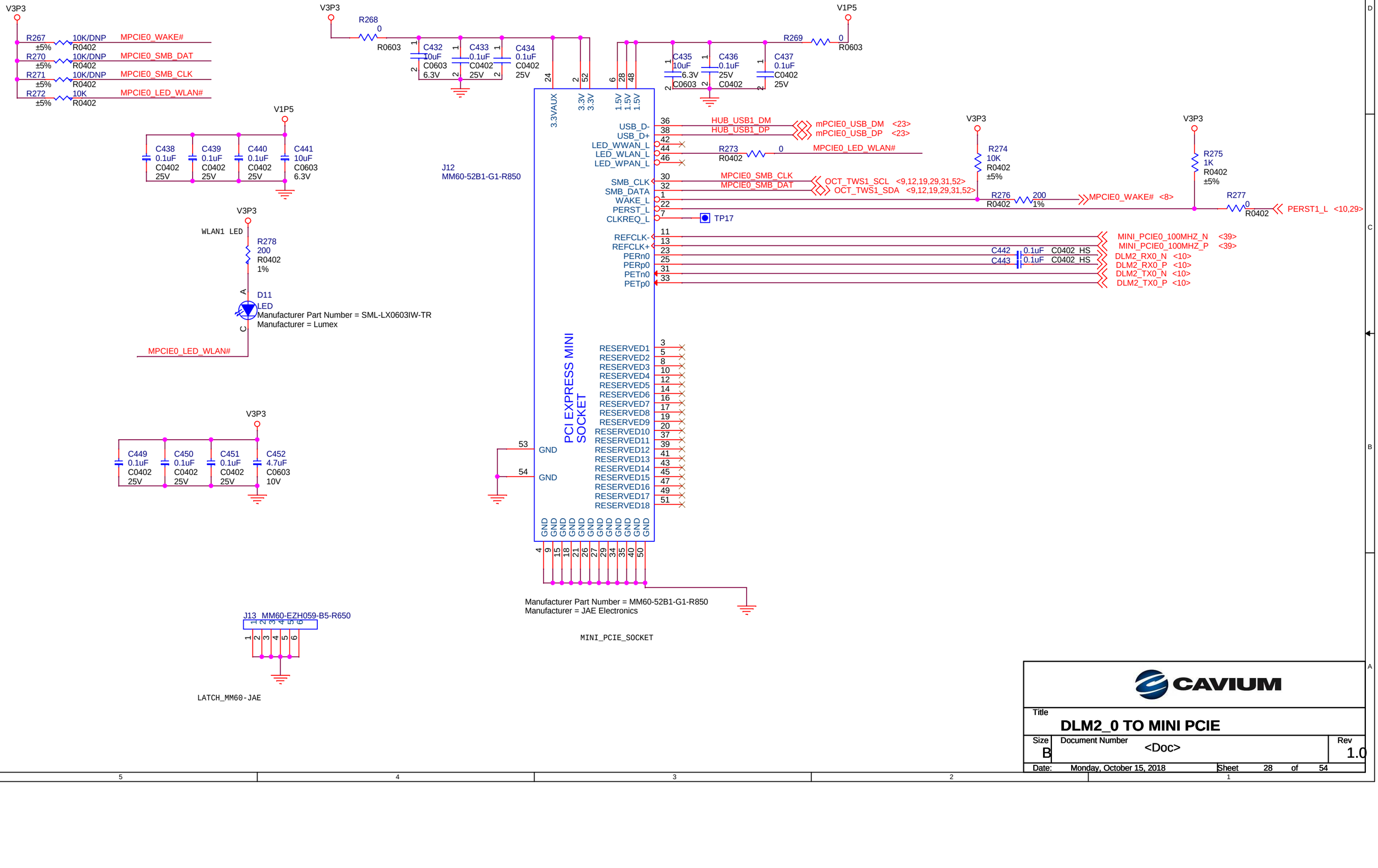
Date:	Sheet 26 of 54	



Title			
OCT-UART 0			
Size: B	Document Number: <Doc>		Rev: 1.0
Date: Monday, October 15, 2018	Sheet 27 of 54		

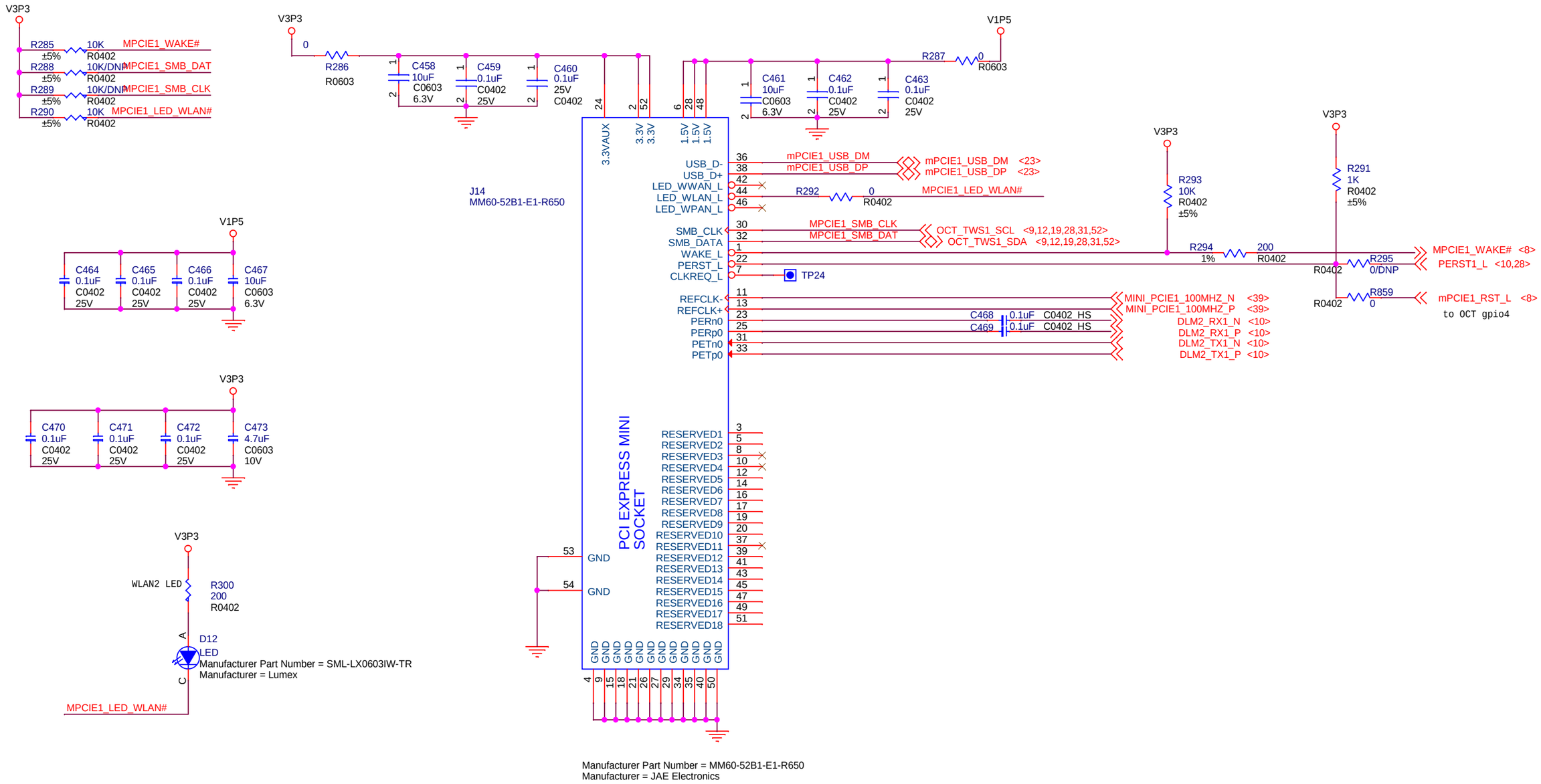


CAVIUM

Title: DLM2_0 TO MINI PCIE

Size	Document Number	Rev
B	<Doc>	1.0

Date: Monday, October 15, 2018 Sheet 28 of 54



CAVIUM

Title: DLM2_1 TO MINI PCIE

Size	Document Number	Rev
B	<Doc>	1.0

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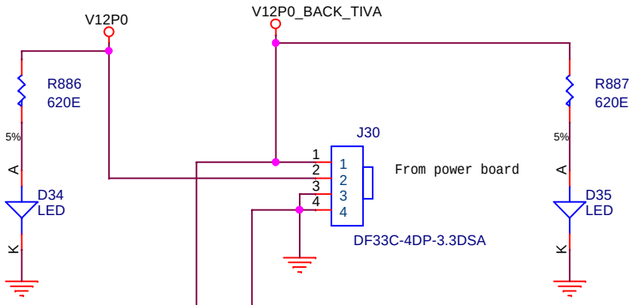
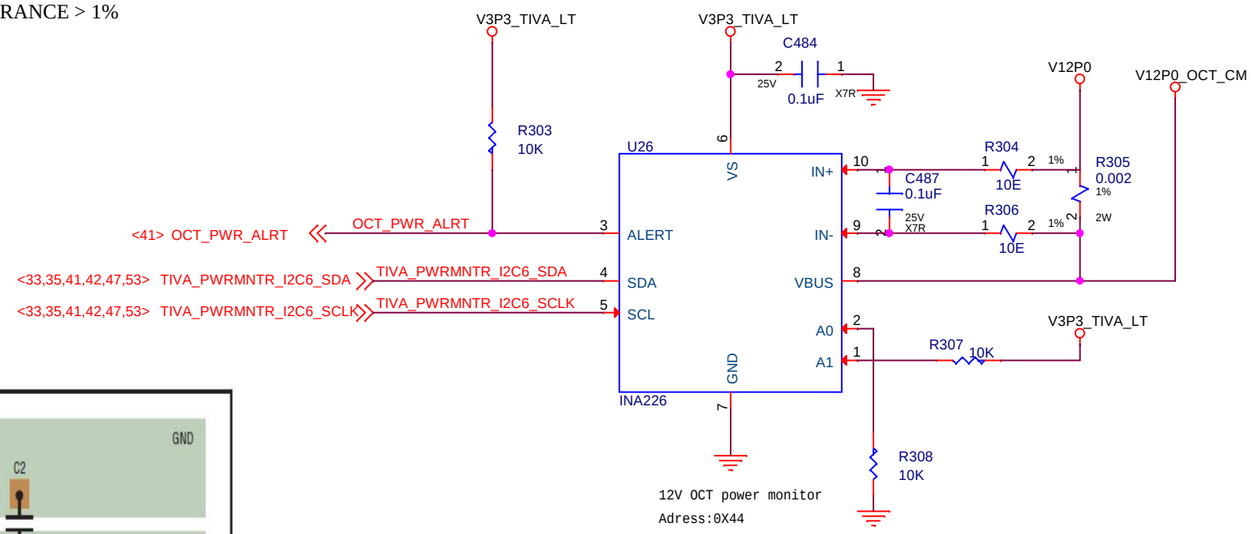
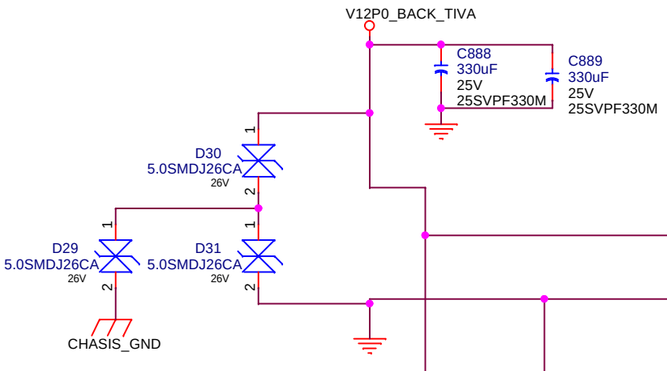
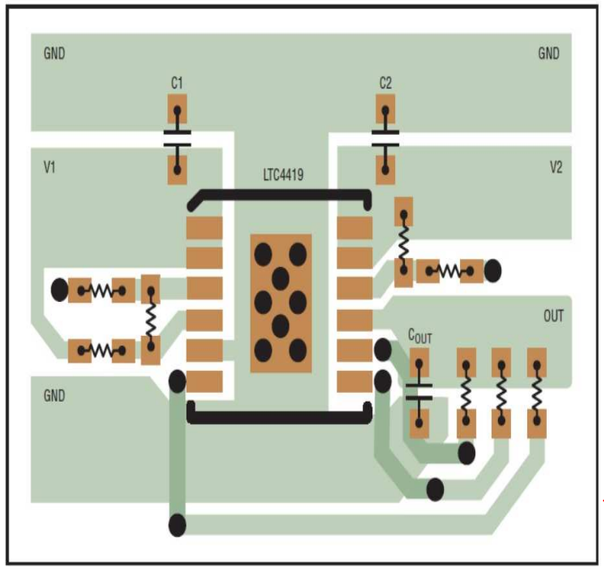
UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 0402 PACKAGE, POWER RATING < 0.5W & TOLERANCE > 1%
CAPACITORS ARE 0402 PACKAGE & TOLERANCE OF 10%

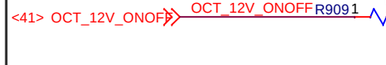


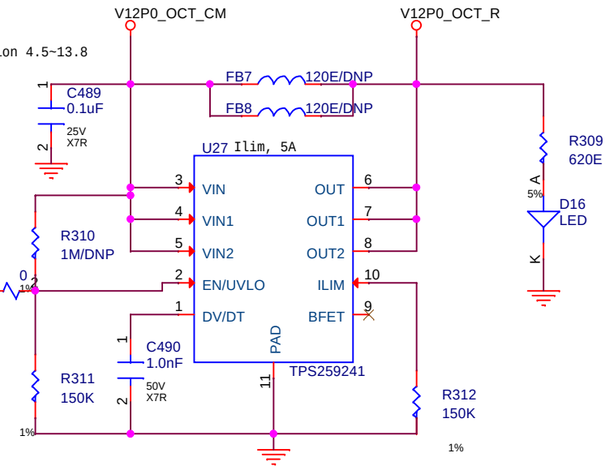






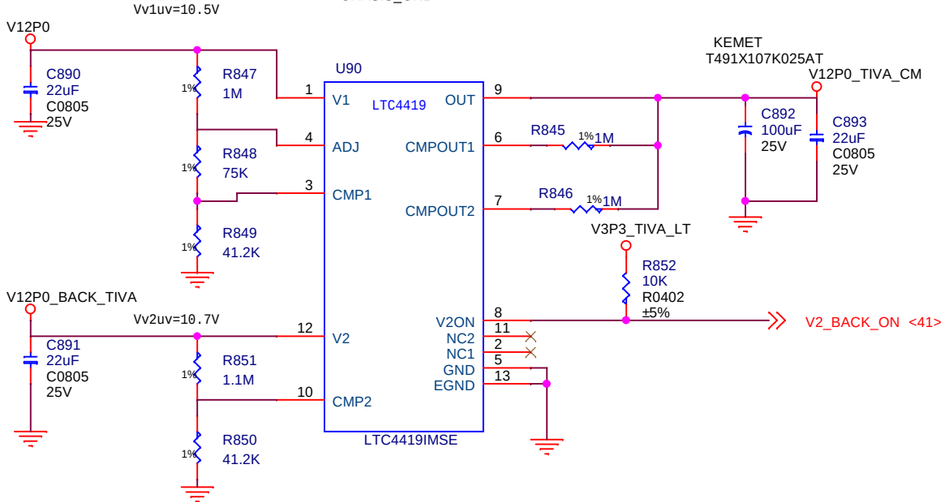
U90 pcb layout recommend





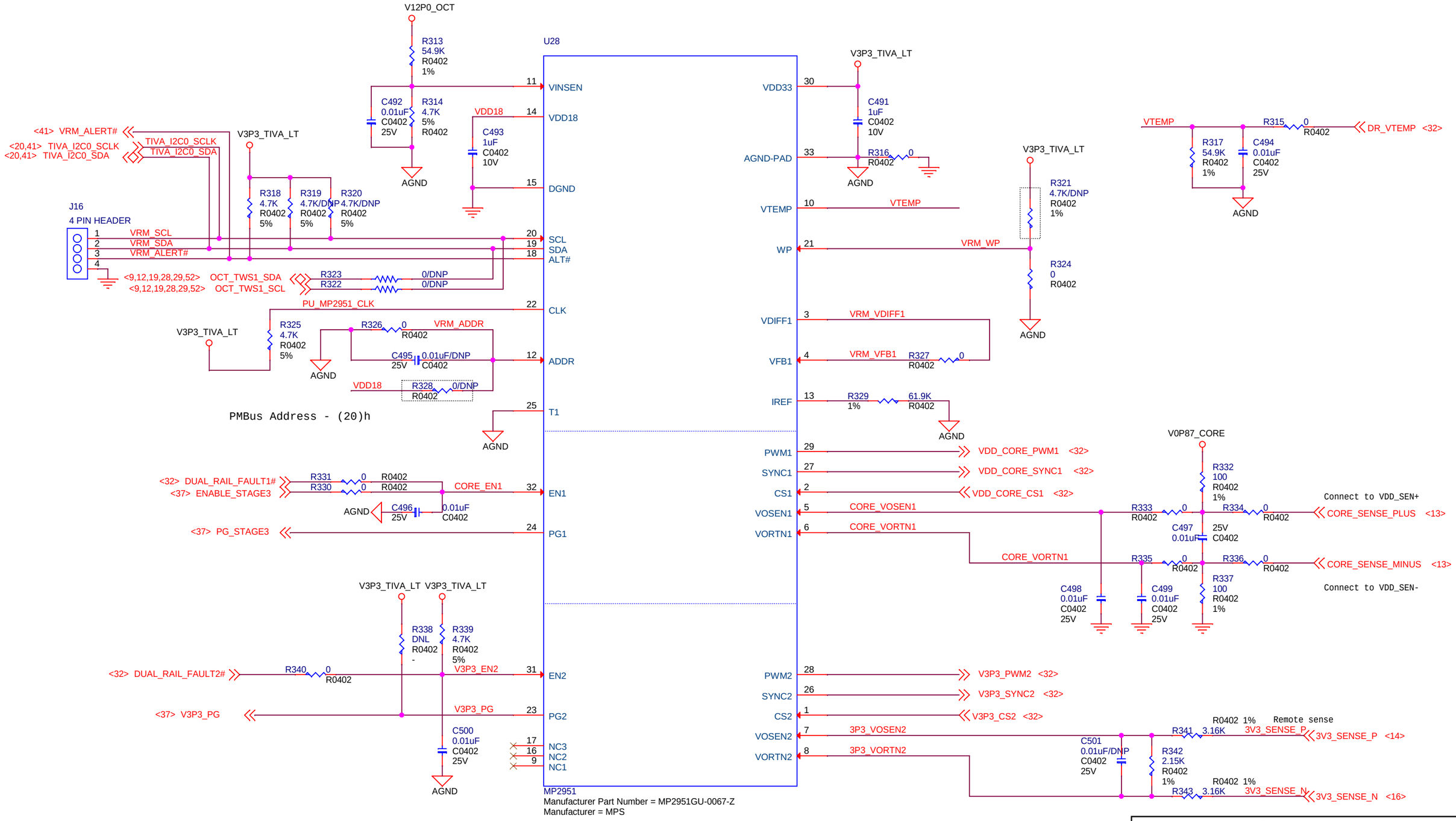
Place R867,R868 after U27

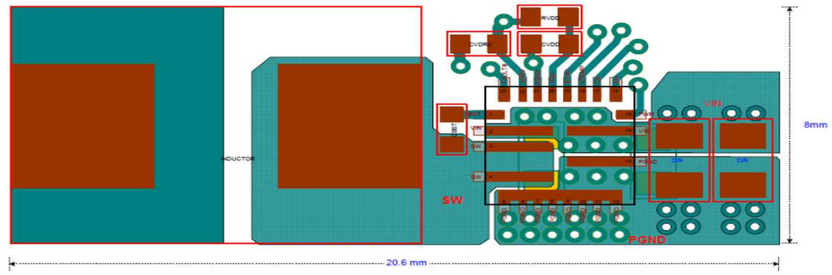
Vsw1=10.06V
Vv1uv=10.5V



CAVIUM

Title: POWER ENTRY		
Size: Custom	Document Number: <Doc>	Rev: 1.0
Date: Monday, October 15, 2018	Sheet 30 of 54	


V12P0_OCT
R313 54.9K R0402 1%
U28
C492 0.01uF C0402 25V
R314 4.7K 5% R0402
AGND
VDD18
C493 1uF C0402 10V
11 VINSEN
14 VDD18
15 DGND
<41> VRM_ALERT#
<20,41> TIVA_I2C0_SCLK
<20,41> TIVA_I2C0_SDA
TIVA_I2C0_SCLK
TIVA_I2C0_SDA
V3P3_TIVA_LT
R318 4.7K R0402 5%
R319 4.7K/DNP R0402 5%
R320 4.7K/DNP R0402 5%
J16
4 PIN HEADER
1 VRM_SCL
2 VRM_SDA
3 VRM_ALERT#
4
20 SCL
19 SDA
18 ALT#
<9,12,19,28,29,52> OCT_TWS1_SDA
<9,12,19,28,29,52> OCT_TWS1_SCL
R323 0/DNP
R322 0/DNP
PU_MP2951_CLK
22 CLK
V3P3_TIVA_LT
R325 4.7K R0402 5%
R326 0 R0402
VRM_ADDR
C495 0.01uF/DNP C0402 25V
12 ADDR
VDD18
R328 0/DNP R0402
PMBus Address - (20)h
25 T1
AGND
<32> DUAL_RAIL_FAULT1#
<37> ENABLE_STAGE3
R331 0 R0402
R330 0 R0402
CORE_EN1
32 EN1
C496 0.01uF C0402 25V
<37> PG_STAGE3
24 PG1
V3P3_TIVA_LT V3P3_TIVA_LT
R338 DNL R0402 -
R339 4.7K R0402 5%
<32> DUAL_RAIL_FAULT2#
R340 0 R0402
V3P3_EN2
31 EN2
<37> V3P3_PG
V3P3_PG
23 PG2
C500 0.01uF C0402 25V
17 NC3
16 NC2
9 NC1
MP2951
Manufacturer Part Number = MP2951GU-0067-Z
Manufacturer = MPS
V3P3_TIVA_LT
30 VDD33
C491 1uF C0402 10V
33 AGND-PAD
R316 0 R0402
AGND
10 VTEMP
VTEMP
21 WP
VRM_WP
R321 4.7K/DNP R0402 1%
R324 0 R0402
AGND
3 VDIFF1
VRM_VDIFF1
4 VFB1
VRM_VFB1
R327 0 R0402
13 IREF
R329 1% 61.9K R0402
AGND
29 PWM1
VDD_CORE_PWM1 <32>
27 SYNC1
VDD_CORE_SYNC1 <32>
2 CS1
VDD_CORE_CS1 <32>
5 VOSEN1
CORE_VOSEN1
6 VORTN1
CORE_VORTN1
28 PWM2
V3P3_PWM2 <32>
26 SYNC2
V3P3_SYNC2 <32>
1 CS2
V3P3_CS2 <32>
7 VOSEN2
3P3_VOSEN2
8 VORTN2
3P3_VORTN2
VTEMP
R315 0 R0402
DR_VTEMP <32>
R317 54.9K R0402 1%
C494 0.01uF C0402 25V
AGND
V0P87_CORE
R332 100 R0402 1%
Connect to VDD_SEN+
R333 0 R0402
R334 0 R0402
CORE_SENSE_PLUS <13>
C497 0.01uF 25V C0402
R335 0 R0402
R336 0 R0402
CORE_SENSE_MINUS <13>
R337 100 R0402 1%
Connect to VDD_SEN-
C498 0.01uF C0402 25V
C499 0.01uF C0402 25V
C501 0.01uF/DNP C0402 25V
R0402 1% Remote sense
R341 3.16K 3V3_SENSE_P
3V3_SENSE_P <14>
R342 2.15K R0402 1%
R0402 1%
R343 3.16K 3V3_SENSE_N
3V3_SENSE_N <16>
CAVIUM
Title
CONTROL:CPU CORE&3V3
Size B
Document Number
54
Rev 1.0
Date: Monday, October 15, 2018
Sheet 31 of



V12P0_OCT

C502 22uF C0805 25V
C503 22uF C0805 25V
C504 22uF C0805 25V
C505 22uF C0805 25V
C506 1uF C0402 25V
C507 1uF C0402 25V

V3P3

R344 2.2R R0402 ±1%
R345 2K R0402 ±5%
C510 1uF C0402 25V
C509 1uF C0402 25V

U29
MP86905
Manufacturer Part Number = MP86905GR
Manufacturer = MPS

2 VIN1
14 VIN2
CORE_VDRV1 22 VDRV
CORE_VDD1 20 VDD
CORE_AGND1 21 AGND
16 EN
<31> VDD_CORE_PWM1 15 PWM
<31> VDD_CORE_SYNC1 19 SYNC
5 6 7 8 9 10 11 12 13 PGND1 PGND2 PGND3 PGND4 PGND5 PGND6 PGND7 PGND8 PGND9

1 CORE_BST BST
C508 1uF C0402 25V
3 SW1
4 SW2
R346 3.32/DNP R0402 ±1%
C516 220pF/DNP C0402 50V

L29
Manufacturer = Coilcraft
Manufacturer Part Number = SLR1050A-151KEB
150nH, 51A

V0P87_CORE
use large copper shape
C511 330uF 6.3V
C512 330uF 6.3V
C513 330uF 6.3V
C514 100uF C1206 6.3V
C515 100uF C1206 6.3V
R347 1K R0402 ±5%
TP29
TP30

18 VTEMP → DR_VTEMP <31,32>
17 CS → VDD_CORE_CS1 <31>
23 FAULT# → DUAL_RAIL_FAULT1# <31>

V12P0_OCT_R
use large copper shape
V12P0_OCT
R871 0
R1218 JUMPER

V12P0_OCT

C517 22uF C0805 25V
C518 22uF C0805 25V
C519 22uF C0805 25V
C520 22uF C0805 25V
C521 1uF C0402 25V
C522 1uF C0402 25V

V3P3_TIVA_LT

R348 2.2R R0402 ±1%
R349 2K R0402 ±5%
C524 1uF C0402 25V
C525 1uF C0402 25V

U30
MP86905
Manufacturer Part Number = MP86905GR
Manufacturer = MPS

2 VIN1
14 VIN2
V3P3_VDRV2 22 VDRV
V3P3_VDD2 20 VDD
V3P3_AGND2 21 AGND
16 EN
<31> V3P3_PWM2 15 PWM
<31> V3P3_SYNC2 19 SYNC
5 6 7 8 9 10 11 12 13 PGND1 PGND2 PGND3 PGND4 PGND5 PGND6 PGND7 PGND8 PGND9

1 V3P3_BST BST
C523 1uF C0402 25V
3 SW1
4 SW2
R350 3.32/DNP R0402 ±1% recalculator the resistor
C531 220pF/DNP C0402 50V

L30
Manufacturer Part Number = XAL7070-651MEC
Manufacturer = Coilcraft
650nH, 40A

use large copper shape
V3P3
3.3V
C526 330uF 6.3V
C527 330uF 6.3V
C528 330uF 6.3V
C529 100uF C1206 6.3V
C530 100uF C1206 6.3V
R351 1K R0402 ±5%
TP31
TP32

18 VTEMP → DR_VTEMP <31,32>
17 CS → V3P3_CS2 <31>
23 FAULT# → DUAL_RAIL_FAULT2# <31>

CAVIUM

Title: GATE DRVRS

Size	Document Number	Rev
B	<Doc>	1.0

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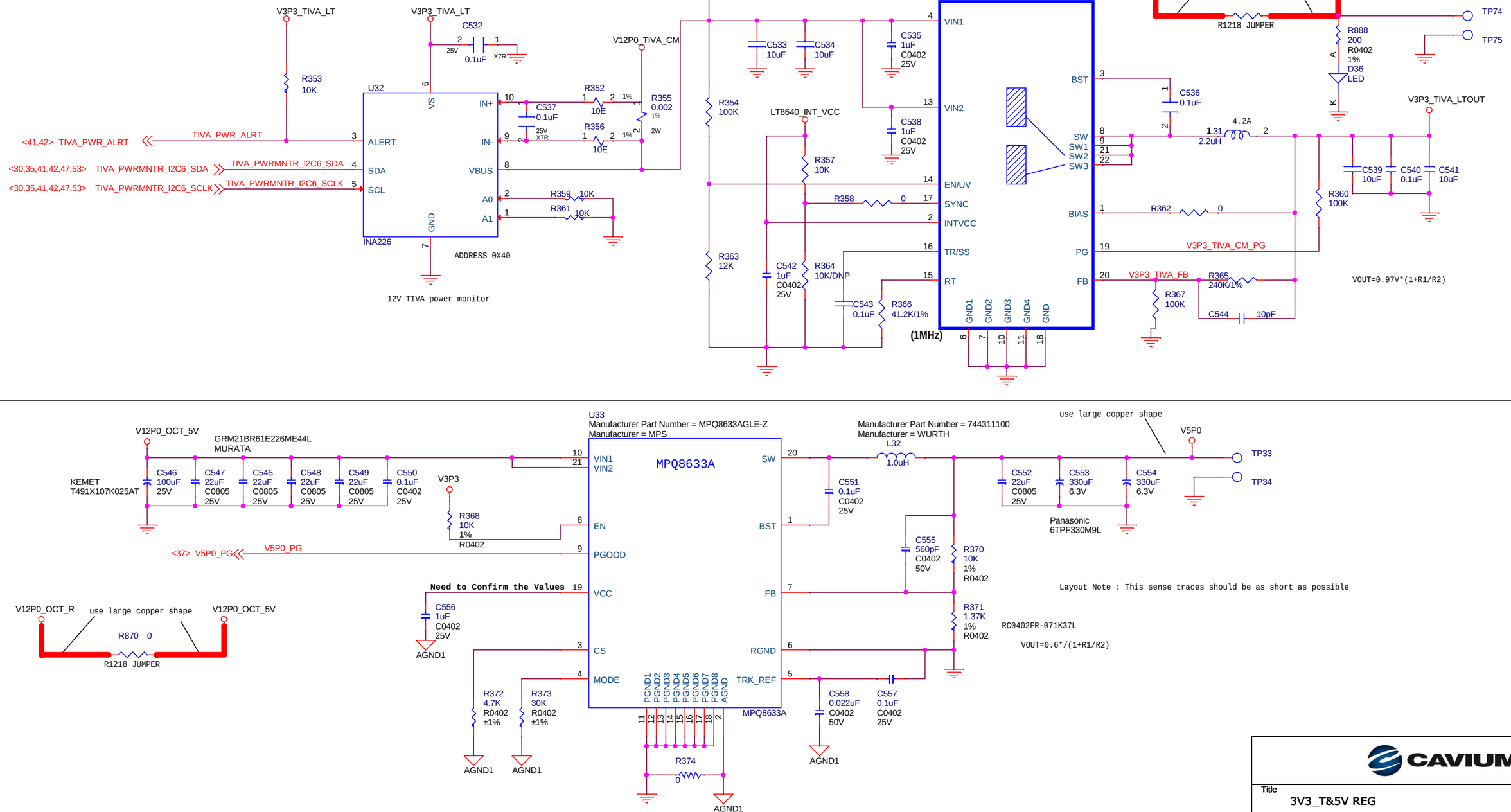
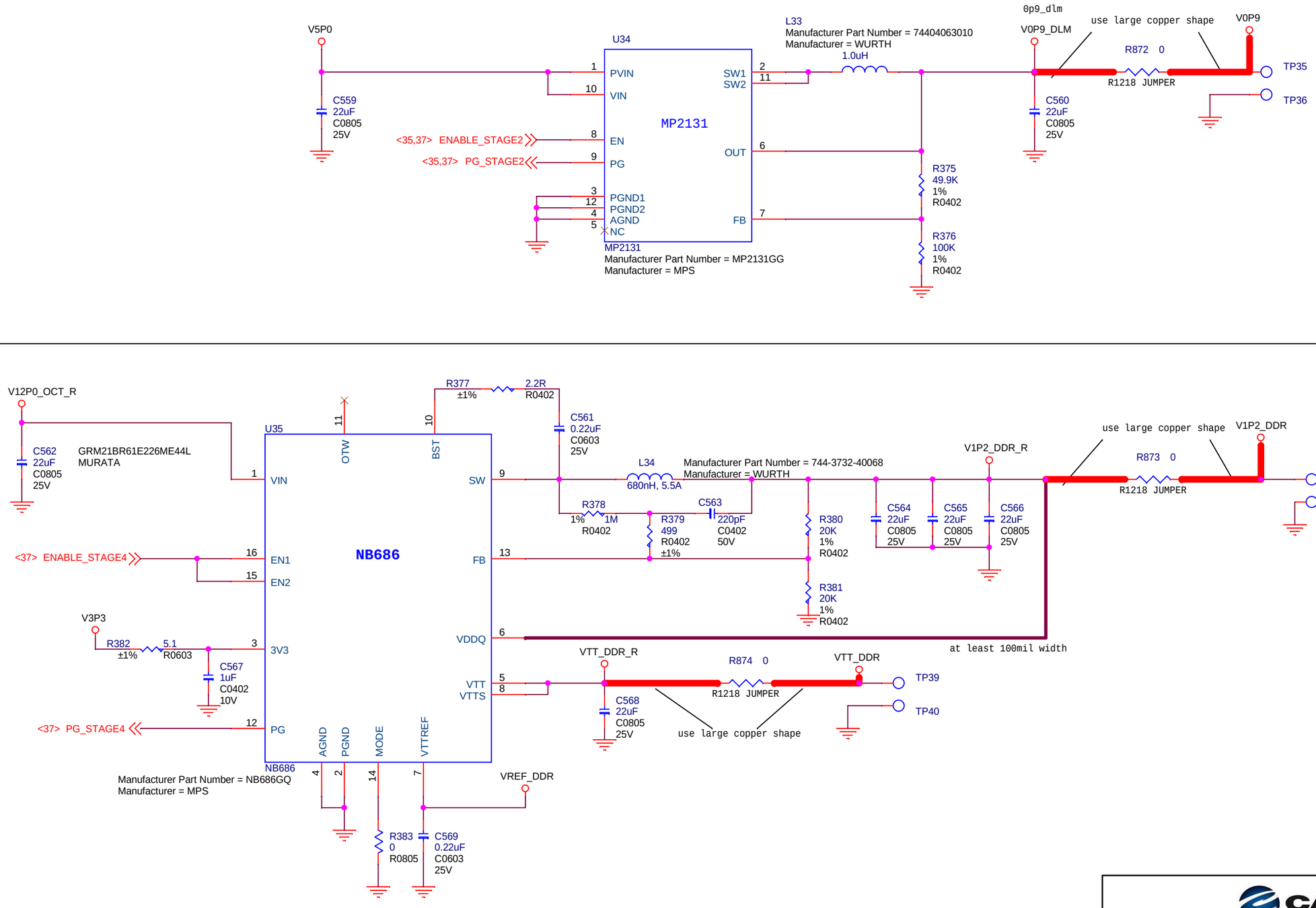


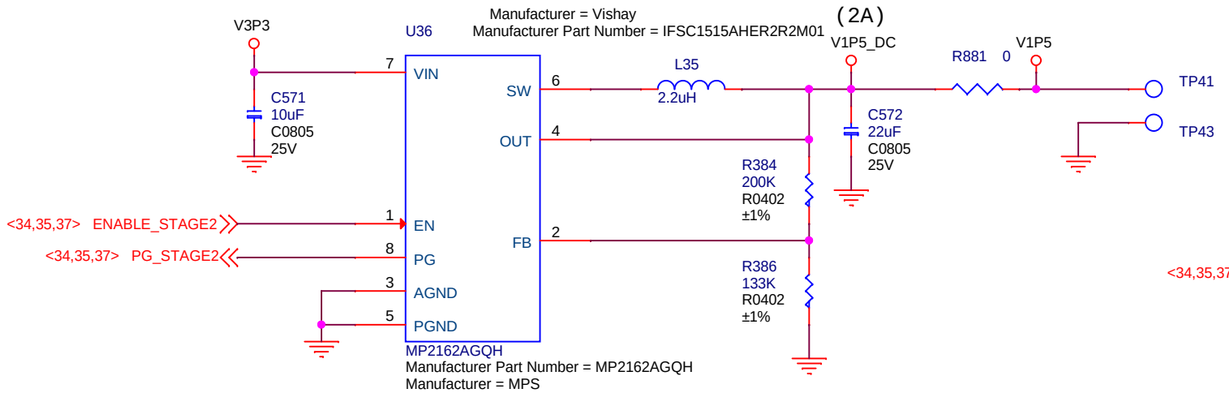
CAVIUM

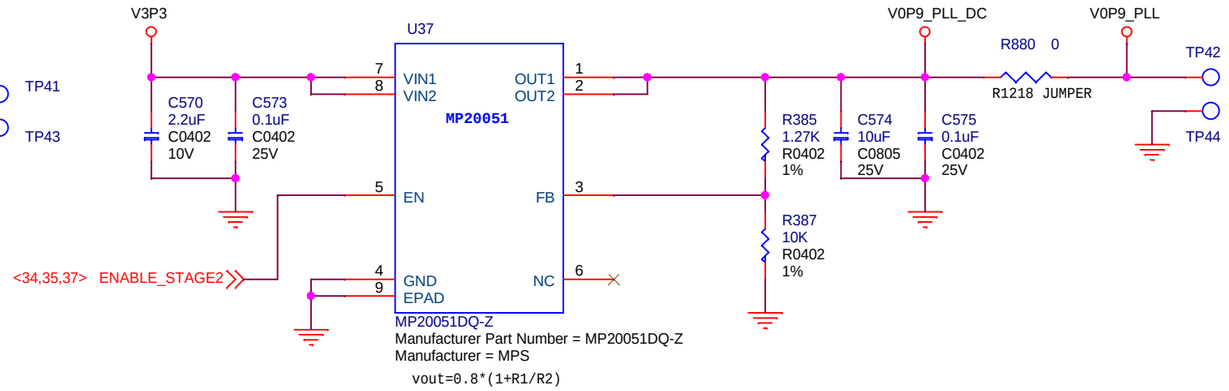
Title: 3V3_T&5V REG		
Size: Custom	Document Number	Rev: 1.0
Date: Monday, October 15, 2018	Sheet 33 of 54	

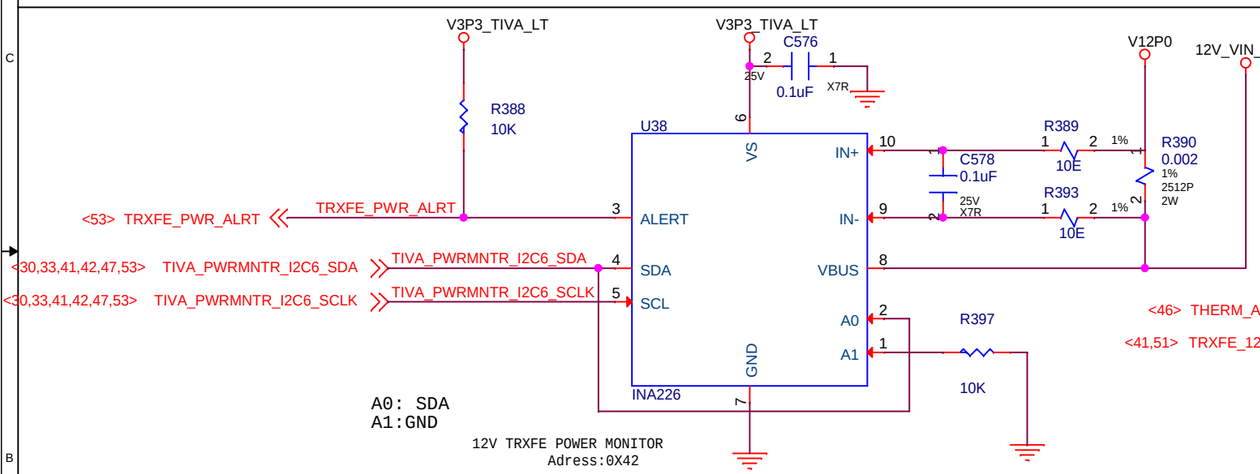


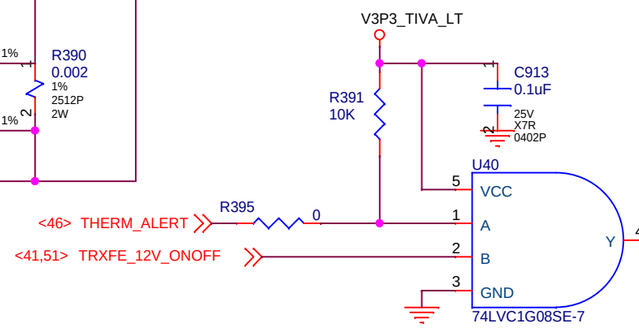
CAVIUM

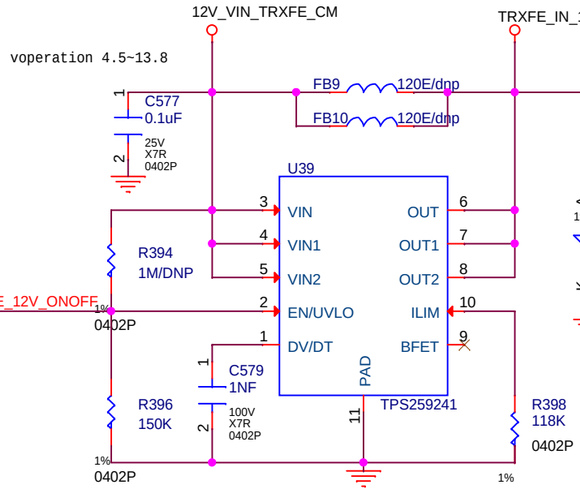
Title: V0P9_DLM&V1P2_DDR		
Size: B	Document Number: <Doc>	Rev: 1.0
Date: Monday, October 15, 2018	Sheet 34 of 54	

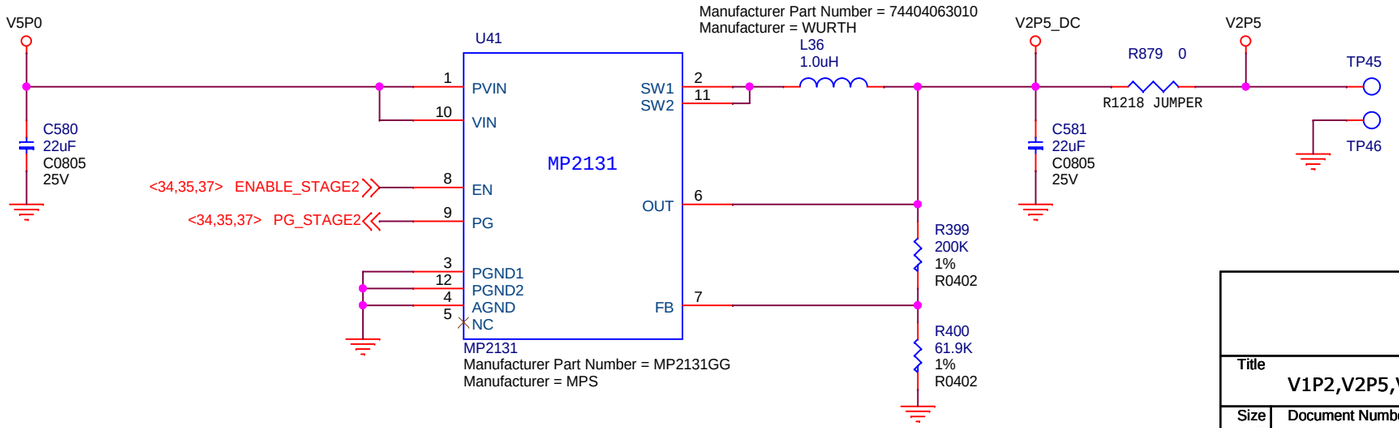


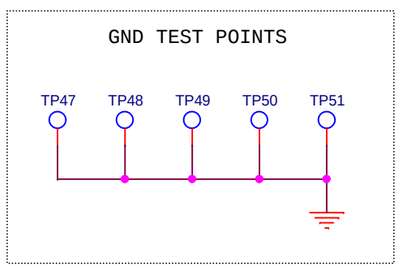












CAVIUM

Title: V1P2,V2P5,V0P9_PLL		
Size: B	Document Number: <Doc>	Rev: 1.0
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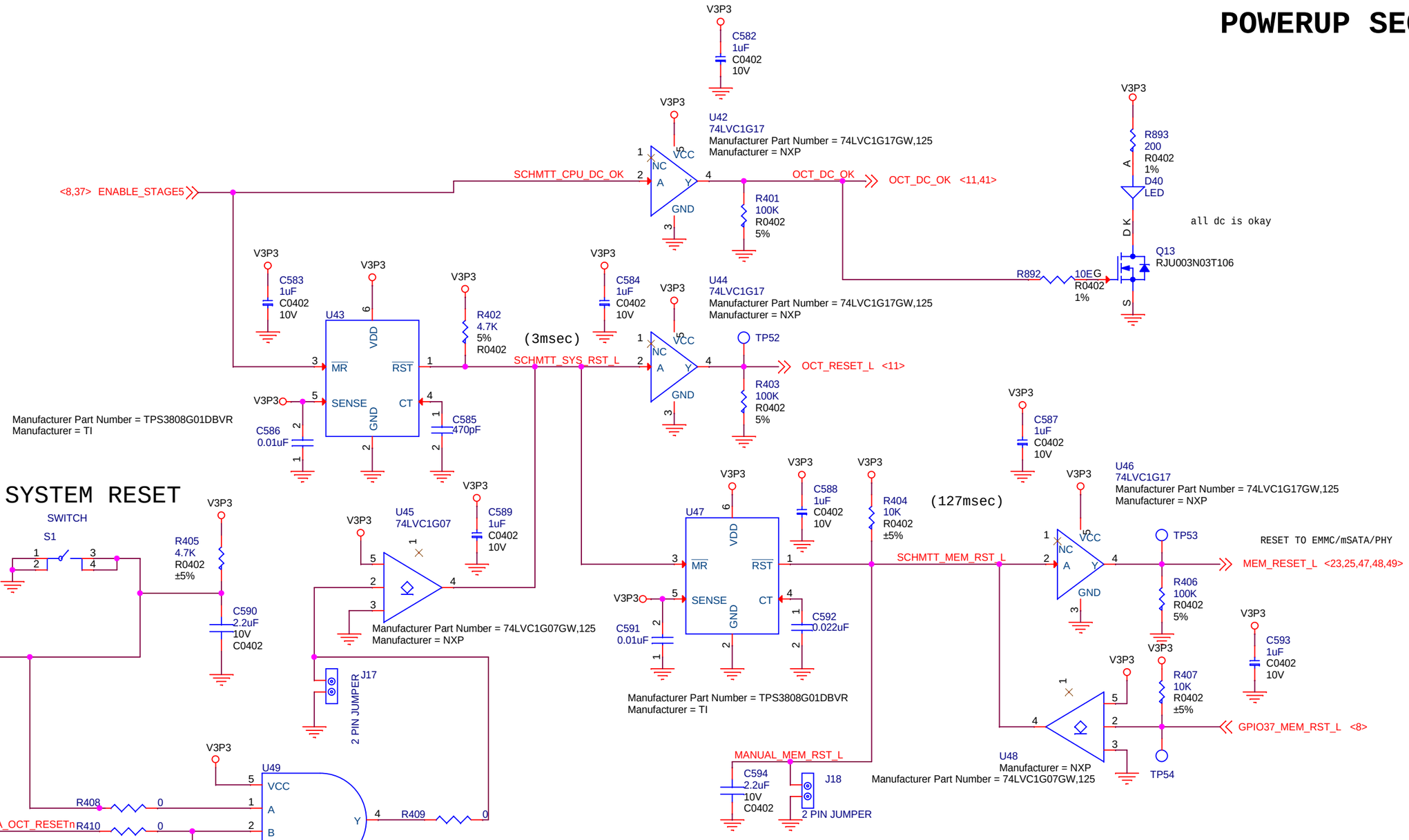
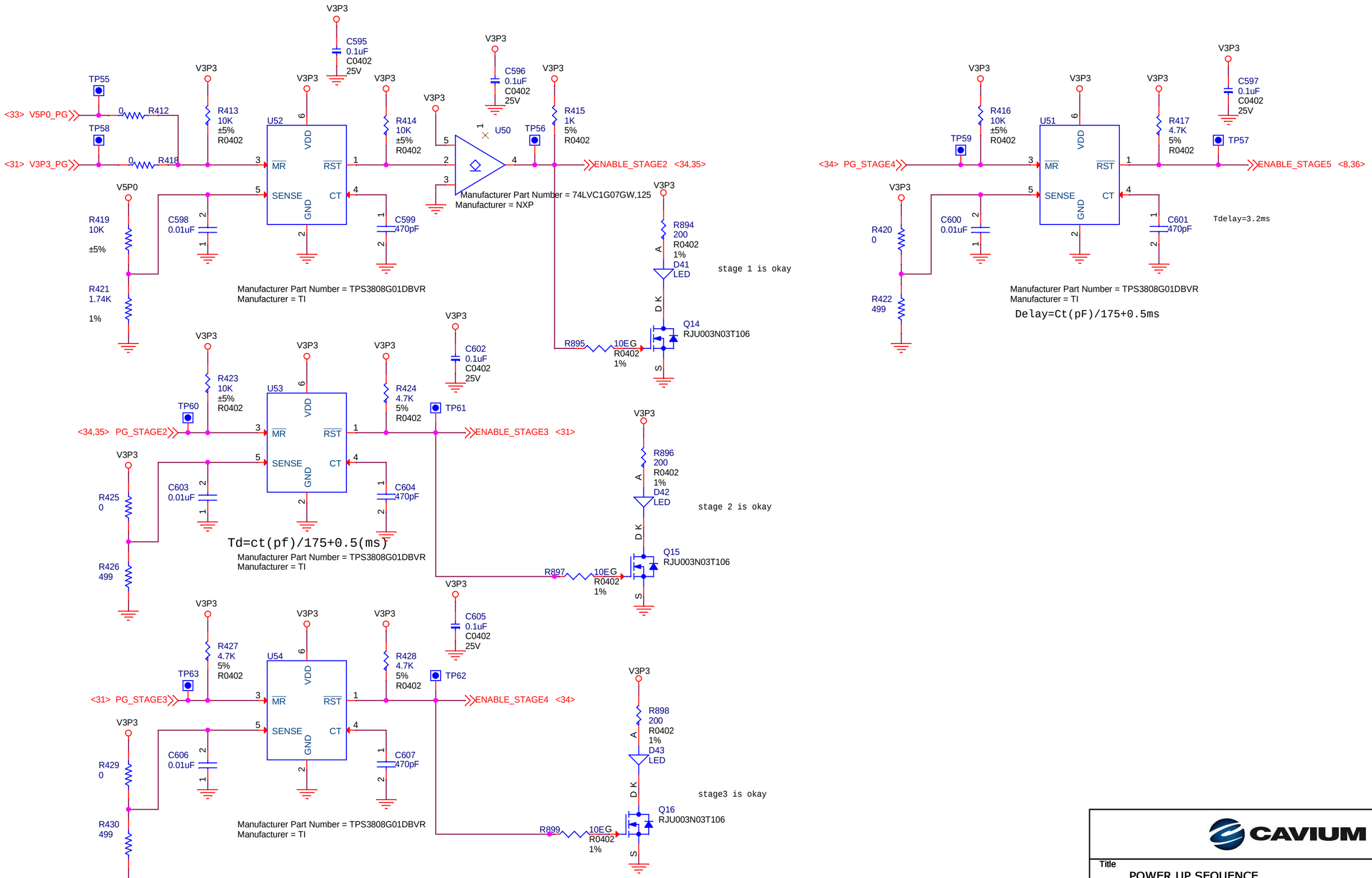
POWERUP SEQUENCE



MANUAL SYSTEM RESET

MANUAL IF RESET

CAVIUM		
Title: POWER AND RESET		
Size: B	Document Number	Rev: 1.0
Date: Monday, October 15, 2018	Sheet 36 of 54	



CAVIUM

Title: POWER UP SEQUENCE		
Size: B	Document Number	Rev: 1.0
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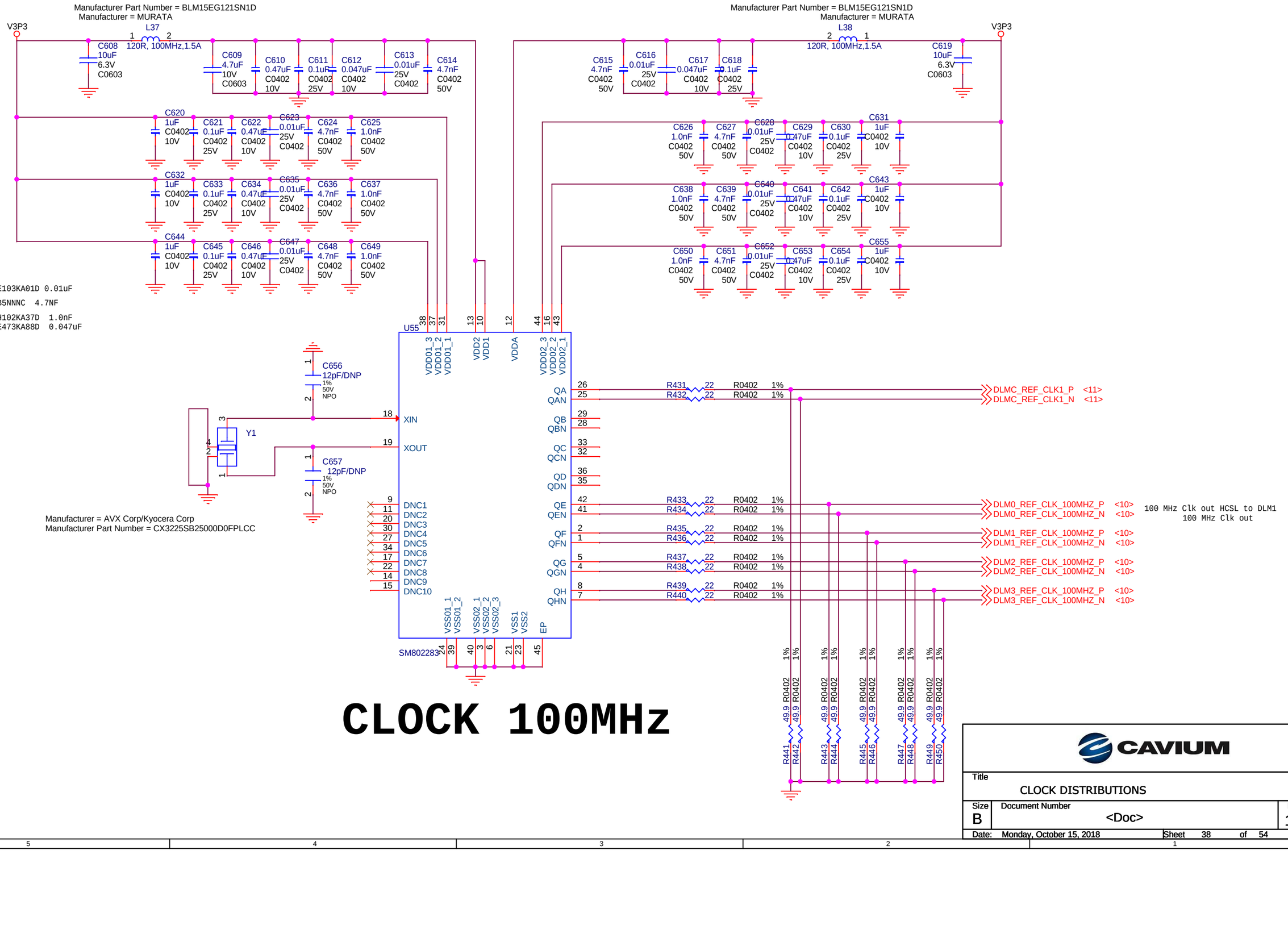
Manufacturer Part Number = BLM15EG121SN1D
Manufacturer = MURATA
L37
120R, 100MHz,1.5A
V3P3
C608 10uF 6.3V C0603
C609 4.7uF 10V C0603
C610 0.47uF C0402 10V
C611 0.1uF C0402 25V
C612 0.047uF C0402 10V
C613 0.01uF 25V C0402
C614 4.7nF C0402 50V
C620 1uF C0402 10V
C621 0.1uF C0402 25V
C622 0.47uF C0402 10V
C623 0.01uF 25V C0402
C624 4.7nF C0402 50V
C625 1.0nF C0402 50V
C632 1uF C0402 10V
C633 0.1uF C0402 25V
C634 0.47uF C0402 10V
C635 0.01uF 25V C0402
C636 4.7nF C0402 50V
C637 1.0nF C0402 50V
C644 1uF C0402 10V
C645 0.1uF C0402 25V
C646 0.47uF C0402 10V
C647 0.01uF 25V C0402
C648 4.7nF C0402 50V
C649 1.0nF C0402 50V
GRM155R71E103KA01D 0.01uF
CL05B472JB5NNNC 4.7NF
GCM155R71H102KA37D 1.0nF
GRM155R71E473KA88D 0.047uF
Manufacturer Part Number = BLM15EG121SN1D
Manufacturer = MURATA
L38
120R, 100MHz,1.5A
V3P3
C615 4.7nF C0402 50V
C616 0.01uF 25V C0402
C617 0.047uF C0402 10V
C618 0.1uF C0402 25V
C619 10uF 6.3V C0603
C626 1.0nF C0402 50V
C627 4.7nF C0402 50V
C628 0.01uF 25V C0402
C629 0.47uF C0402 10V
C630 0.1uF C0402 25V
C631 1uF C0402 10V
C638 1.0nF C0402 50V
C639 4.7nF C0402 50V
C640 0.01uF 25V C0402
C641 0.47uF C0402 10V
C642 0.1uF C0402 25V
C643 1uF C0402 10V
C650 1.0nF C0402 50V
C651 4.7nF C0402 50V
C652 0.01uF 25V C0402
C653 0.47uF C0402 10V
C654 0.1uF C0402 25V
C655 1uF C0402 10V
U55
SM802283
VDD01_3 38
VDD01_2 37
VDD01_1 31
VDD2 13
VDD1 10
VDDA 12
VDD02_3 44
VDD02_2 16
VDD02_1 43
C656 12pF/DNP 1% 50V NPO
C657 12pF/DNP 1% 50V NPO
Y1
XIN 18
XOUT 19
Manufacturer = AVX Corp/Kyocera Corp
Manufacturer Part Number = CX3225SB25000D0FPLCC
DNC1 9
DNC2 11
DNC3 20
DNC4 30
DNC5 27
DNC6 34
DNC7 17
DNC8 22
DNC9 14
DNC10 15
QA 26
QAN 25
QB 29
QBN 28
QC 33
QCN 32
QD 36
QDN 35
QE 42
QEN 41
QF 2
QFN 1
QG 5
QGN 4
QH 8
QHN 7
R431 22 R0402 1%
R432 22 R0402 1%
R433 22 R0402 1%
R434 22 R0402 1%
R435 22 R0402 1%
R436 22 R0402 1%
R437 22 R0402 1%
R438 22 R0402 1%
R439 22 R0402 1%
R440 22 R0402 1%
R441 49.9 R0402 1%
R442 49.9 R0402 1%
R443 49.9 R0402 1%
R444 49.9 R0402 1%
R445 49.9 R0402 1%
R446 49.9 R0402 1%
R447 49.9 R0402 1%
R448 49.9 R0402 1%
R449 49.9 R0402 1%
R450 49.9 R0402 1%
VSS01_1 24
VSS01_2 39
VSS02_1 40
VSS02_2 3
VSS02_3 6
VSS1 21
VSS2 23
EP 45
DLMC_REF_CLK1_P <11>
DLMC_REF_CLK1_N <11>
DLM0_REF_CLK_100MHZ_P <10>
DLM0_REF_CLK_100MHZ_N <10>
100 MHz Clk out HCSL to DLM1
100 MHz Clk out
DLM1_REF_CLK_100MHZ_P <10>
DLM1_REF_CLK_100MHZ_N <10>
DLM2_REF_CLK_100MHZ_P <10>
DLM2_REF_CLK_100MHZ_N <10>
DLM3_REF_CLK_100MHZ_P <10>
DLM3_REF_CLK_100MHZ_N <10>
CLOCK 100MHz
CAVIUM
Title
CLOCK DISTRIBUTIONS
Size B
Document Number <Doc>
Rev 1.0
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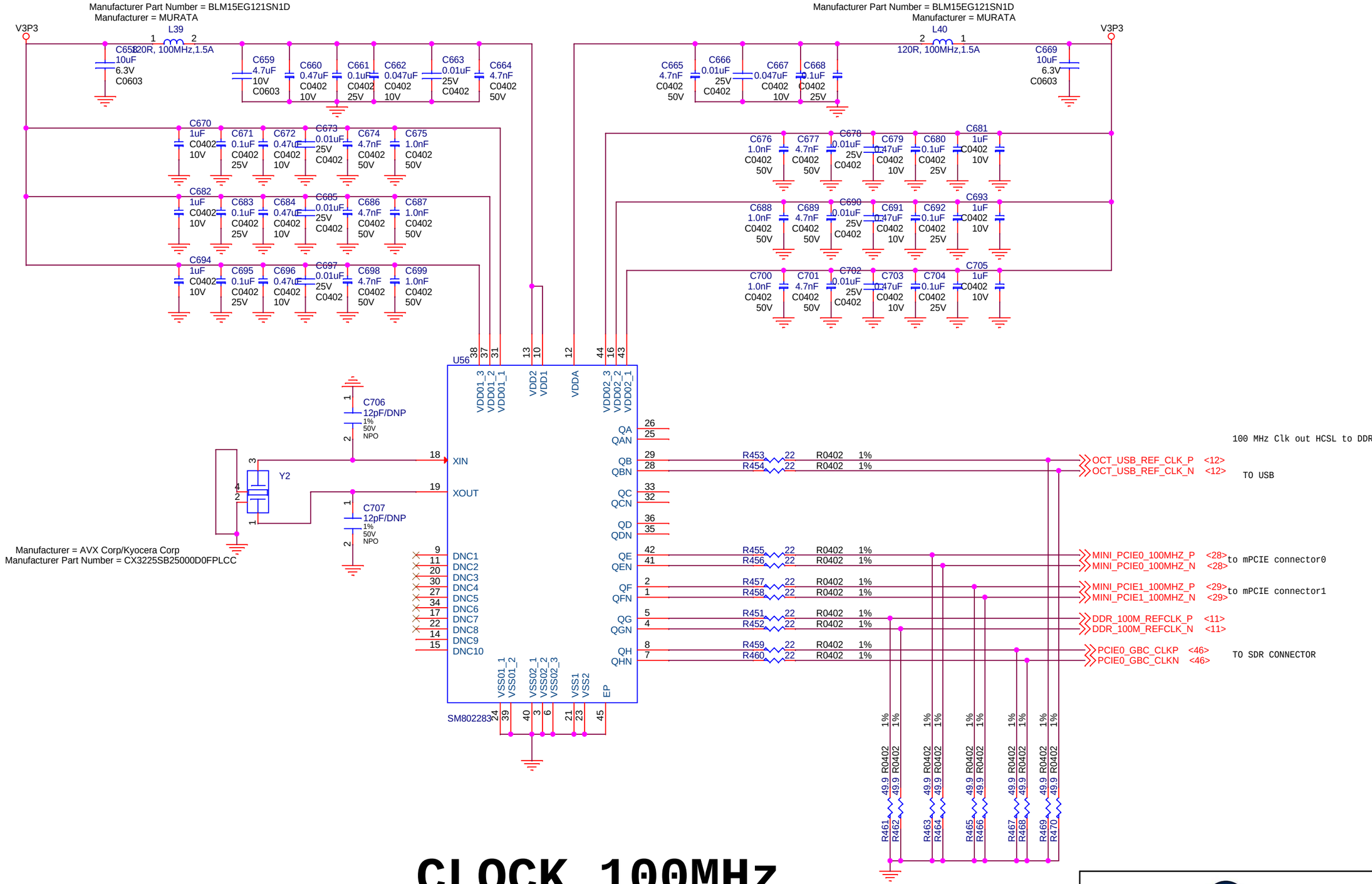

CLOCK 100MHz

CAVIUM

Title: CLOCK DISTRIBUTIONS		
Size: B	Document Number: <Doc>	Rev: 1.0
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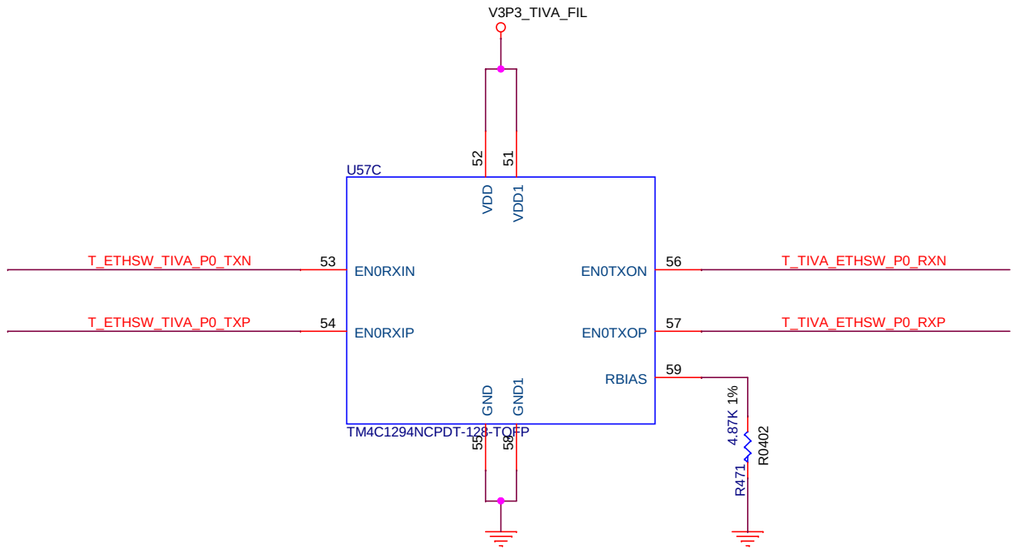

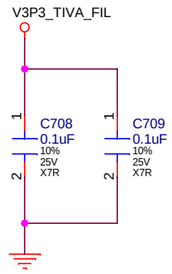

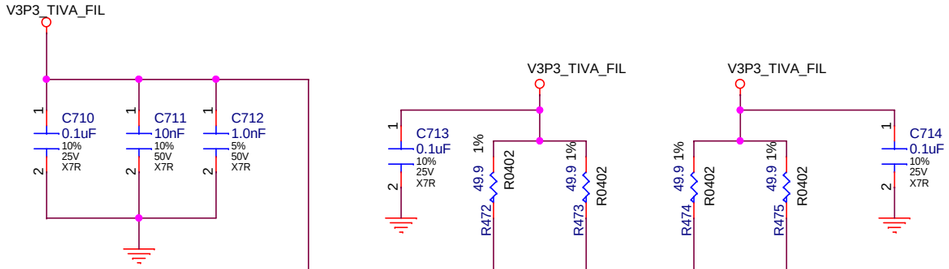

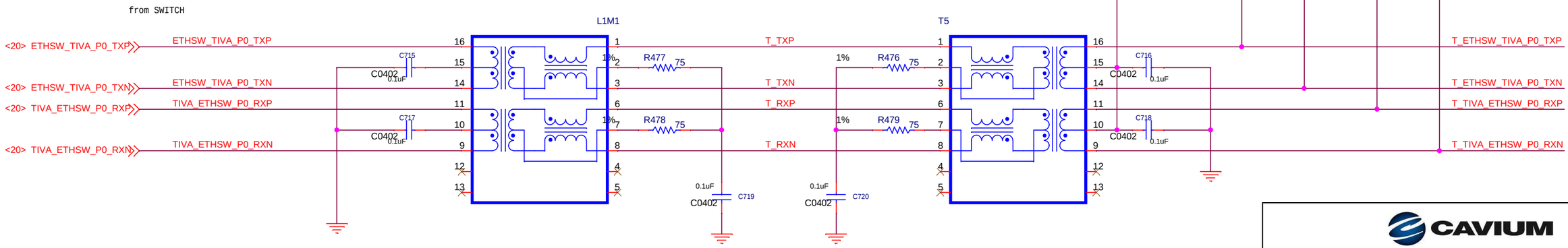

CAVIUM

Title: TIVA ETHERNET		
Size: Custom	Document Number: <Doc>	Rev: 1.0
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UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 0402 PACKAGE, POWER RATING < 0.5W & TOLERANCE > 1%
CAPACITORS ARE 0402 PACKAGE & TOLERANCE OF 10%

U57A

TM4C1294NCPDT-128-TQFP

PA0/U0RX	33	TIVA_DEBUG_RX	R487	22	TIVA_DEBUG_RX	<43>	TIVA_DEBUG_RX
PA1/U0TX	34	TIVA_DEBUG_TX	R481	22	TIVA_DEBUG_TX	<43>	TIVA_DEBUG_TX
PA2/SSI0CLK	35	TIVA_PSE_I2C8_SCLK	R488	22	TIVA_PSE_I2C8_SCLK	<45,46,50>	TIVA_PSE_I2C8_SCLK
PA3/SSI0FSS	36	TIVA_PSE_I2C8_SDA	R482	22	TIVA_PSE_I2C8_SDA	<45,46,50>	TIVA_PSE_I2C8_SDA
PA4/SSI0XDAT0	37	TIVA_OCT_UART3_RX	R491	22	TIVA_OCT_UART3_RX	<27>	TIVA_OCT_UART3_RX
PA5/SSI0XDAT1	38	TIVA_OCT_UART3_TX	R484	22	TIVA_OCT_UART3_TX	<27>	TIVA_OCT_UART3_TX
PA6	40	TIVA_PWRMNTR_I2C6_SCLK	R494	22	TIVA_PWRMNTR_I2C6_SCLK	<30,33,35,42,47,53>	TIVA_PWRMNTR_I2C6_SCLK
PA7	41	TIVA_PWRMNTR_I2C6_SDA	R495	22	TIVA_PWRMNTR_I2C6_SDA	<30,33,35,42,47,53>	TIVA_PWRMNTR_I2C6_SDA
PC0/TCK/SWCLK	100	TIVA_JTAG_TCK	R498	22	TIVA_JTAG_TCK	<43>	TIVA_JTAG_TCK
PC1/TMS/SWDIO	99	TIVA_JTAG_TMS	R499	22	TIVA_JTAG_TMS	<43>	TIVA_JTAG_TMS
PC2/TDI	98	TIVA_JTAG_TDI	R501	22	TIVA_JTAG_TDI	<43>	TIVA_JTAG_TDI
PC3/TDO/SWO	97	TIVA_JTAG_TDO	R485	22	TIVA_JTAG_TDO	<43>	TIVA_JTAG_TDO
PC4/C1-	25	SYNCCONN_TIVA_UART_RX	R503	22	SYNCCONN_TIVA_UART_RX	<46>	SYNCCONN_TIVA_UART_RX
PC5/C1+	24	TIVA_SYNCCONN_UART_TX	R486	22	TIVA_SYNCCONN_UART_TX	<46>	TIVA_SYNCCONN_UART_TX
PC6/C0+	23	OCT_THERMAL_TRIP_L	R506	22	OCT_THERMAL_TRIP_L	<11>	OCT_THERMAL_TRIP_L
PC7/C0-	22	V2_BACK_ON	R507	22	V2_BACK_ON	<30>	V2_BACK_ON
PE0/AIN3	15	IOEXP_TIVA_INT				<53>	IOEXP_TIVA_INT
PE1/AIN2	14	FE_12V_CTRL				<46>	FE_12V_CTRL
PE2/AIN1	13	TIVA_OCT_GPIO1	R512	0	TIVA_OCT_GPIO1	<8>	TIVA_OCT_GPIO1
PE3/AIN0	12	TIVA_OCT_GPIO2	R514	0	TIVA_OCT_GPIO2	<8>	TIVA_OCT_GPIO2
PE4/AIN9	123	TIVA_FLASH_MOSI	R515	0	TIVA_FLASH_MOSI	<44>	TIVA_FLASH_MOSI
PE5/AIN8	124	TIVA_FLASH_MISO	R516	0	TIVA_FLASH_MISO	<44>	TIVA_FLASH_MISO
PG0	49	TIVA_TEMPSEN_I2C1_SCLK	R518	22	TIVA_TEMPSEN_I2C1_SCLK	<50>	TIVA_TEMPSEN_I2C1_SCLK
PG1	50	TIVA_TEMPSEN_I2C1_SDA	R519	22	TIVA_TEMPSEN_I2C1_SDA	<50>	TIVA_TEMPSEN_I2C1_SDA
PJ0	116	CFG_IOEXP_TIVA_INT				<53>	CFG_IOEXP_TIVA_INT
PJ1	117	OCT_PWR_ALRT	R520	22	OCT_PWR_ALRT	<30>	OCT_PWR_ALRT
PL0	81	TIVA_TRXFECONN_I2C2_SDA	R521	22	TIVA_TRXFECONN_I2C2_SDA	<51,52>	TIVA_TRXFECONN_I2C2_SDA
PL1	82	TIVA_TRXFECONN_I2C2_SCLK	R523	22	TIVA_TRXFECONN_I2C2_SCLK	<51,52>	TIVA_TRXFECONN_I2C2_SCLK
PL2	83					<48>	MSATA1_TIVA_DAS
PL3	84	TIVA_OCT_GPIO3				<8>	TIVA_OCT_GPIO3
PL4	85	TIVA_OCT_GPIO4				<8>	TIVA_OCT_GPIO4
PL5	86	TIVA_GPIO_PL5	R527	22	TIVA_GPIO_PL5	<22>	TIVA_GPIO_PL5
PL6/USB0DP	94	TIVA_USB0_DP	R529	22	TIVA_USB0_DP	<23>	TIVA_USB0_DP
PL7/USB0DM	93	TIVA_USB0_DM	R530	22	TIVA_USB0_DM	<23>	TIVA_USB0_DM
PN0	107	ETHSW_INT_TIVA				<20>	ETHSW_INT_TIVA
PN1	108	TIVA_TRXFECONN_GPIO5	R533	0	TIVA_TRXFECONN_GPIO5	<46>	BB_SENSOR_ALERT
PN2	109	TIVA_TRXFECONN_GPIO1	R535	0	TIVA_TRXFECONN_GPIO1	<51>	TIVA_TRXFECONN_GPIO1
PN3	110	TIVA_TRXFECONN_GPIO2	R536	0	TIVA_TRXFECONN_GPIO2	<51>	TIVA_TRXFECONN_GPIO2
PN4	111	TIVA_TRXFECONN_GPIO3	R538	0	TIVA_TRXFECONN_GPIO3	<51>	TIVA_TRXFECONN_GPIO3
PN5	112	TIVA_MODULE_UART1_RIN		0		<46>	TIVA_MODULE_UART1_RIN
PQ0	5	TIVA_TRXFECONN_RESET	R541	0			
PQ1	6	MSATA0_TIVA_DAS				<47>	MSATA0_TIVA_DAS
PQ2	11	SATA_PWR_ALERT				<47>	SATA_PWR_ALERT
PQ3	27	TIVA_RESET_TO_PROC	R544	22	TIVA_RESET_TO_PROC	<44>	TIVA_RESET_TO_PROC
PQ4	102	TIVA_SYNC_RESET	R545	22	TIVA_SYNC_RESET	<44>	TIVA_SYNC_RESET

PB0/USB0ID	95	TIVA_USB_ID					
PB1/USB0VBUS	96			22			
PB2/I2C0SCL	91	R489	22		TIVA_I2C0_SCLK	<20,31>	TIVA_I2C0_SCLK
PB3/I2C0SDA	92	R483	22		TIVA_I2C0_SDA	<20,31>	TIVA_I2C0_SDA
PB4/AIN10	121	R492	22		TIVA_FLASH_nCS	<44>	TIVA_FLASH_nCS
PB5/AIN11	120	R493	22		TIVA_FLASH_CLK	<44>	TIVA_FLASH_CLK
			22				
PD0/AIN15	1	R496	22		TIVA_I2C7_SCL	<43>	TIVA_I2C7_SCL
PD1/AIN14	2	R497	22		TIVA_I2C7_SDA	<43>	TIVA_I2C7_SDA
PD2/AIN13	3				BUZZER_ON	<43>	BUZZER_ON
PD3/AIN12	4	R500	22		LIGHT_SENSE_INT		LIGHT_SENSE_INT <50>
PD4/AIN7	125	R939	22		TRXFE_DET		TRXFE_DET <42,46>
PD5/AIN6	126	R914	20E		UART_SEL		UART_SEL <8,27>
PD6/AIN5	127				TPM_INT_REQ		TPM_INT_REQ <52>
PD7/AIN4	128	R505	20		SYNC_TIVA_INT		SYNC_TIVA_INT <46>
PF0	42	R508	22		TIVA_JTAG_TRD2	<43>	TIVA_JTAG_TRD2
PF1	43	R509	22		TIVA_JTAG_TRD1	<43>	TIVA_JTAG_TRD1
PF2	44	R510	22		TIVA_JTAG_TRD0	<43>	TIVA_JTAG_TRD0
PF3	45	R511	22		TIVA_JTAG_TRCLK	<43>	TIVA_JTAG_TRCLK
PF4	46	R513	22		TIVA_JTAG_TRD3	<43>	TIVA_JTAG_TRD3
			22				
PH0	29				TIVA_GPIO_PH0		
PH1	30				MSATA_PWR_EN		MSATA_PWR_EN <47>
PH2	31	R517	22		OCT_12V_ONOFF		OCT_12V_ONOFF <30>
PH3	32				TIVA_PWR_ALRT		TIVA_PWR_ALRT <33,42>
PK0/AIN16	18				TIVA_UART4_RXD		
PK1/AIN17	19				TIVA_UART4_TXD		TIVA_UART4_RXD <46>
PK2/AIN18	20				TIVA_UART4_RTS		TIVA_UART4_TXD <46>
PK3/AIN19	21				TIVA_UART4_CTS		TIVA_UART4_RTS <46>
PK4	63	R522	22		TIVA_TRXFECONN_I2C3_SCLK		TIVA_UART4_CTS <46>
PK5	62	R524	22		TIVA_TRXFECONN_I2C3_SDA		TIVA_I2C3_SCLK <46>
PK6	61	R525	22		TIVA_TRXFECONN_I2C4_SCLK		TIVA_I2C3_SDA <46>
PK7	60	R526	22		TIVA_TRXFECONN_I2C4_SDA		TIVA_TRXFECONN_I2C4_SCLK <46>
			22				TIVA_TRXFECONN_I2C4_SDA <46>
PM0	78				TPM_I2C_MUX_SEL		
PM1	77				LED_TIVA_GPIO		TPM_I2C_MUX_SEL <52>
PM2	76	R531	22		TIVA_FE_RESET_OUT		LED_TIVA_GPIO <43>
PM3	75		22		VRM_ALERT#		TIVA_FE_RESET_OUT <44>
PM4	74	R532	22		TIVA_TRXFECONN_GPIO6		VRM_ALERT# <31>
PM5	73	R534	22		TIVA_ETHSW_RESET		TRXFE_SENSOR_ALERT <46>
PM6	72		0		TIVA_GPIO_PM6		TIVA_ETHSW_RESET <44>
PM7	71	R537	22		WD_INPUT		TIVA_GPIO_PM6 <22>
							WD_INPUT <44>
PP0/C2+	118	R539	22		TIVA_UART6_RX		
PP1/C2-	119	R540	22		TIVA_UART6_TX		TIVA_UART6_RX <22>
PP2	103	R542	22		TRXFE_12V_ONOFF		TIVA_UART6_TX <22>
PP3	104	R913	22		OCT_DC_OK		TRXFE_12V_ONOFF <35,51>
PP4	105	R543	22		TIVA_TRXFE_RESET		OCT_DC_OK <11,36>
PP5	106		22		TIVA_DEBUG		TIVA_TRXFE_RESET <44>

V3P3_TIVA
R490 10K/DNP
NM
TIVA_USB_ID
FE_12V_CTRL
R502 10K
R504 10K

V5_USB_TIVA
R945 10K/DNP 5% 1/10W
R480 10K 5% 1/10W

V3P3_TIVA
R528 10K
TIVA_MODULE_UART1_RIN

V3P3_TIVA
R548 2.2K 1%
R549 2.2K 1%
R550 2.2K 1%
R551 2.2K 1%
R552 2.2K 1%
R553 2.2K 1%
R920 2.2K 1%
R921 2.2K 1%
TIVA_I2C7_SCL
TIVA_I2C7_SDA
TIVA_TRXFECONN_I2C3_SCLK
TIVA_TRXFECONN_I2C3_SDA
TIVA_TRXFECONN_I2C4_SCLK
TIVA_TRXFECONN_I2C4_SDA
TIVA_TRXFECONN_I2C2_SCLK
TIVA_TRXFECONN_I2C2_SDA

V3P3_TIVA_LT
R546 10K
<46> TRXFECONN_RESET
K D18 A
PMEG3010ER,115
TIVA_TRXFECONN_RESET

V3P3_TIVA
R554 2.2K 1%
R555 2.2K 1%
R556 2.2K 1%
R557 2.2K 1%
R558 2.2K 1%
R559 2.2K 1%
R560 2.2K 1%
R561 2.2K 1%
TIVA_PWRMNTR_I2C6_SDA
TIVA_PWRMNTR_I2C6_SCLK
TIVA_I2C0_SCLK
TIVA_I2C0_SDA
TIVA_TEMPSEN_I2C1_SCLK
TIVA_TEMPSEN_I2C1_SDA
TIVA_PSE_I2C8_SCLK
TIVA_PSE_I2C8_SDA

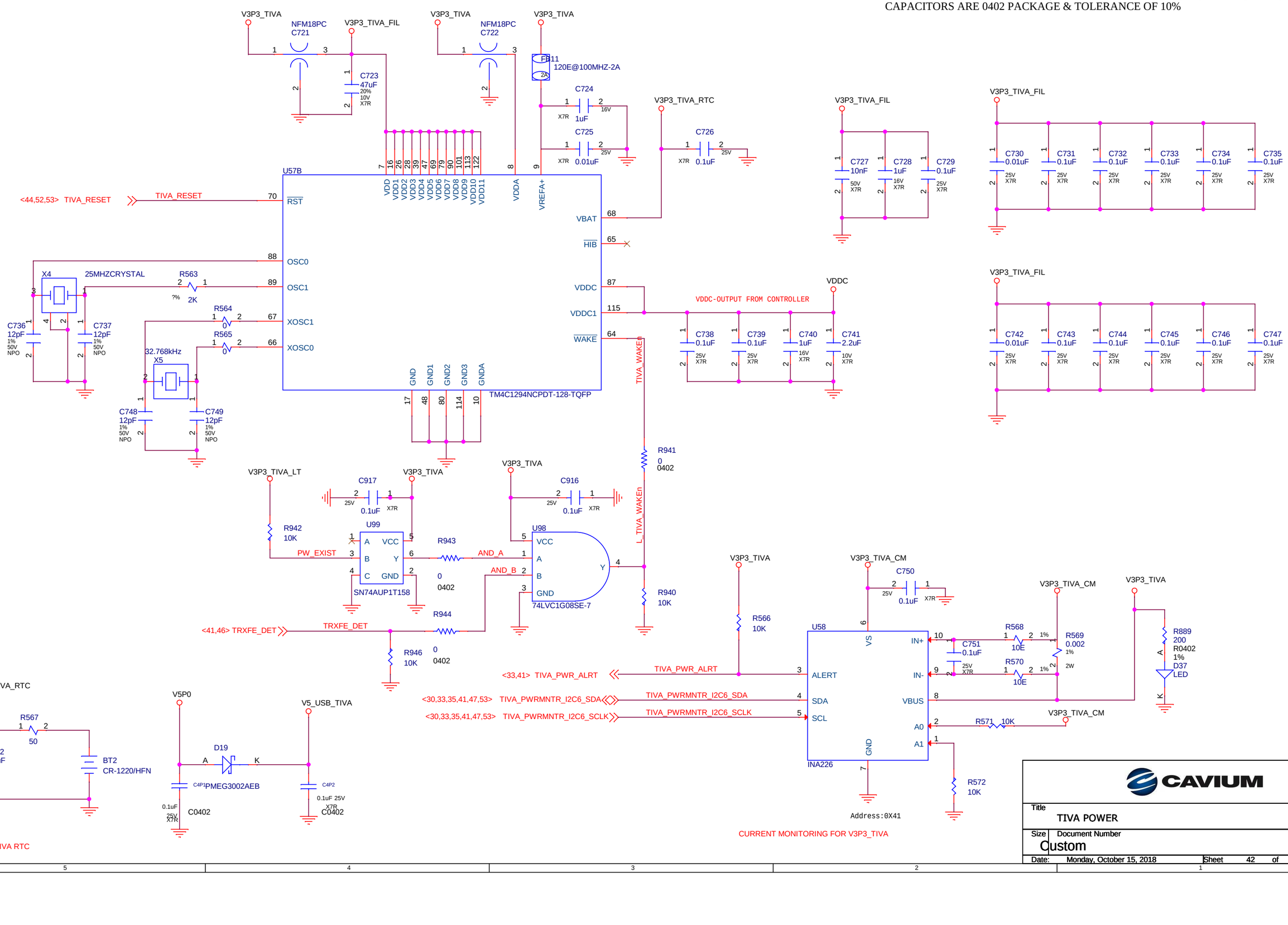
MH14 MH14 place 2inch away from J29
Mounting_Hole
A6
Custom Board Spacer
9774070243R
J29 V3P3_TIVA
1 2 3 4 5 6
TIVA_GPIO_PH0
TIVA_I2C0_SCLK
TIVA_I2C0_SDA
91601-306LF

V3P3_TIVA
R547 1K
JP1 1 2
826926-2
TIVA_DEBUG
R562 10K

CAVIUM

Title	TIVA IO'S		
Size	Document Number	<Doc>	Rev
Custom			1.0
Date:	Monday, October 15, 2018	Sheet 41 of 54	

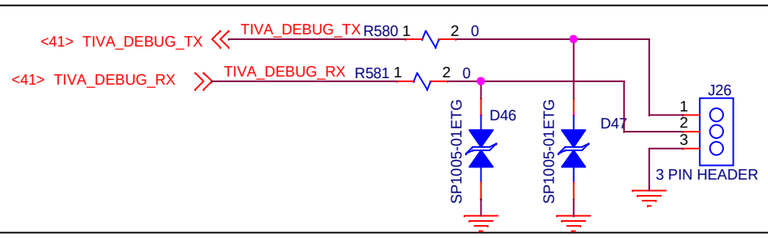
UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 0402 PACKAGE, POWER RATING < 0.5W & TOLERANCE > 1%
CAPACITORS ARE 0402 PACKAGE & TOLERANCE OF 10%

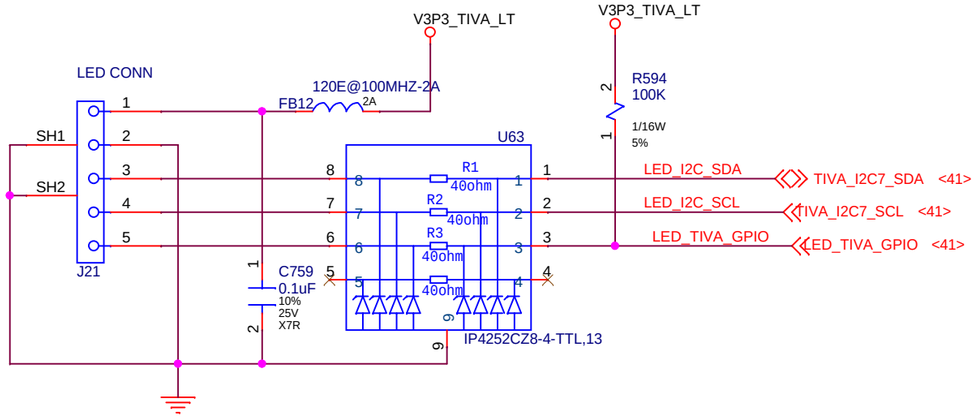


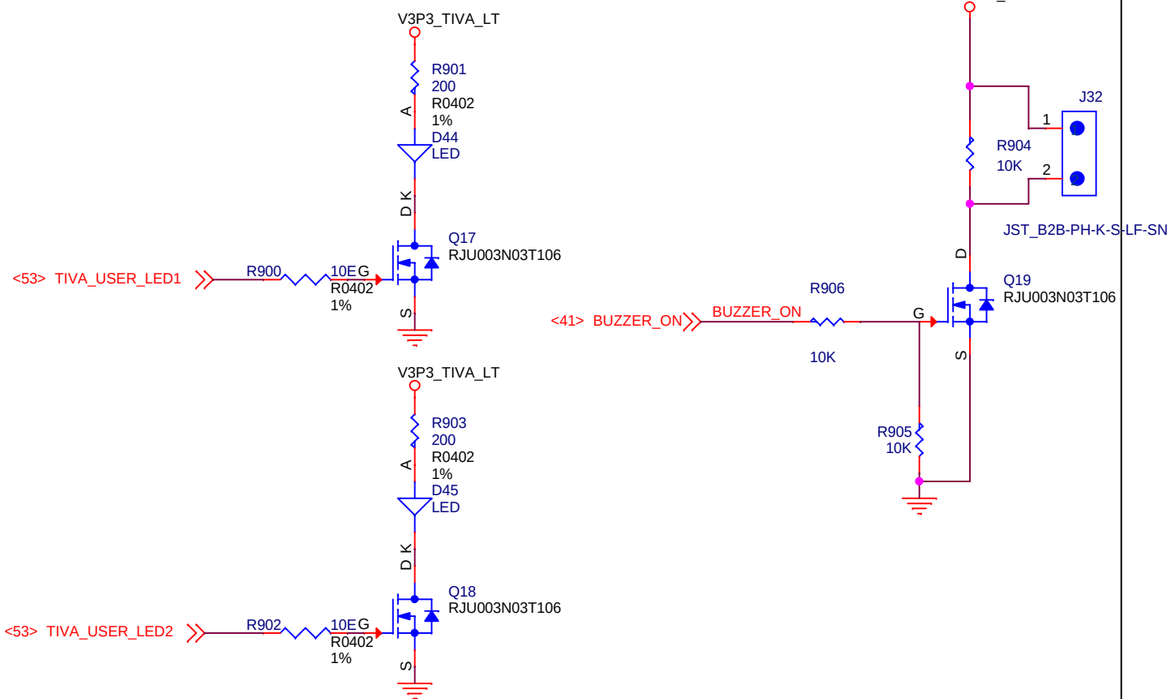
Title: TIVA POWER

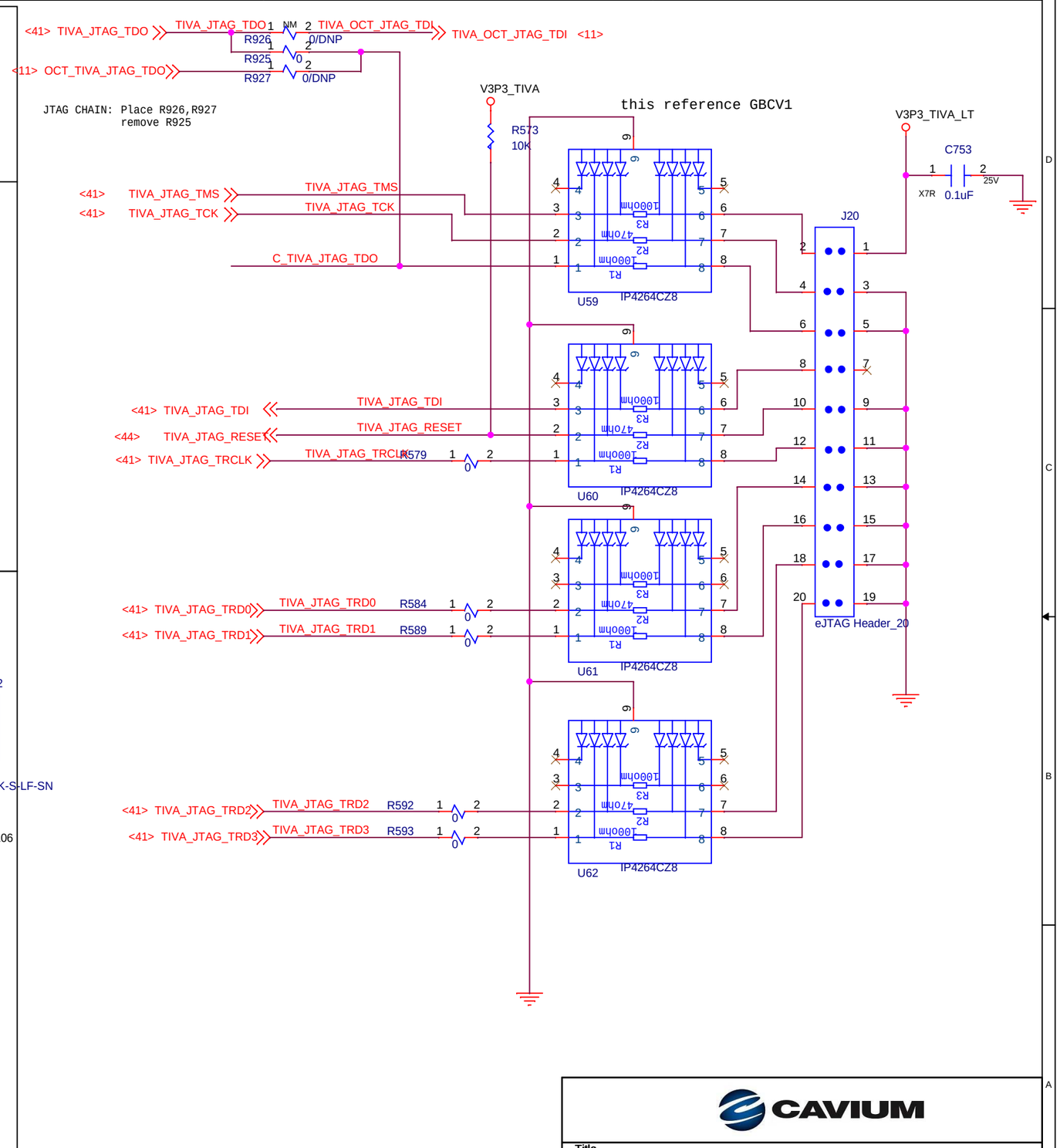
Size: Custom | Document Number | Rev: 1.0

Date: Monday, October 15, 2018 | Sheet 42 of 54



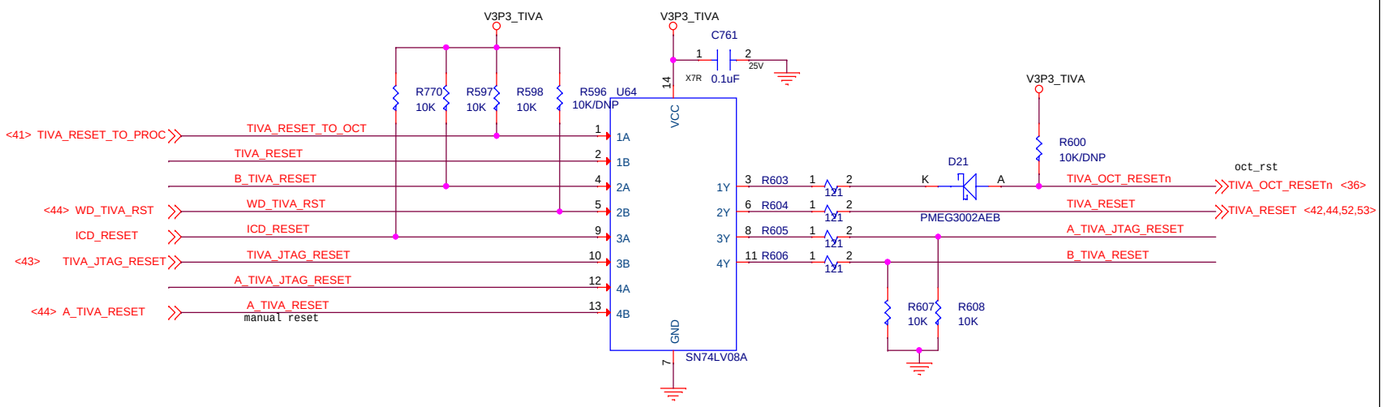


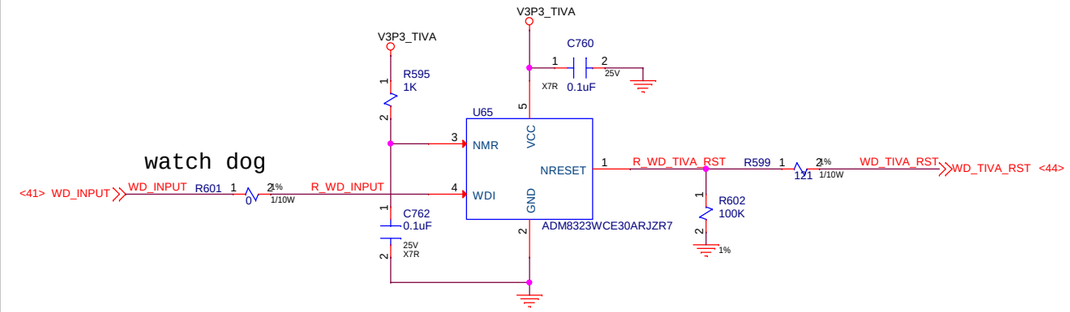


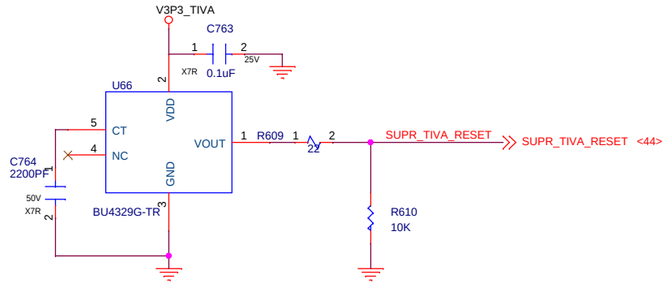


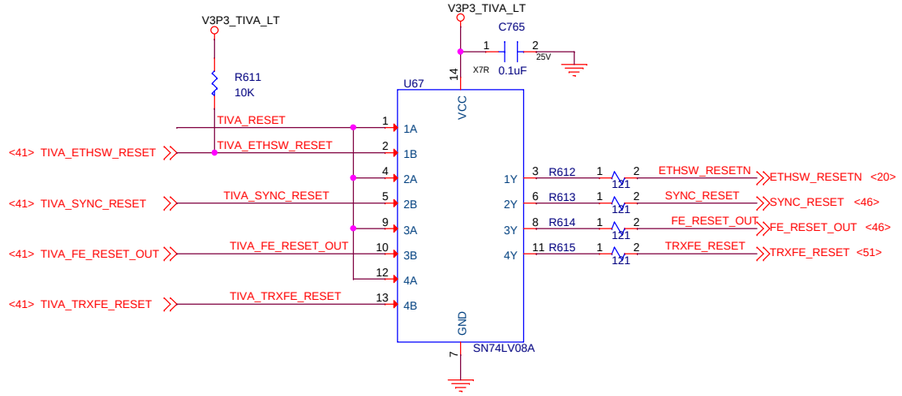
CAVIUM

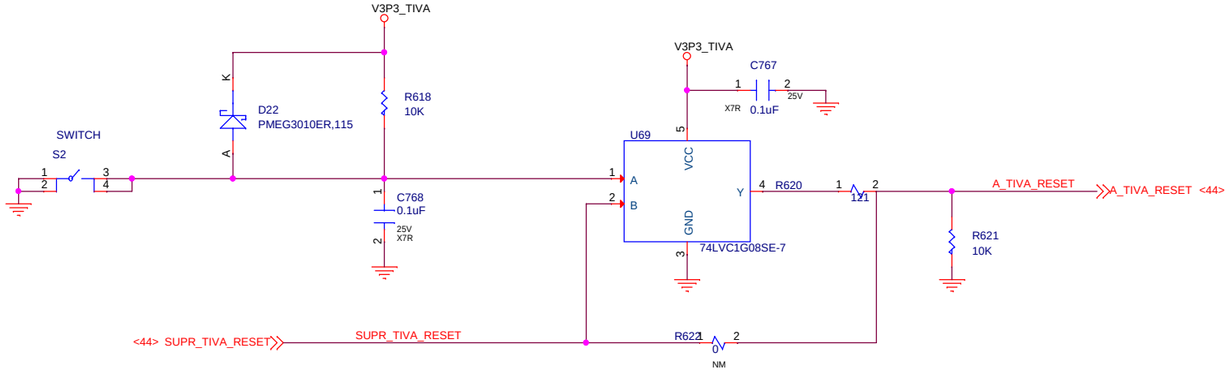
Title: TIVA JTAG CONNECTOR		
Size: B	Document Number: <Doc>	Rev: 1.0
Date: Monday, October 15, 2018	Sheet 43 of 54	

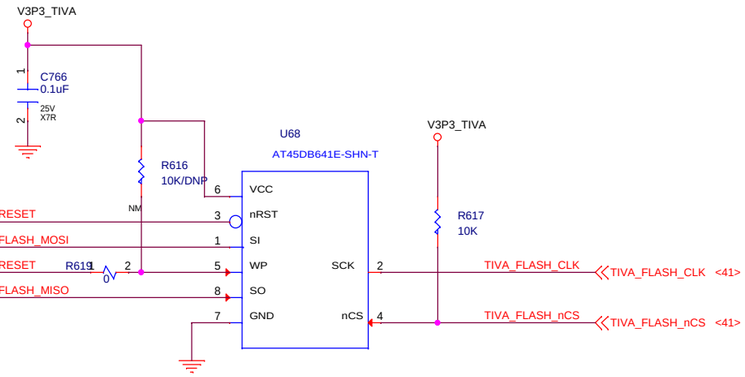






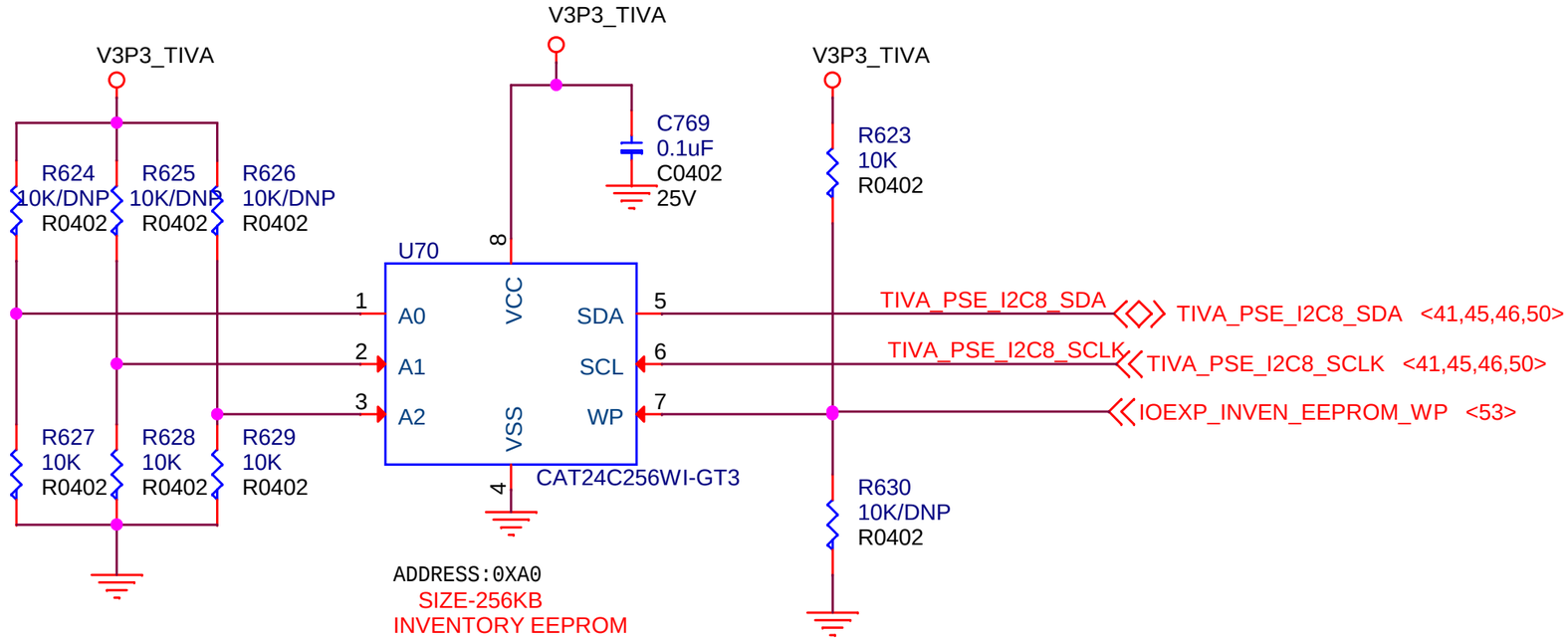


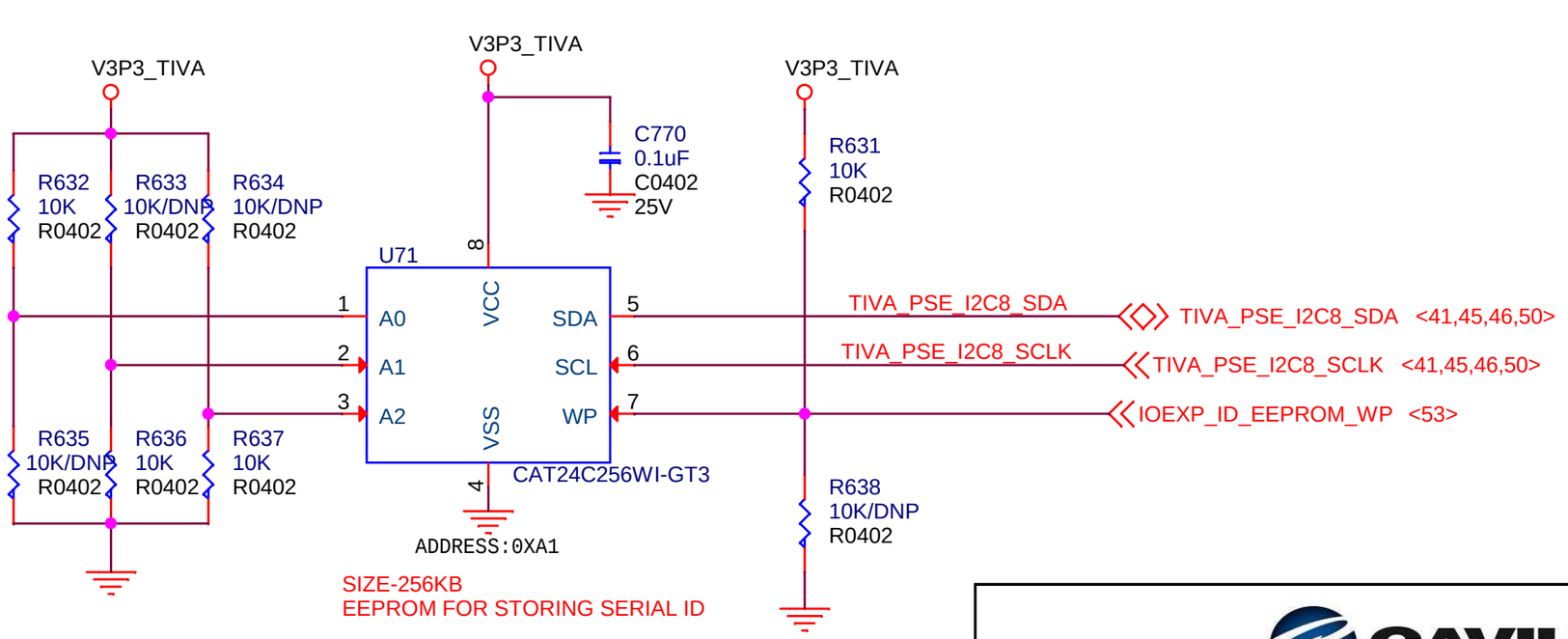




CAVIUM

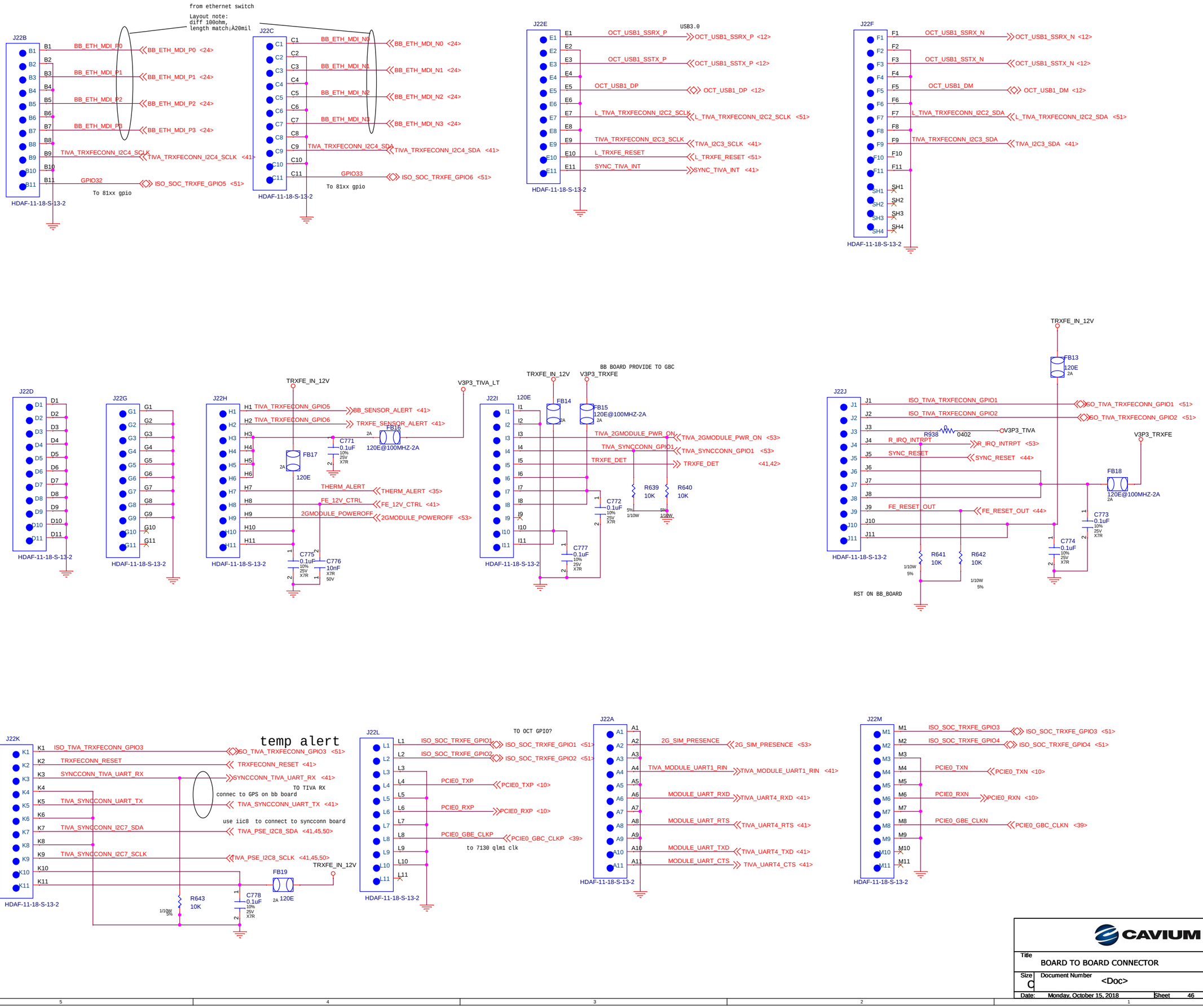
Title	TIVA FLASH & RESET		
Size: Custom	Document Number: <Doc>		Rev: 1.0
Date: Monday, October 15, 2018	Sheet 44 of 54		





CAVIUM

Title: TIVA EEPROM		
Size: A	Document Number: <Doc>	Rev: 1.0
Date: Monday, October 15, 2018	Sheet 45 of 54	



CAVIUM

Title: BOARD TO BOARD CONNECTOR

Size	Document Number	Rev
C	<Doc>	1.0

Date: Monday, October 15, 2018 Sheet 46 of 54

UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 0402 PACKAGE, POWER RATING < 0.5W & TOLERANCE > 1%
CAPACITORS ARE 0402 PACKAGE & TOLERANCE OF 10%

MSATA_V3P3
C3N1 22uF 6.3V 20%
C3A1 10uF 10V X7R
C3L1 0.1uF 25V X7R
J3M1
MPCIE_52P_NUTS_KIT
HALF_MINI_CARD
+1.5V
+3.3VAUX
WAKE_N
CLKREQ_N
COEX1
COEX2
KEY
W_DISABLE_N
PERST_N
RESERVED/UIM_C8
RESERVED/UIM_C4
RESERVED
RESERVED
RESERVED
MP1
MP2
REFCLK+
REFCLK-
UIM_DATA
UIM_CLK
UIM_RESET
UIM_PWR
UIM_VPP
GND
PETP0
PETN0
PERP0
PERN0
LED_WPAN_N
LED_WLAN_N
LED_WWAN_N
USB_D+
USB_D-
SMB_DATA
SMB_CLK
C779 SATA0_TX_P 10nF
C780 SATA0_TX_N 10nF
C782 SATA0_RX_P 10NF
C783 SATA0_RX_N 10NF
L_SATA0_TXP
L_SATA0_TXN
L_SATA0_RXP
L_SATA0_RXN
SATA0_TX_P <10>
SATA0_TX_N <10>
SATA0_RX_P <10>
SATA0_RX_N <10>
MSATA_V3P3
R647 10K
<23,25,36,48,49> MEM_RESET_L
R648 0
MSATA0_RESET
MSATA0_DAS
R650 0
RESV0
R2B1 0/dnp
A1 mSATA mini 3ME3
A2 MSATA Spacer 9774030243R
G52469-001
mSATA CONNECTOR

V3P3_TIVA_LT
R644 10K
R645 0
MSATA0_TIVA_DAS
MSATA0_TIVA_DAS <41>
Q9 2N7002L
MSATA0_DAS
R646 100K
C781 0.1uF 25V X7R

Provision,If mSATA does not have LED indication
MSATA_V3P3
R649 4.7K R0402 ±5%
SATA0_LED_L
Q3A1 FDG6301N
D71685-001
mSATA 0 STATUS LED
R651 10K/DNP
MSATA0_DAS
R918 0
R652 4.7K ±5%
NM
R3A1 200
D23 LED

V3P3_TIVA_LT
C784 0.1uF 25V X7R
R908 10K
U72
INA226
VS
GND
ALERT
SDA
SCL
IN+
IN-
VBUS
A0
A1
R653 10E
R654 0.002 1% 2W
R655 10E
C785 0.1uF
R656 10K
R657 10K
V3P3
MSATA_V3P3_CM
<41> SATA_PWR_ALERT
SATA_PWR_ALERT
<30,33,35,41,42,53> TIVA_PWRMNTR_I2C6_SDA
TIVA_PWRMNTR_I2C6_SDA
<30,33,35,41,42,53> TIVA_PWRMNTR_I2C6_SCLK
TIVA_PWRMNTR_I2C6_SCLK
ADDRESS 45
mSATA CURRENT MONITOR

MSATA_V3P3_CM
mSATA LOAD SWITCH
U3B1 TPS22922
C3B1 10uF 6.3V 20% C0402 X6S
C3B2 0.1uF 25V
C3B3 22uF 6.3V 20% XR5
C0402 X7R
2A MAX
<41> MSATA_PWR_EN
MSATA_PWR_EN
R2L1 0
R912 10K
VIN1 VIN2 ON VOUT1 VOUT2 GND
IC E64793-001

CAVIUM

Title: mSATA connector0

Size	Document Number	Rev
	Custom	1.0

Date: Monday, October 15, 2018 Sheet 47 of 54

UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 0402 PACKAGE, POWER RATING < 0.5W & TOLERANCE > 1%
CAPACITORS ARE 0402 PACKAGE & TOLERANCE OF 10%

MSATA_V3P3
22uF 6.3V C3N2 XR5 20%
C3A2 10uF 10V X7R
C3L2 0.1uF 25V X7R

J3M2
MPCIE_52P_NUTS_KIT
HALF_MINI_CARD

6	+1.5V	REFCLK+	13
2	+3.3VAUX	REFCLK-	11
		UIM_DATA	10
1	WAKE_N	UIM_CLK	12
7	CLKREQ_N	UIM_RESET	14
		UIM_PWR	8
		UIM_VPP	16
3	COEX1	GND	4
5	COEX2	GND	9
		GND	15
	KEY		
28	+1.5V	PETP0	33
48	+1.5V	PETN0	31
24	+3.3VAUX	PERP0	25
39	+3.3VAUX	PERN0	23
41	+3.3VAUX		
52	+3.3VAUX		
		LED_WPAN_N	46
		LED_WLAN_N	44
		LED_WWAN_N	42
20	W_DISABLE_N		
		USB_D+	38
		USB_D-	36
22	PERST_N		
		SMB_DATA	32
		SMB_CLK	30
17	RESERVED/UIM_C8	GND	18
19	RESERVED/UIM_C4	GND	21
45	RESERVED	GND	26
47	RESERVED	GND	27
49	RESERVED	GND	29
51	RESERVED	GND	34
		GND	35
		GND	37
		GND	40
MP1	MP1	GND	43
MP2	MP2	GND	50

C786 SATA1_TX_P 10nF X7R 50V — SATA1_TX_P <10>
C787 SATA1_TX_N 10nF X7R 50V — SATA1_TX_N <10>
C789 SATA1_RX_P 10nF X7R 50V — SATA1_RX_P <10>
C790 SATA1_RX_N 10nF X7R 50V — SATA1_RX_N <10>

CAD NOTE: PLACE C1833 AND C1834 NEAR U3C1
CAD NOTE: PLACE C1835 AND C1836 NEAR J3M1

MSATA_V3P3
R661 10K
MEM_RESET_L
<3,25,36,47,49> MEM_RESET_L R662 0 MSATA1_RESET
MSATA1_DAS R664 0
R2B2 0/dnp CH NM
MP1 MP2

A3 mSATA mini 3ME3
A4 MSATA Spacer
9774030151R

G52469-001

mSATA CONNECTOR

V3P3_TIVA_LT
R658 10K
R659 0 MSATA1_TIVA_DAS — MSATA1_TIVA_DAS <41>
Q10 2N7002L
MSATA1_DAS
R660 100K
C788 0.1uF 25V X7R

Provision,If mSATA does not have LED indication

MSATA_V3P3
R663 4.7K R0402 ±5%
Q3A2 FDG6301N D71685-001
mSATA STATUS LED
R665 10K/DNP
MSATA1_DAS R919 0
MSATA_V3P3
R666 R0402 4.7K ±5%
NM

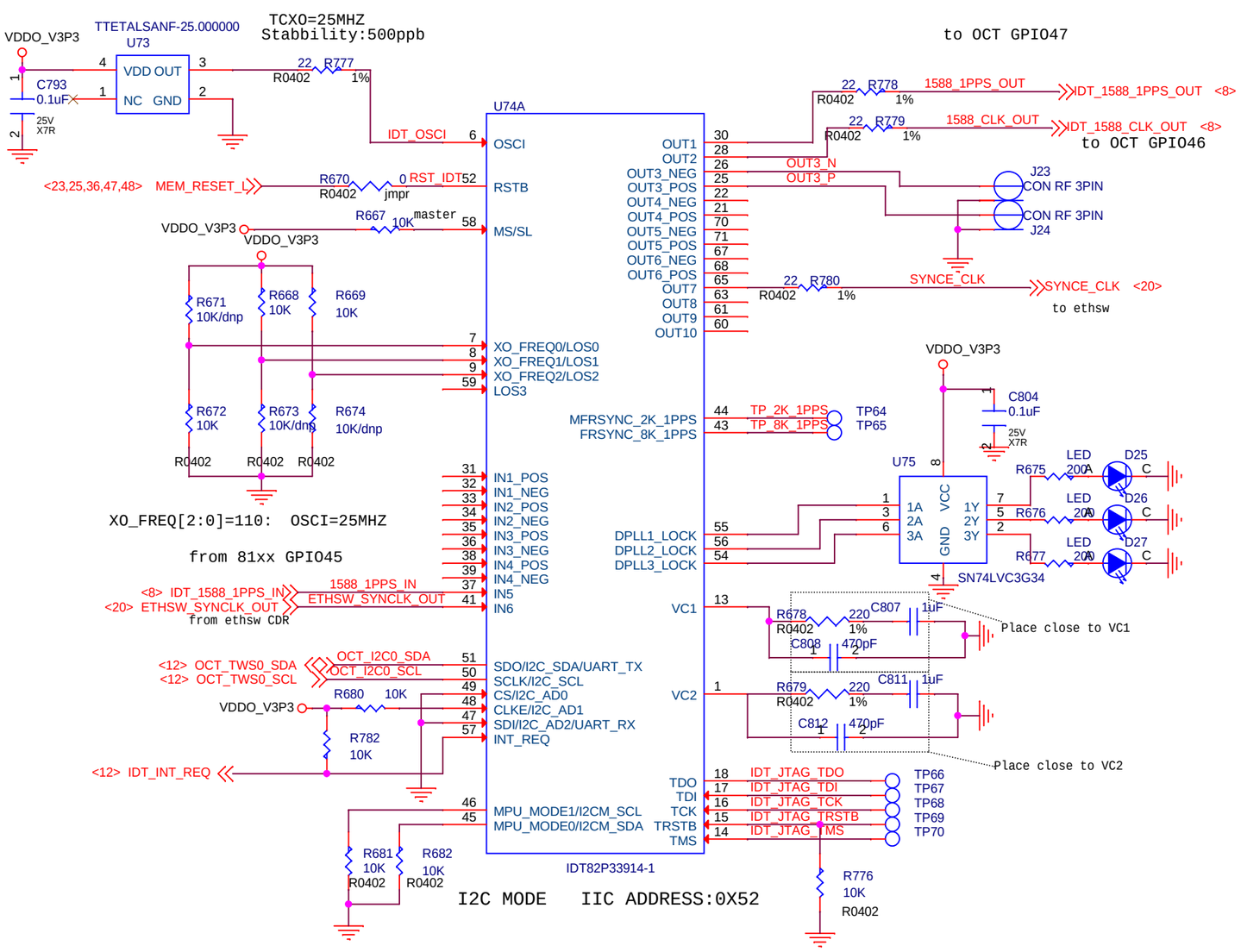
MSATA_V3P3
R3A2 200 NM
D24 LED NM

CAVIUM

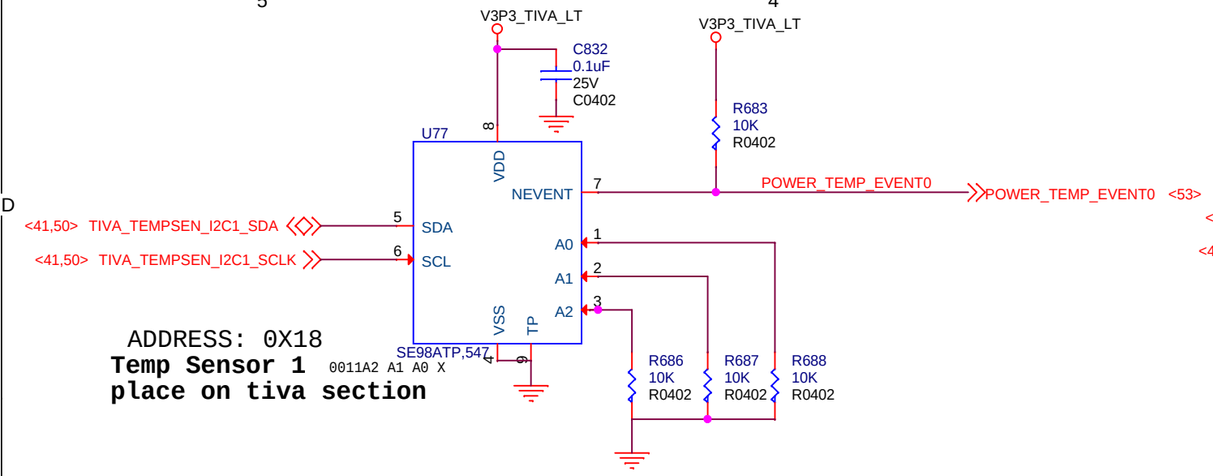
Title: mSATA connector1

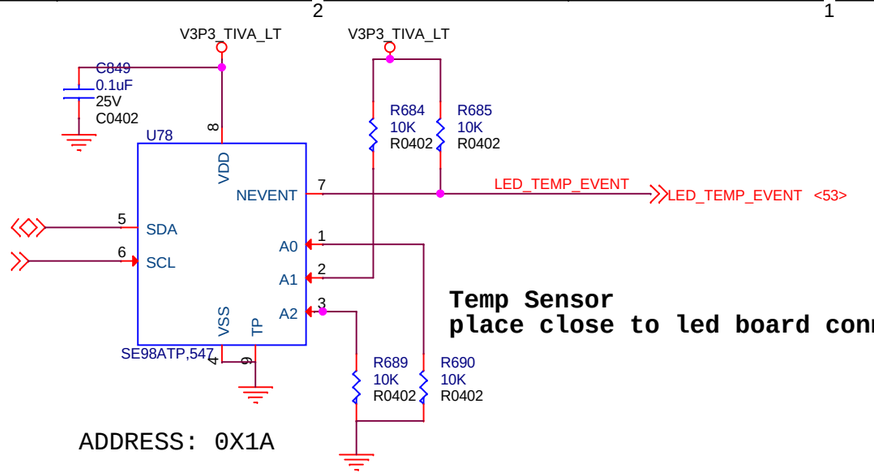
Size	Document Number	Rev
	Custom	1.0

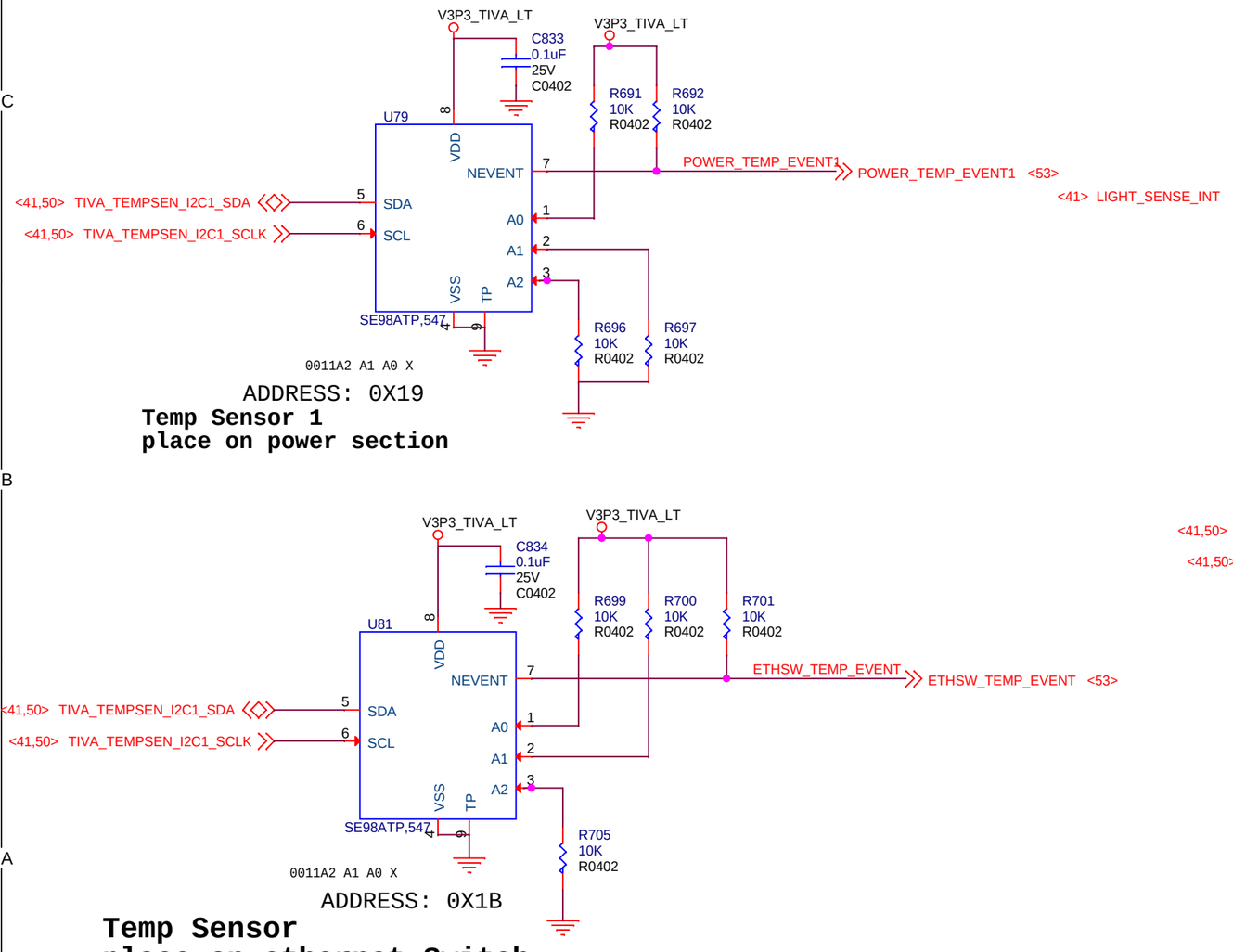
Date: Monday, October 15, 2018 Sheet 48 of 54

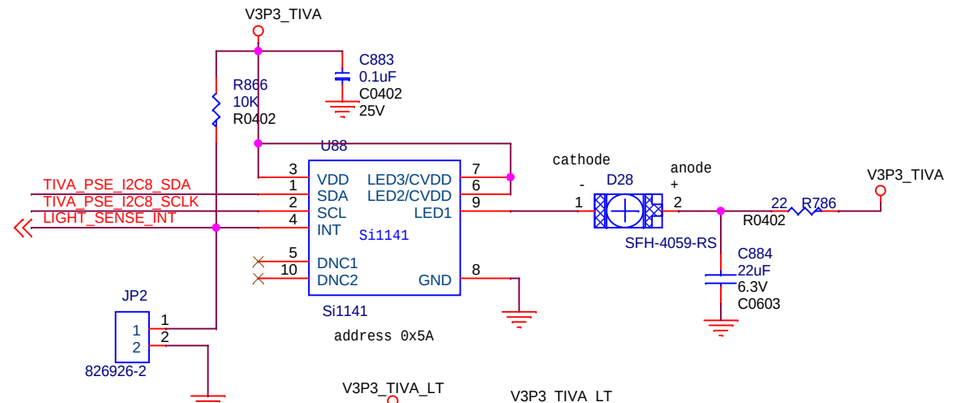


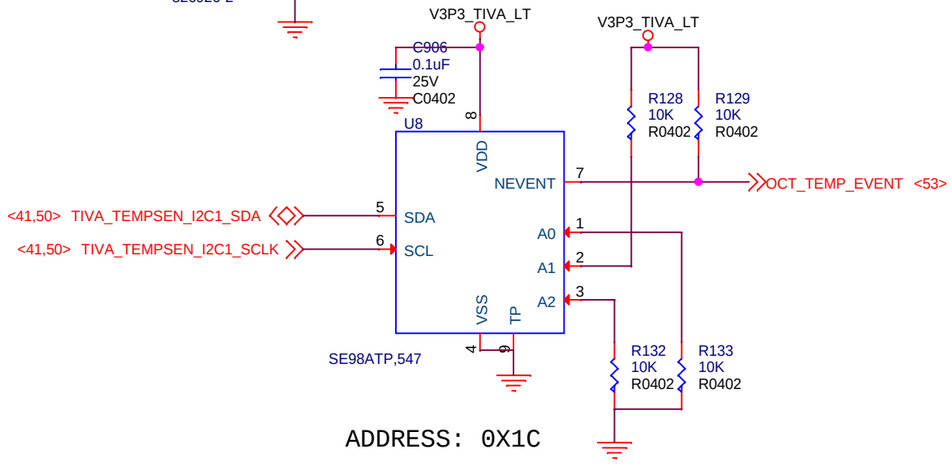
Title	PTP Moduel	
Size: B	Document Number: <Doc>	Rev: 1.0
Date: Monday, October 15, 2018	Sheet 49 of 54	











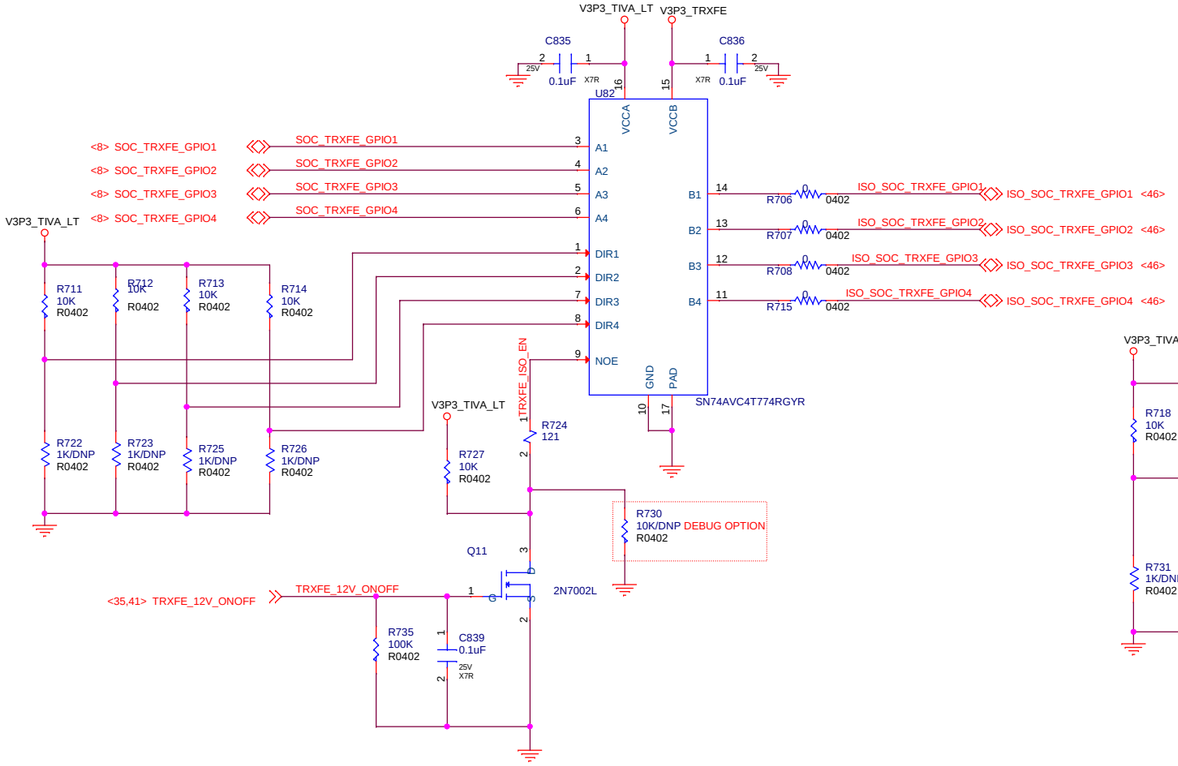
CAVIUM

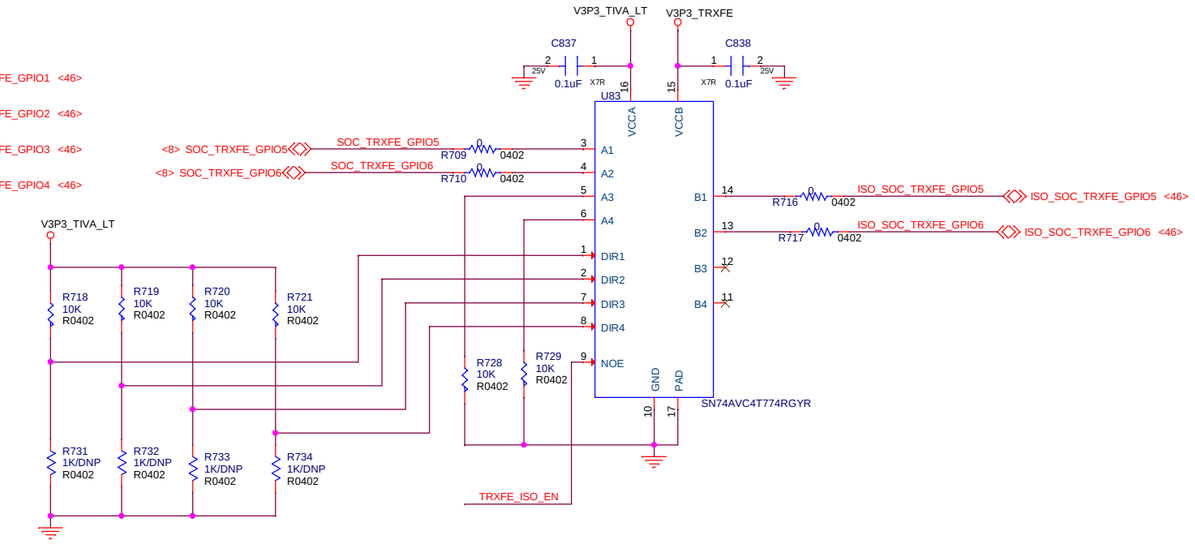
Title: TEMP SENSOR

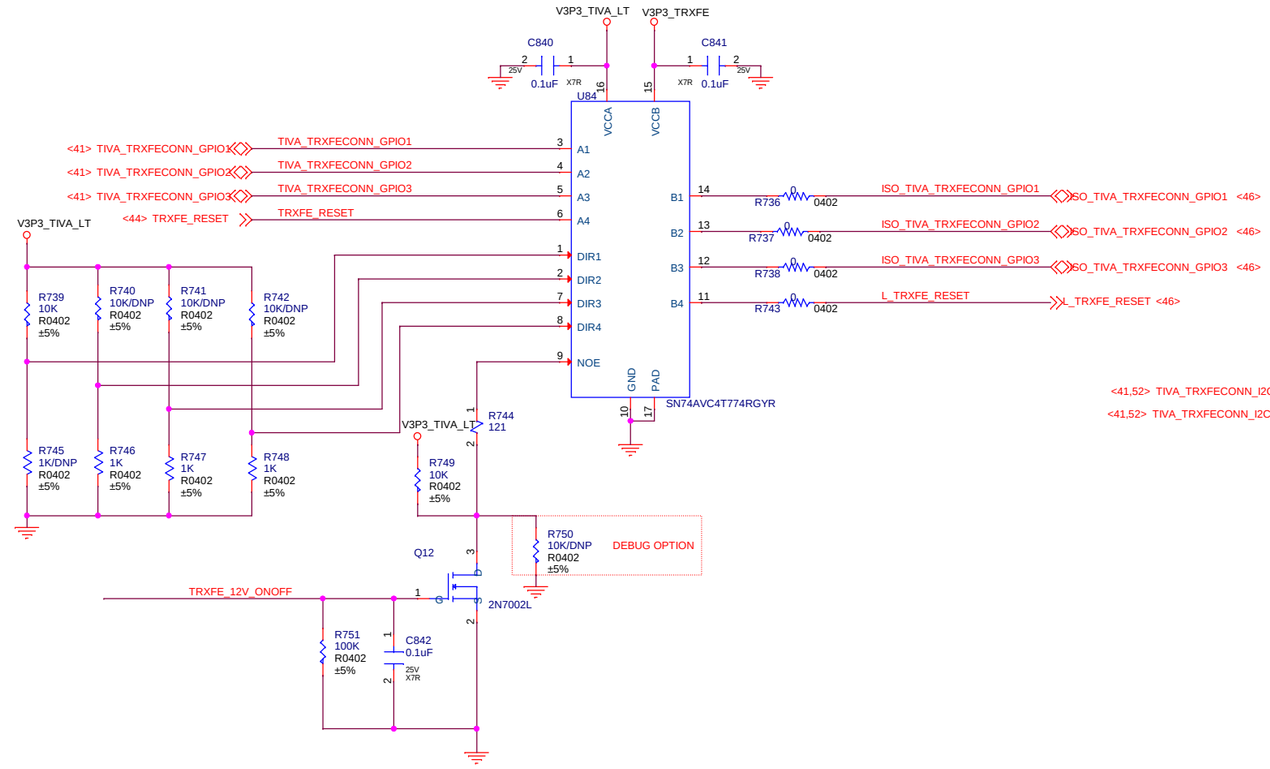
Size	Document Number	Rev
B	<Doc>	1.0

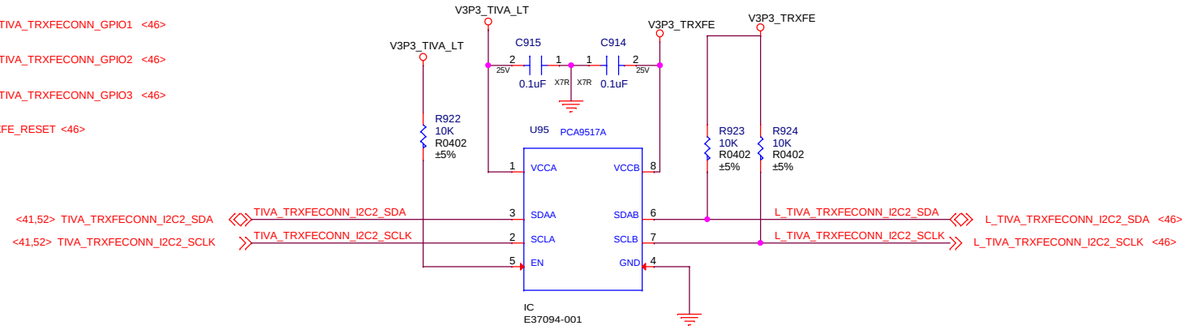
Date: Monday, October 15, 2018 Sheet 50 of 54

UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 0402 PACKAGE, POWER RATING < 0.5W & TOLERANCE > 1%
CAPACITORS ARE 0402 PACKAGE & TOLERANCE OF 10%









CAVIUM

Title: TIVA OCT-IO ISOLATION

Size	Document Number	Rev
C	<Doc>	1.0

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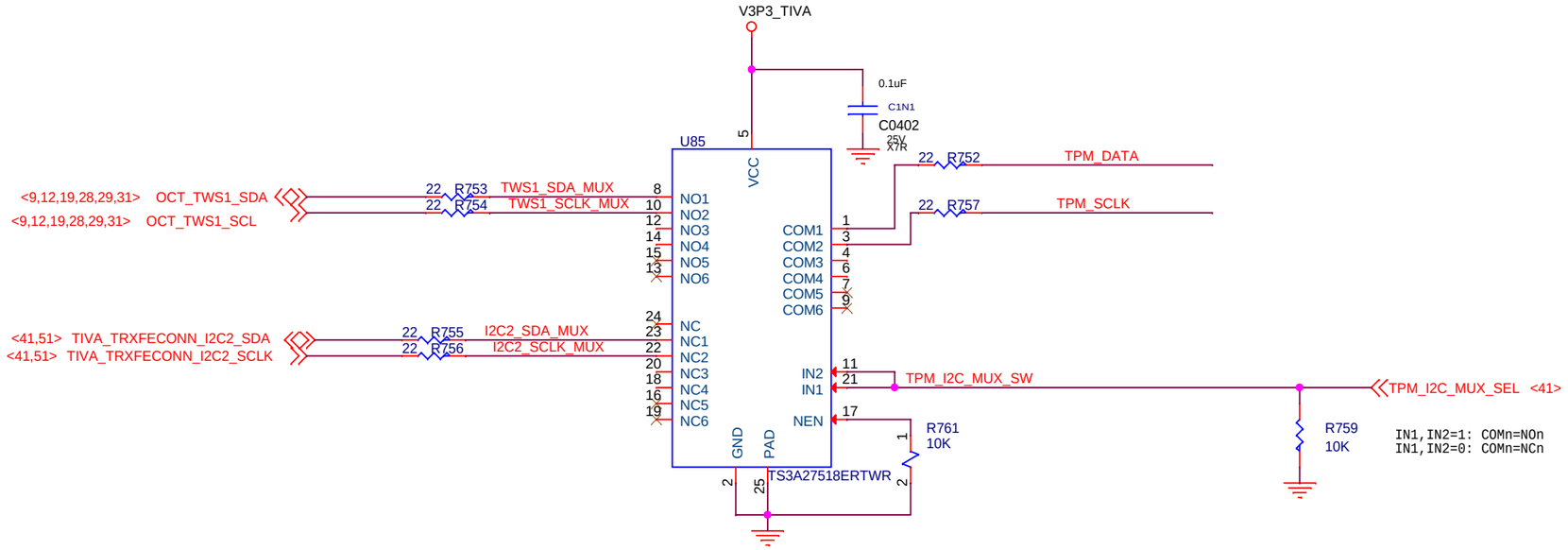

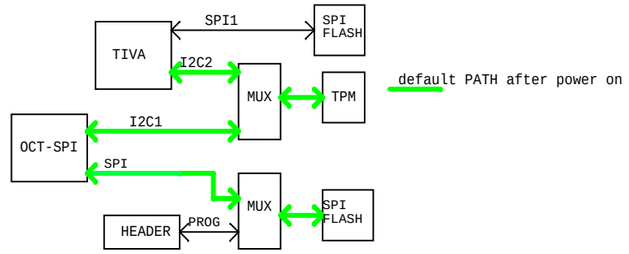

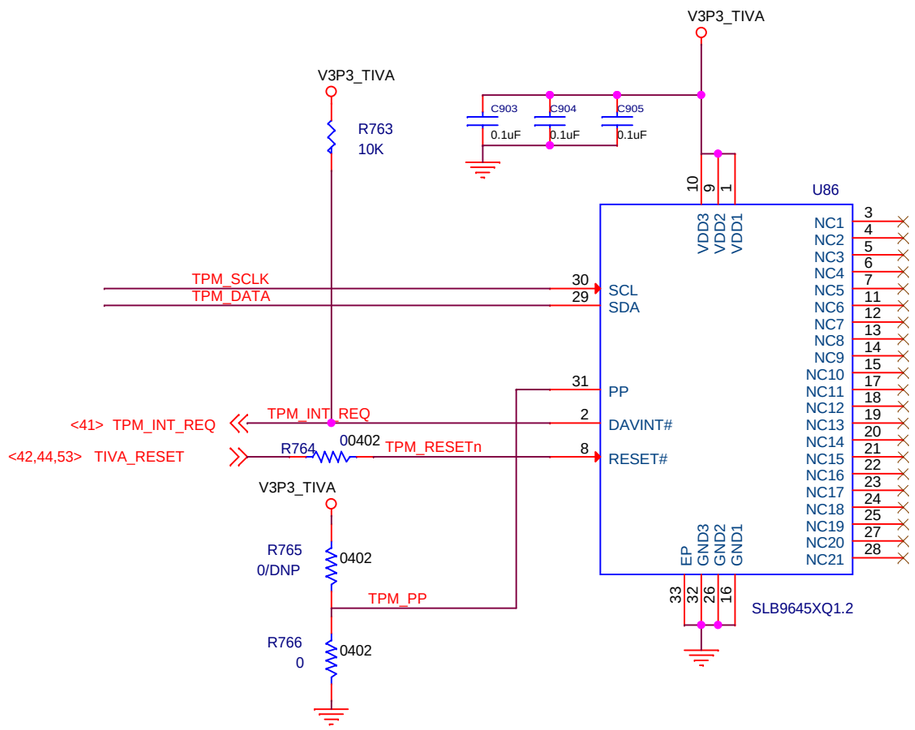

CAVIUM

Title: Trusted Platform Modul		
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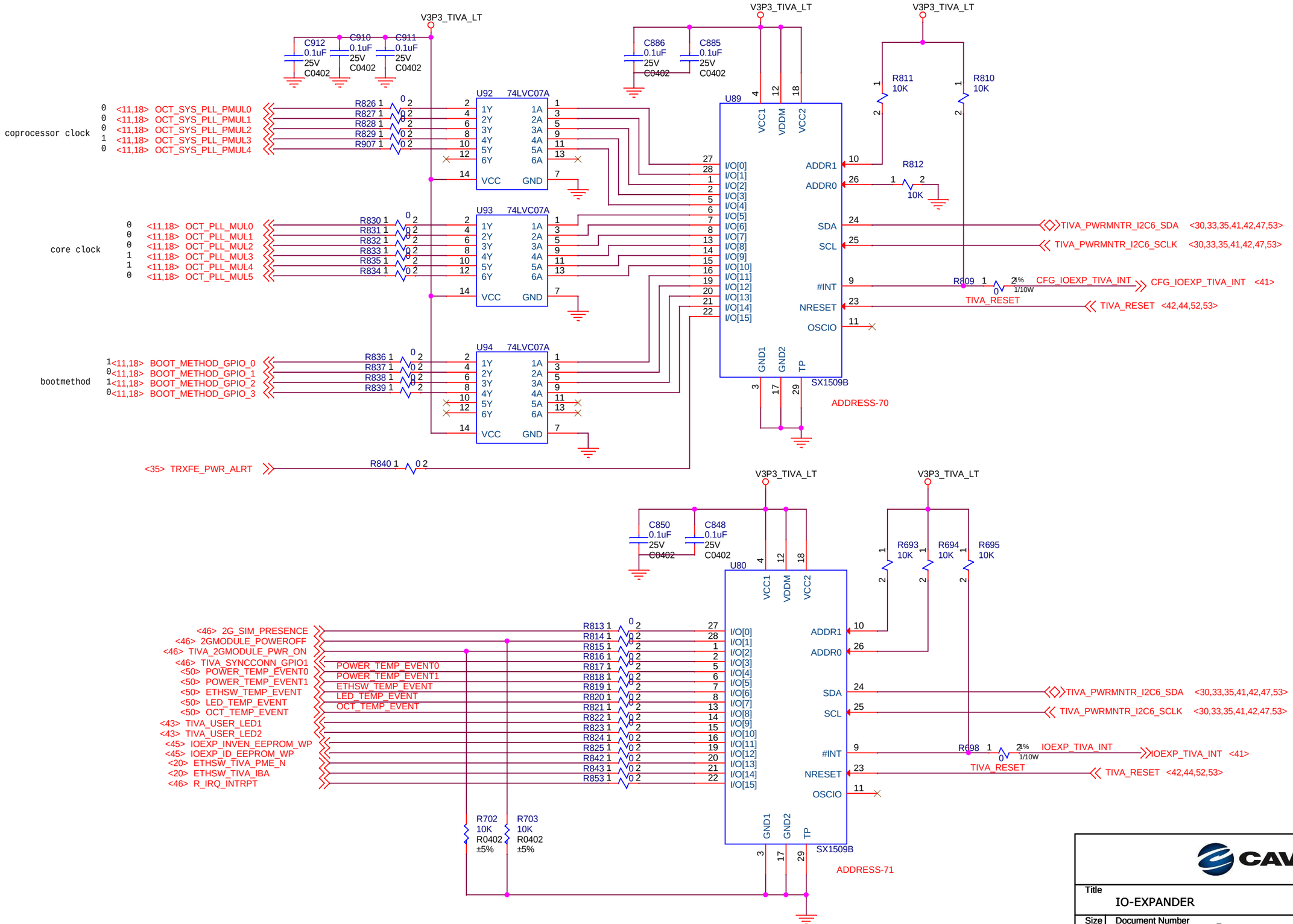

CAVIUM

Title	IO-EXPANDER	
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when V1 fall to 3.0V ,V2 on
when V1 raise to 3.2V ,V2 off

V3P3_TIVA_LT

R783
267K
1%

C879
10uF
C0603
6.3V

U87

IN1_1
IN1_2
OUT1_2
OUT1_1
LTC4415
EN1
EN2
WARN1
WARN2
STAT2
STAT1
CLIM1
CLIM2
IN2_1
IN2_2
OUT2_2
OUT2_1
EGND
LTC4415IMSE

V3P3_TIVA_CM

C881
10uF
C0603
6.3V

C882
10uF
C0603
6.3V

calculate the resistor

R784
7.5K
?%
R0402

LT4415_EN
LT4415_EN2n

R785
100K
1%
R0402

R854
1M
1%

R855
1M
1%

TP73
TP72

J28
91601-306LF

SuperCap_VCC

C880
10uF
C0603
6.3V

J28

MH13 should place 1.5inch away from J28

MH13

MH13
Mounting_Hole

A5
Custom Board Spacer
9774070243R

MH6 Mounting_Hole
MH5 Mounting_Hole
MH8 Mounting_Hole
MH3 Mounting_Hole

MH10 Mounting_Hole
MH1 Mounting_Hole
MH2 Mounting_Hole

C843
1000PF
X7R
3KV
10%

CHASIS_GND
SHIELD_GND_B
CHASIS_GND

CAVIUM

Title: TIVA BackUp Power

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A	<Doc>	1.0

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