OPEN CELLULAR REFERENCE BOARD

Cavium CNF7130

P R E L I M I N A R Y S C H E M A T I C

CAVIUM

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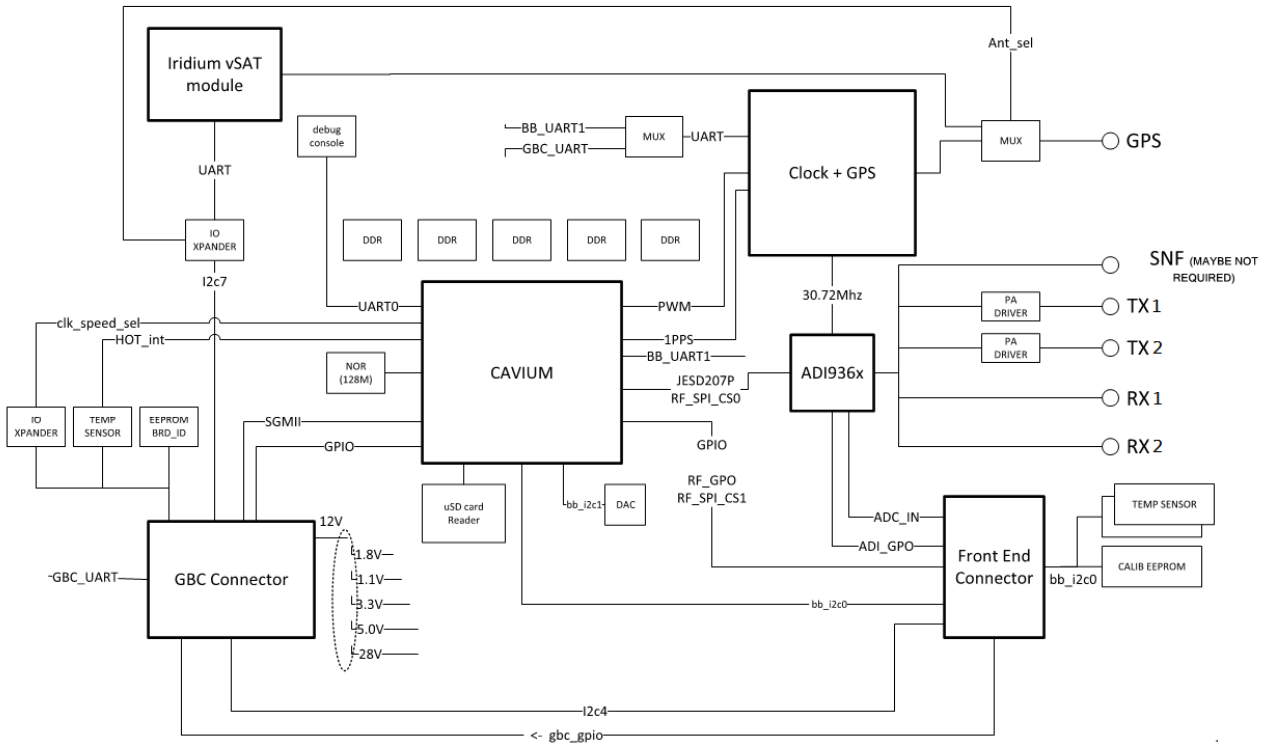
OPEN CELLULAR REFERENCE BOARD BLOCK DIAGRAM



Revision History:

Rev	Description	Date	Approved
1	Preliminary Release	2017/05/26	
2	DNP R447 ,R44 Add R9,R471,R489,R490,R491, R492 to 10K ohm Change C419,C427,C530,C532 to 33pF DNP C534,C535,C531,C533,U57,U59 Change L47,L50 partnumber Change J13,J15,J16,J17 to U.FL Add R470,R472,R473,R474, R475,R476,R477,R413R478, R479,R480,R481,R482,R483, R484,R485,R487,R493,R494, R495,R314,R321 to 0 ohm	2017/08/03	
2	R42,R43,R45,R46 change to 3K01 DNP J10 C453,C454,C463,C464,C465 change to 22uF/35V/1206	2017/08/30	
2	DNP J26,J27,J28,J29 ,U45 Change L51,L48 to 0 ohm Add R274, R275 0 ohm	2017/09/06	

3	Add R496,R497,R498,R512 0 ohm
	Add R513~R519,U73,C540
	Add R500~R511
	DNP R417,C233,J22,J23,R441
	Add C546,C555 10uF
	delete C234,C232,R155
	Add C551,C560 3.3pF
	Add C547,C556 1uF
	Add C548,C552,C553,C557,C561,C562 100pF
	Add C542,C544,C549,C558 33pF
	Add C541 2.2uF
	DNP FB2 0/0805
	DNP J22,J23
	DNP R267,R269,R458,R457,R456,R455,R451,
	R452,R453,R454
	Add L48,L51,R192,R265,R266,R460,R461,
	R462,R463,R464,R465,
	R466,R467,R472,R473,R474,R475,R476,
	R477,R478,R479,
	R480,R481,R482,R483,R484,R506,R507,R508,
	R509,R512,
	R514,R518,R524 0 OHM
	Add R4,R352,R359,R489,R492,R504,R505,R513,
	R517
	change R154 from 10k/1% to 25k/1%
	change R152 from 53.6k/1% to 100k/1%
	Add R522,R523 33k
	Add U73
	Add U74,U77
	Add U75,U78
	Add U79,U76
	Change U18
	Change R358,R351
	Change R43 ,R46 to 1K
		2017/12/20	

3	Add C566,C567
	Add R525
	Add U80,U81
	Change J19 to J31
	Add R526~R551,R552~R555
	delete C444,C445,C446,R524
	Change R42,R45 to 1K
		2018/05/10	

3	Delete R306,C391,C395,C397,R305,L39,J30 Change R300 to 43K Change R303 to 27K Add U82,U83 Change U53 to ADP1755 Add R556,R557,R558,R559,C568,R560,R561,R562 DNP R542,R543	2018/06/08	

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Title: **Notes & Block Diagram**

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Core

Internal pull down 50K ohm

Coprocessor

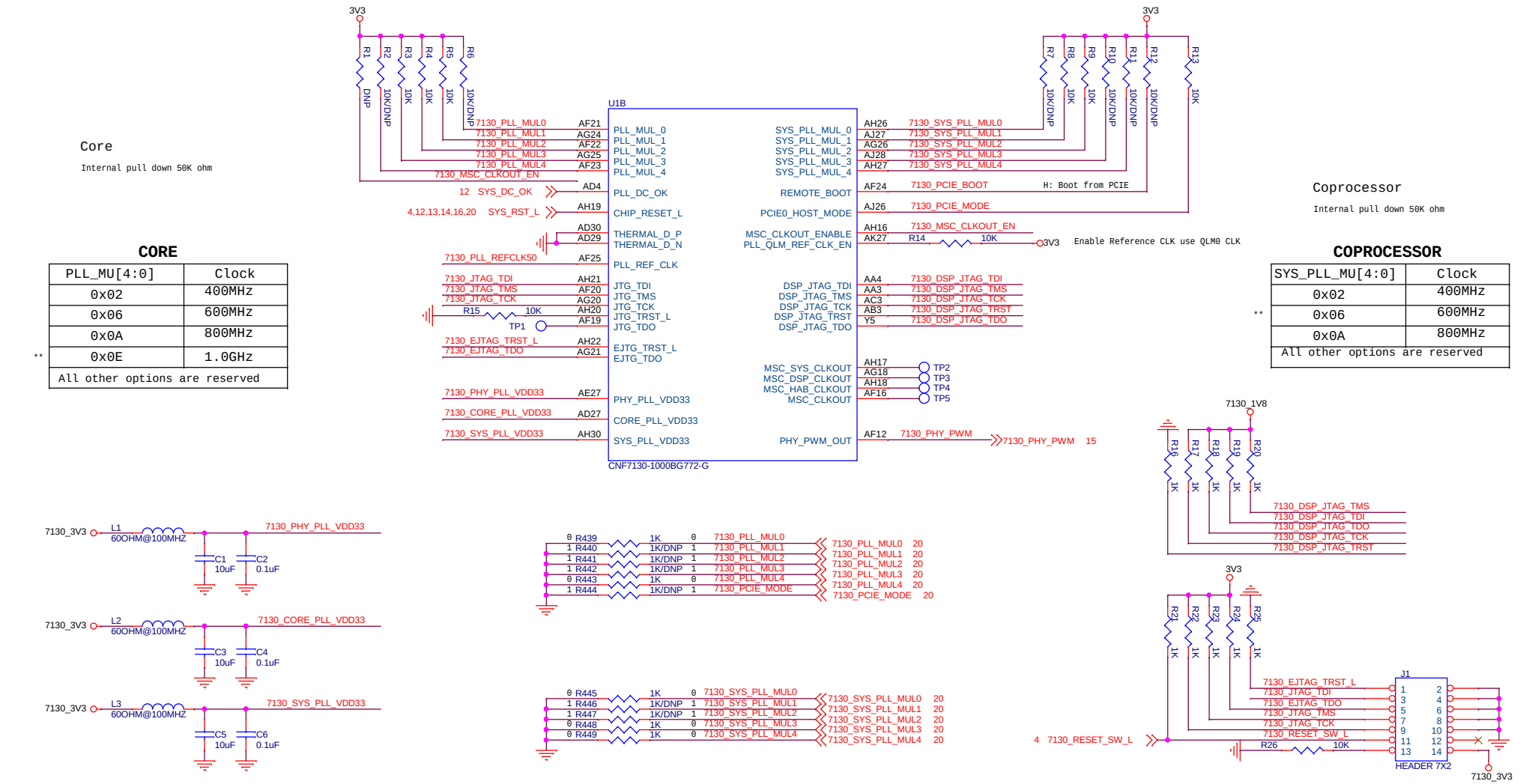
Internal pull down 50K ohm

CORE

PLL_MU[4:0]	Clock
0x02	400MHz
0x06	600MHz
0x0A	800MHz
** 0x0E	1.0GHz
All other options are reserved	

COPROCESSOR

SYS_PLL_MU[4:0]	Clock
0x02	400MHz
** 0x06	600MHz
0x0A	800MHz
All other options are reserved	



CAVIUM

Title: **CNF7130 Config & JTAG**

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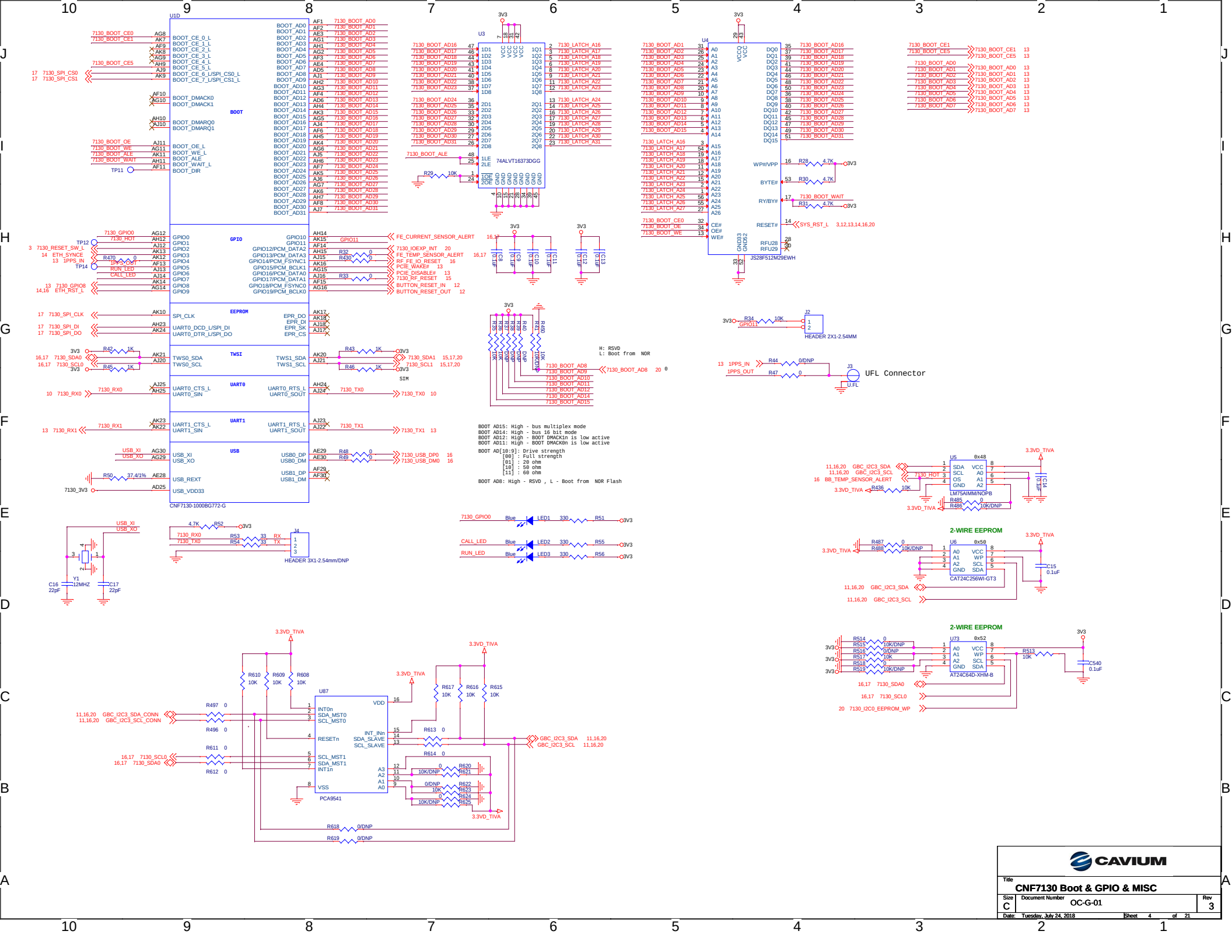
U1D
BOOT
GPIO
EEPROM
TWSI
UART0
UART1
USB
CNF7130-1000BG772-G
U3
74ALVT16373DGG
U4
JS28F512M29EWH
U87
PCA9541
SIM
UFL Connector
HEADER 2X1-2.54MM
HEADER 3X1-2.54mm/DNP
LM75AIMM/NOPB
2-WIRE EEPROM
CAT24C256WI-GT3
AT24C64D-XHM-B
BOOT AD15: High - bus multiplex mode
BOOT AD14: High - bus 16 bit mode
BOOT AD12: High - BOOT DMACK1n is low active
BOOT AD11: High - BOOT DMACK0n is low active
BOOT AD[10:9]: Drive strength
[00] : Full strength
[01] : 20 ohm
[10] : 50 ohm
[11] : 60 ohm
BOOT AD8: High - RSVD , L - Boot from NOR Flash
H: RSVD
L: Boot from NOR
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CNF7130 Boot & GPIO & MISC
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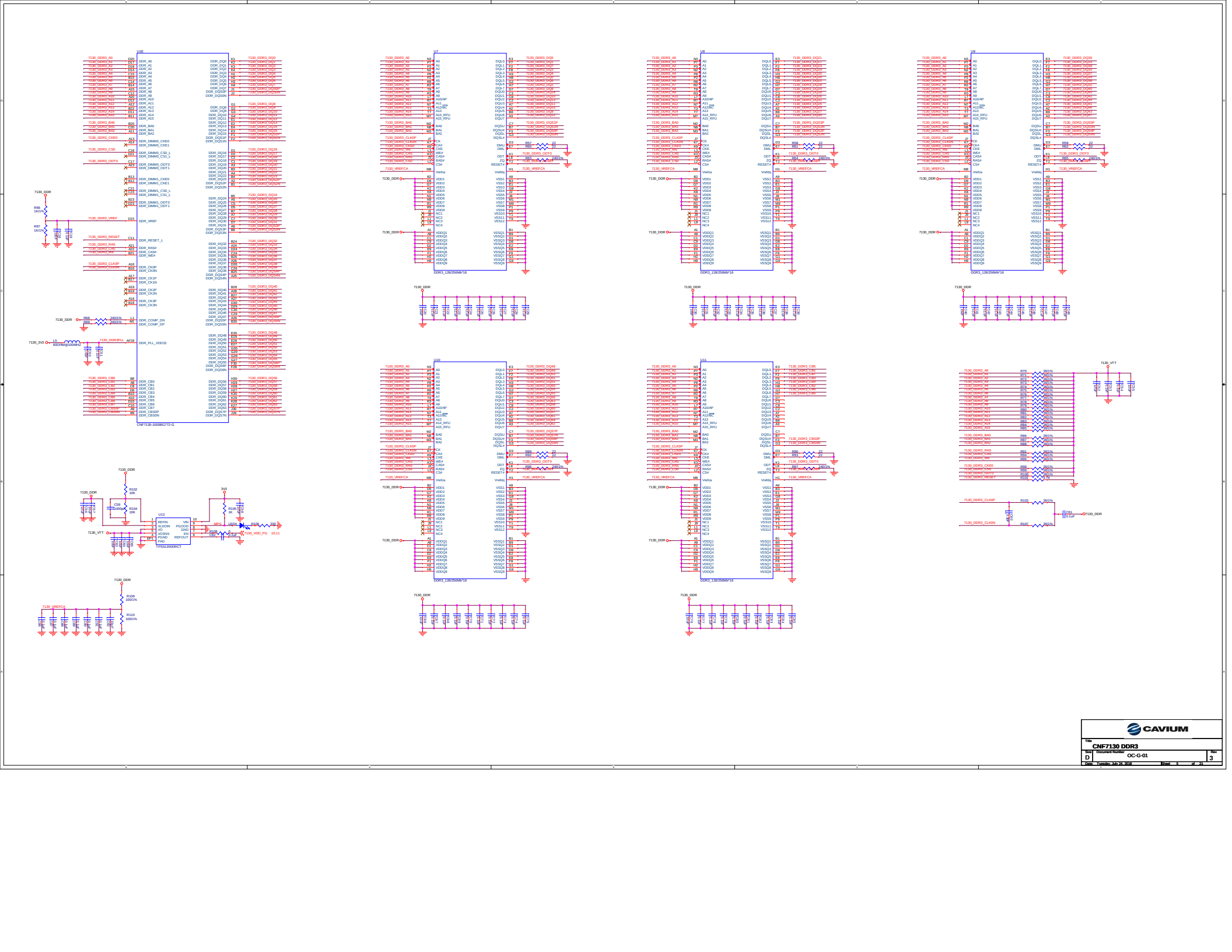

Title	CNF7130 DDR3
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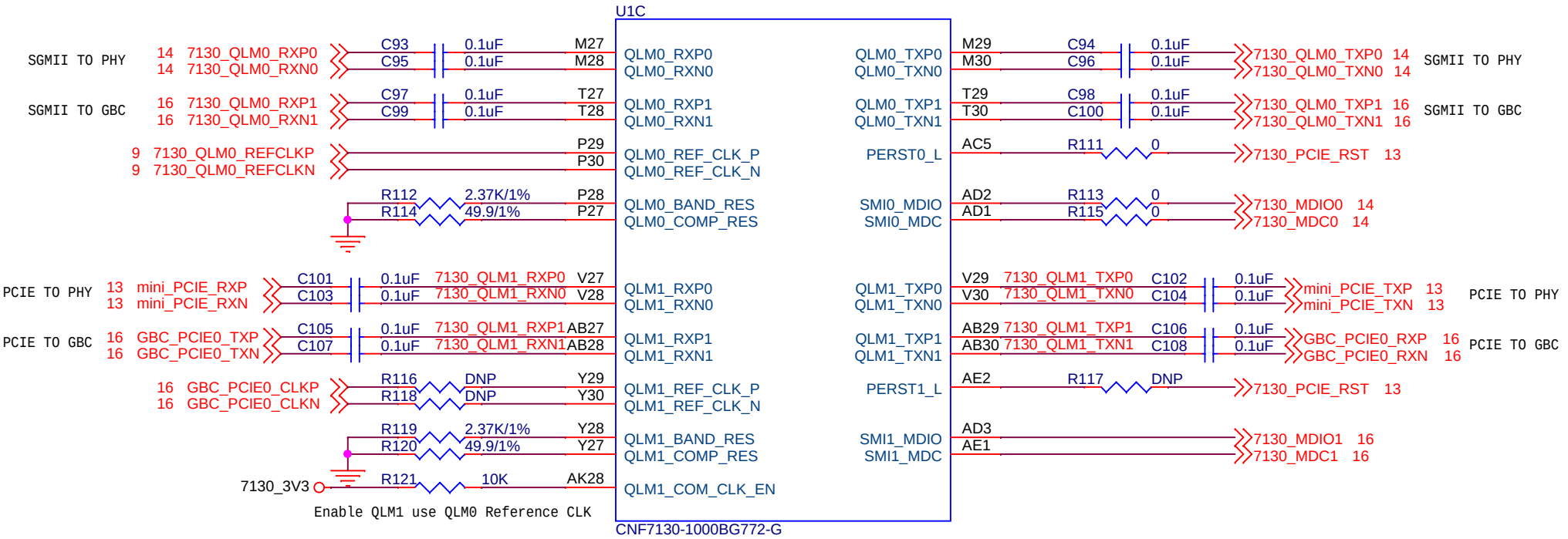

CAVIUM

Title

CNF7130 QLM0-QLM1

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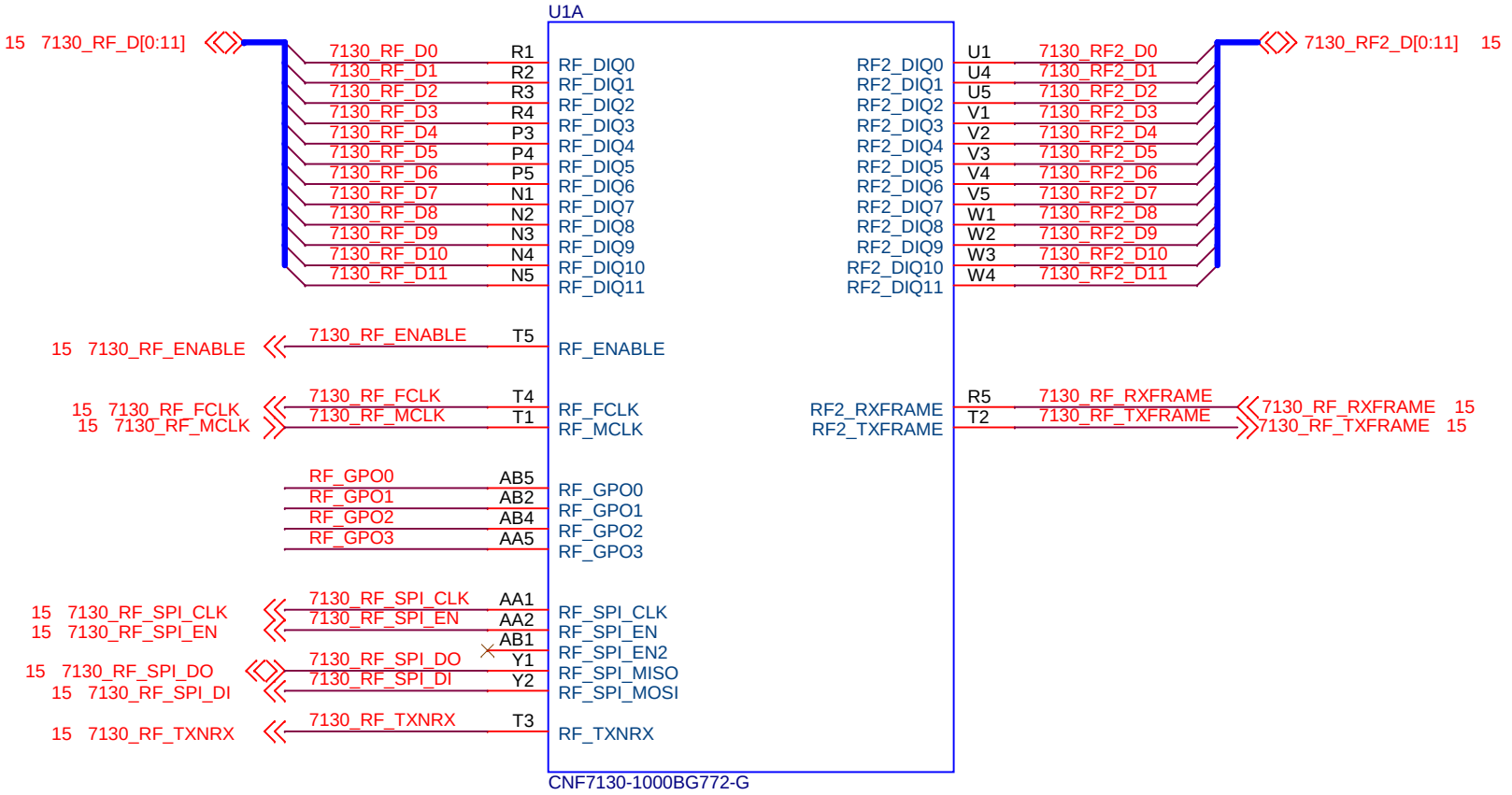

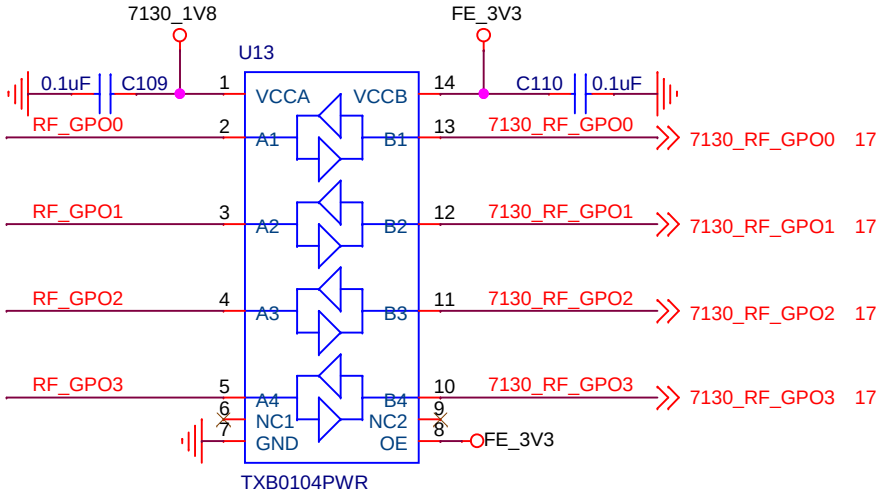

CAVIUM

Title
CNF7130 RF Interface

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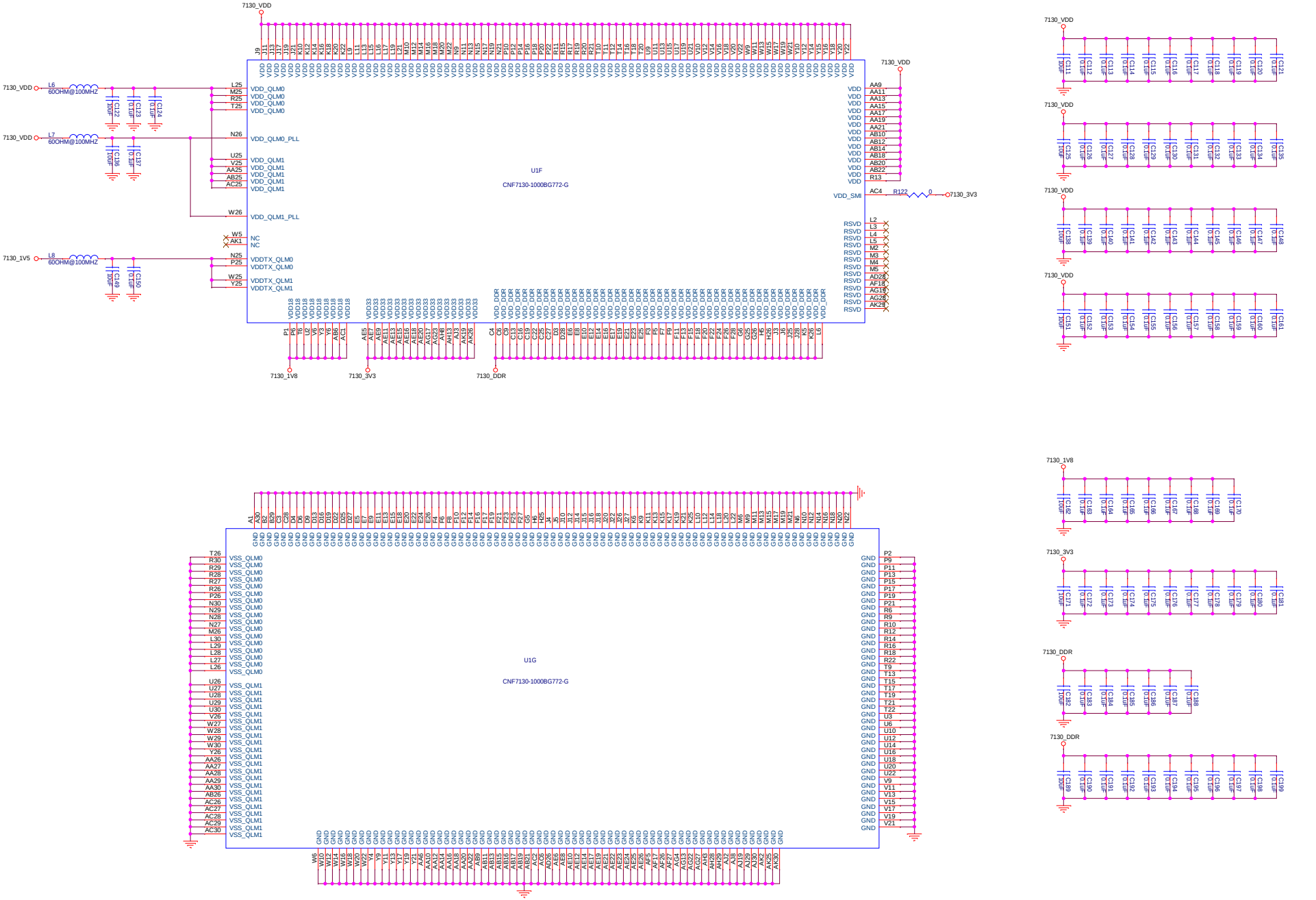

CAVIUM

Title	CNF7130 Decoupling	
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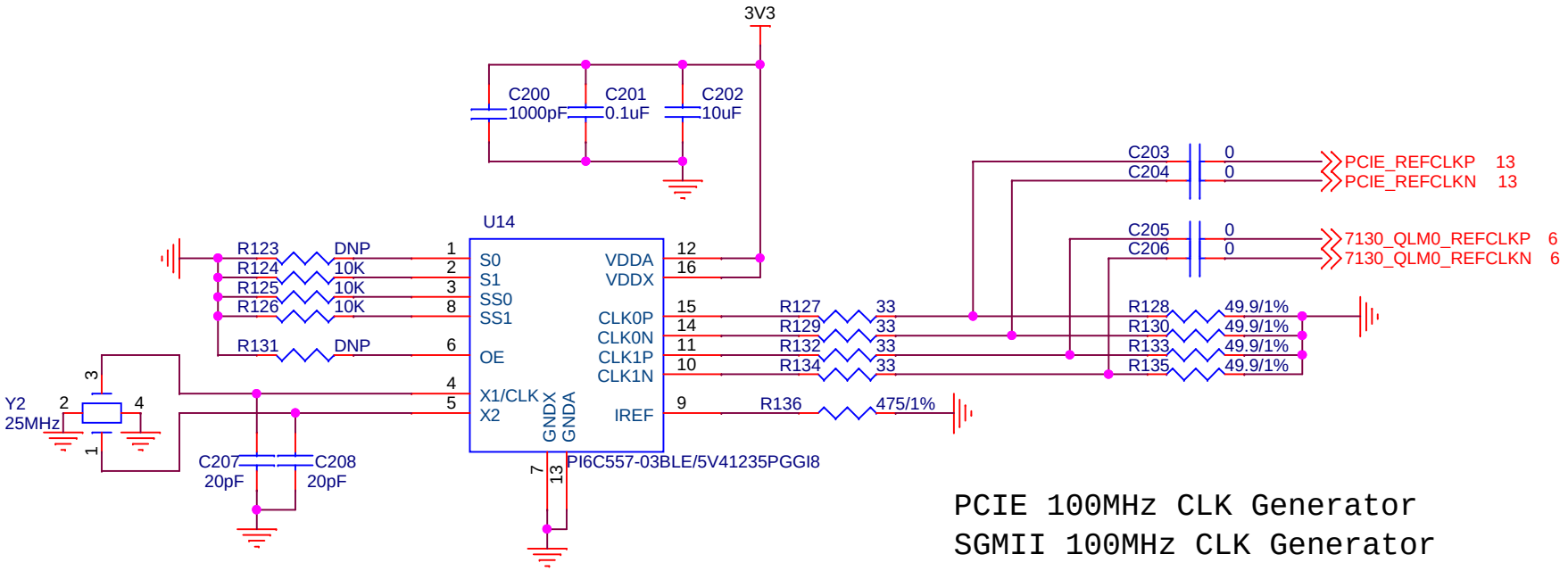

PCIE 100MHz CLK Generator
SGMII 100MHz CLK Generator

S1	S0	CLK
0	0	25
0	1	100
1	0	125
1	1	200

SS1	SS0	Spread
0	0	No Spread
0	1	Down-0.5
1	0	Down-0.75
1	1	No Spread

Internal Pull-up resistor

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Title
CNF7130 Clock Generator

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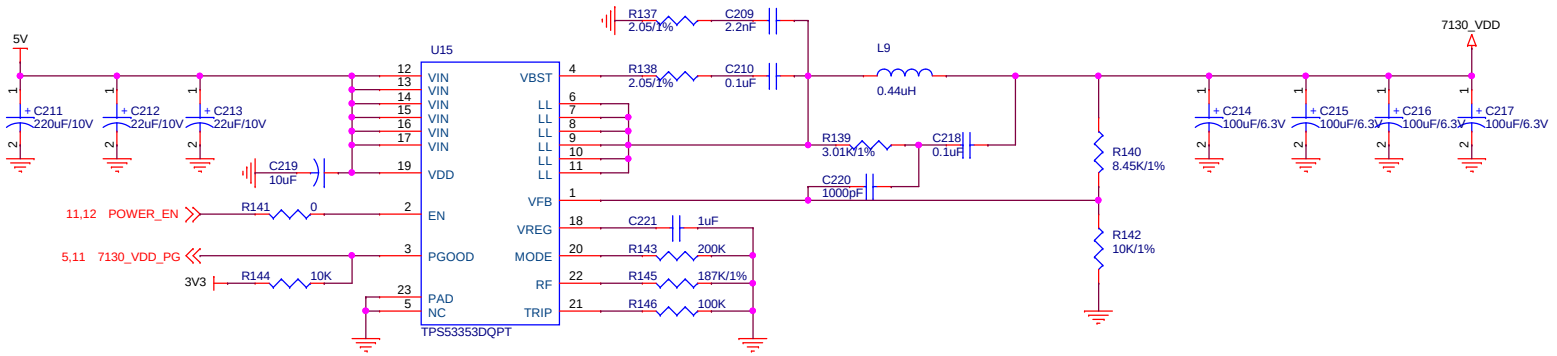
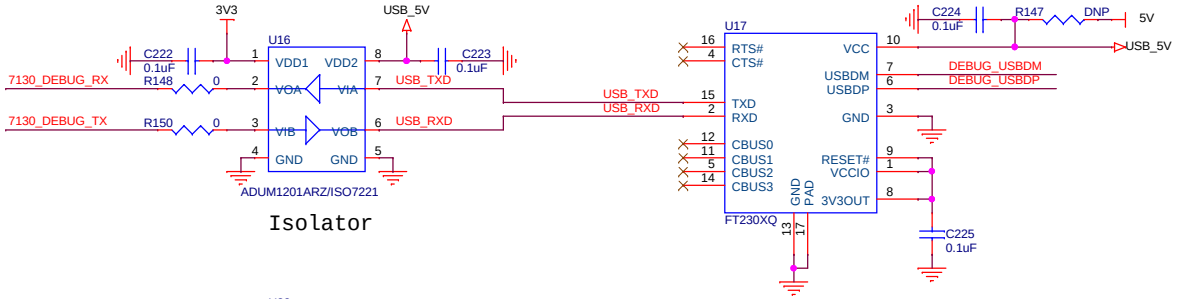
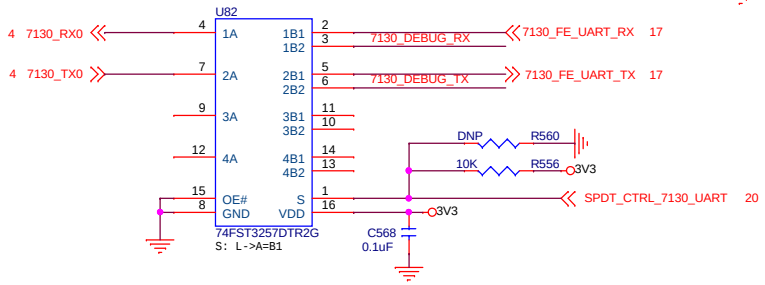


1.1V @20A

Vout=0.6*(1+R1/R2)





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Title: **CNF7130 Core Power & Debug**

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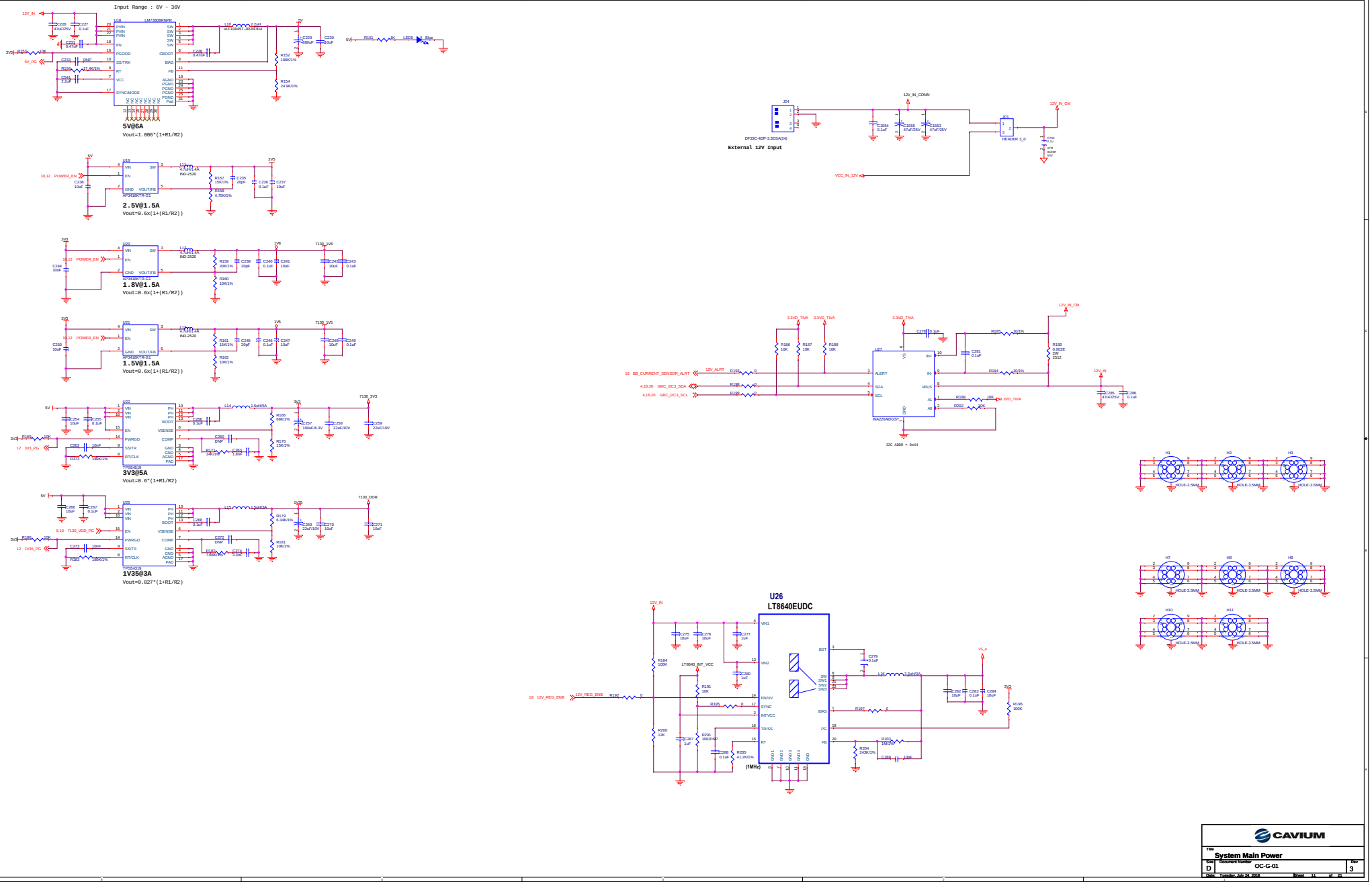
Input Range : 6V ~ 36V
5V@6A
Vout=1.806*(1+R1/R2)
2.5V@1.5A
Vout=0.6x(1+(R1/R2))
1.8V@1.5A
Vout=0.6x(1+(R1/R2))
1.5V@1.5A
Vout=0.6x(1+(R1/R2))
3V3@5A
Vout=0.6*(1+R1/R2)
1V35@3A
Vout=0.827*(1+R1/R2)
External 12V Input
U26
LT8640EUDC
(1MHz)
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System Main Power
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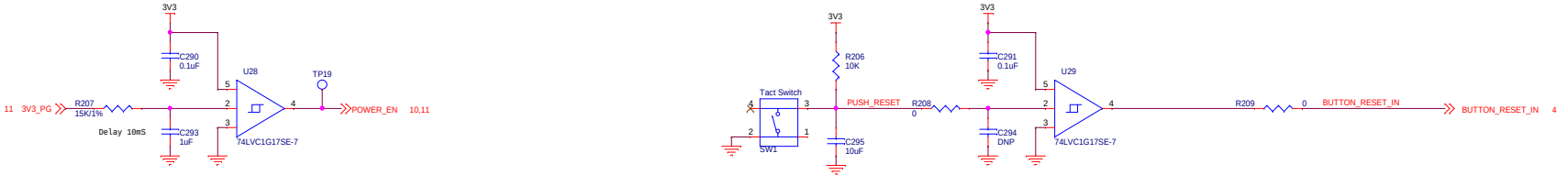
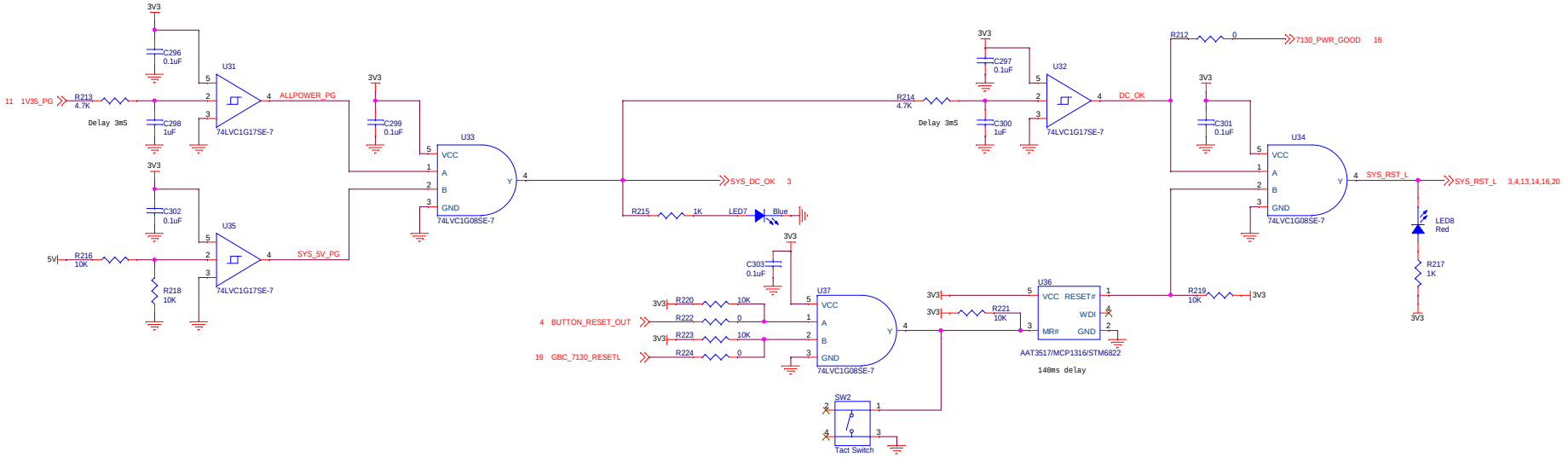


Push Button Reset



Debug Reset Push Button

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Title: System Power Sequence & Reset		
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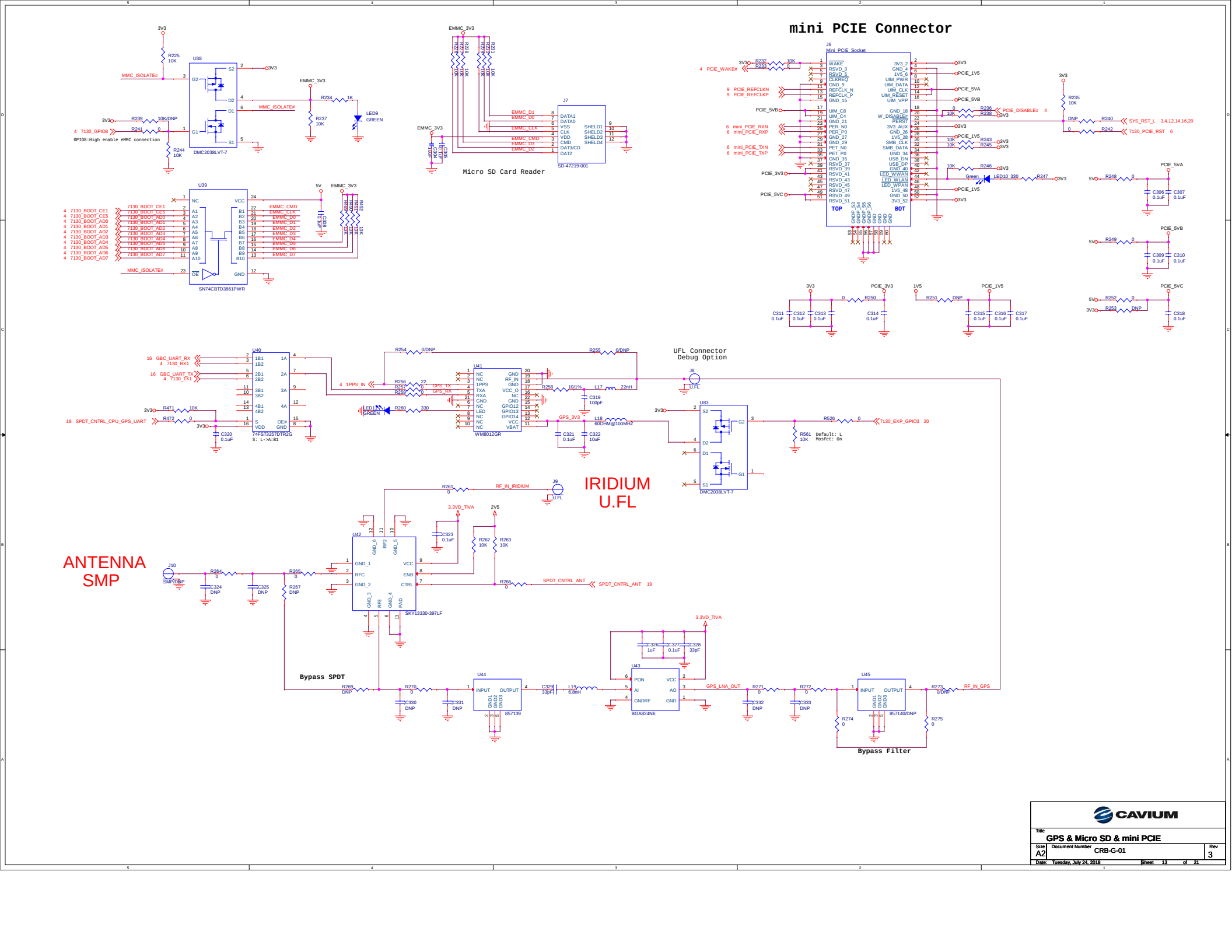
mini PCIE Connector
Micro SD Card Reader
UFL Connector
Debug Option
IRIDIUM
U.FL
ANTENNA
SMP
Bypass SPDT
Bypass Filter
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GPS & Micro SD & mini PCIE
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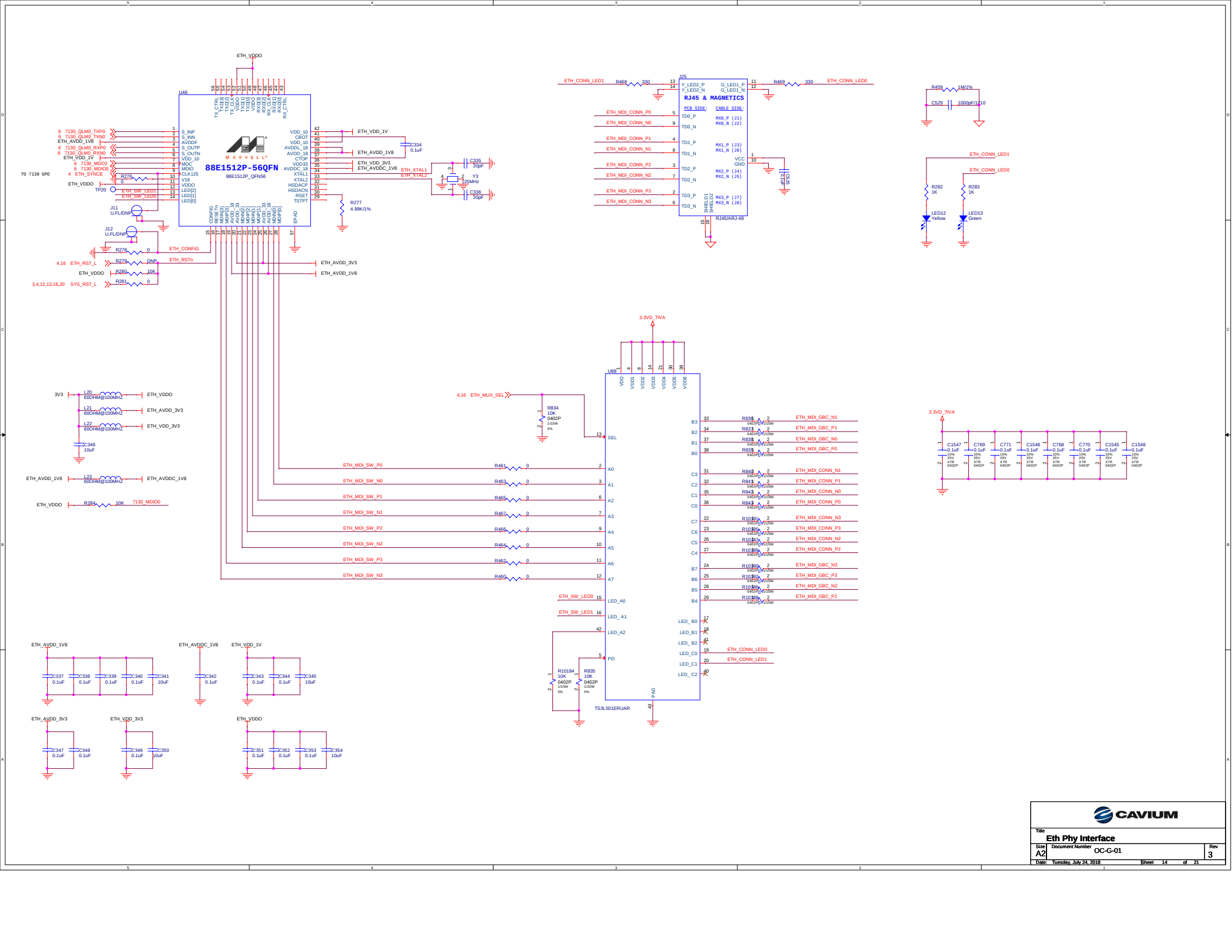

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Title	Eth Phy Interface	
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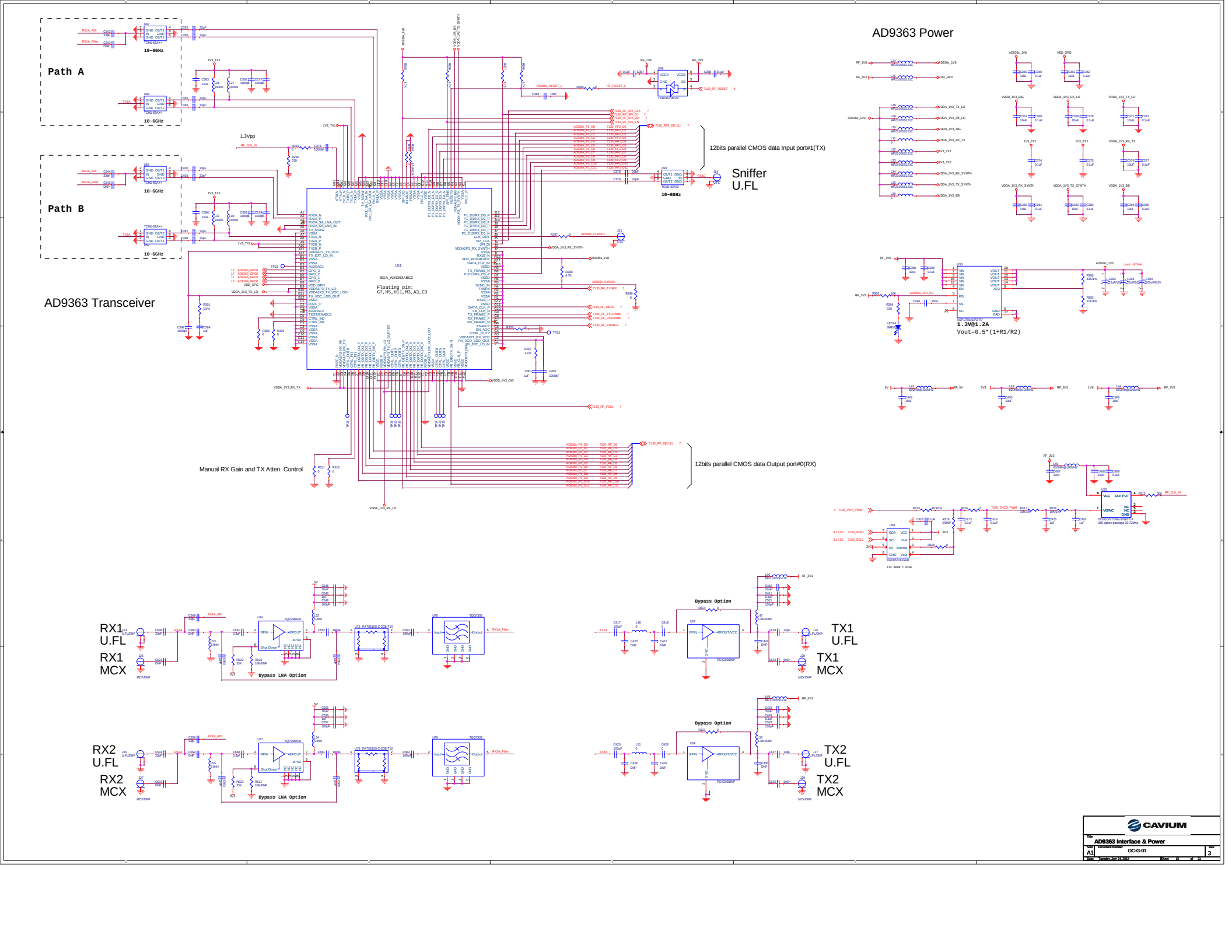
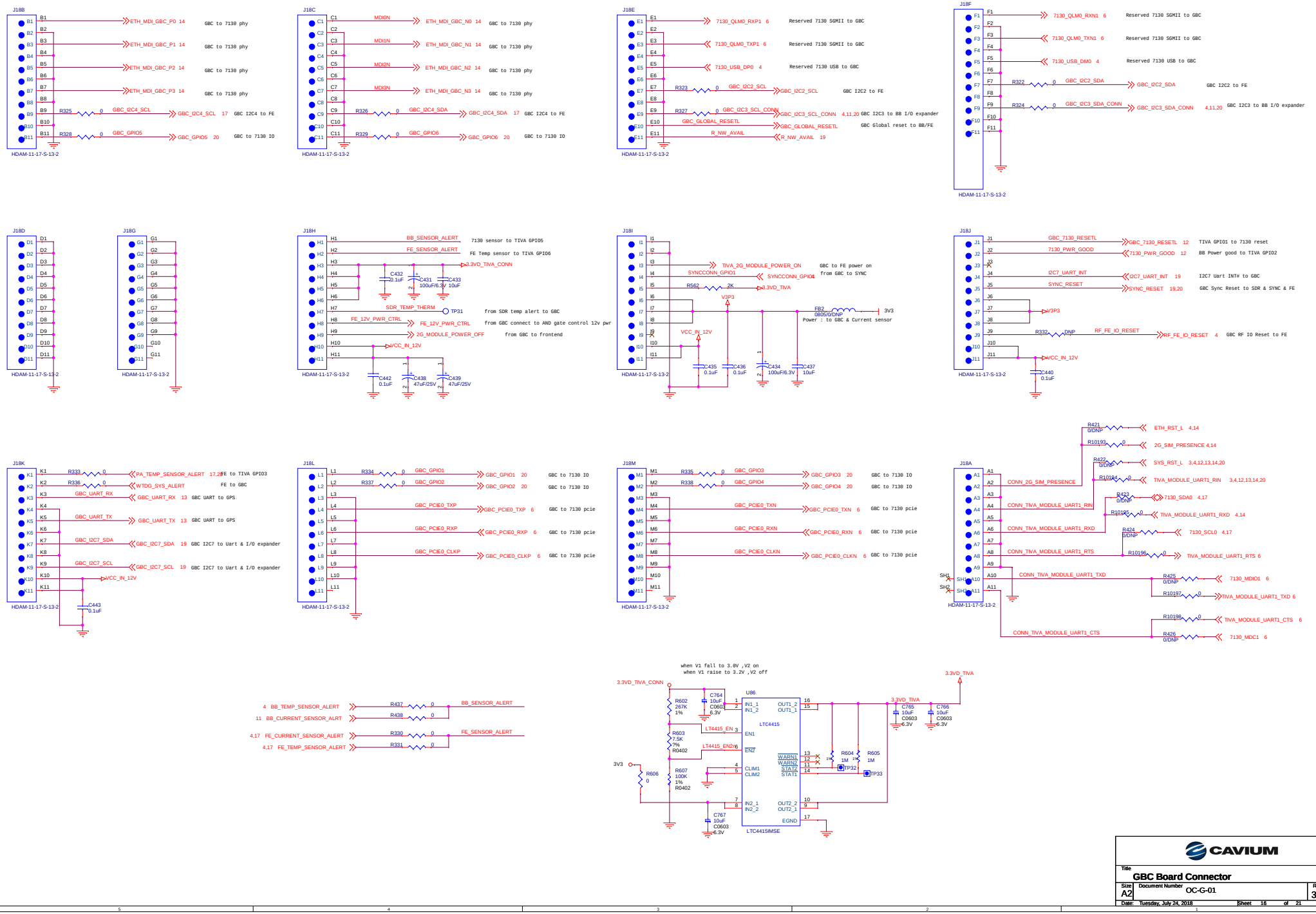

Path A
Path B
AD9363 Transceiver
AD9363 Power
Sniffer U.FL
12bits parallel CMOS data Input port#1(TX)
12bits parallel CMOS data Output port#0(RX)
Manual RX Gain and TX Atten. Control
1.3Vpp
Floating pin: G7,H5,H11,M3,A3,C3
BGA_AD9363ABCZ
1.3W@1.2A
Vout=0.5*(1+R1/R2)
RX1 U.FL
RX1 MCX
RX2 U.FL
RX2 MCX
TX1 U.FL
TX1 MCX
TX2 U.FL
TX2 MCX
Bypass LNA Option
Bypass Option
CAVIUM
AD9363 Interface & Power
OC-G-01



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Title: GBC Board Connector

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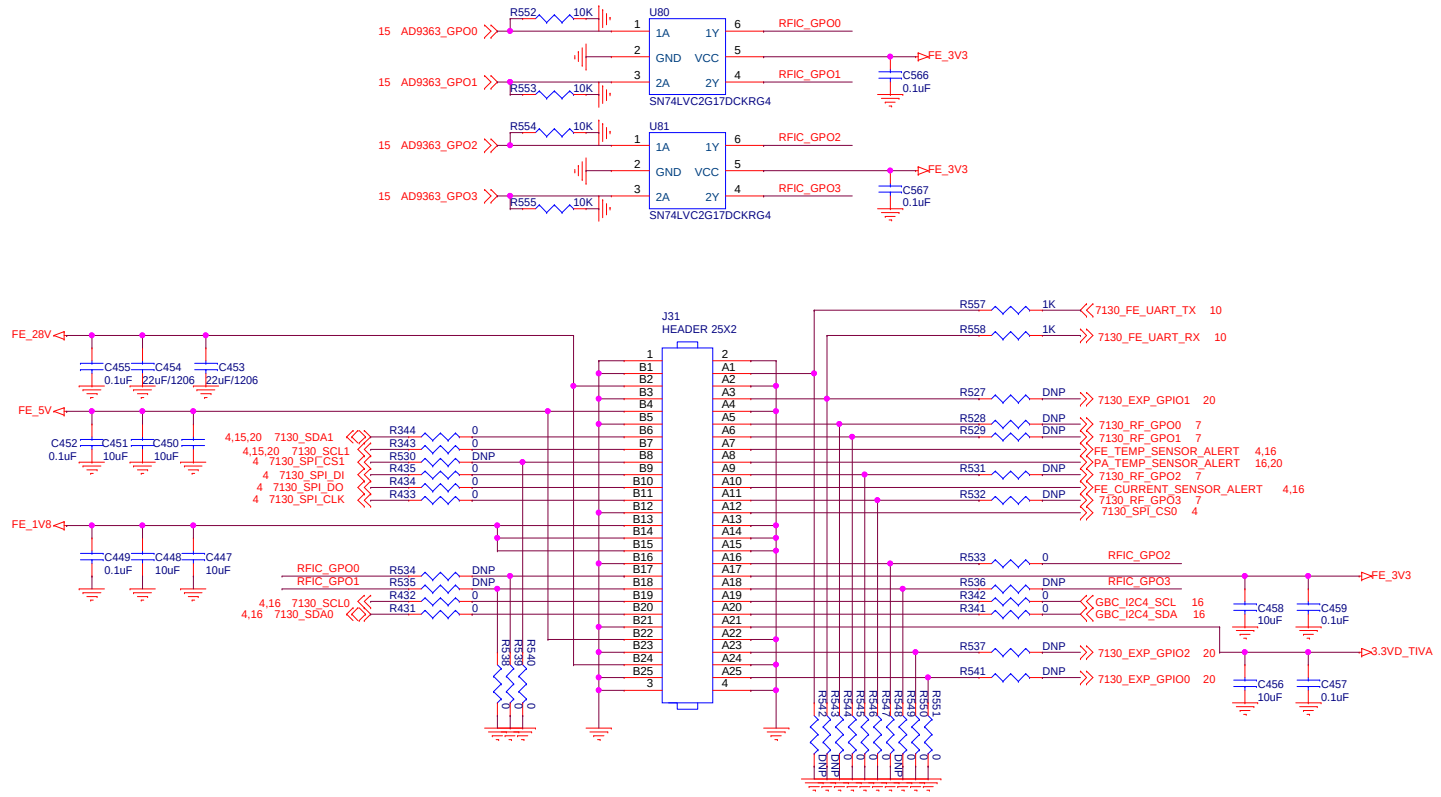
Front End Board Connector



Title	Front End Board Connector		
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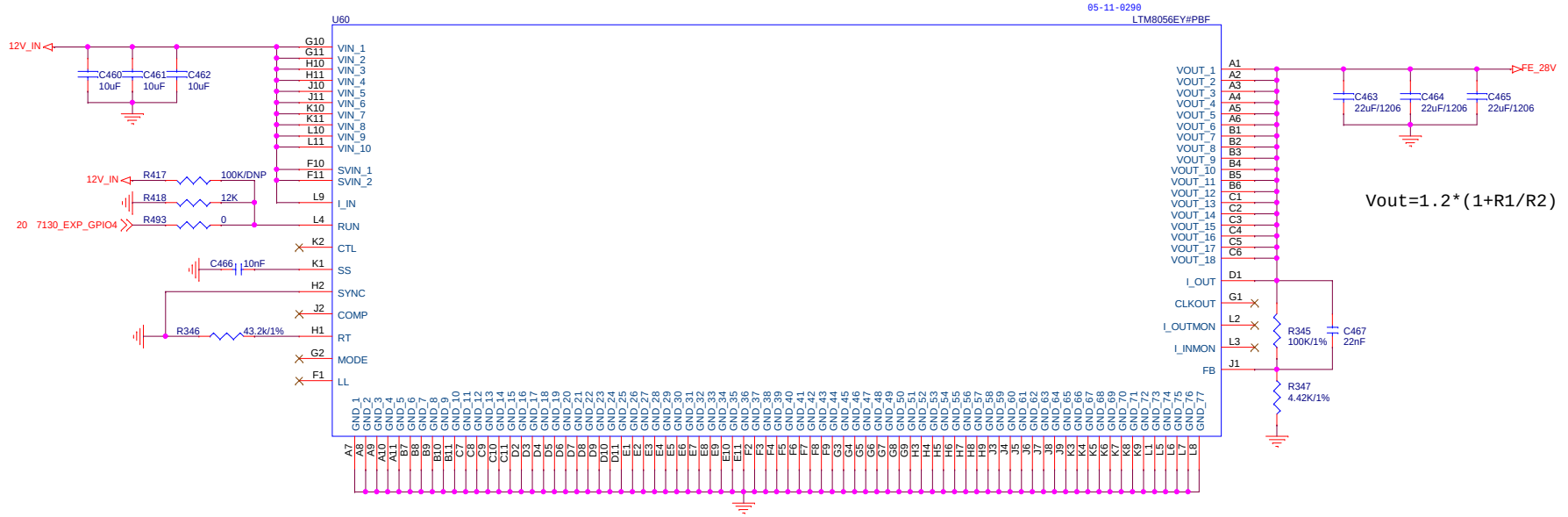

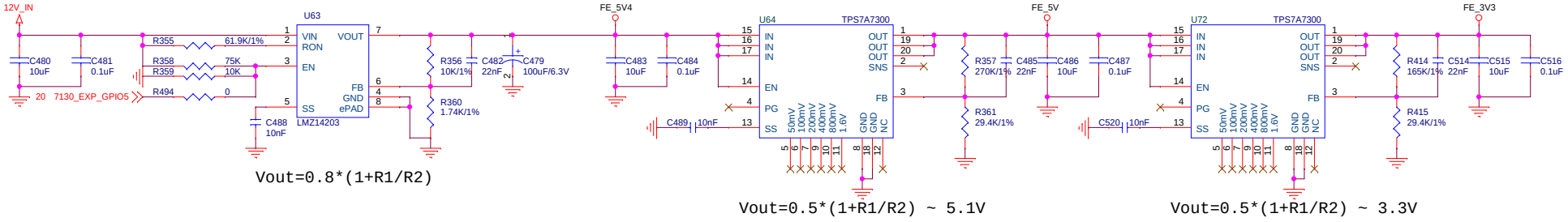

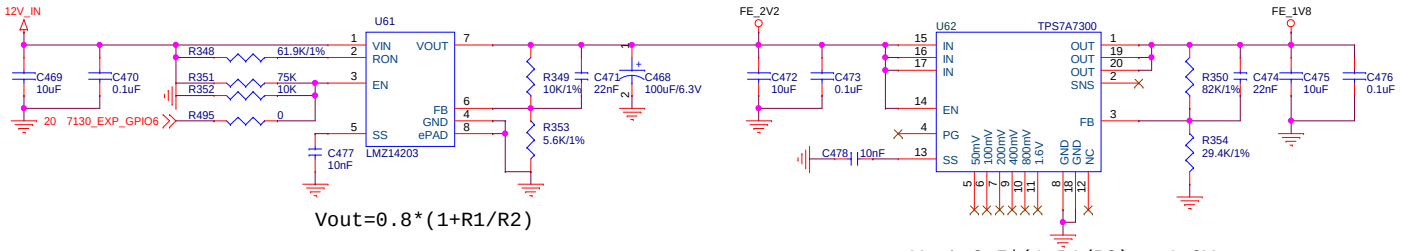

CAVIUM

Title
Front End Board Power

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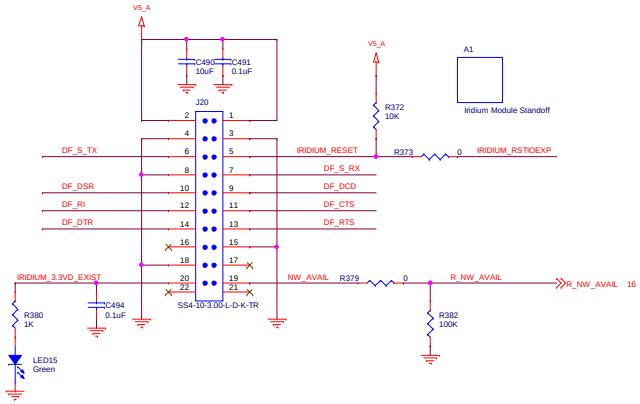
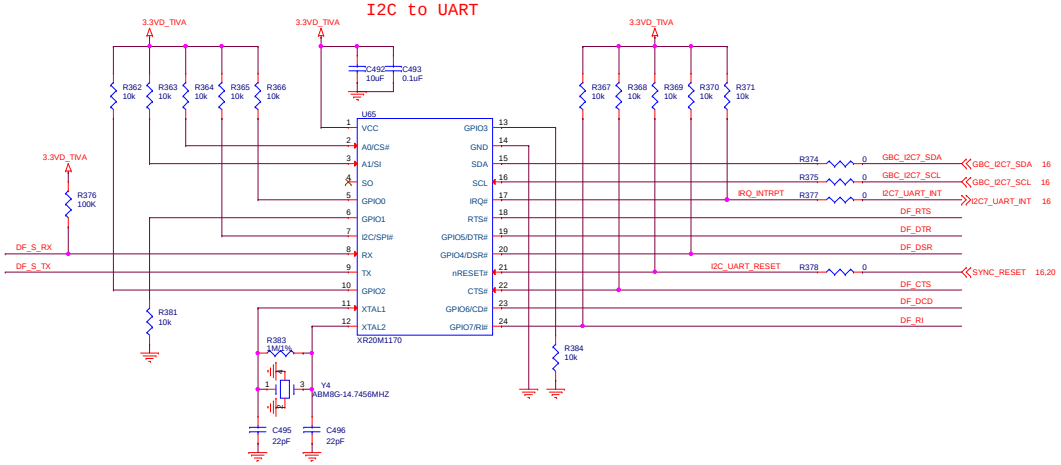
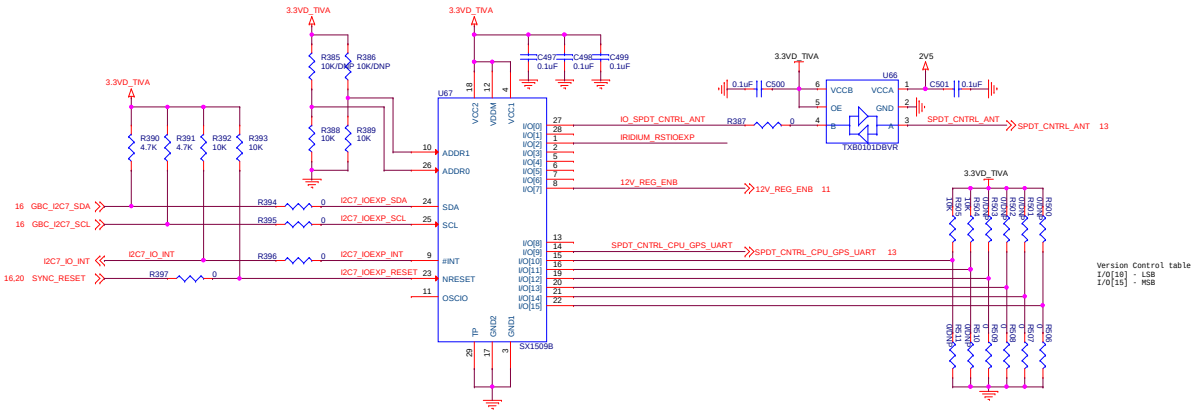
IRIDIUM CONNECTOR

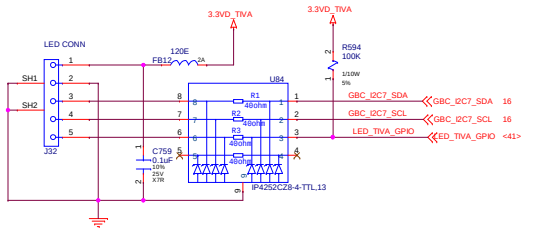


I2C to UART



IO EXPANDER





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Title: IRIDIUM & I2c to UART

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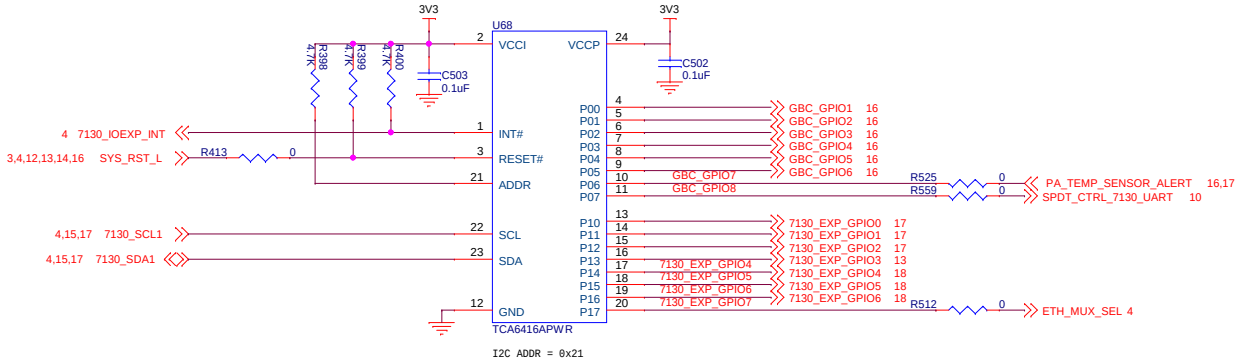
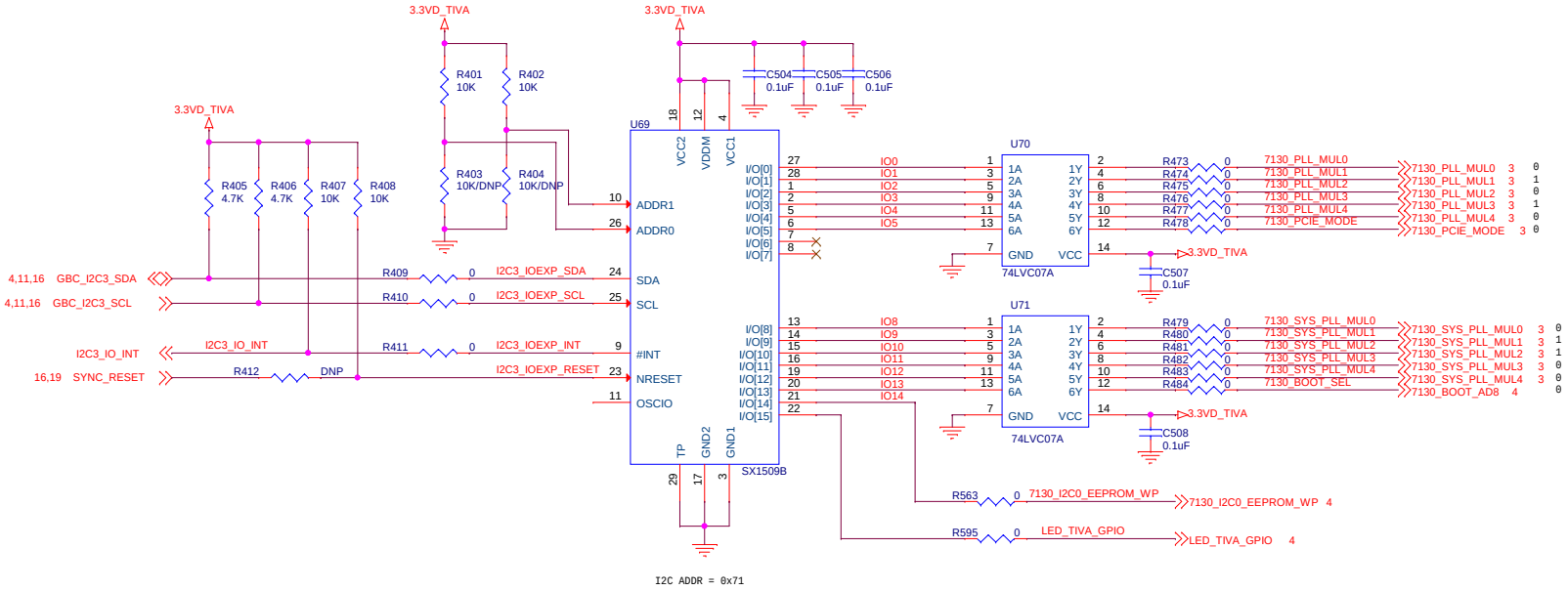
7130 IO EXPANDER



I2C3 IO EXPANDER



CAVIUM

Title: **GBC I2C3 & 7130 I/O Expander**

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T.B.D

Layout Notes:

1. Discrete (especially resistors) should be placed close to Large components which are on the same schematic page

NOTES, UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES IN OHMS.
2. CAPACITANCE VALUES IN MICROFARADS.
3. REFERENCE DESIGNATORS USED.
4. ALL 0.1 uF CAPACITORS ARE DECOUPLING CAPS UNLESS OTHERWISE NOTED. THEY ARE SHOWN ON THE PAGE WITH THE INTEGRATED CIRCUITS THEY SHOULD BE PLACED NEAR.
5. BOARD PROPERTIES:
   - A. FR-4 RoHS COMPLIANT MATERIAL PER IPC-4101/129 OR BETTER
   - B. ALL SIGNAL LAYERS - 0.5 OZ CU
   - C. PLANE LAYERS - 0.5 OZ CU
   - D. IMPEDENCE CONTROL:
     50 OHMS +/- 10% SINGLE ENDED TRACES
     60 OHMS +/- 10% SINGLE ENDED TRACES
     90 OHMS +/- 10% SINGLE ENDED TRACES
     100 OHMS +/- 10% DIFFERENTIAL TRACES
   - E. LAYER STACKUP:

CAVIUM

Title: **HF Return Path Capacitor**

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