CN8100-GBCv2

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REVISION HISTORY

REV	DESCRIPTION	DATE
1.0	initial version	2017-12-12
1.1	1.modfiy ethernet swith to KSZ9897R 2. modify clk distribution to microsemi solution 3. add power supply(1.2V,2.5V) for KSZ9897R	2018-1-18
1.1.1	1. change ddr4 to DDR4 SO-DIMM 2.update reset squence and spi flash,delete boot nand 3.add TPM ,modify SPI connection	2018-3-12 2018-3-13
1.1.2	1. updated the packages of many part 2. add IDT PTP module 3. modify uart,iic etc. 4. add power monitor,temp sensor etc	2018-3-14
1.1.3	1. delete the LT8640 and ORING power switch, page30 2. add power block diagram page5 3.connect tiva_syncconn_gpio1 to U82 4.modify some error of offpage connector name 5.add isolation between SDR and TIVA/SOC 6.add function block diagram page4	2018-3-29
1.1.4	1.update the iic device of tiva in blockdiagram and circult,page3 2.modify PTP connection accord IDT recommendations.page49 3.add OCT power control switch and 2pin header at page30. 4.add two eeprom for TIVA saving ID,inventory. page45 5.update the pcb_footprint of all components 6. remove LT8640 at page30	2018-3-30
1.1.5	1.Modify some part's pin name to generate list rightlly(U9,U86,U22-U25) 2.reannotate the part's reference 3. Don't place R178 4.update uSD connector 5.Add MTGHOLE at page52. 6.modified schemaitc accoard the excel review list v1.6, 7.update table content 8.modify ethsw to KSZ9897S,,add R769page 20,21 add SGMII path from ethsw to octeon.dlm1 ,page20 through out PME signal to TIVA,page20 through out IBA signal to TIVA,page20 9.delete TRXFE power ,page35, As will powering RF through separate cable from power board T 10,change R312 TO 150K 11. modify the errors according the review list ver0.17 12. modifiy KSZ9897S to KSZ9567S,Add syncE option. page20 13. modify errors on ksz9897s base MicroChip's review, page20 14, add syncE option ,page49.	2018-4-11
1.1.6	1.add series resistor,R777~R780, at page40 2.Modifiy some resistor to DNP, at page51 3. modify some component's footprint,and part-number 4.modify JTB1 pin2,pin3 to V12P0, JTB1 pin5,pin4 to GND,page30 5.Modify S1 same as S2, Modify RJ45/J10/JTAG pcb_foorprint. 6.delete the no-used connection to Rsvd-pin on mini-pcie.page28,page29 7.modify BT1 same with BT2	2018-4-20
1.1.7	1.update power block,page4 2. add 12V backup related circult (LTC4419), page30, 3.add super cap for tiva/tpm/ir, page54 4.add IR sensor, 5.delete T2,J27, modify ethsw port1,port2 connect to FX18-40s-0.8sh . 6.add U89, page53, 7. modify OCT strapping resistor, connect PLL configuration to U89,page53 8,connect BOOT method configer to U89 page53	2018-4-23
1.1.8	1.add USB hub 2.add 0ohm resistor(package=25120 for DVT test) 3.modify J13,J15 pcb footprint 4.Delete D13~D15,C485,C486,C488 5.change J2 package 6,add J32,Buzzer circult add led:D34,D35,D36,D39,D40,D41,D42,D43,D44,D45 7,Add MH2,MH3 8.modify default boot method to SPI 9.modify J3M2 PCB Footprint with mount ing hole 10.add c908,c909	2018-4-27
1.1.9	1. add U92 ,U93,U94,C910~C912 2.add JP2,R908 3.bring back U38,U39 related circuit for TRXFE_12V at page35	2018-5-4
1.1.10	1.add R909,R910,R911,R912,R913,R914,R915,R916,R917 2.modify MH16 pcb footprint, 3.modify some error net	2018-5-7
1.1.11	1.Change R796.1 to GND, setting core clock defult 1.5G(Since the CPU max speed is1.5Ghz)	2018-5-9

REV	DESCRIPTION	DATE
1.2	1. Remove V5P0_EN,V3P3_EN from TIVA to U33,U28 respectively, 2.delete R767,R916, Place R339 3.Delete R910 ,Connect R368 to V3P3 4.Delete net: SATA0_LED_N,SATA1_LED_N, 5.add R918,R919 0ohm 6.Connect TIVA PP0,PP1 to J31 as UART IF 7,Connect TIVA_FE_RESET_OUT to TIVA PM2 8.Connect TIVA_USER_LED1/2 to IO expander 9.use TIVA PD0/PD1 as IIC7,connect to LED board, add R920,R921 2.2k 10.Add U96,U97 11. Add U95 related circult for IIC isolation	2018-5-11
1.2.1	1.modify T1 connection order for easily layout 2.modify U59~U62 pin order for easily layout 3.add jtag chain,R925~R937 0ohm for jtag chain 4.add D46,D47 ESD protection diode	2018-5-15
1.2.2	1.Add TRXFE_DET net for BB board present detection 2.add TIVA waken function page42	2018-5-17
1.2.3	1.add EBMP feature at page8, add U100,J33	2018-5-25

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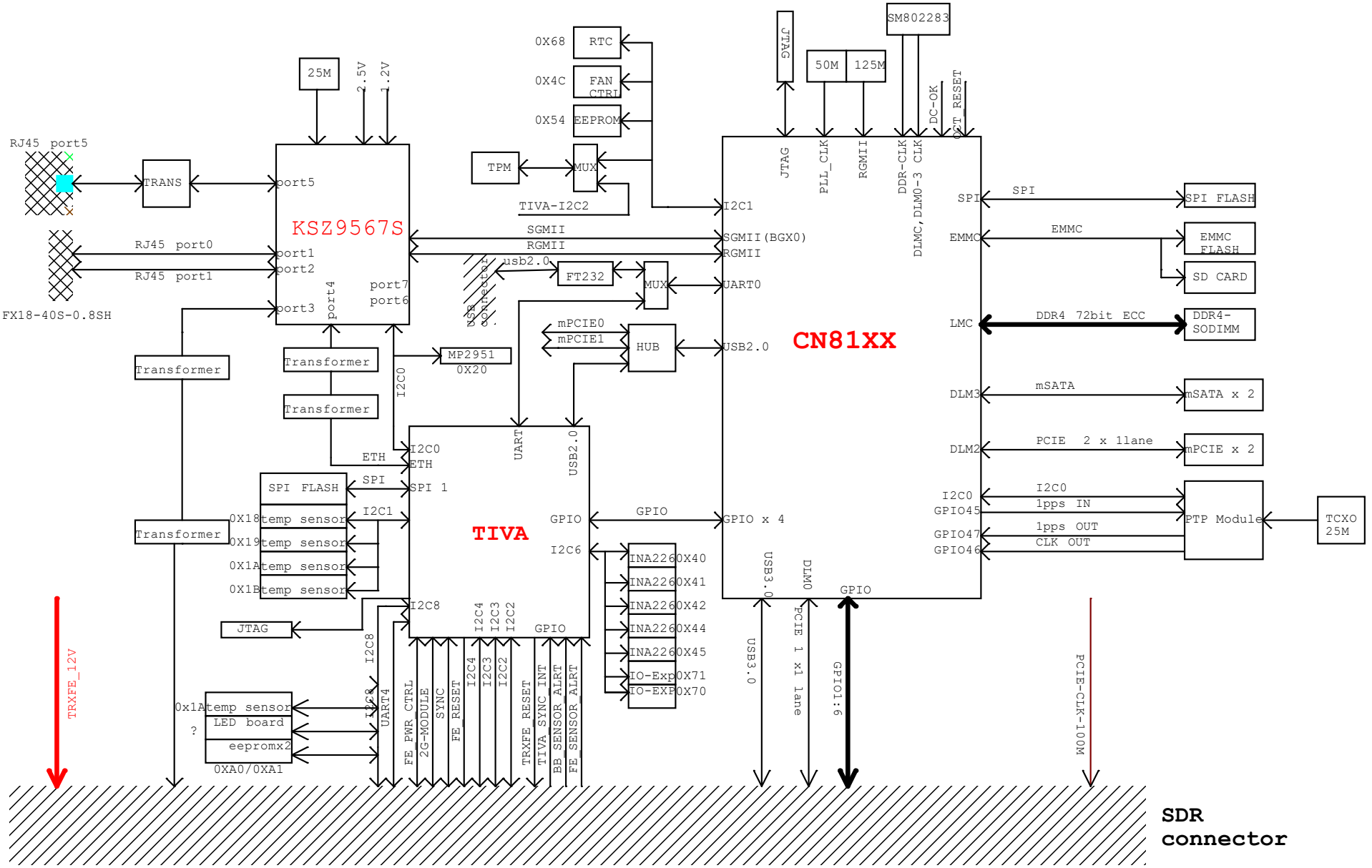

ICD TEST CONNECTOR

Need confirm and discuss

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Title: FUNCTIONAL BLOCK DIAGRAM

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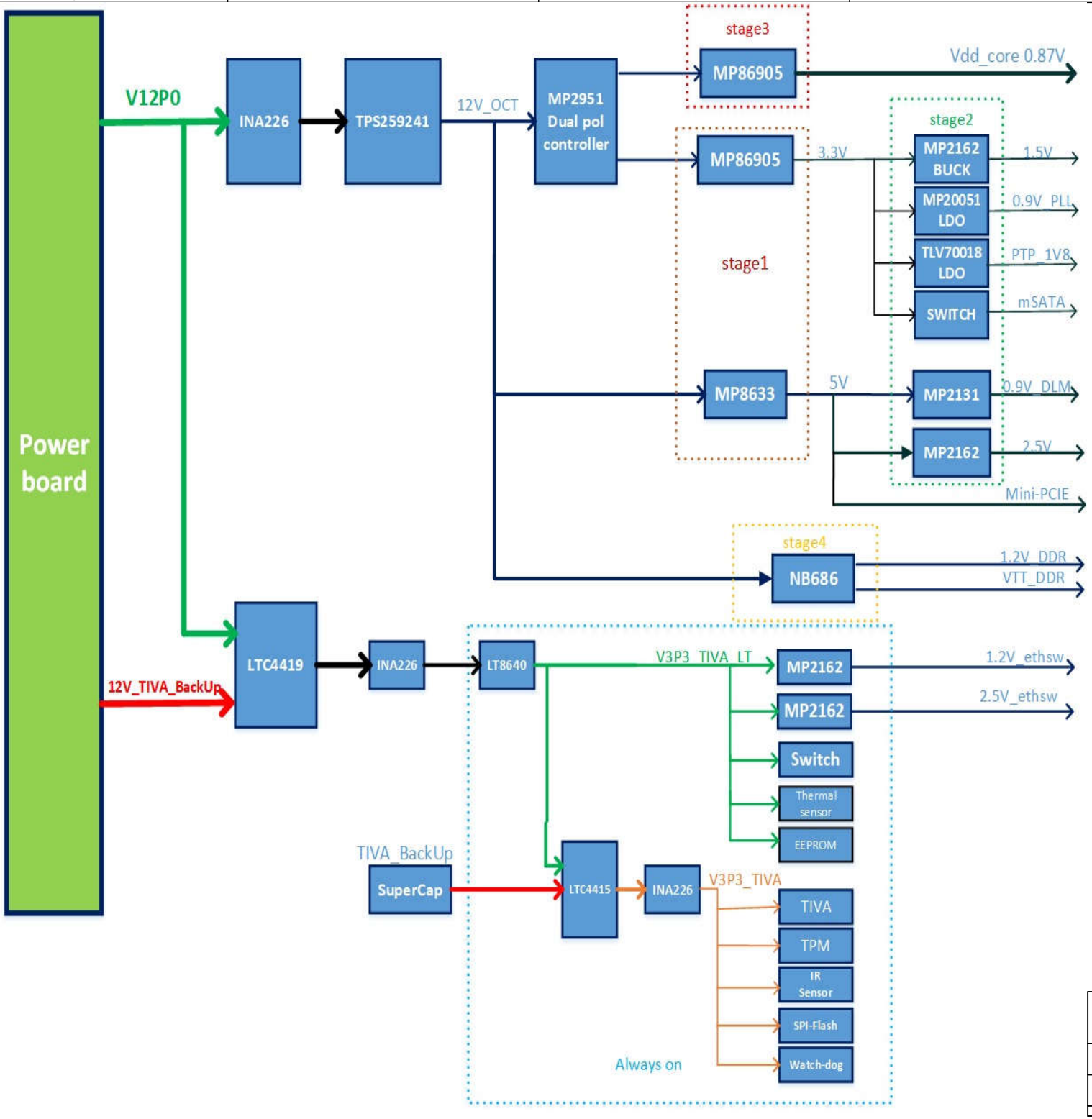

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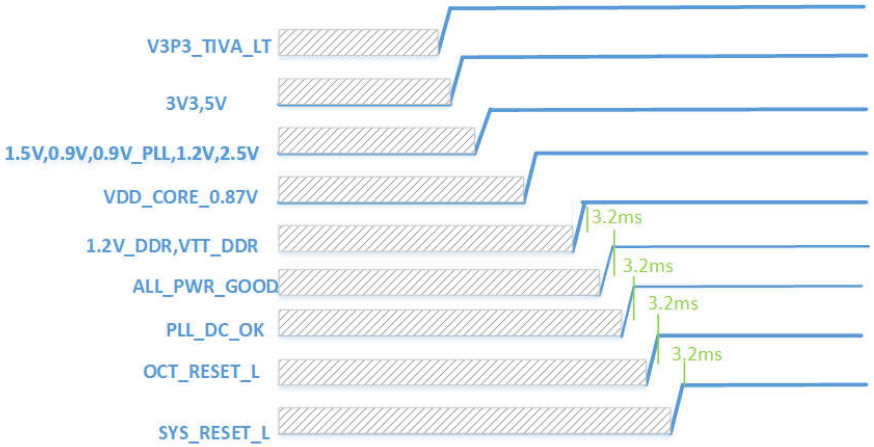

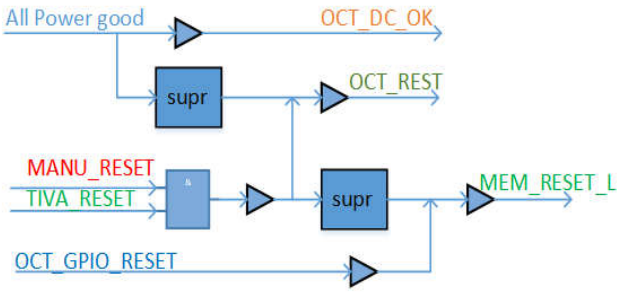

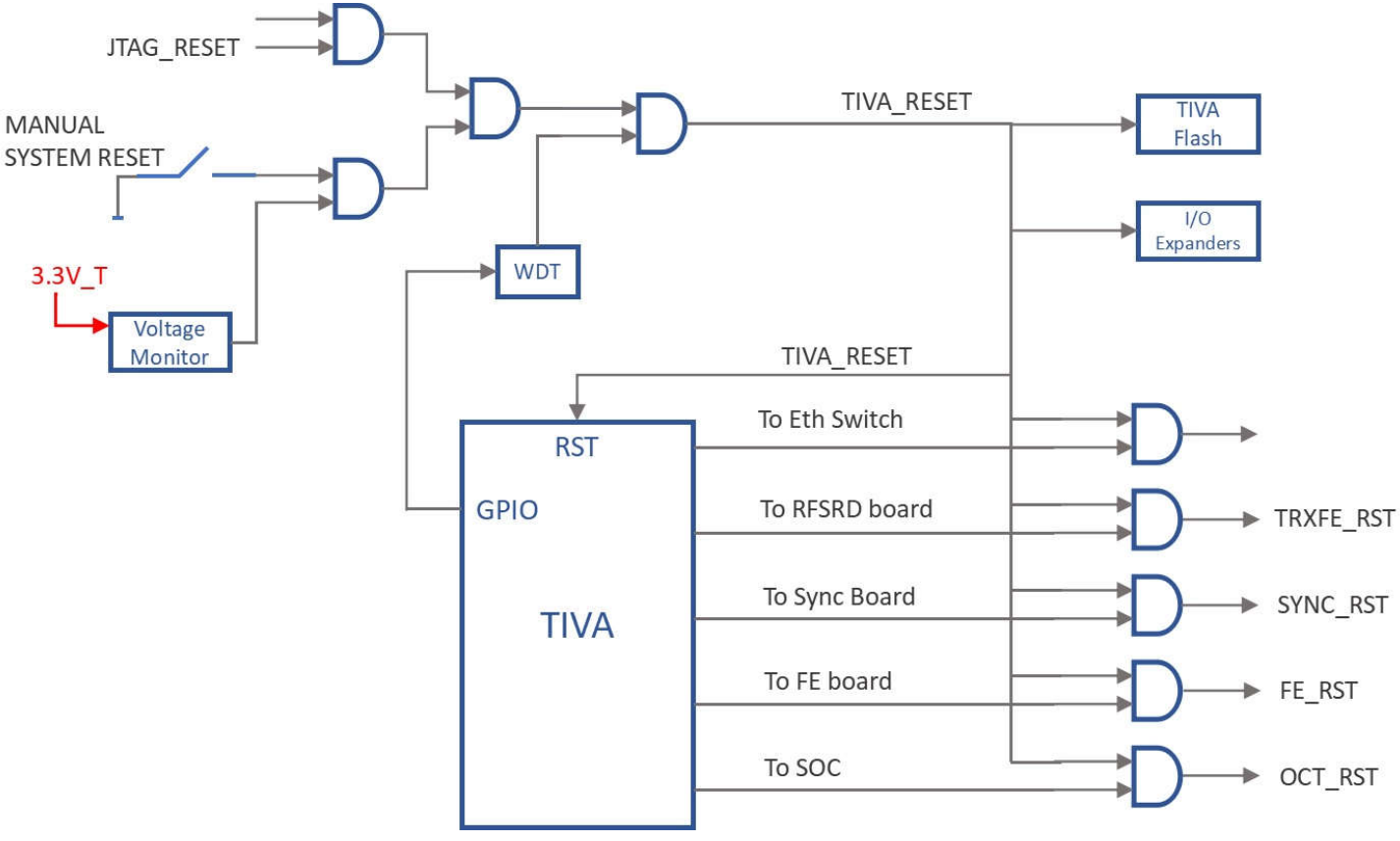

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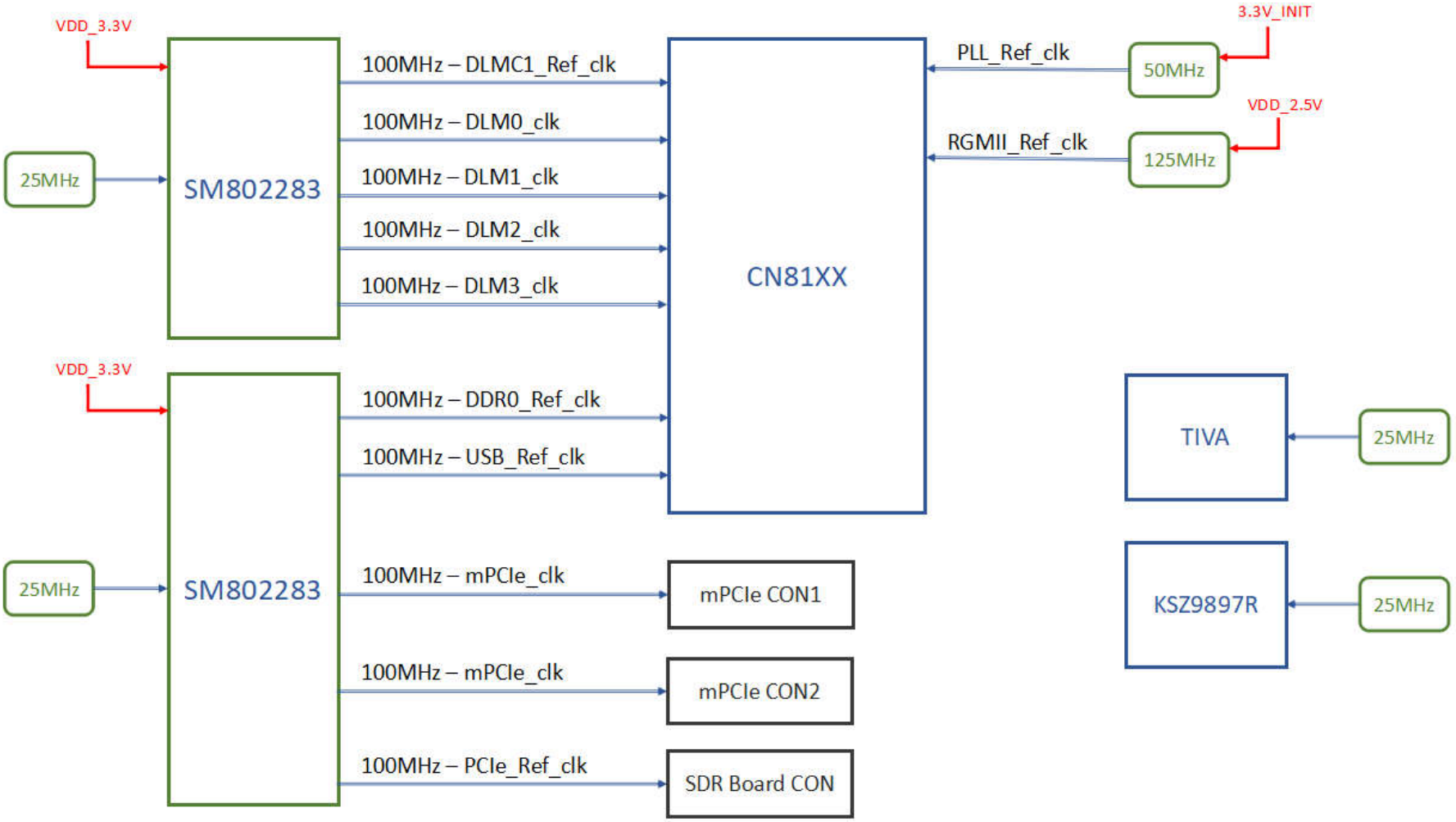

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Title: **CLOCK ARCHITECTURE**

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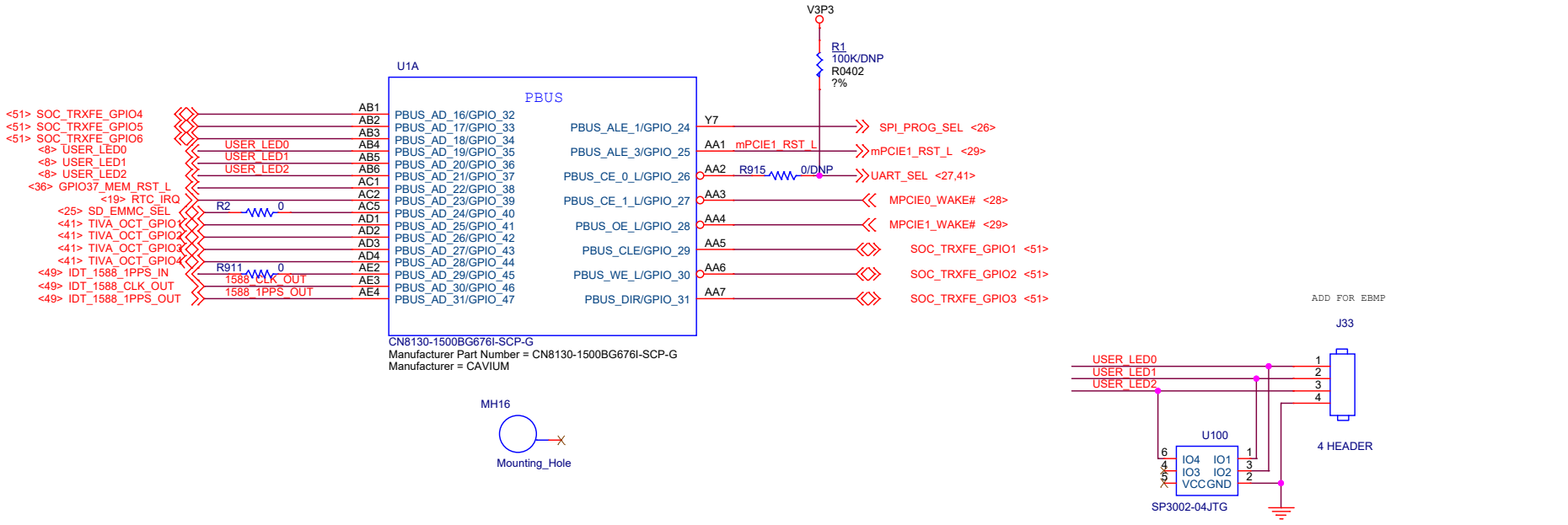

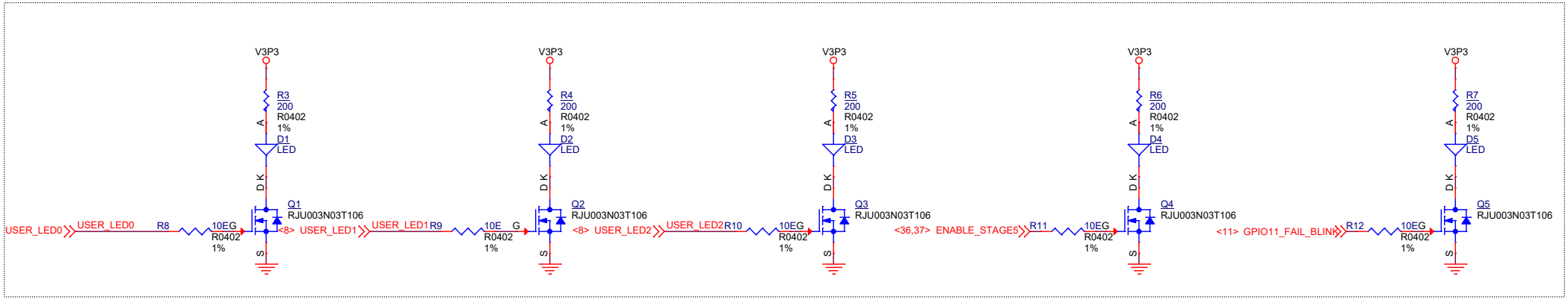

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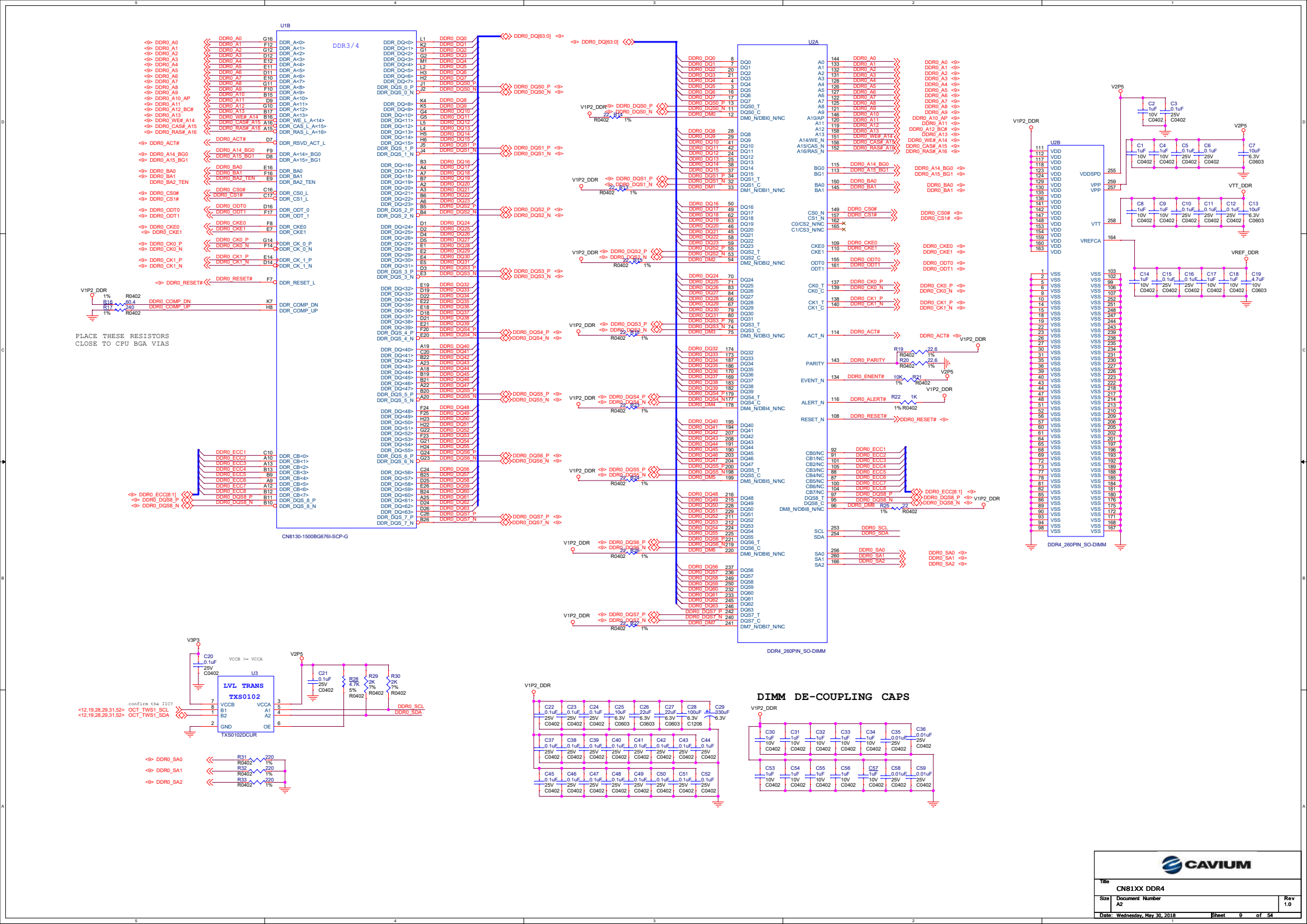
U1B
DDR3/4
CN8130-1500BG676I-SCP-G
U2A
DDR4_260PIN_SO-DIMM
PLACE THESE RESISTORS
CLOSE TO CPU BGA VIAS
U3
LVL TRANS
TXS0102
TXS0102DCUR
DDR4_260PIN_SO-DIMM
DIMM DE-COUPLING CAPS
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DLM Configuration		
DLM#	MAC	OCT IOT/ROUTER Gateway
DLM0	PEM0	1x1 PCIe
DLM1	BGX0	1x1 SGMII
DLM2	PEM1	2x1 PCIE
DLM3	SATA0-1	2X1 SATA

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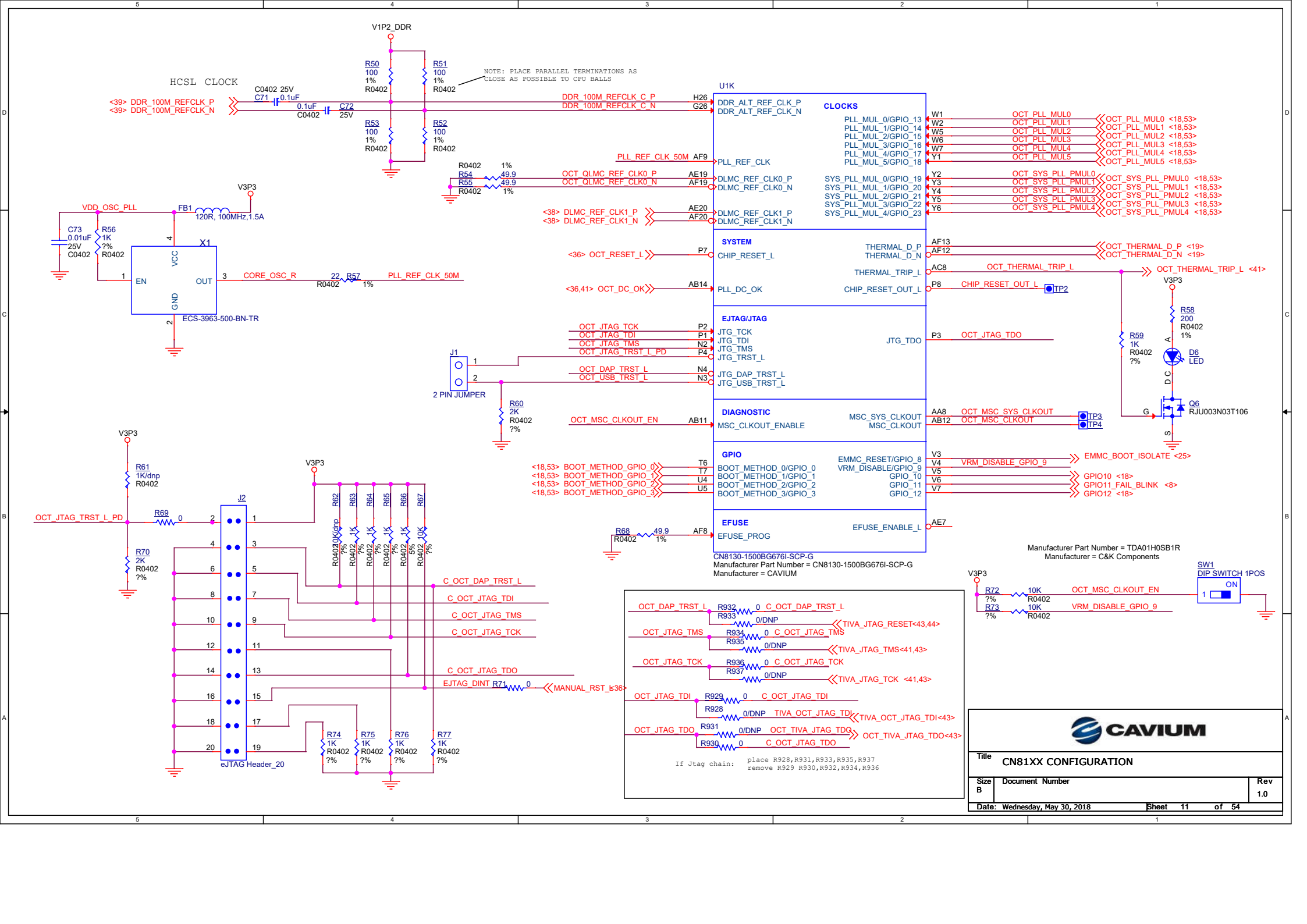
HCSL CLOCK
NOTE: PLACE PARALLEL TERMINATIONS AS CLOSE AS POSSIBLE TO CPU BALLS
U1K
CLOCKS
SYSTEM
EJTAG/JTAG
DIAGNOSTIC
GPIO
EFUSE
CN8130-1500BG676I-SCP-G
Manufacturer Part Number = CN8130-1500BG676I-SCP-G
Manufacturer = CAVIUM
Manufacturer Part Number = TDA01H0SB1R
Manufacturer = C&K Components
2 PIN JUMPER
eJTAG Header_20
ECS-3963-500-BN-TR
RJU003N03T106
If Jtag chain: place R928,R931,R933,R935,R937 remove R929 R930,R932,R934,R936
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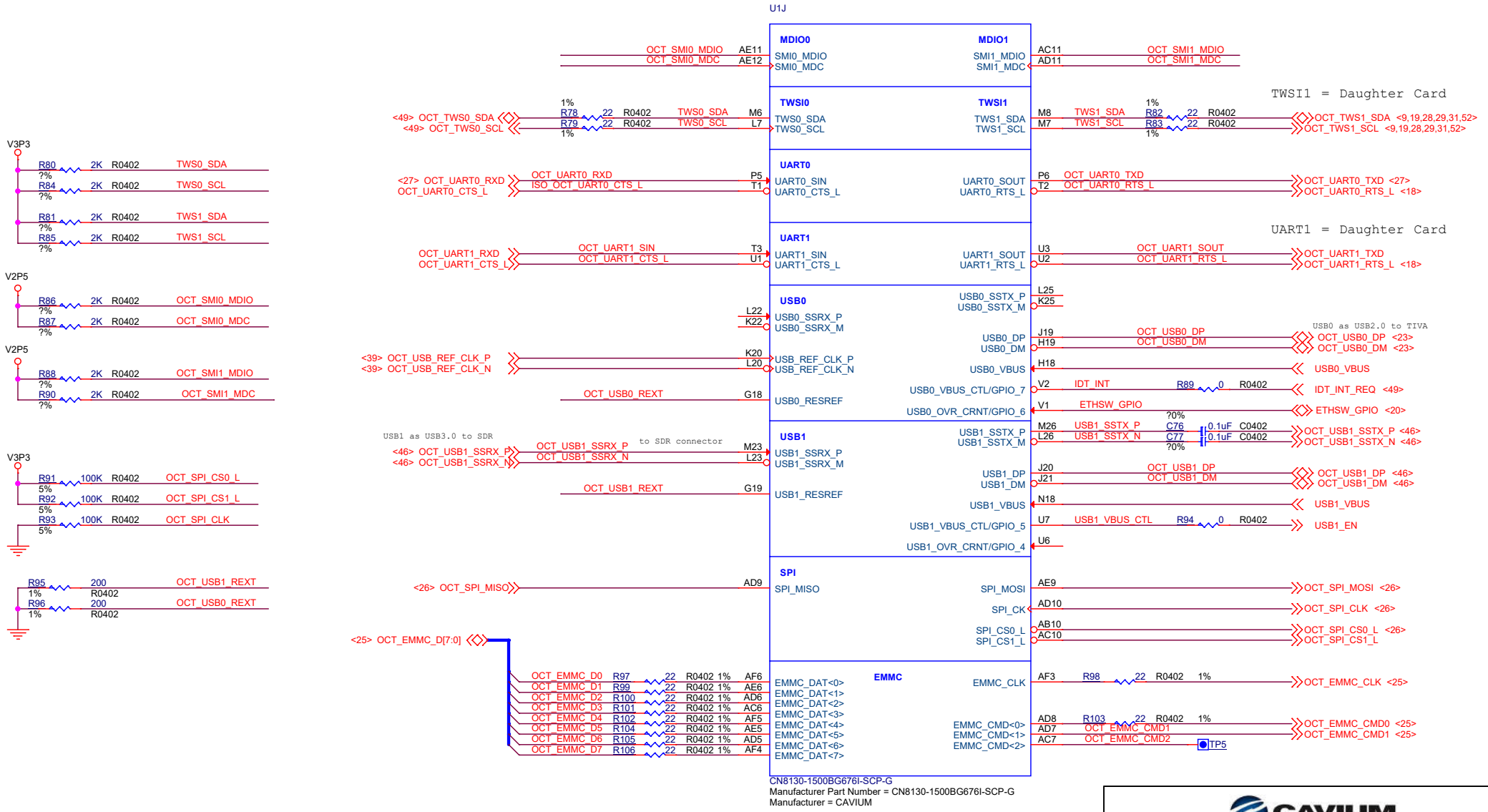
U1J
MDIO0
MDIO1
TWSI0
TWSI1
UART0
UART1
USB0
USB1
SPI
EMMC
TWSI1 = Daughter Card
UART1 = Daughter Card
USB0 as USB2.0 to TIVA
USB1 as USB3.0 to SDR
to SDR connector
CN8130-1500BG676I-SCP-G
Manufacturer Part Number = CN8130-1500BG676I-SCP-G
Manufacturer = CAVIUM
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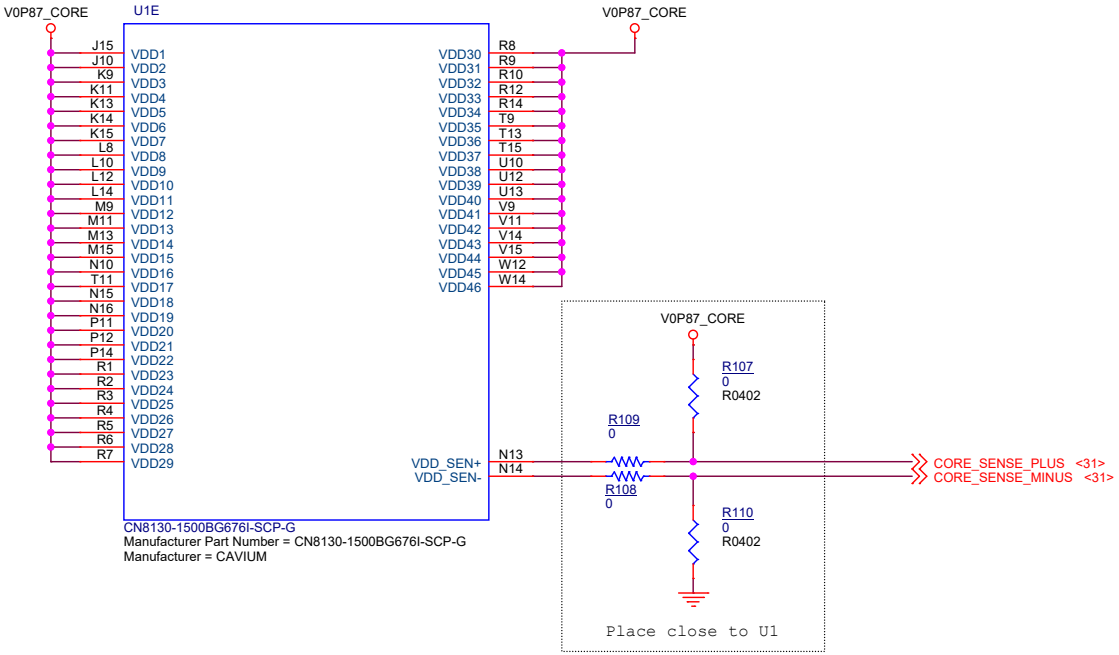

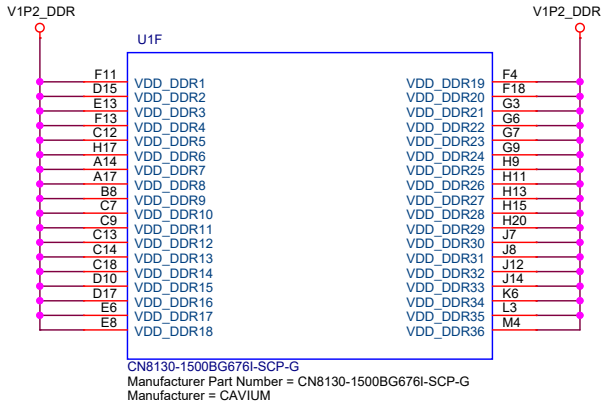

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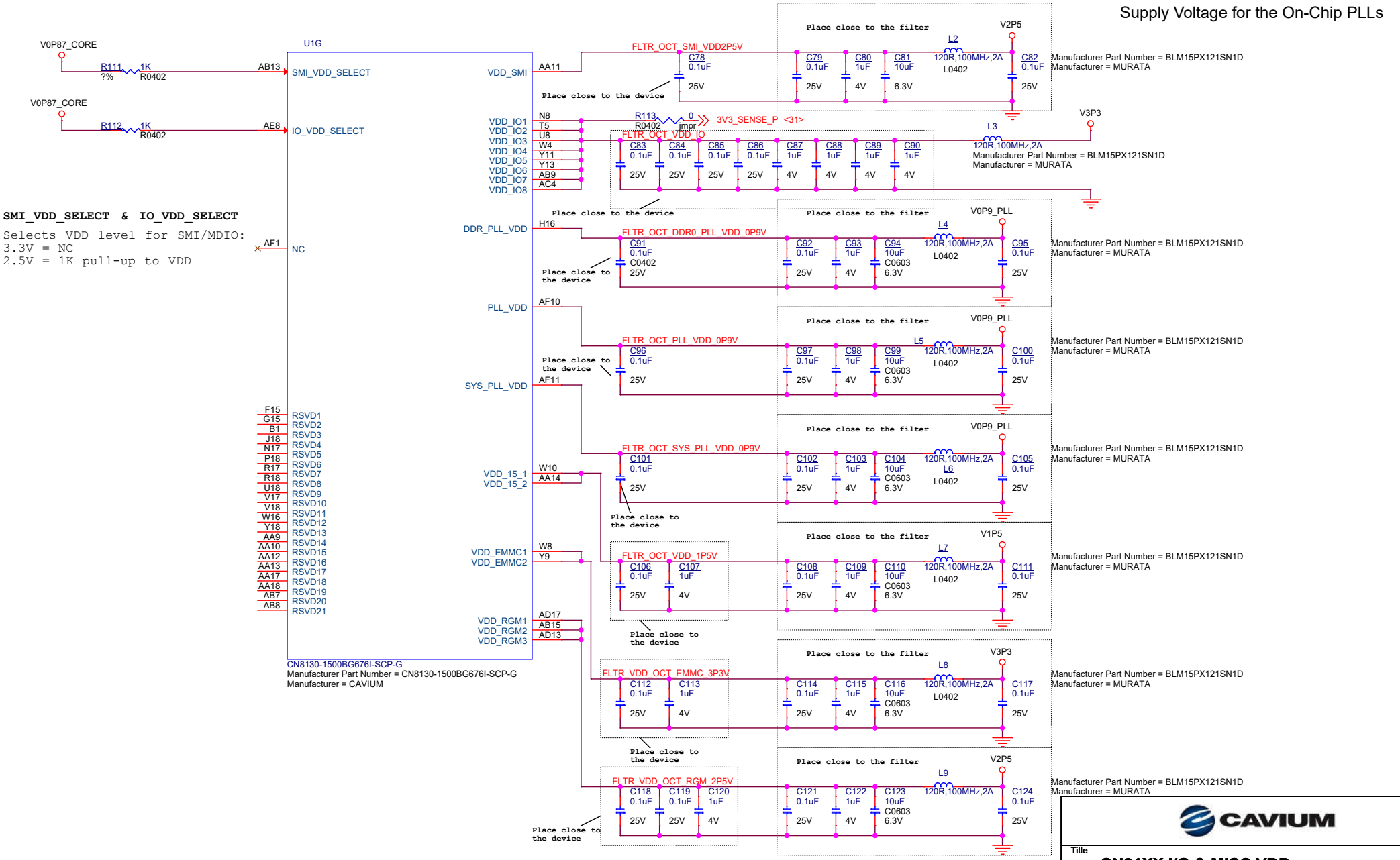
Supply Voltage for the On-Chip PLLs



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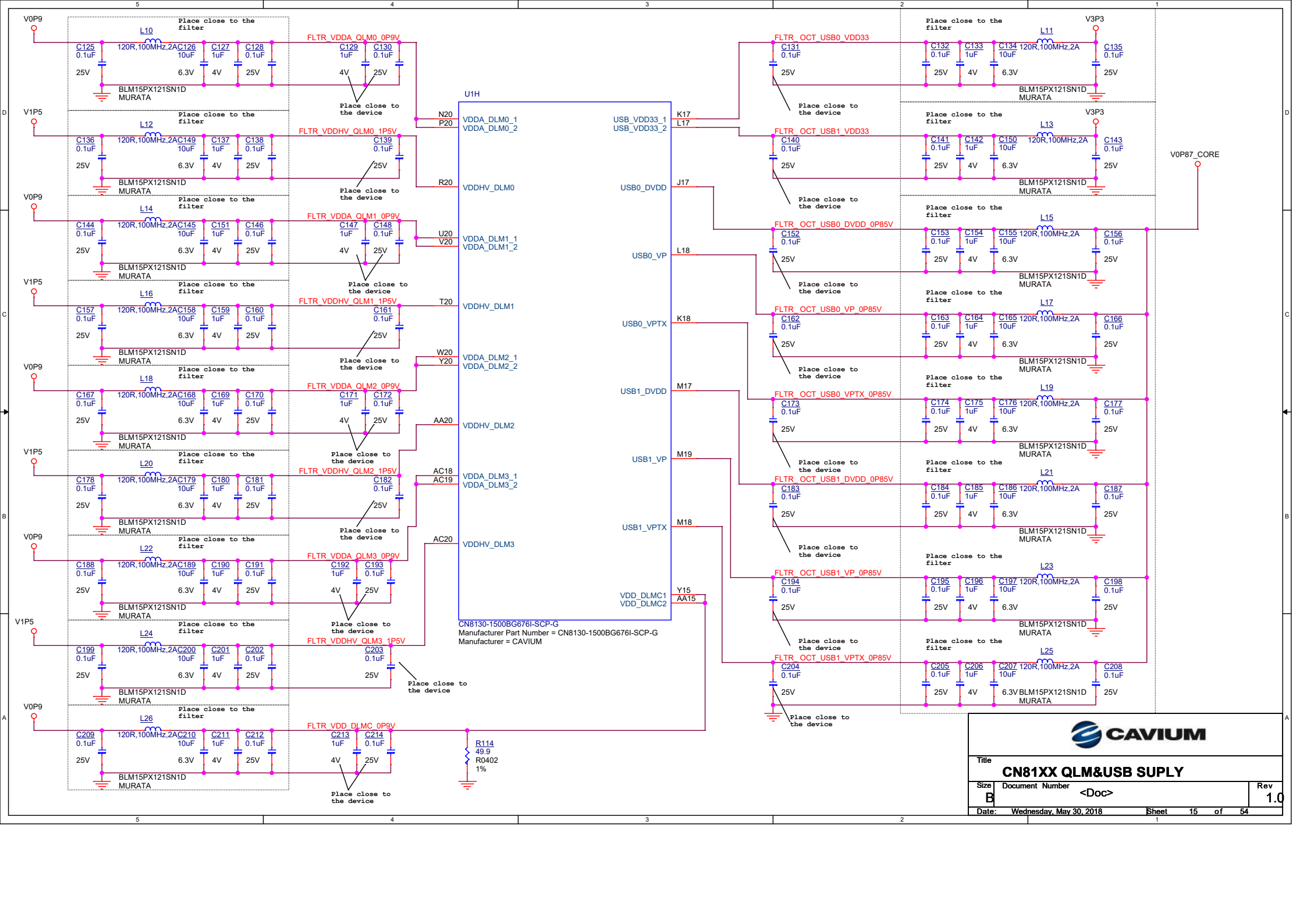
V0P9
V1P5
V3P3
V0P87_CORE
Place close to the filter
Place close to the device
L10
L11
L12
L13
L14
L15
L16
L17
L18
L19
L20
L21
L22
L23
L24
L25
L26
120R,100MHz,2A
BLM15PX121SN1D
MURATA
U1H
CN8130-1500BG676I-SCP-G
Manufacturer Part Number = CN8130-1500BG676I-SCP-G
Manufacturer = CAVIUM
VDDA_DLM0_1
VDDA_DLM0_2
VDDHV_DLM0
VDDA_DLM1_1
VDDA_DLM1_2
VDDHV_DLM1
VDDA_DLM2_1
VDDA_DLM2_2
VDDHV_DLM2
VDDA_DLM3_1
VDDA_DLM3_2
VDDHV_DLM3
USB_VDD33_1
USB_VDD33_2
USB0_DVDD
USB0_VP
USB0_VPTX
USB1_DVDD
USB1_VP
USB1_VPTX
VDD_DLMC1
VDD_DLMC2
FLTR_VDDA_QLM0_0P9V
FLTR_VDDHV_QLM0_1P5V
FLTR_VDDA_QLM1_0P9V
FLTR_VDDHV_QLM1_1P5V
FLTR_VDDA_QLM2_0P9V
FLTR_VDDHV_QLM2_1P5V
FLTR_VDDA_QLM3_0P9V
FLTR_VDDHV_QLM3_1P5V
FLTR_VDD_DLMC_0P9V
FLTR_OCT_USB0_VDD33
FLTR_OCT_USB1_VDD33
FLTR_OCT_USB0_DVDD_0P85V
FLTR_OCT_USB0_VP_0P85V
FLTR_OCT_USB0_VPTX_0P85V
FLTR_OCT_USB1_DVDD_0P85V
FLTR_OCT_USB1_VP_0P85V
FLTR_OCT_USB1_VPTX_0P85V
R114
49.9
R0402
1%
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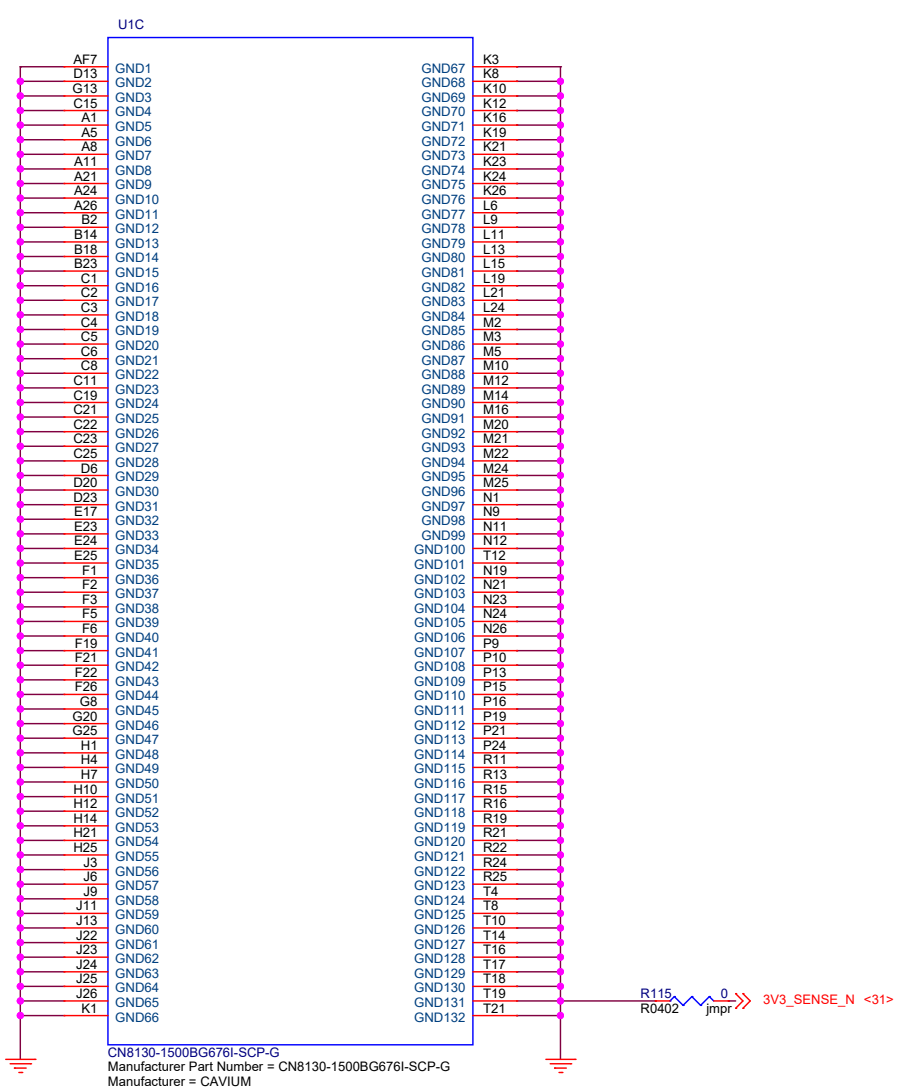

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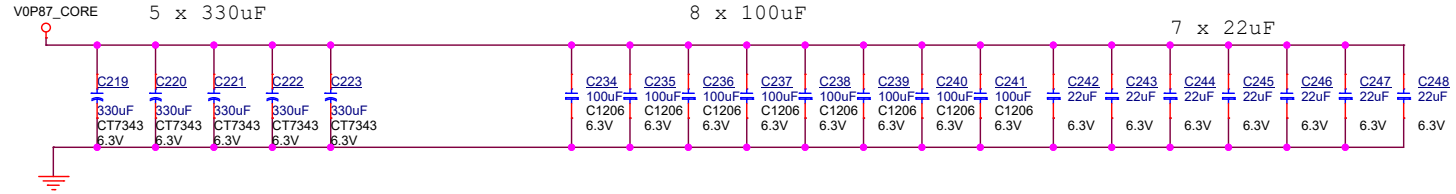
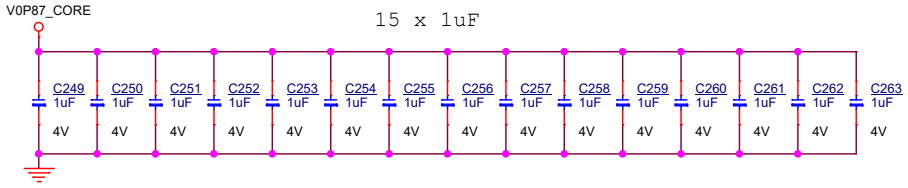
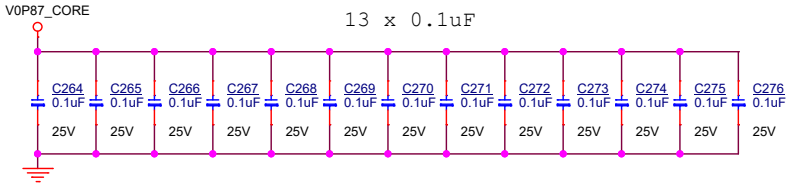
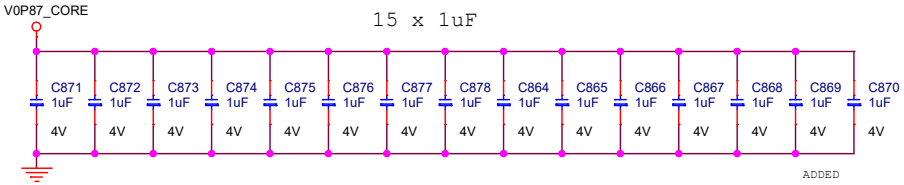
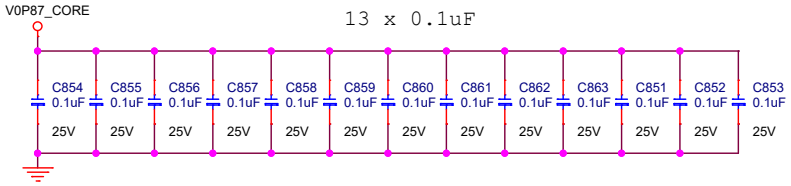
Delete C215~C218



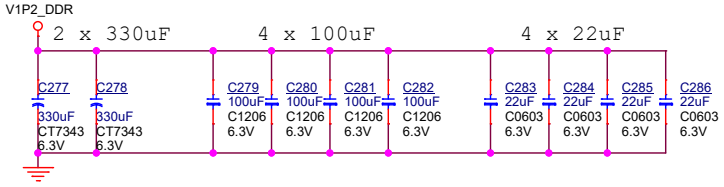


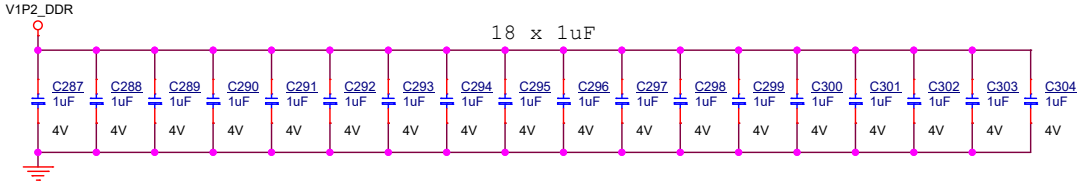


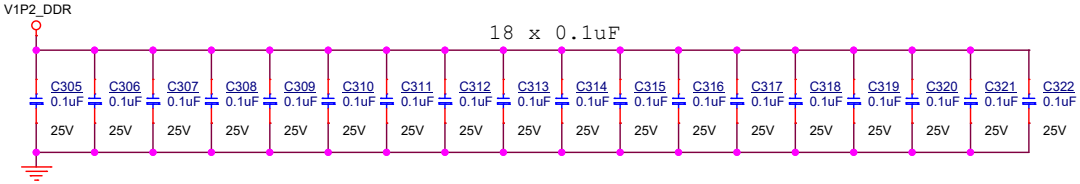




Layout Note: Use 10 mil for power vias







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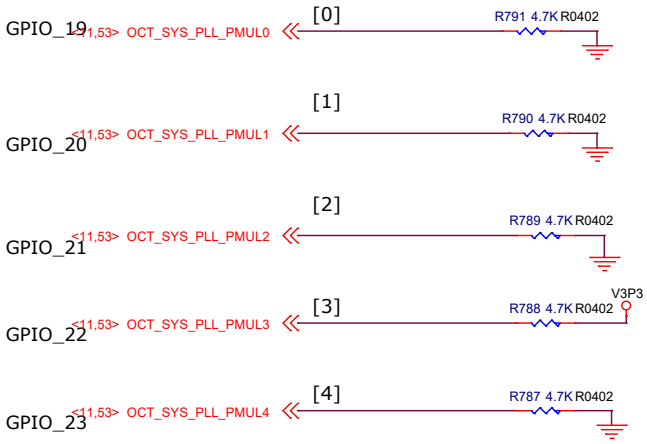
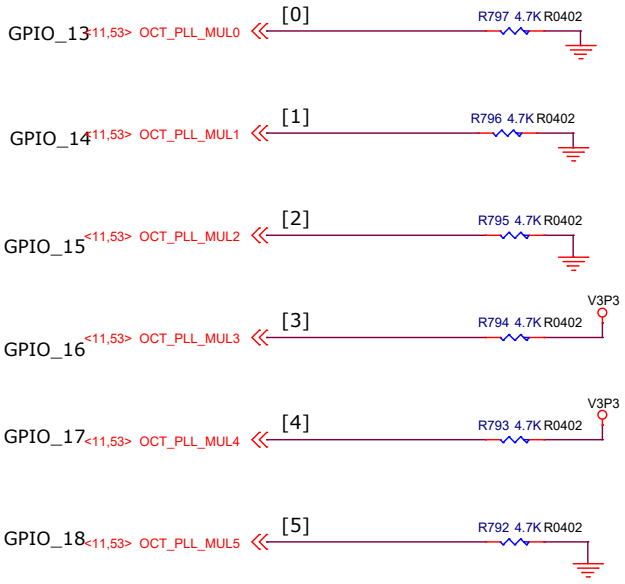
Coprocessor-clock (SCLK) PLL multiplier



Description :

0 0 0 0 1	= 350 MHz.
0 0 0 1 0	= 400 MHz.
0 0 0 1 1	= 450 MHz.
0 0 1 0 0	= 500 MHz
0 0 1 0 1	= 550 MHz.
0 0 1 1 0	= 600 MHz.
0 0 1 1 1	= 650 MHz.
0 1 0 0 0	**= 700 MHz. (DEFAULT)**

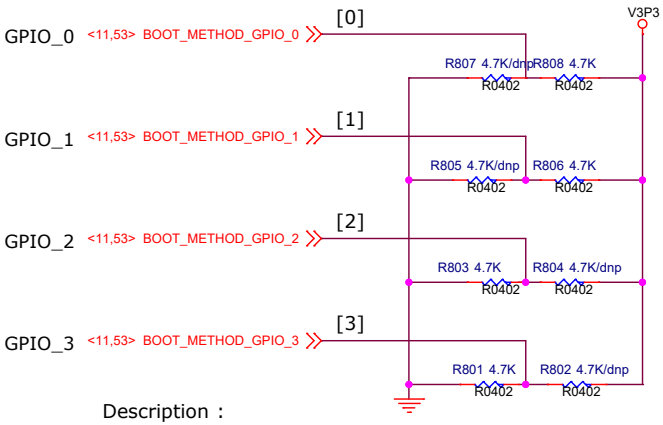
Core-clock (RCLK) PLL multiplier



Description :

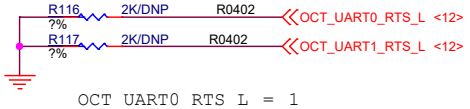
0 0 0 0	0 1 1 0	= 600 MHz.
0 0 0 0	1 0 1 0	= 800 MHz.
0 0 0 0	1 1 1 0	= 1000 MHz.
0 0 0 1	0 0 1 0	= 1200 MHz.
0 0 0 1	0 1 1 0	= 1400 MHz.
0 0 0 1	1 0 0 0	**= 1500 MHz.(DEFAULT)**
0 0 0 1	**1 0 1 0**	**= 1600 MHz.**
0 0 0 1	1 1 1 0	= 1800 MHz.
0 0 1 0	0 0 1 0	= 2000 MHz.

RST Boot-strap Method Enumeration

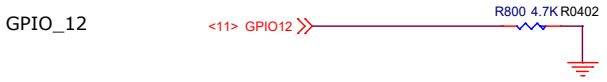


Description :

0 0 1 0	= EMMC_SS
0 0 1 1	= EMMC_LS (Default boot from SD
0 1 0 1	**= SPI24**
0 1 1 0	= SPI32
1 0 0 0	= REMOTE
1 0 0 1	= CCPI0
1 0 1 0	= CCPI1
1 0 1 1	= CCPI2
1 1 0 0	= PCIE0
1 1 0 1	= PCIE2

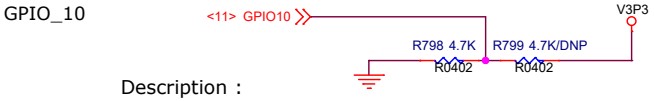



```
OCT_UART0_RTS_L = 1
OCT_UART1_RTS_L = 1
PLL_SOURCE = PLL_REF_CLK
```



During flash boot, reserved.
Post-boot, free for board use.

Trusted-mode



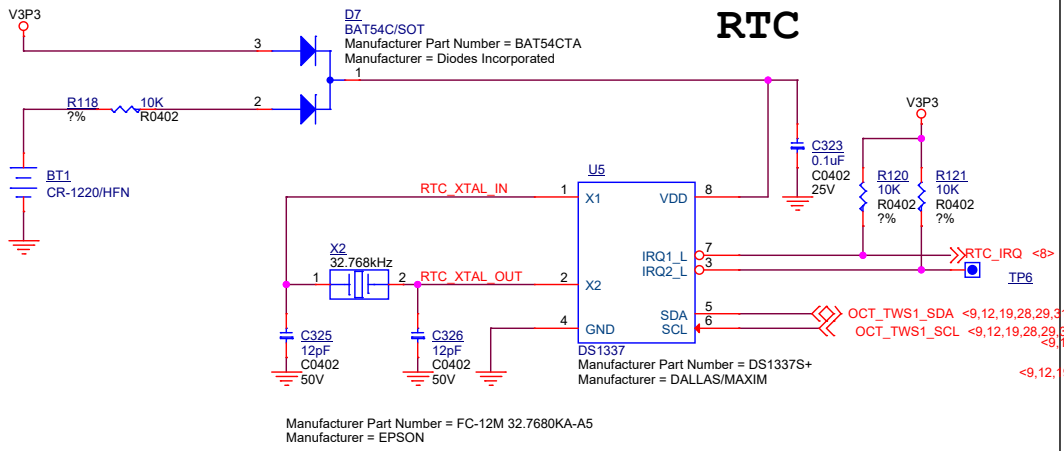
Description :

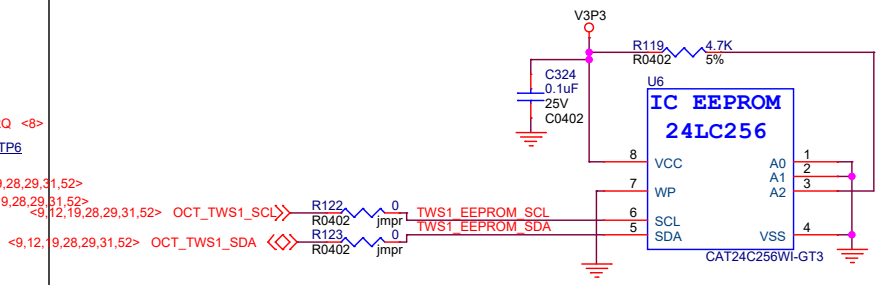
0 = Non-trusted boot.

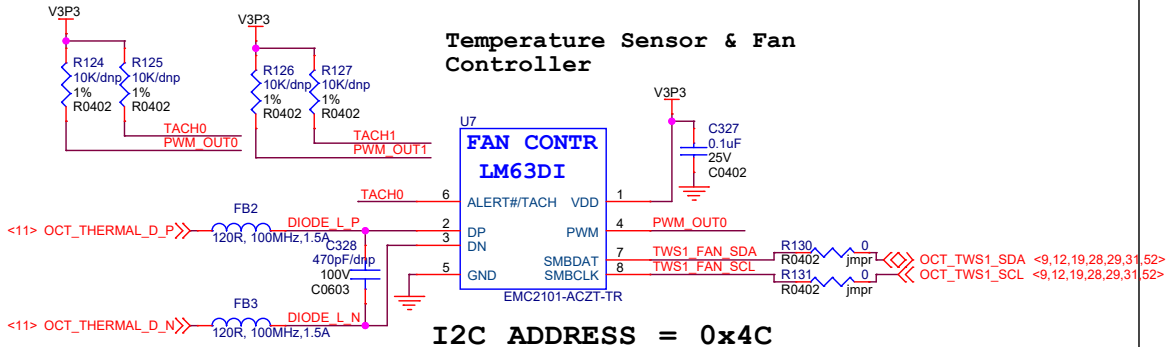
1 = Trusted boot.

CAVIUM

Title	**CN81XX STRAPPING**	
Size: B	Document Number: <Doc>	Rev: 1.0
Date: Wednesday, May 30, 2018	Sheet 18 of 54	

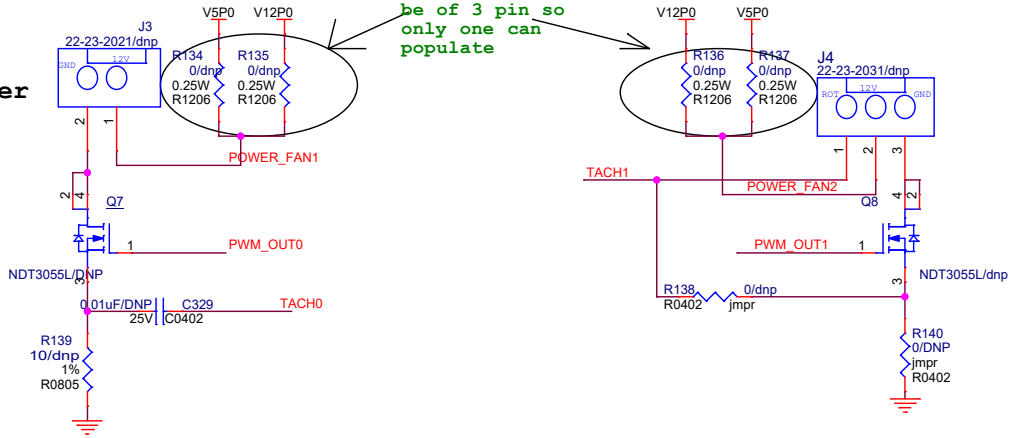






I2C ADDRESS = 0x4C

BGA Fan Header



Layout Notes:
Resistors should be of 3 pin so only one can populate

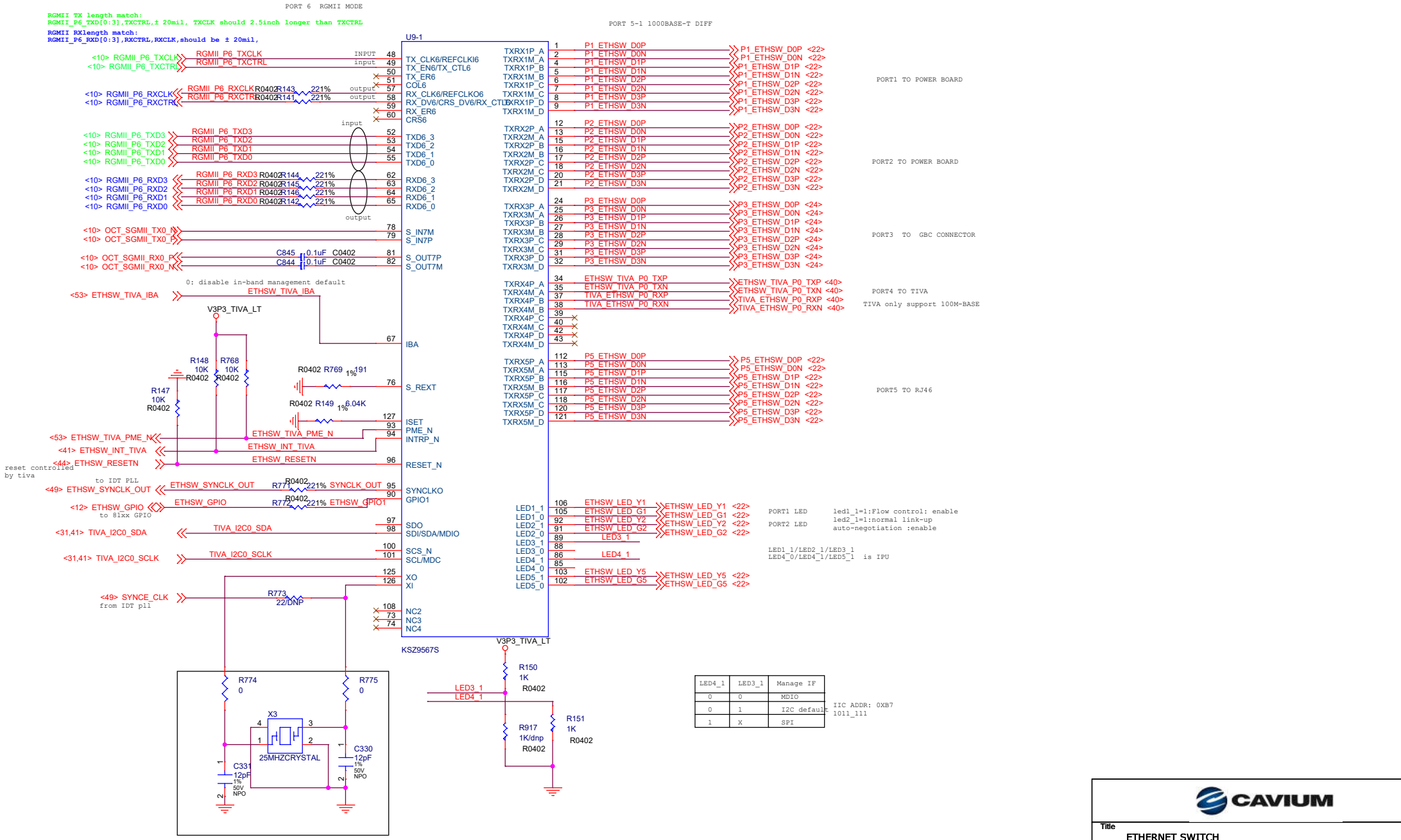
Chassis Fan Header

CAVIUM

Title: RTC & THERMAL SENSORS

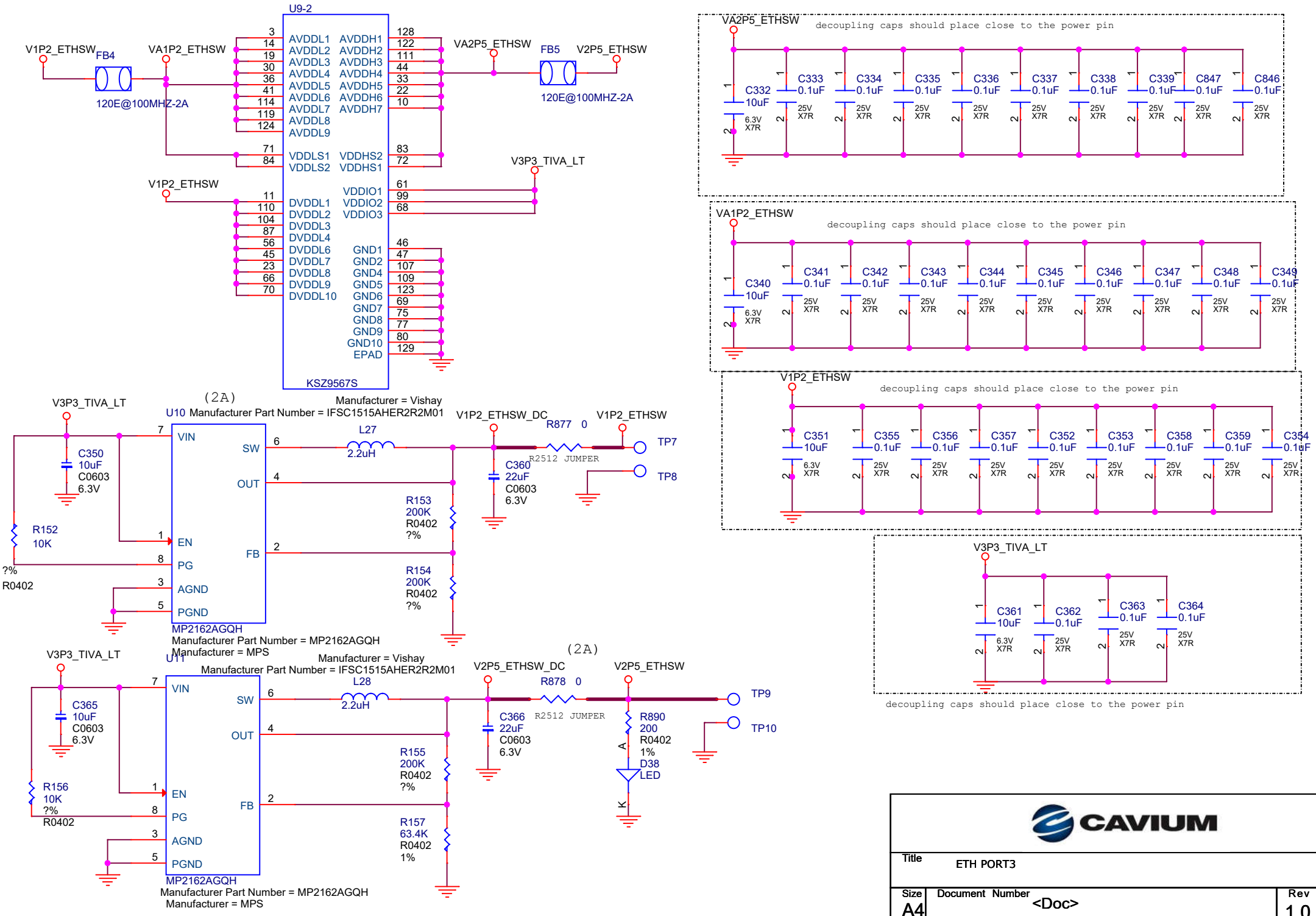
Size	Document Number	Rev
B	<Doc>	1.0

Date: Wednesday, May 30, 2018 Sheet 19 of 54



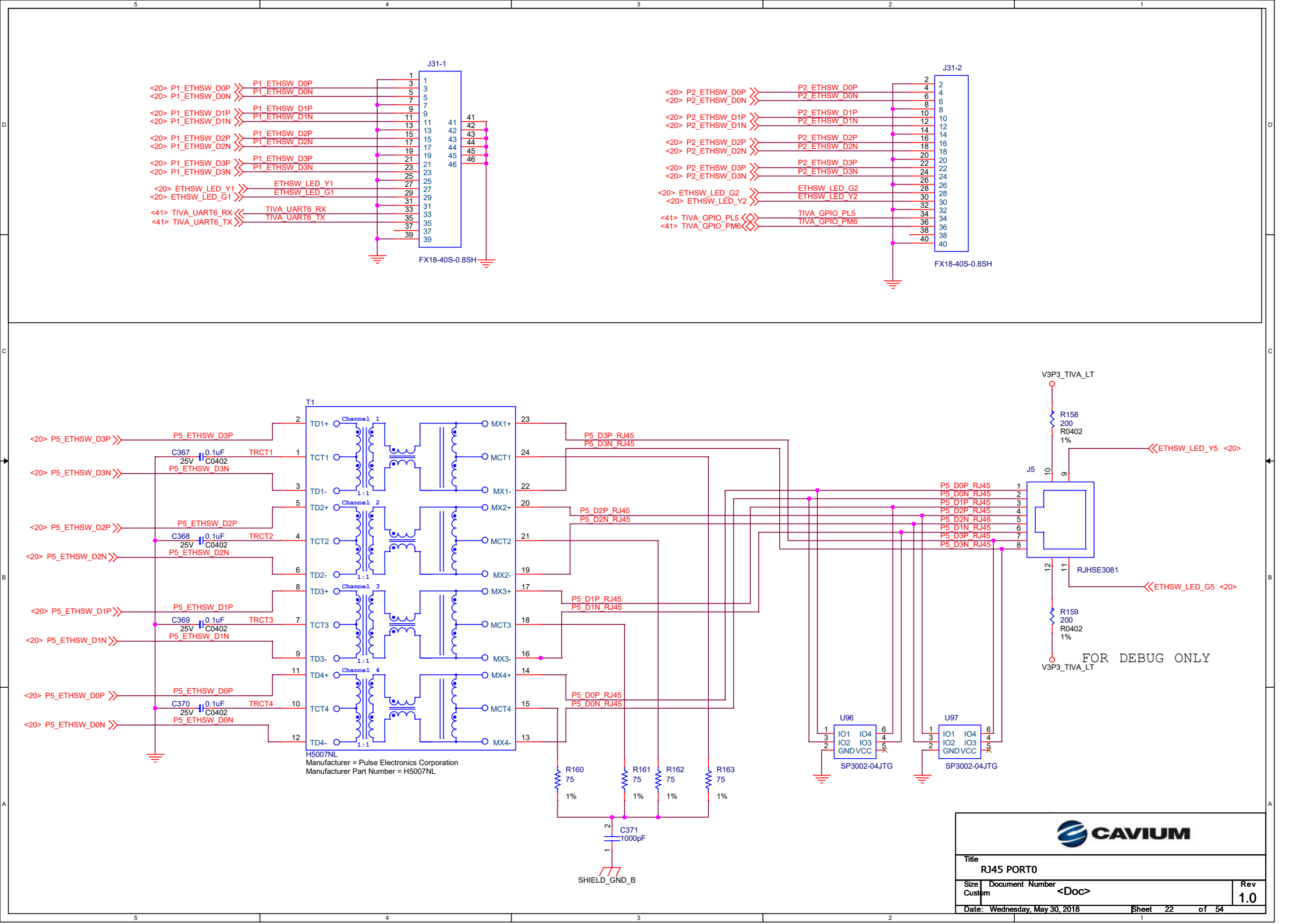
CAVIUM

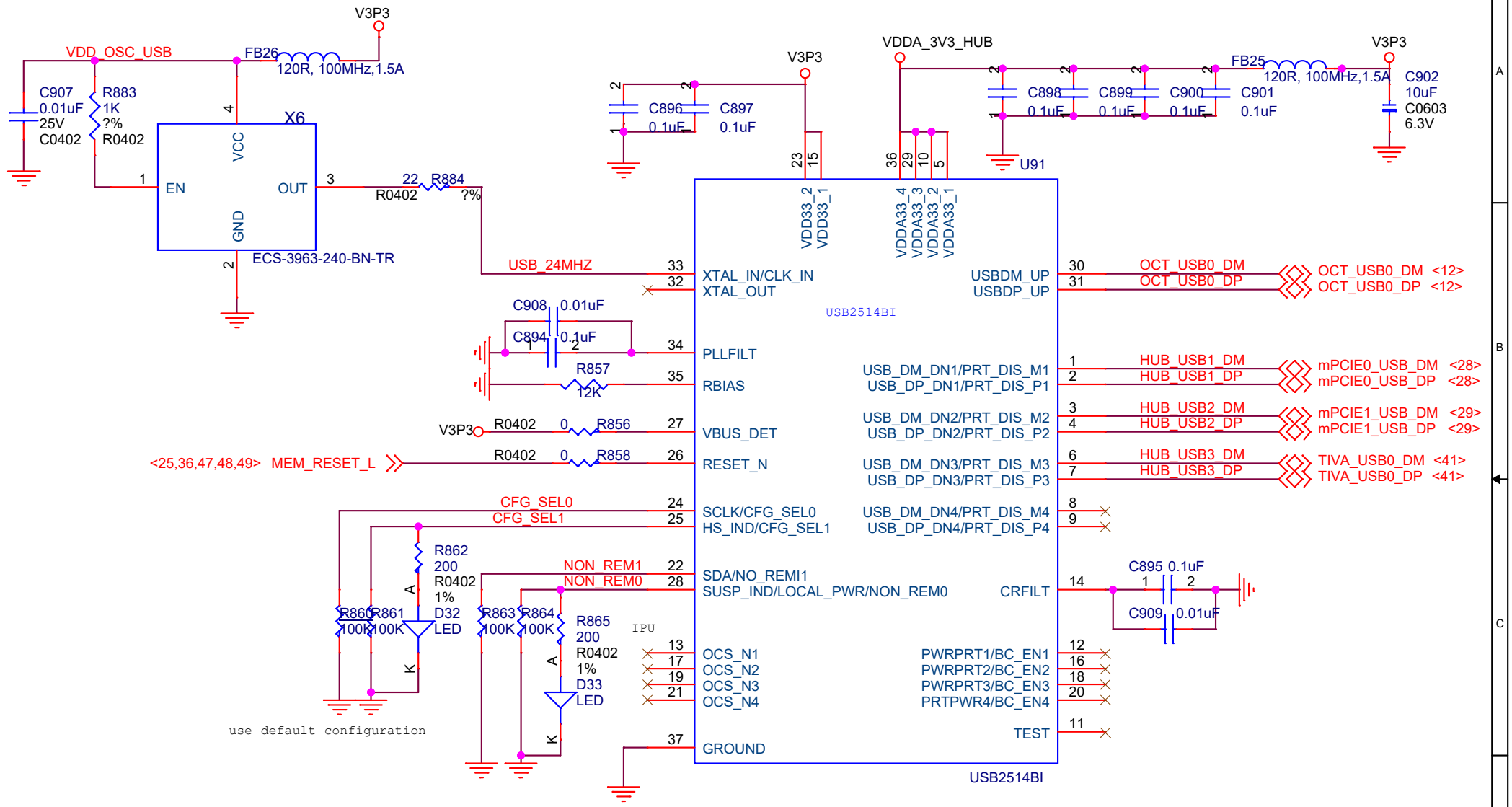
Title: ETHERNET SWITCH		
Size: Custom	Document Number: <Doc>	Rev: 1.0
Date: Wednesday, May 30, 2018	Sheet 20 of 54	



CAVIUM

Title	ETH PORT3	
Size A4	Document Number <Doc>	Rev 1.0
Date: Wednesday, May 30, 2018	Sheet 21 of 54	


J31-1
<20> P1_ETHSW_D0P
<20> P1_ETHSW_D0N
P1_ETHSW_D0P
P1_ETHSW_D0N
<20> P1_ETHSW_D1P
<20> P1_ETHSW_D1N
P1_ETHSW_D1P
P1_ETHSW_D1N
<20> P1_ETHSW_D2P
<20> P1_ETHSW_D2N
P1_ETHSW_D2P
P1_ETHSW_D2N
<20> P1_ETHSW_D3P
<20> P1_ETHSW_D3N
P1_ETHSW_D3P
P1_ETHSW_D3N
<20> ETHSW_LED_Y1
<20> ETHSW_LED_G1
ETHSW_LED_Y1
ETHSW_LED_G1
<41> TIVA_UART6_RX
<41> TIVA_UART6_TX
TIVA_UART6_RX
TIVA_UART6_TX
FX18-40S-0.8SH
J31-2
<20> P2_ETHSW_D0P
<20> P2_ETHSW_D0N
P2_ETHSW_D0P
P2_ETHSW_D0N
<20> P2_ETHSW_D1P
<20> P2_ETHSW_D1N
P2_ETHSW_D1P
P2_ETHSW_D1N
<20> P2_ETHSW_D2P
<20> P2_ETHSW_D2N
P2_ETHSW_D2P
P2_ETHSW_D2N
<20> P2_ETHSW_D3P
<20> P2_ETHSW_D3N
P2_ETHSW_D3P
P2_ETHSW_D3N
<20> ETHSW_LED_G2
<20> ETHSW_LED_Y2
ETHSW_LED_G2
ETHSW_LED_Y2
<41> TIVA_GPIO_PL5
<41> TIVA_GPIO_PM6
TIVA_GPIO_PL5
TIVA_GPIO_PM6
FX18-40S-0.8SH
T1
<20> P5_ETHSW_D3P
<20> P5_ETHSW_D3N
<20> P5_ETHSW_D2P
<20> P5_ETHSW_D2N
<20> P5_ETHSW_D1P
<20> P5_ETHSW_D1N
<20> P5_ETHSW_D0P
<20> P5_ETHSW_D0N
P5_ETHSW_D3P
P5_ETHSW_D3N
P5_ETHSW_D2P
P5_ETHSW_D2N
P5_ETHSW_D1P
P5_ETHSW_D1N
P5_ETHSW_D0P
P5_ETHSW_D0N
C367 0.1uF 25V C0402
C368 0.1uF 25V C0402
C369 0.1uF 25V C0402
C370 0.1uF 25V C0402
TRCT1
TRCT2
TRCT3
TRCT4
TD1+
TD1-
TD2+
TD2-
TD3+
TD3-
TD4+
TD4-
TCT1
TCT2
TCT3
TCT4
MX1+
MX1-
MX2+
MX2-
MX3+
MX3-
MX4+
MX4-
MCT1
MCT2
MCT3
MCT4
Channel 1
Channel 2
Channel 3
Channel 4
1:1
H5007NL
Manufacturer = Pulse Electronics Corporation
Manufacturer Part Number = H5007NL
P5_D3P_RJ45
P5_D3N_RJ45
P5_D2P_RJ45
P5_D2N_RJ45
P5_D1P_RJ45
P5_D1N_RJ45
P5_D0P_RJ45
P5_D0N_RJ45
R160 75 1%
R161 75 1%
R162 75 1%
R163 75 1%
C371 1000pF
SHIELD_GND_B
U96
U97
IO1 IO4
IO2 IO3
GND VCC
SP3002-04JTG
J5
P5_D0P_RJ45
P5_D0N_RJ45
P5_D1P_RJ45
P5_D2P_RJ45
P5_D2N_RJ46
P5_D1N_RJ45
P5_D3P_RJ45
P5_D3N_RJ45
RJHSE3081
V3P3_TIVA_LT
R158 200 R0402 1%
R159 200 R0402 1%
ETHSW_LED_Y5 <20>
ETHSW_LED_G5 <20>
FOR DEBUG ONLY
CAVIUM
Title
RJ45 PORT0
Size Custom
Document Number <Doc>
Rev 1.0
Date: Wednesday, May 30, 2018
Sheet 22 of 54

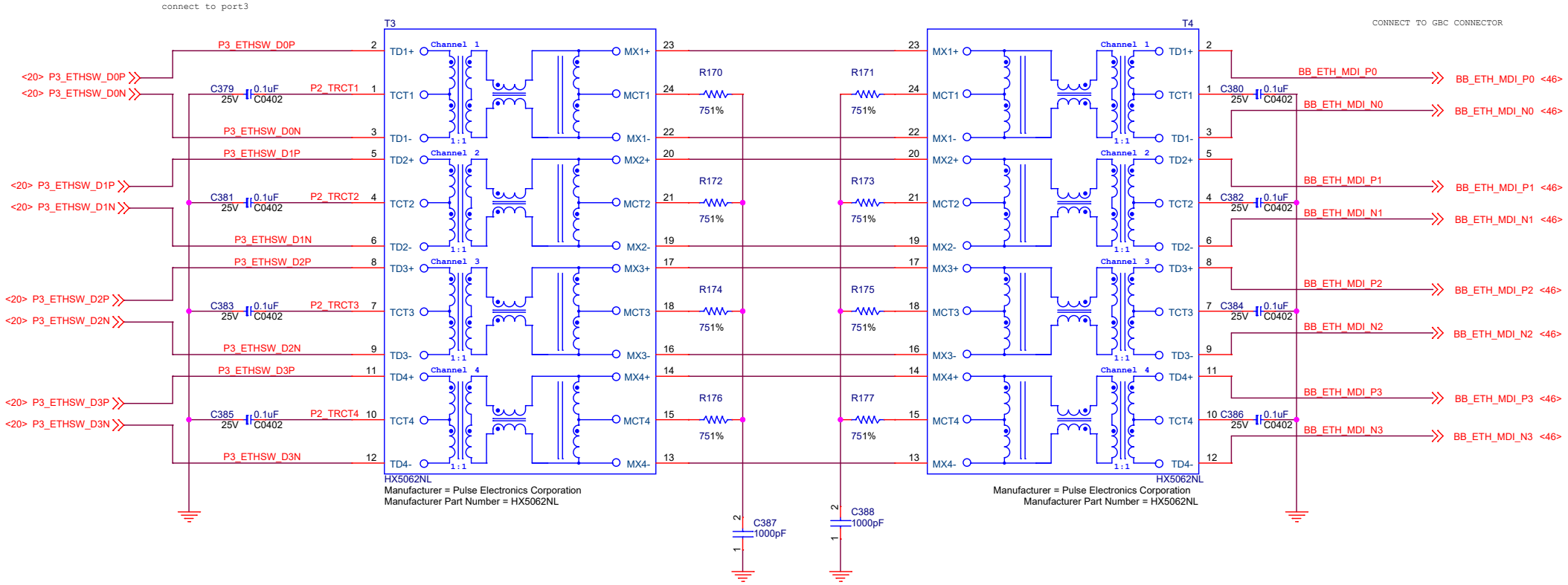


CAVIUM

Title
USB2514BI-USB HUB

Size	Document Number	Rev
A		1.0

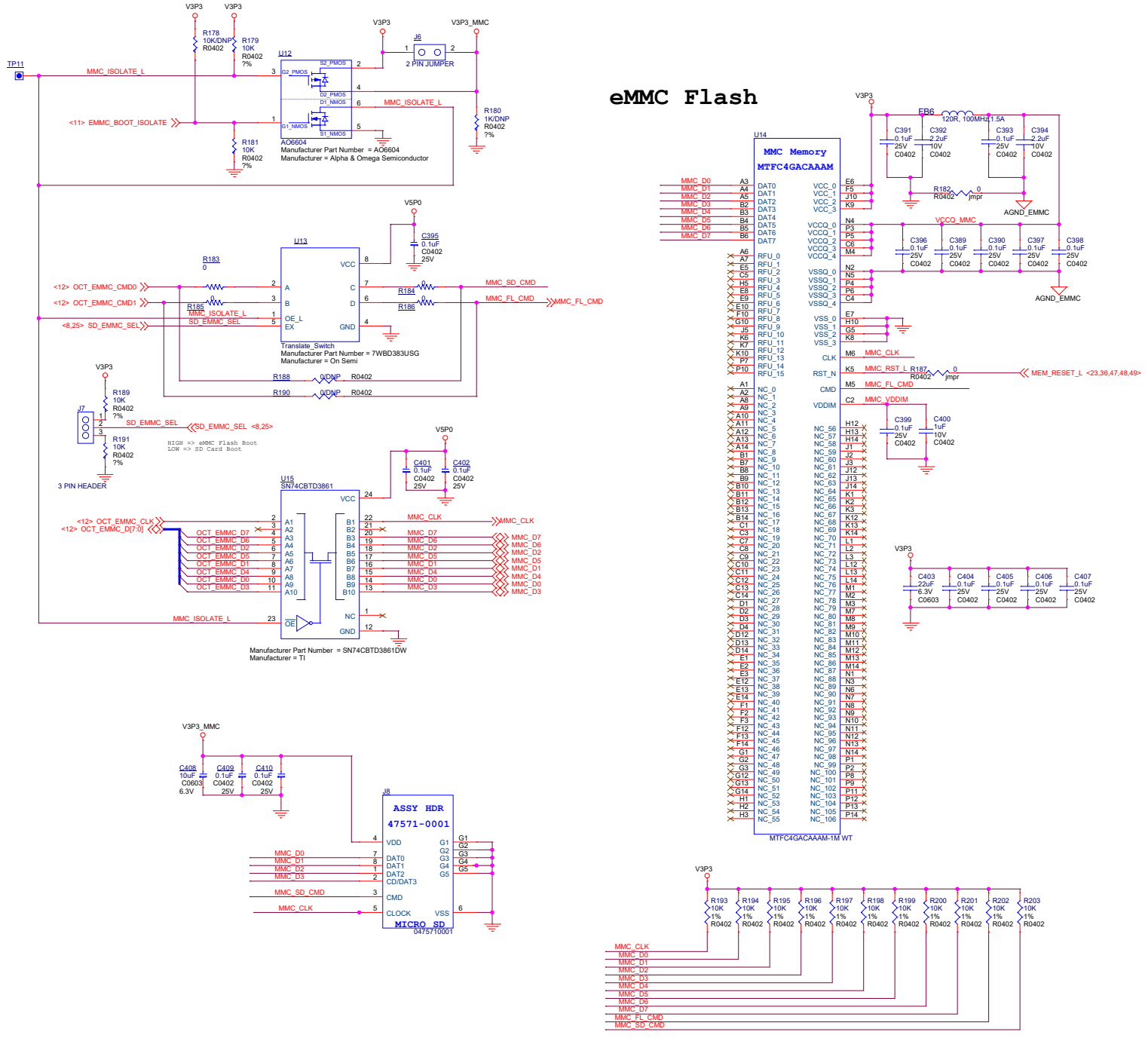
Date: Wednesday, May 30, 2018 Sheet 23 of 54



CAVIUM

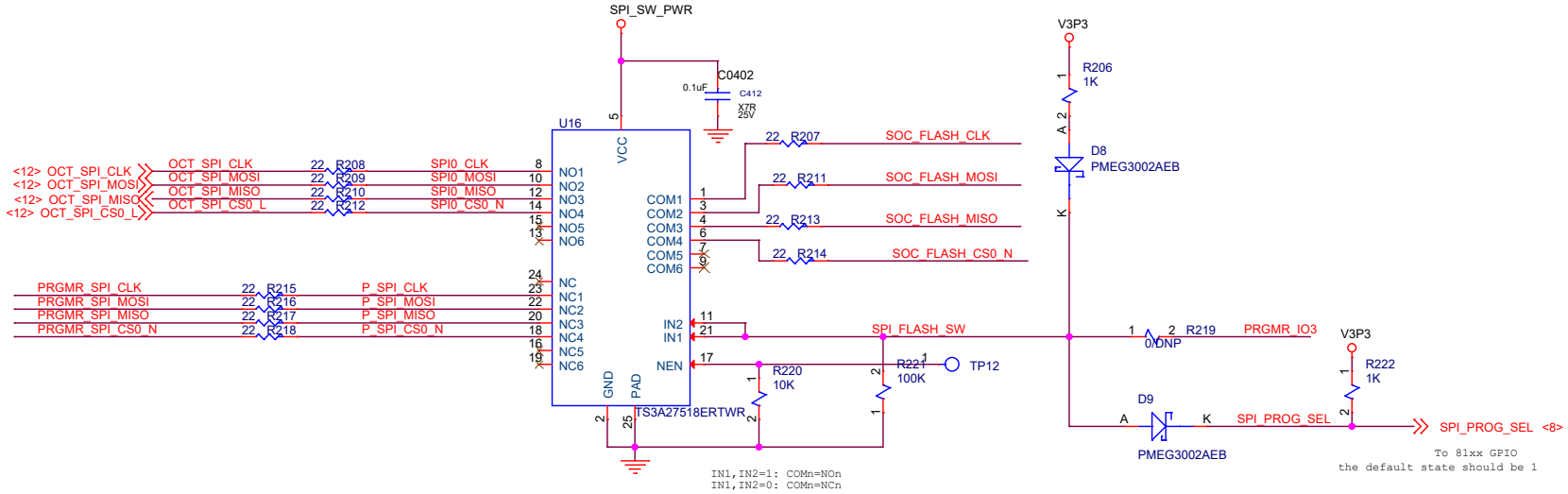
Title: ETH PORT3 TO BB		
Size: B	Document Number: <Doc>	Rev: 1.0
Date: Wednesday, May 30, 2018	Sheet 24 of 54	

eMMC Flash

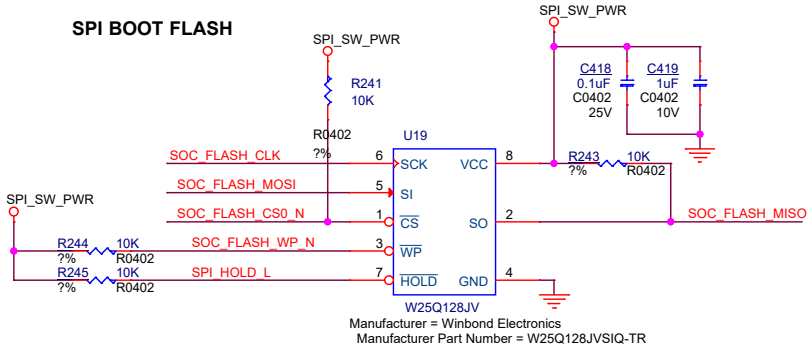


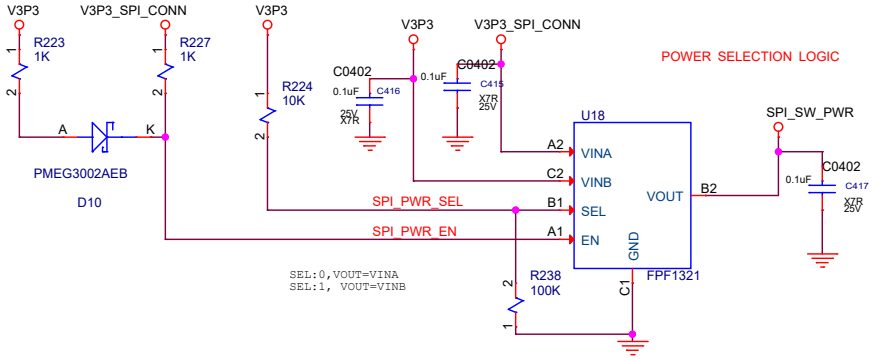
CAVIUM

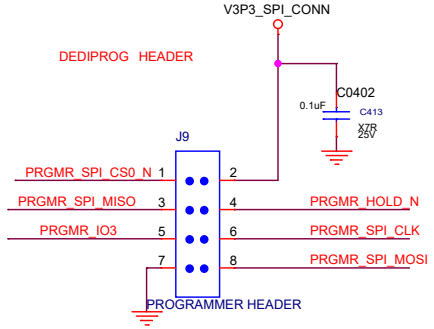
Title	BOOT EMMC/MMC	
Size: Custom	Document Number: <Doc>	Rev: 1.0
Date: Wednesday, May 30, 2018	Sheet 25 of 54	

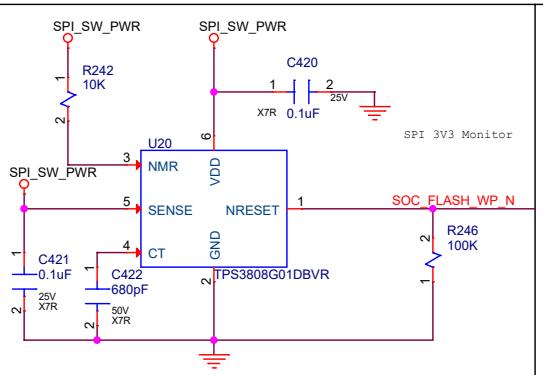


SPI BOOT FLASH







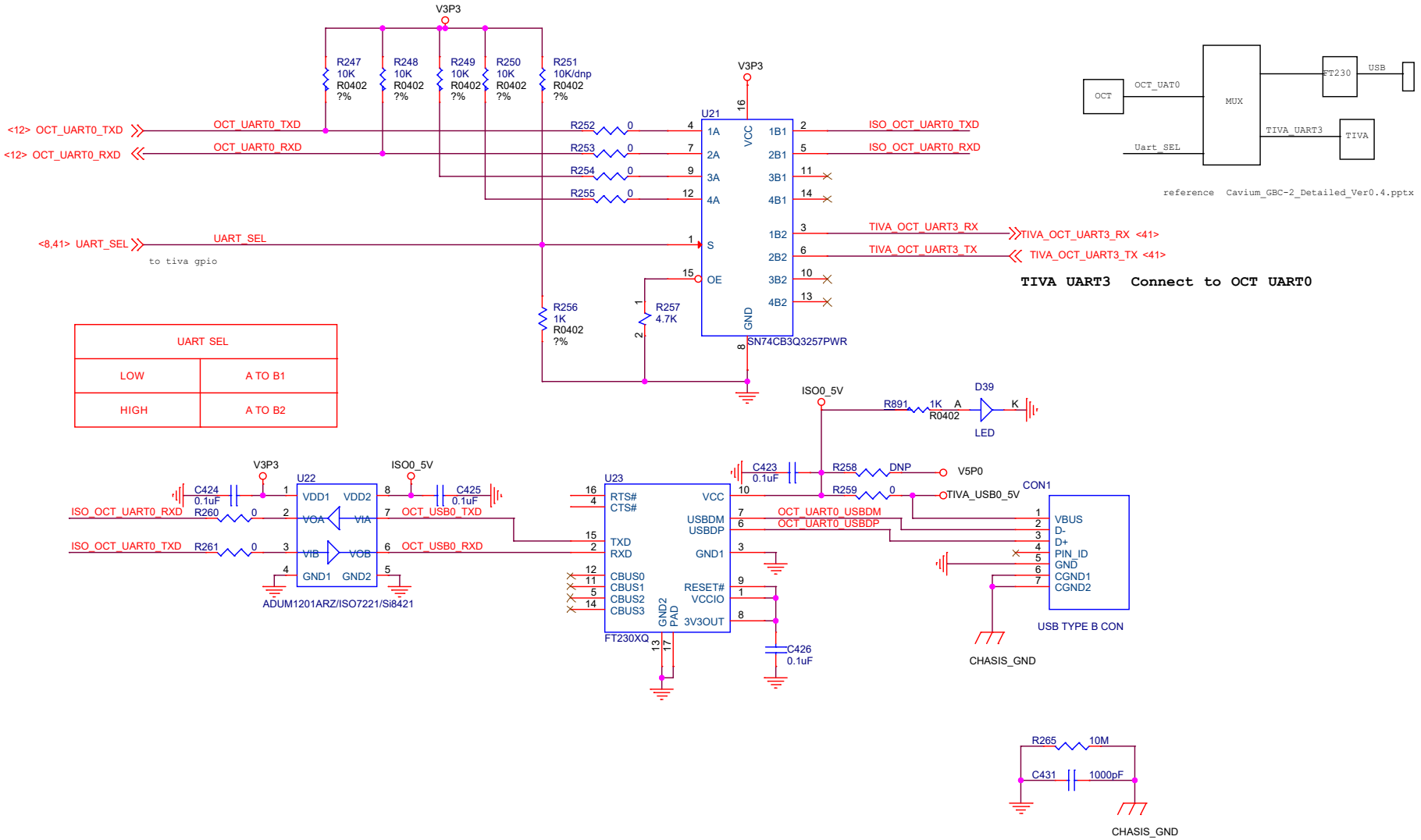


CAVIUM

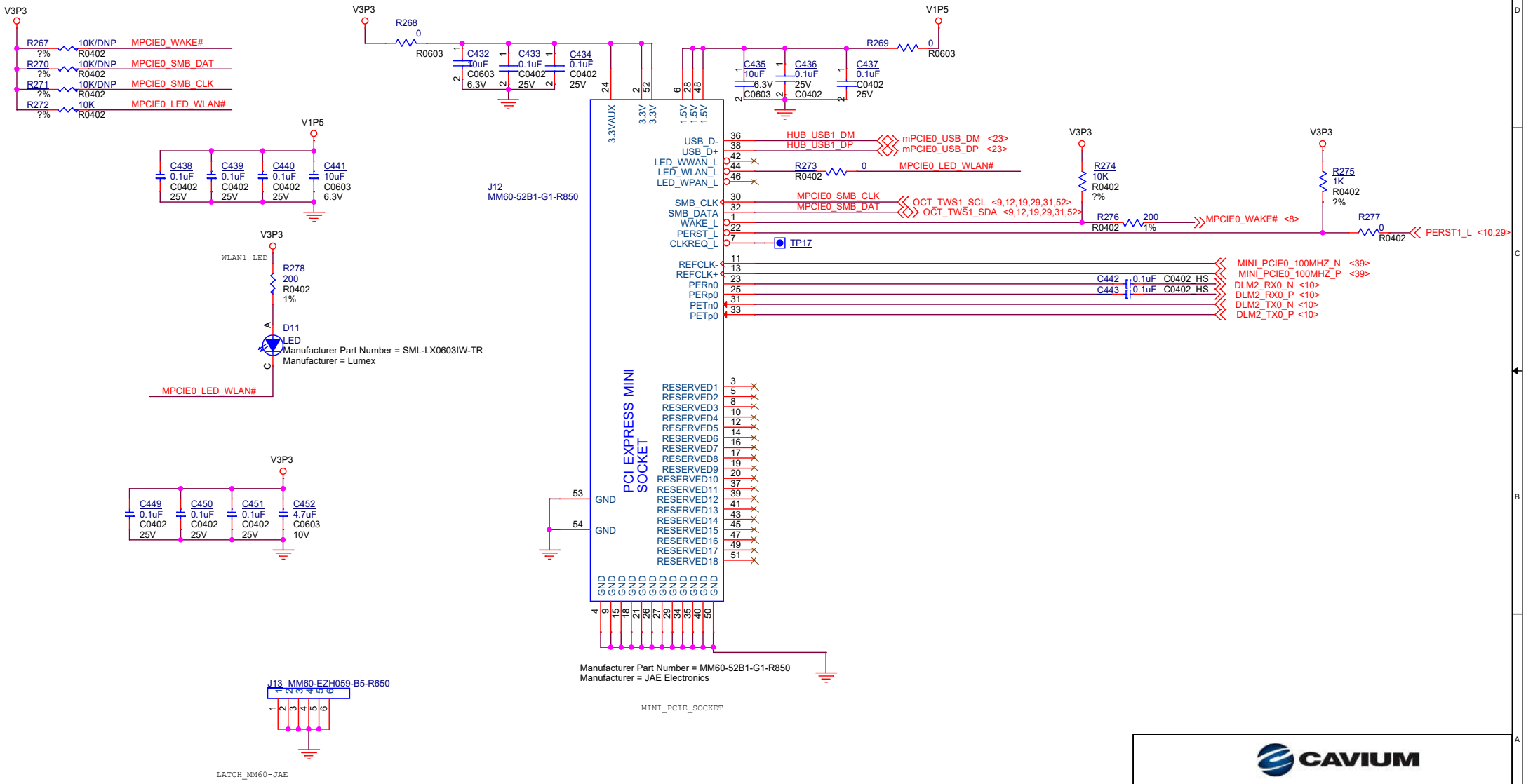
Title
BOOT SPI FLASH & NAND FLASH

Size	Document Number	Rev
B	Wednesday, May 30, 2018	1.0

Date: Sheet 26 of 54

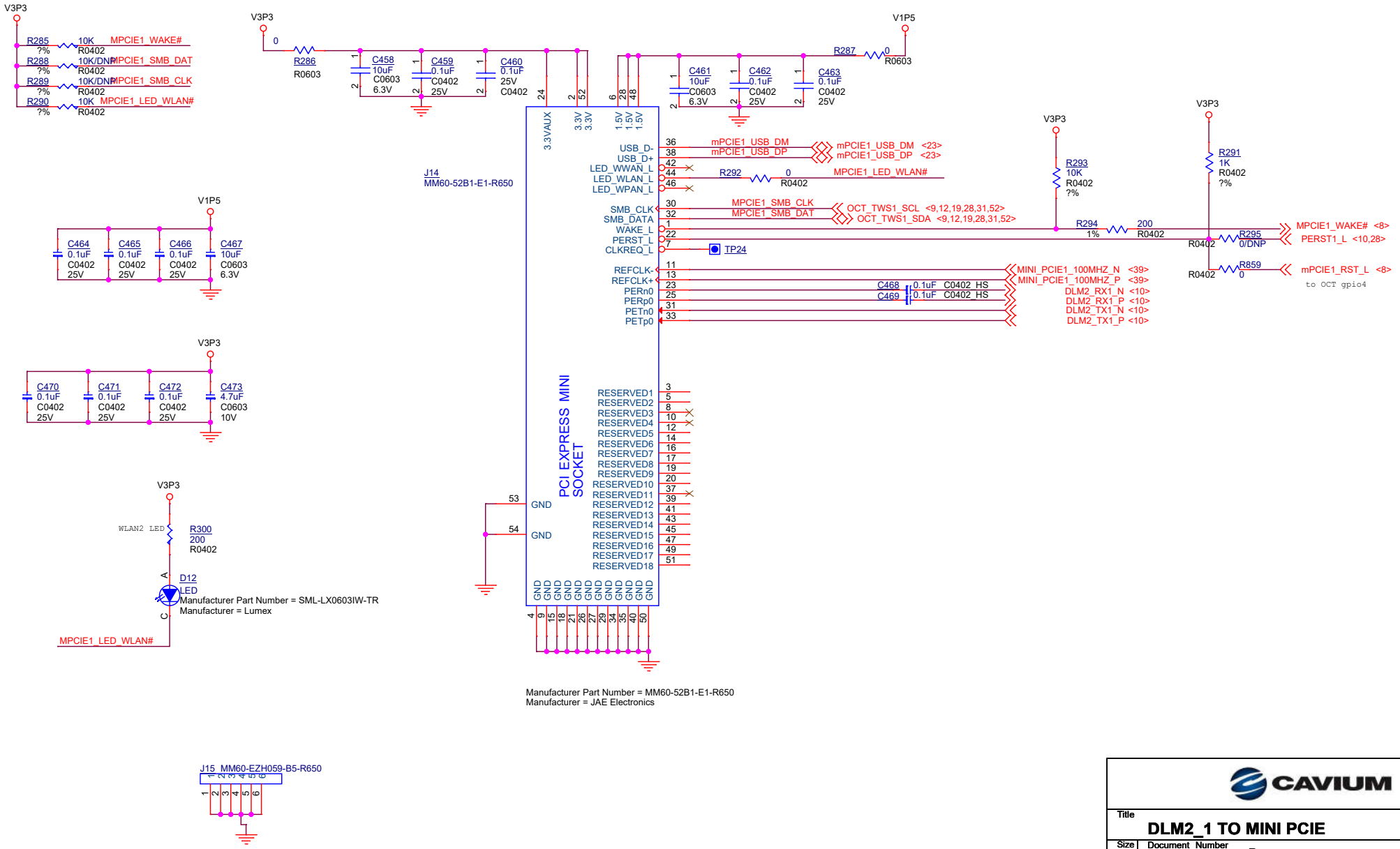


Title	OCT-UART 0
Size	B
Document Number	<Doc>
Rev	1.0
Date:	Wednesday, May 30, 2018
Sheet	27 of 54



CAVIUM

Title: DLM2_0 TO MINI PCIE		
Size: B	Document Number: <Doc>	Rev: 1.0
Date: Wednesday, May 30, 2018	Sheet 28 of 54	



CAVIUM

Title: DLM2_1 TO MINI PCIE

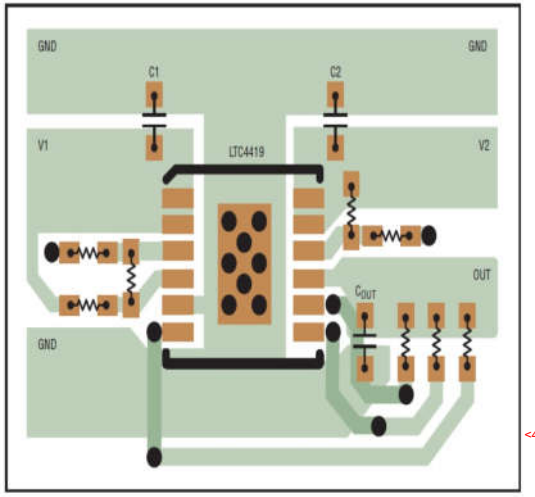
Size	Document Number	Rev
B	<Doc>	1.0

Date: Wednesday, May 30, 2018 Sheet 29 of 54

UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 0402 PACKAGE, POWER RATING < 0.5W & TOLERANCE > 1%
CAPACITORS ARE 0402 PACKAGE & TOLERANCE OF 10%

V12P0
R886 620E
D34 LED
V12P0_BACK_TIVA
R887 620E
D35 LED
J30
From power board
DF33C-4DP-3.3DSA

V3P3_TIVA_LT
R303 10K
C484 0.1uF
V12P0
V12P0_OCT_CM
R304 10E
R305 0.002 2W
C487 0.1uF
R306 10E
U26
VS
IN+
IN-
VBUS
A0
A1
GND
ALERT
SDA
SCL
INA226
<41> OCT_PWR_ALRT
OCT_PWR_ALRT
<33,35,41,42,47,53> TIVA_PWRMNTR_I2C6_SDA
TIVA_PWRMNTR_I2C6_SDA
<33,35,41,42,47,53> TIVA_PWRMNTR_I2C6_SCLK
TIVA_PWRMNTR_I2C6_SCLK
R307 10K
R308 10K
12V OCT power monitor
Adress:0X44



U90 pcb layout recommend

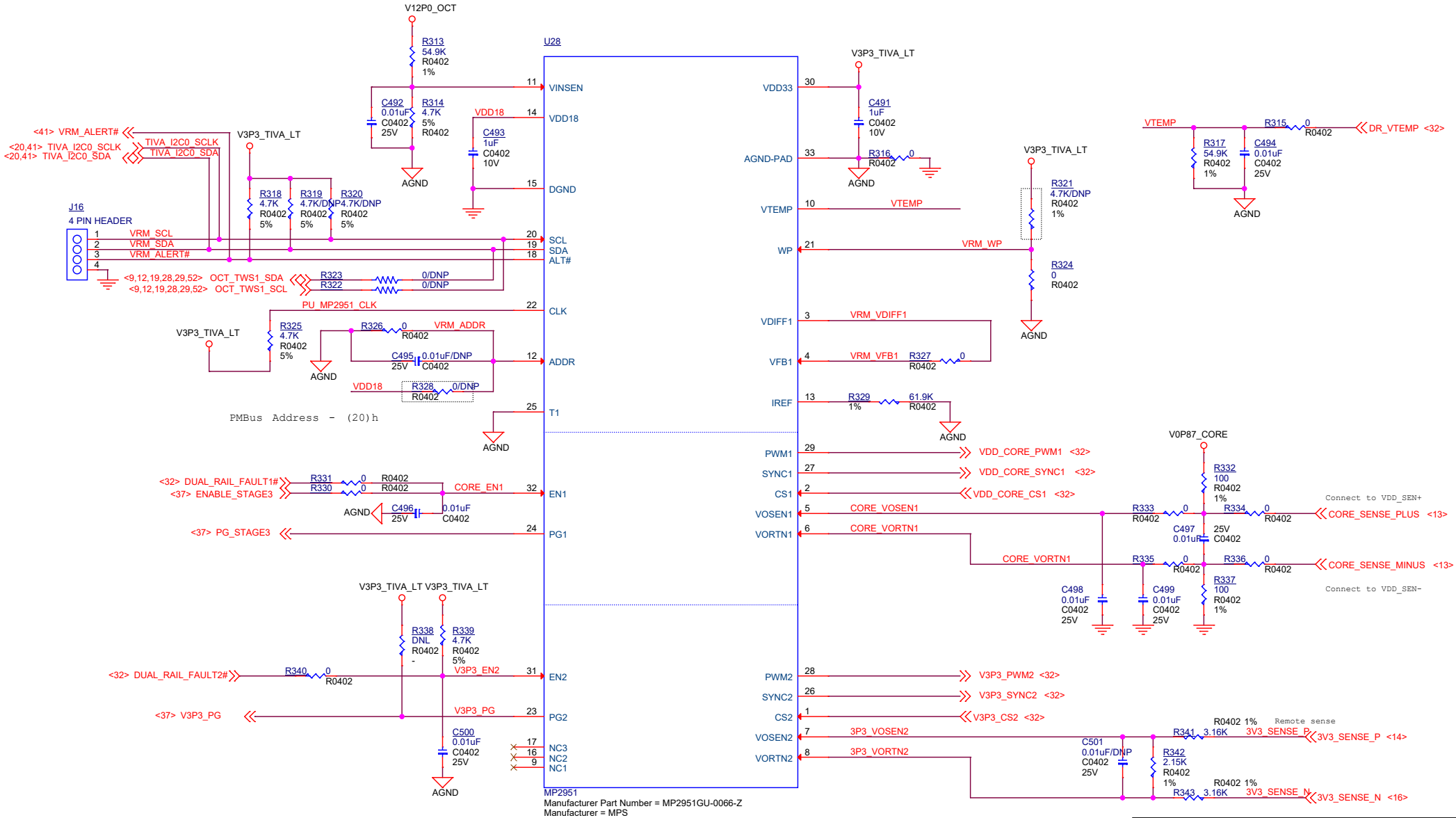
V12P0_BACK_TIVA
C888 330uF 25V 25SVPF330M
C889 330uF 25V 25SVPF330M
D30 5.0SMDJ26CA
D29 5.0SMDJ26CA
D31 5.0SMDJ26CA
CHASIS_GND
C887 0.47UF 100V
CHASIS_GND

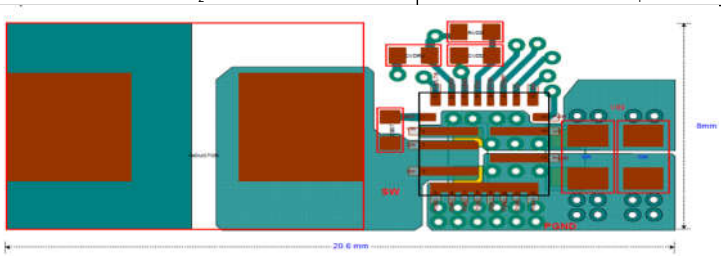
V12P0_OCT_CM
V12P0_OCT_R
voperation 4.5~13.8
C489 0.1uF
FB7 120E/DNP
FB8 120E/DNP
U27 Ilim, 5A
VIN
VIN1
VIN2
EN/UVLO
DV/DT
OUT
OUT1
OUT2
ILIM
BFET
PAD
TPS259241
R309 620E
D16 LED
R310 1M/DNP
R909 0
<41> OCT_12V_ONOFF
OCT_12V_ONOFF
C490 1.0nF
R311 150K
R312 150K
Place R867,R868 after U27

Vsw1=10.06V
Vvluv=10.5V
V12P0
C890 22uF C0805 25V
R847 1M
R848 75K
R849 41.2K
U90
LTC4419
V1
ADJ
CMP1
CMP2
OUT
CMPOUT1
CMPOUT2
V2
V2ON
NC2
NC1
GND
EGND
LTC4419IMSE
R845 1M
R846 1M
KEMET T491X107K025AT
V12P0_TIVA_CM
C892 100uF 25V
C893 22uF C0805 25V
V3P3_TIVA_LT
R852 10K R0402 ?%
V2_BACK_ON <41>
V12P0_BACK_TIVA
Vv2uv=10.7V
C891 22uF C0805 25V
R851 1.1M
R850 41.2K

CAVIUM

Title: POWER ENTRY		
Size: Custom	Document Number: <Doc>	Rev: 1.0
Date: Wednesday, May 30, 2018	Sheet 30 of 54	


V12P0_OCT
R313 54.9K R0402 1%
U28
VINSEN
VDD18
DGND
SCL
SDA
ALT#
CLK
ADDR
T1
EN1
PG1
EN2
PG2
NC3
NC2
NC1
VDD33
AGND-PAD
VTEMP
WP
VDIFF1
VFB1
IREF
PWM1
SYNC1
CS1
VOSEN1
VORTN1
PWM2
SYNC2
CS2
VOSEN2
VORTN2
MP2951
Manufacturer Part Number = MP2951GU-0066-Z
Manufacturer = MPS
V3P3_TIVA_LT
AGND
C492 0.01uF C0402 25V
R314 4.7K 5% R0402
VDD18
C493 1uF C0402 10V
C491 1uF C0402 10V
R316 0 R0402
<41> VRM_ALERT#
<20,41> TIVA_I2C0_SCLK
<20,41> TIVA_I2C0_SDA
TIVA_I2C0_SCLK
TIVA_I2C0_SDA
R318 4.7K R0402 5%
R319 4.7K/DNP R0402 5%
R320 4.7K/DNP R0402 5%
J16
4 PIN HEADER
VRM_SCL
VRM_SDA
VRM_ALERT#
<9,12,19,28,29,52> OCT_TWS1_SDA
<9,12,19,28,29,52> OCT_TWS1_SCL
R323 0/DNP
R322 0/DNP
PU_MP2951_CLK
R325 4.7K R0402 5%
R326 0 R0402
VRM_ADDR
C495 0.01uF/DNP 25V C0402
VDD18
R328 0/DNP R0402
PMBus Address - (20)h
<32> DUAL_RAIL_FAULT1#
<37> ENABLE_STAGE3
R331 0 R0402
R330 0 R0402
CORE_EN1
C496 25V 0.01uF C0402
<37> PG_STAGE3
R338 DNL R0402 -
R339 4.7K R0402 5%
<32> DUAL_RAIL_FAULT2#
R340 0 R0402
V3P3_EN2
<37> V3P3_PG
V3P3_PG
C500 0.01uF C0402 25V
R321 4.7K/DNP R0402 1%
R324 0 R0402
VRM_WP
VRM_VDIFF1
VRM_VFB1
R327 0 R0402
R329 1% 61.9K R0402
VTEMP
R315 0 R0402
DR_VTEMP <32>
R317 54.9K R0402 1%
C494 0.01uF C0402 25V
V0P87_CORE
R332 100 R0402 1%
R333 0 R0402
R334 0 R0402
Connect to VDD_SEN+
CORE_SENSE_PLUS <13>
C497 0.01uF 25V C0402
CORE_VORTN1
R335 0 R0402
R336 0 R0402
CORE_SENSE_MINUS <13>
R337 100 R0402 1%
Connect to VDD_SEN-
C498 0.01uF C0402 25V
C499 0.01uF C0402 25V
VDD_CORE_PWM1 <32>
VDD_CORE_SYNC1 <32>
VDD_CORE_CS1 <32>
CORE_VOSEN1
CORE_VORTN1
V3P3_PWM2 <32>
V3P3_SYNC2 <32>
V3P3_CS2 <32>
3P3_VOSEN2
3P3_VORTN2
C501 0.01uF/DNP C0402 25V
R342 2.15K R0402 1%
R0402 1% Remote sense
R341 3.16K 3V3_SENSE_P
3V3_SENSE_P <14>
R0402 1%
R343 3.16K 3V3_SENSE_N
3V3_SENSE_N <16>
CAVIUM
Title
CONTROL:CPU CORE&3V3
Size B
Document Number
54
Rev 1.0
Date: Wednesday, May 30, 2018
Sheet 31 of



V12P0_OCT
C502 22uF C0805 25V
C503 22uF C0805 25V
C504 22uF C0805 25V
C505 22uF C0805 25V
C506 1uF C0402 25V
C507 1uF C0402 25V
V3P3
R344 2.2R R0402 ?%
CORE_VDRV1
CORE_VDD1
CORE_AGND1
R345 2K R0402 ?%
C510 1uF C0402 25V
C509 1uF C0402 25V
<31> VDD_CORE_PWM1
<31> VDD_CORE_SYNC1
V12P0_OCT_R
use large copper shape
V12P0_OCT
R871 0
R2512 JUMPER

U29
MP86905
Manufacturer Part Number = MP86905GR
Manufacturer = MPS
VIN1 2
VIN2 14
VDRV 22
VDD 20
AGND 21
EN 16
PWM 15
SYNC 19
PGND1 5
PGND2 6
PGND3 7
PGND4 8
PGND5 9
PGND6 10
PGND7 11
PGND8 12
PGND9 13
BST 1
SW1 3
SW2 4
VTEMP 18
CS 17
FAULT# 23

CORE_BST
C508 1uF C0402 25V
L29
Manufacturer = Coilcraft
Manufacturer Part Number = SLR1050A-151KEB
150nH, 51A
R346 3.32/DNP R0402 ?%
C516 220pF/DNP C0402 50V
C511 330uF 6.3V
C512 330uF 6.3V
C513 330uF 6.3V
C514 100uF C1206 6.3V
C515 100uF C1206 6.3V
R347 1K R0402 ?%
V0P87_CORE_R
TP29
TP30
DR_VTEMP <31,32>
VDD_CORE_CS1 <31>
DUAL_RAIL_FAULT1# <31>
V0P87_CORE_R
R2512 JUMPER
V0P87_CORE
R867 0
R868 0
use large copper shape

V12P0_OCT
C517 22uF C0805 25V
C518 22uF C0805 25V
C519 22uF C0805 25V
C520 22uF C0805 25V
C521 1uF C0402 25V
C522 1uF C0402 25V
V3P3_TIVA_LT
R348 2.2R R0402 ?%
V3P3_VDRV2
V3P3_VDD2
V3P3_AGND2
R349 2K R0402 ?%
C524 1uF C0402 25V
C525 1uF C0402 25V
<31> V3P3_PWM2
<31> V3P3_SYNC2

U30
MP86905
VIN1 2
VIN2 14
VDRV 22
VDD 20
AGND 21
EN 16
PWM 15
SYNC 19
PGND1 5
PGND2 6
PGND3 7
PGND4 8
PGND5 9
PGND6 10
PGND7 11
PGND8 12
PGND9 13
BST 1
SW1 3
SW2 4
VTEMP 18
CS 17
FAULT# 23
Manufacturer Part Number = MP86905GR
Manufacturer = MPS

V3P3_BST
C523 1uF C0402 25V
L30
Manufacturer Part Number = XAL7070-651MEC
Manufacturer = Coilcraft
650nH, 40A
R350 3.32/DNP R0402 ?%
recalculator the resistor
C531 220pF/DNP C0402 50V
C526 330uF 6.3V
C527 330uF 6.3V
C528 330uF 6.3V
C529 100uF C1206 6.3V
C530 100uF C1206 6.3V
R351 1K R0402 ?%
3.3V
V3P3_R
TP31
TP32
DR_VTEMP <31,32>
V3P3_CS2 <31>
DUAL_RAIL_FAULT2# <31>
V3P3_R
use large copper shape
V3P3
R869 0
R2512 JUMPER

CAVIUM

Title: GATE DRVRS
Size: B
Document Number: <Doc>
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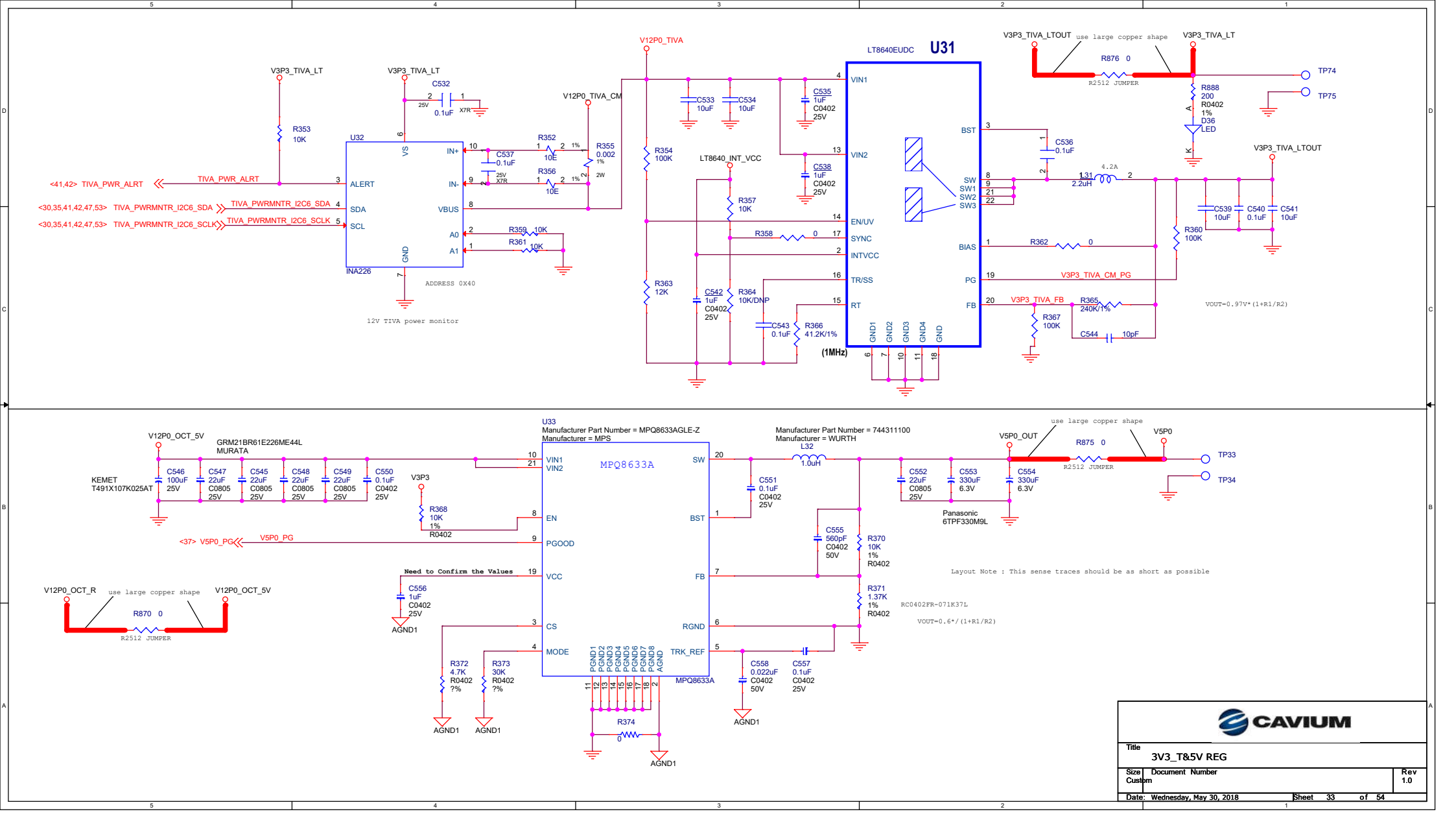
V3P3_TIVA_LT
V3P3_TIVA_LT
C532
2
25V
1
0.1uF
X7R
V12P0_TIVA_CM
V12P0_TIVA
LT8640EUDC
U31
V3P3_TIVA_LTOUT
use large copper shape
V3P3_TIVA_LT
R876 0
R2512 JUMPER
TP74
TP75
R888
200
R0402
1%
D36
LED
R353
10K
U32
VS
IN+
IN-
VBUS
A0
A1
GND
SDA
SCL
ALERT
INA226
ADDRESS 0X40
R352
10E
R355
0.002
1%
2W
R356
10E
C537
0.1uF
25V
X7R
R359 10K
R361 10K
<41,42> TIVA_PWR_ALRT
TIVA_PWR_ALRT
<30,35,41,42,47,53> TIVA_PWRMNTR_I2C6_SDA
TIVA_PWRMNTR_I2C6_SDA
<30,35,41,42,47,53> TIVA_PWRMNTR_I2C6_SCLK
TIVA_PWRMNTR_I2C6_SCLK
12V TIVA power monitor
C533
10uF
C534
10uF
C535
1uF
C0402
25V
C538
1uF
C0402
25V
R354
100K
R357
10K
LT8640_INT_VCC
R358 0
R363
12K
C542
1uF
C0402
25V
R364
10K/DNP
C543
0.1uF
R366
41.2K/1%
(1MHz)
VIN1
VIN2
EN/UV
SYNC
INTVCC
TR/SS
RT
BST
SW
SW1
SW2
SW3
BIAS
PG
FB
GND1
GND2
GND3
GND4
GND
C536
0.1uF
L31
2.2uH
4.2A
C539
10uF
C540
0.1uF
C541
10uF
R360
100K
R362 0
V3P3_TIVA_CM_PG
V3P3_TIVA_FB
R365
240K/1%
R367
100K
C544
10pF
VOUT=0.97V*(1+R1/R2)
U33
Manufacturer Part Number = MPQ8633AGLE-Z
Manufacturer = MPS
MPQ8633A
V12P0_OCT_5V
GRM21BR61E226ME44L
MURATA
KEMET
T491X107K025AT
C546
100uF
25V
C547
22uF
C0805
25V
C545
22uF
C0805
25V
C548
22uF
C0805
25V
C549
22uF
C0805
25V
C550
0.1uF
C0402
25V
V3P3
R368
10K
1%
R0402
<37> V5P0_PG
V5P0_PG
Need to Confirm the Values
C556
1uF
C0402
25V
AGND1
R372
4.7K
R0402
?%
R373
30K
R0402
?%
R374
0
VIN1
VIN2
EN
PGOOD
VCC
CS
MODE
SW
BST
FB
RGND
TRK_REF
PGND1
PGND2
PGND3
PGND4
PGND5
PGND6
PGND7
PGND8
AGND
Manufacturer Part Number = 744311100
Manufacturer = WURTH
L32
1.0uH
C551
0.1uF
C0402
25V
C555
560pF
C0402
50V
R370
10K
1%
R0402
R371
1.37K
1%
R0402
RC0402FR-071K37L
VOUT=0.6*/(1+R1/R2)
Layout Note : This sense traces should be as short as possible
C558
0.022uF
C0402
50V
C557
0.1uF
C0402
25V
V5P0_OUT
use large copper shape
V5P0
R875 0
R2512 JUMPER
TP33
TP34
C552
22uF
C0805
25V
C553
330uF
6.3V
Panasonic
6TPF330M9L
C554
330uF
6.3V
V12P0_OCT_R
use large copper shape
V12P0_OCT_5V
R870 0
R2512 JUMPER
CAVIUM
Title
3V3_T&5V REG
Size
Custom
Document Number
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1.0
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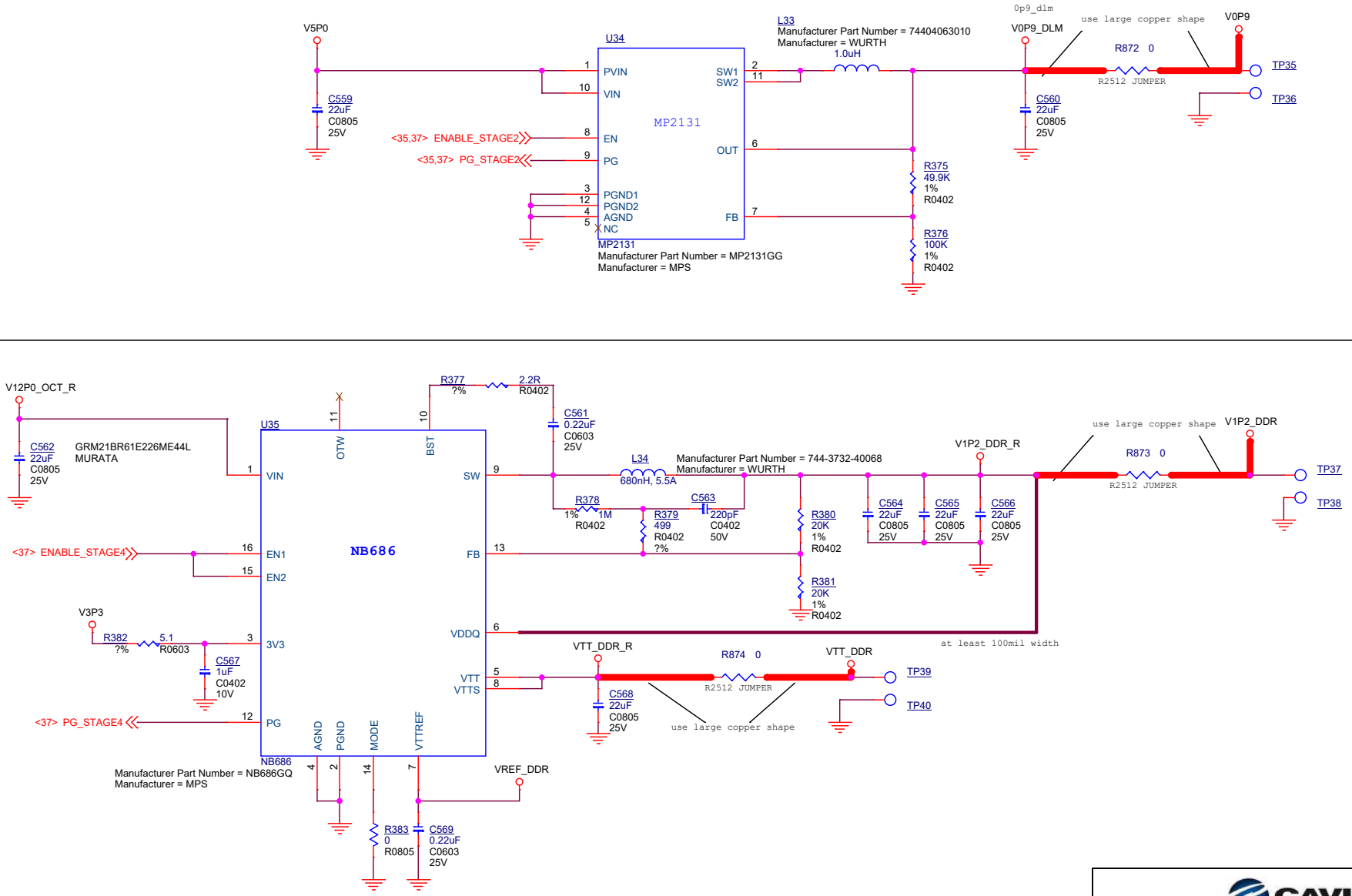

CAVIUM

Title: V0P9_DLM&V1P2_DDR		
Size: B	Document Number: <Doc>	Rev: 1.0
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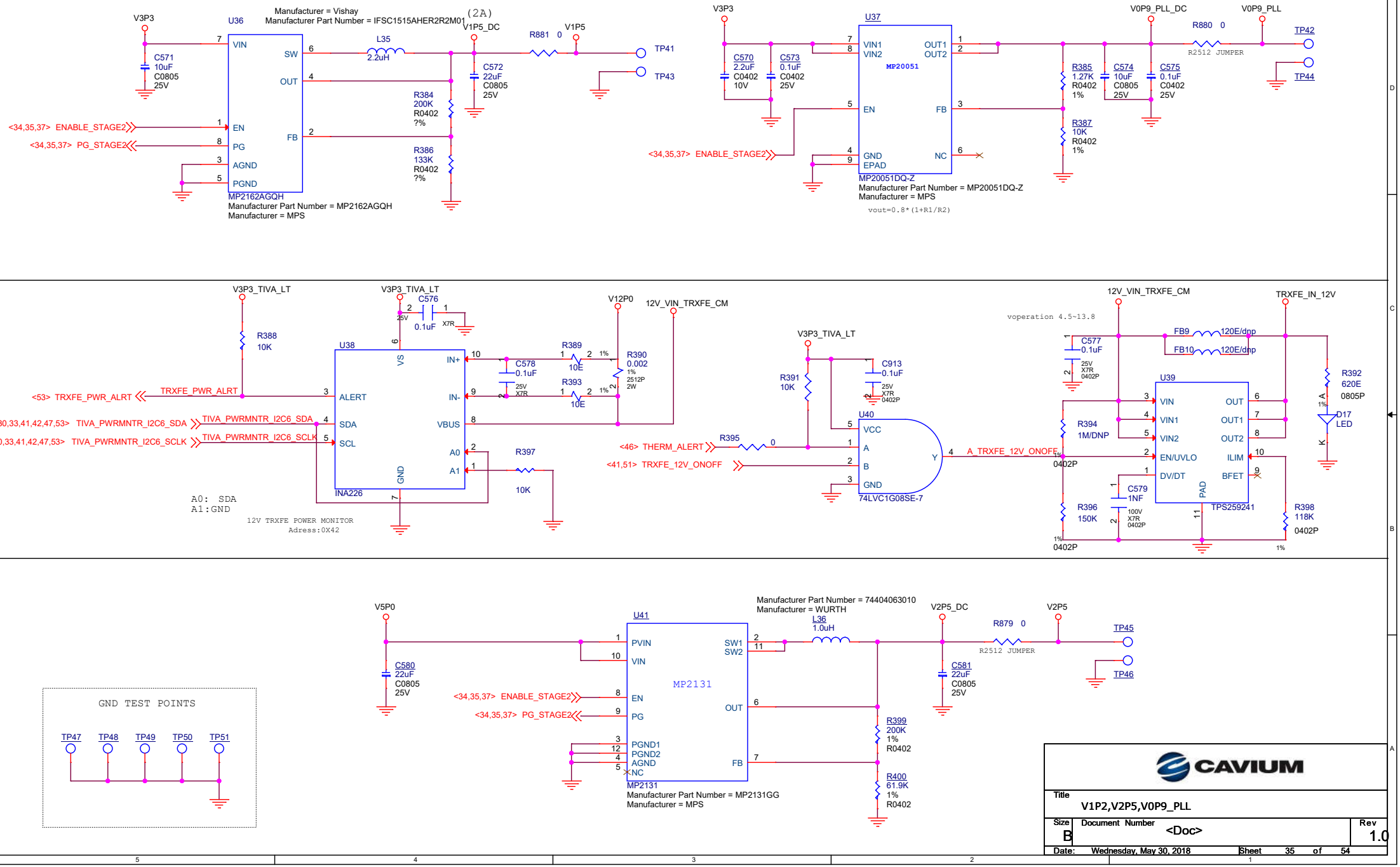
V3P3
U36
Manufacturer = Vishay
Manufacturer Part Number = IFSC1515AHER2R2M01
(2A)
V1P5_DC
R881 0
V1P5
TP41
TP43
L35
2.2uH
C571
10uF
C0805
25V
C572
22uF
C0805
25V
R384
200K
R0402
?%
R386
133K
R0402
?%
VIN
SW
OUT
EN
FB
PG
AGND
PGND
<34,35,37> ENABLE_STAGE2
<34,35,37> PG_STAGE2
MP2162AGQH
Manufacturer Part Number = MP2162AGQH
Manufacturer = MPS
V3P3
U37
C570
2.2uF
C0402
10V
C573
0.1uF
C0402
25V
VIN1
VIN2
OUT1
OUT2
MP20051
EN
FB
GND
EPAD
NC
<34,35,37> ENABLE_STAGE2
MP20051DQ-Z
Manufacturer Part Number = MP20051DQ-Z
Manufacturer = MPS
vout=0.8*(1+R1/R2)
V0P9_PLL_DC
R880 0
V0P9_PLL
TP42
TP44
R2512 JUMPER
R385
1.27K
R0402
1%
R387
10K
R0402
1%
C574
10uF
C0805
25V
C575
0.1uF
C0402
25V
V3P3_TIVA_LT
R388
10K
<53> TRXFE_PWR_ALRT
TRXFE_PWR_ALRT
U38
ALERT
SDA
SCL
<30,33,41,42,47,53> TIVA_PWRMNTR_I2C6_SDA
TIVA_PWRMNTR_I2C6_SDA
<30,33,41,42,47,53> TIVA_PWRMNTR_I2C6_SCLK
TIVA_PWRMNTR_I2C6_SCLK
A0: SDA
A1:GND
INA226
12V TRXFE POWER MONITOR
Adress:0X42
V3P3_TIVA_LT
C576
0.1uF
X7R
VS
GND
IN+
IN-
VBUS
A0
A1
C578
0.1uF
R389
10E
R393
10E
R390
0.002
1%
2512P
2W
R397
10K
V12P0
12V_VIN_TRXFE_CM
V3P3_TIVA_LT
R391
10K
C913
0.1uF
U40
VCC
A
B
GND
Y
<46> THERM_ALERT
R395
0
<41,51> TRXFE_12V_ONOFF
74LVC1G08SE-7
A_TRXFE_12V_ONOFF
12V_VIN_TRXFE_CM
voperation 4.5~13.8
C577
0.1uF
FB9
120E/dnp
FB10
120E/dnp
U39
VIN
VIN1
VIN2
EN/UVLO
DV/DT
OUT
OUT1
OUT2
ILIM
BFET
PAD
TPS259241
R394
1M/DNP
R396
150K
C579
1NF
100V
R398
118K
R392
620E
0805P
D17
LED
TRXFE_IN_12V
V5P0
U41
C580
22uF
C0805
25V
PVIN
VIN
SW1
SW2
EN
PG
OUT
PGND1
PGND2
AGND
NC
FB
MP2131
<34,35,37> ENABLE_STAGE2
<34,35,37> PG_STAGE2
Manufacturer Part Number = 74404063010
Manufacturer = WURTH
L36
1.0uH
V2P5_DC
R879 0
V2P5
TP45
TP46
R2512 JUMPER
C581
22uF
C0805
25V
R399
200K
1%
R0402
R400
61.9K
1%
R0402
MP2131
Manufacturer Part Number = MP2131GG
Manufacturer = MPS
GND TEST POINTS
TP47
TP48
TP49
TP50
TP51
CAVIUM
Title
V1P2,V2P5,V0P9_PLL
Size
B
Document Number
<Doc>
Rev
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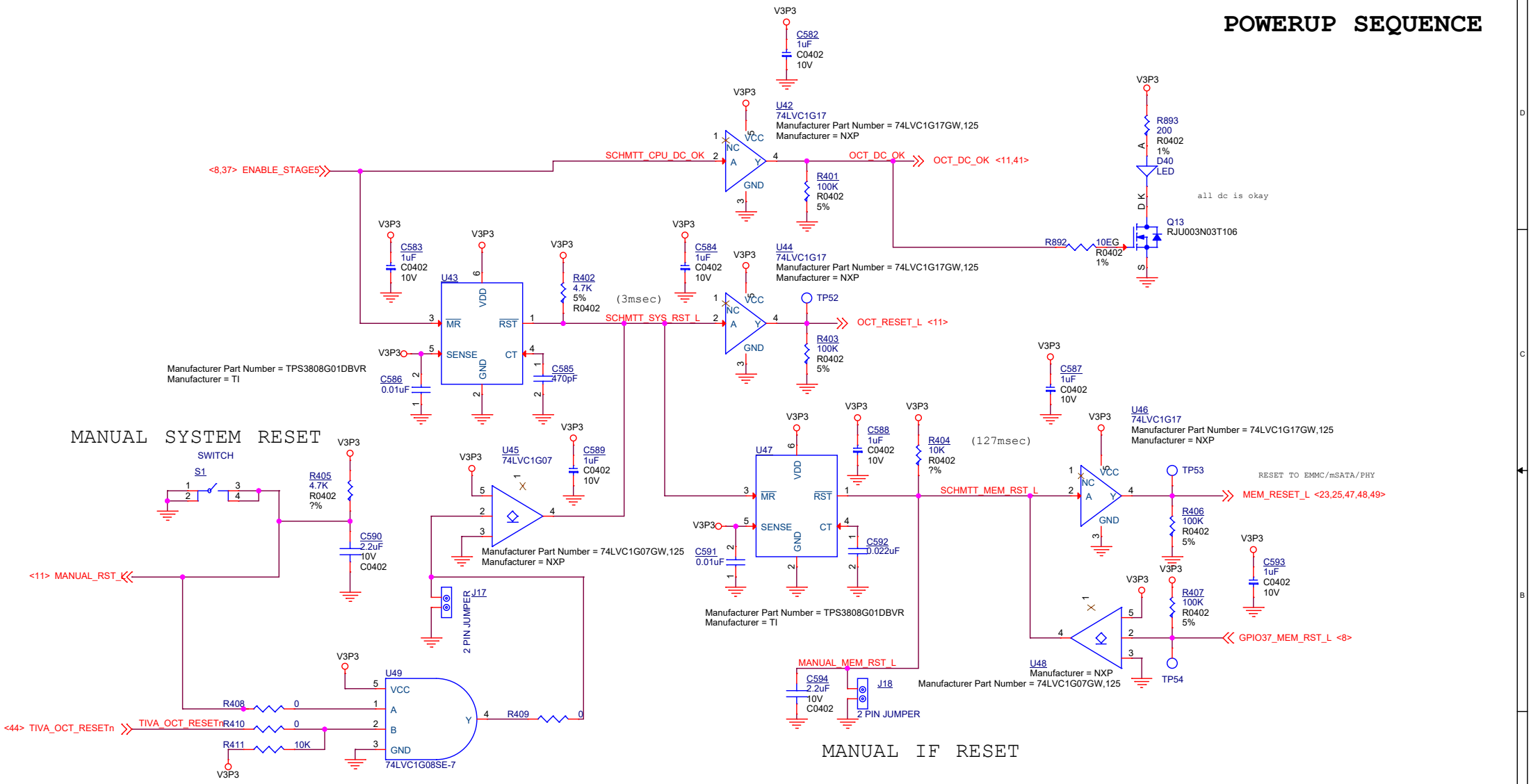
54

POWERUP SEQUENCE



Title	POWER AND RESET	
Size B	Document Number	Rev 1.0
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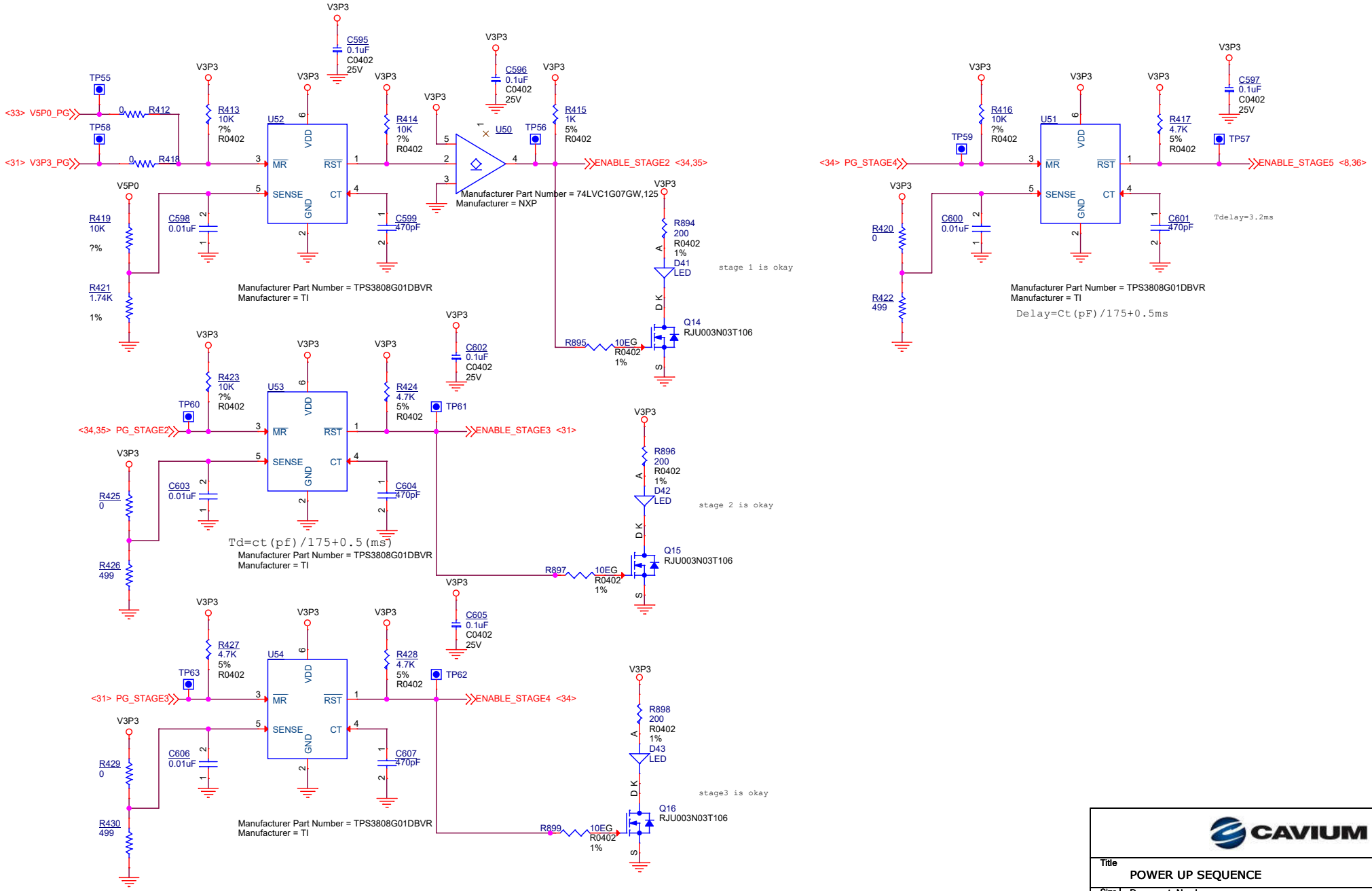
V3P3
C595 0.1uF C0402 25V
C596 0.1uF C0402 25V
C597 0.1uF C0402 25V
TP55
TP58
<33> V5P0_PG
<31> V3P3_PG
R412 0
R416 0
R413 10K ?% R0402
R414 10K ?% R0402
R415 1K 5% R0402
R416 10K ?% R0402
R417 4.7K 5% R0402
U52
U50
U51
VDD
MR
RST
SENSE
CT
GND
TP56
TP59
TP57
ENABLE_STAGE2 <34,35>
ENABLE_STAGE5 <8,36>
<34> PG_STAGE4
V5P0
R419 10K ?%
R421 1.74K 1%
C598 0.01uF
C599 470pF
C600 0.01uF
C601 470pF
R420 0
R422 499
Tdelay=3.2ms
Manufacturer Part Number = 74LVC1G07GW,125
Manufacturer = NXP
Manufacturer Part Number = TPS3808G01DBVR
Manufacturer = TI
Delay=Ct(pF)/175+0.5ms
R894 200 R0402 1%
D41 LED
stage 1 is okay
R895 10EG R0402 1%
Q14 RJU003N03T106
C602 0.1uF C0402 25V
R423 10K ?% R0402
R424 4.7K 5% R0402
TP60
TP61
<34,35> PG_STAGE2
ENABLE_STAGE3 <31>
R425 0
R426 499
C603 0.01uF
C604 470pF
Td=ct(pf)/175+0.5(ms)
R896 200 R0402 1%
D42 LED
stage 2 is okay
R897 10EG R0402 1%
Q15 RJU003N03T106
C605 0.1uF C0402 25V
R427 4.7K 5% R0402
R428 4.7K 5% R0402
TP63
TP62
<31> PG_STAGE3
ENABLE_STAGE4 <34>
R429 0
R430 499
C606 0.01uF
C607 470pF
R898 200 R0402 1%
D43 LED
stage3 is okay
R899 10EG R0402 1%
Q16 RJU003N03T106
CAVIUM
Title
POWER UP SEQUENCE
Size B
Document Number
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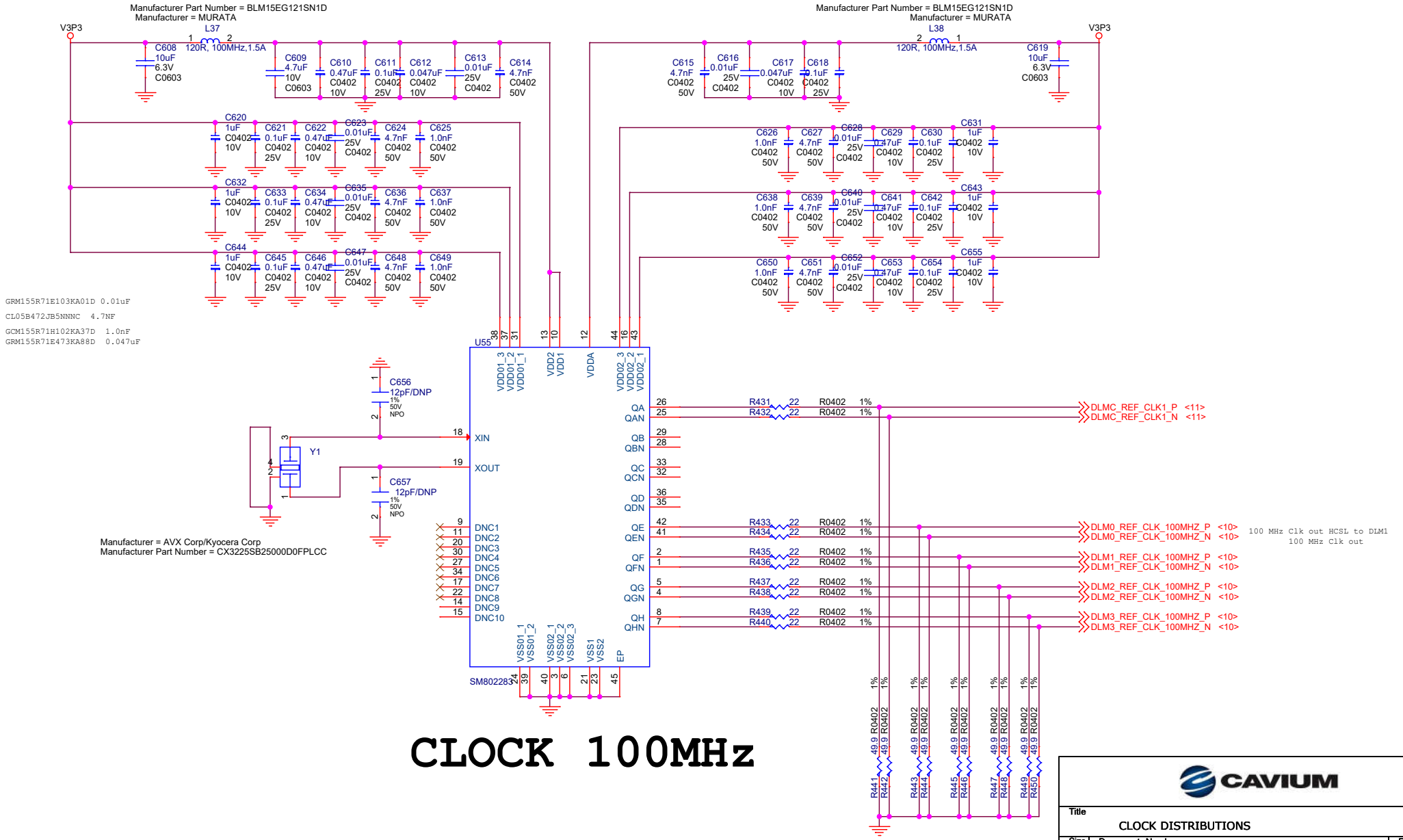
Manufacturer Part Number = BLM15EG121SN1D
Manufacturer = MURATA
L37
120R, 100MHz,1.5A
Manufacturer Part Number = BLM15EG121SN1D
Manufacturer = MURATA
L38
120R, 100MHz,1.5A
V3P3
V3P3
GRM155R71E103KA01D 0.01uF
CL05B472JB5NNNC 4.7NF
GCM155R71H102KA37D 1.0nF
GRM155R71E473KA88D 0.047uF
U55
SM802283
XIN
XOUT
Y1
C656 12pF/DNP
C657 12pF/DNP
Manufacturer = AVX Corp/Kyocera Corp
Manufacturer Part Number = CX3225SB25000D0FPLCC
DLMC_REF_CLK1_P <11>
DLMC_REF_CLK1_N <11>
DLM0_REF_CLK_100MHZ_P <10>
DLM0_REF_CLK_100MHZ_N <10>
100 MHz Clk out HCSL to DLM1
100 MHz Clk out
DLM1_REF_CLK_100MHZ_P <10>
DLM1_REF_CLK_100MHZ_N <10>
DLM2_REF_CLK_100MHZ_P <10>
DLM2_REF_CLK_100MHZ_N <10>
DLM3_REF_CLK_100MHZ_P <10>
DLM3_REF_CLK_100MHZ_N <10>
CLOCK 100MHz
CAVIUM
Title
CLOCK DISTRIBUTIONS
Size B
Document Number <Doc>
Rev 1.0
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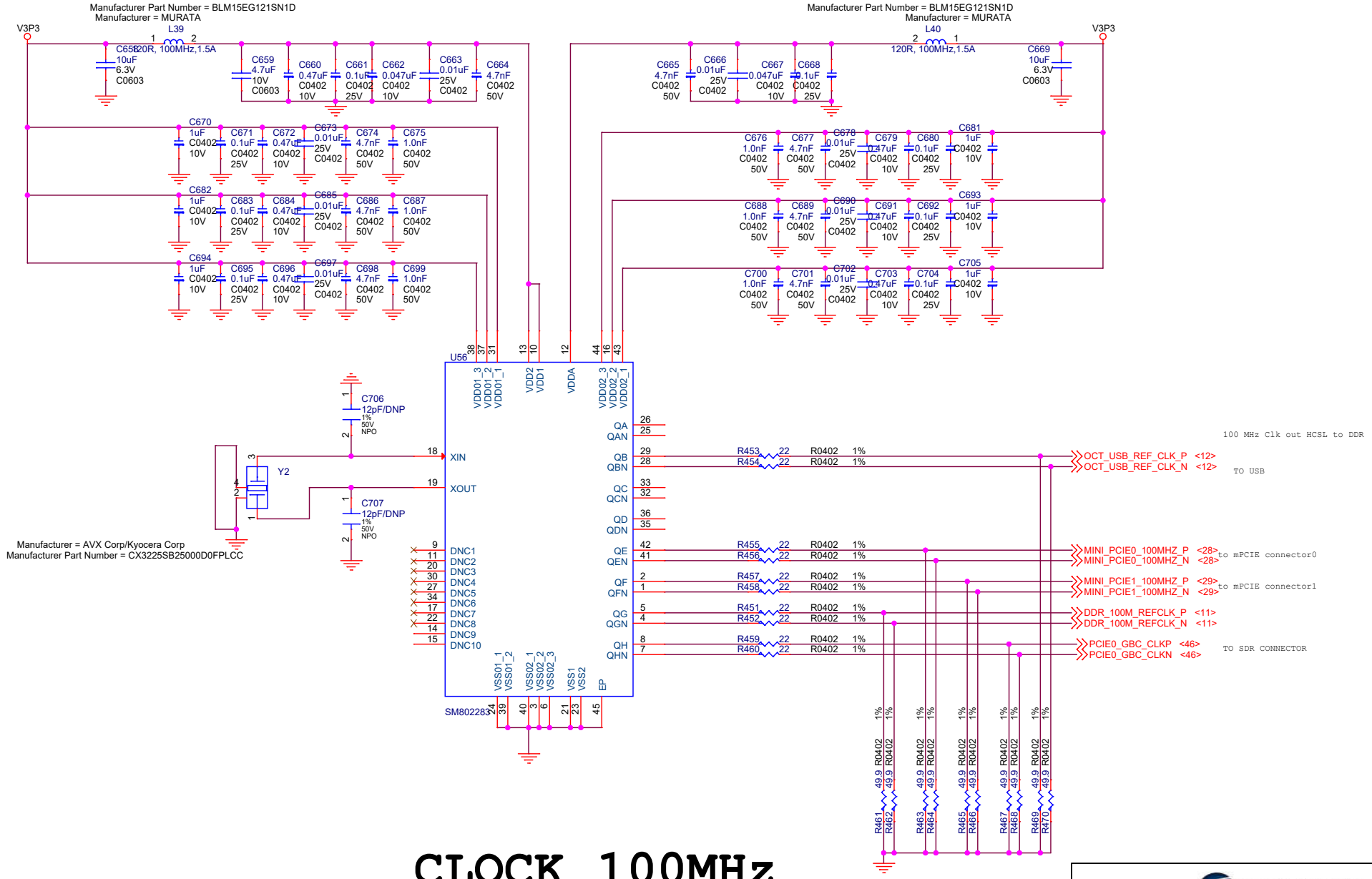

CLOCK 100MHz

CAVIUM

Title	CLOCK DISTRIBUTIONS	
Size B	Document Number <Doc>	Rev 1.0
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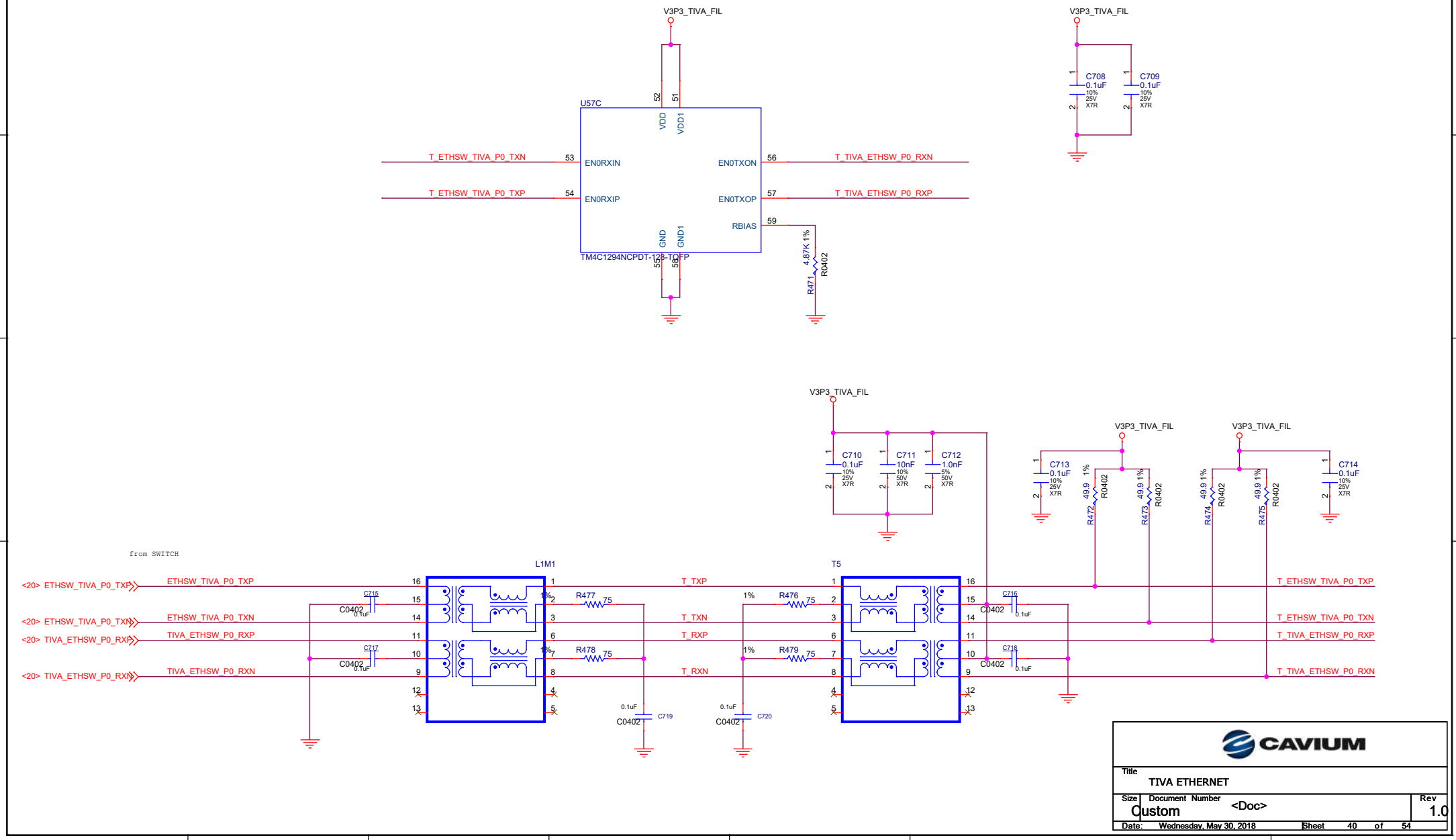

CAVIUM

Title: TIVA ETHERNET		
Size: Custom	Document Number: <Doc>	Rev: 1.0
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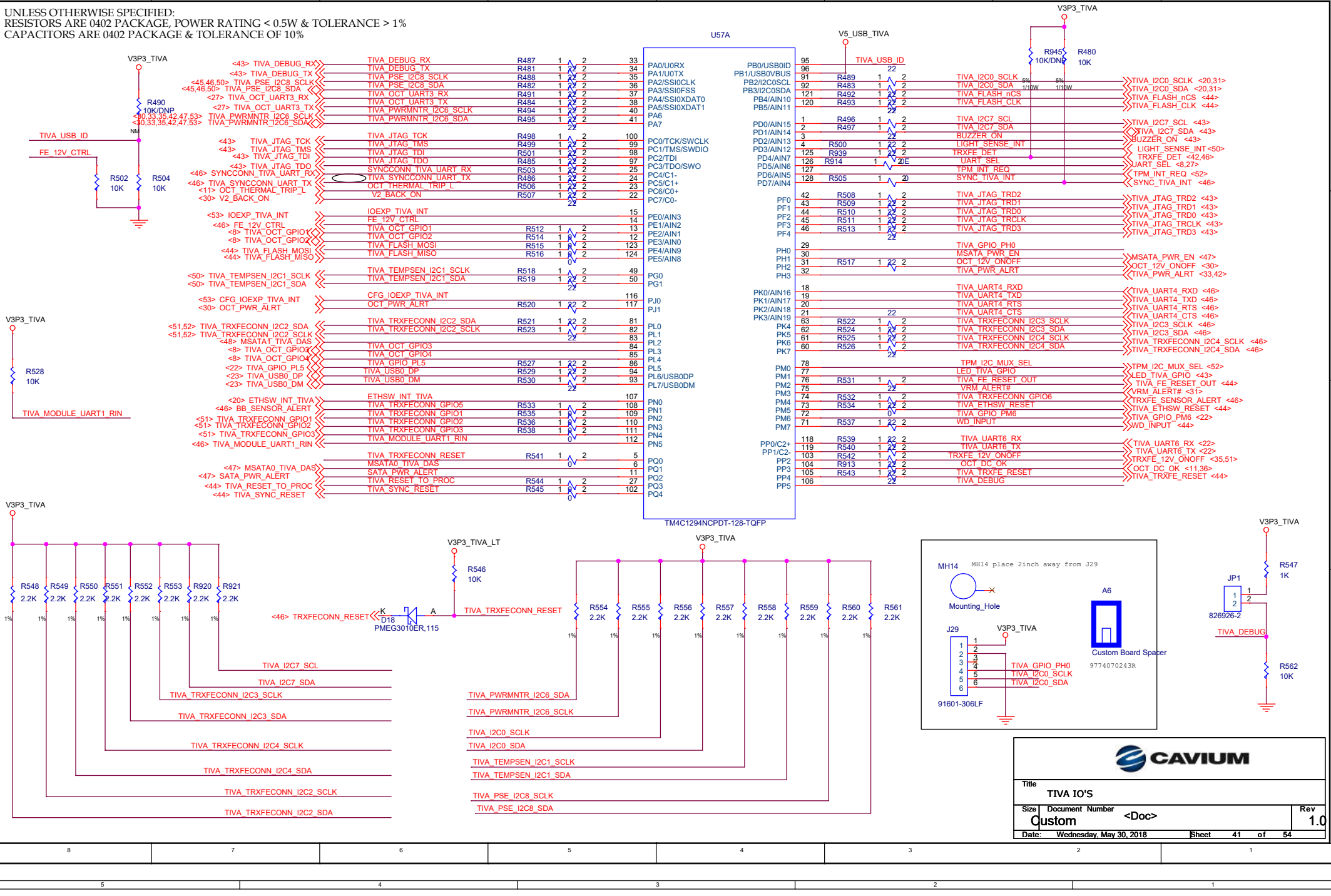
UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 0402 PACKAGE, POWER RATING < 0.5W & TOLERANCE > 1%
CAPACITORS ARE 0402 PACKAGE & TOLERANCE OF 10%



CAVIUM

Title	TIVA IO'S
Size	Custom
Document Number	<Doc>
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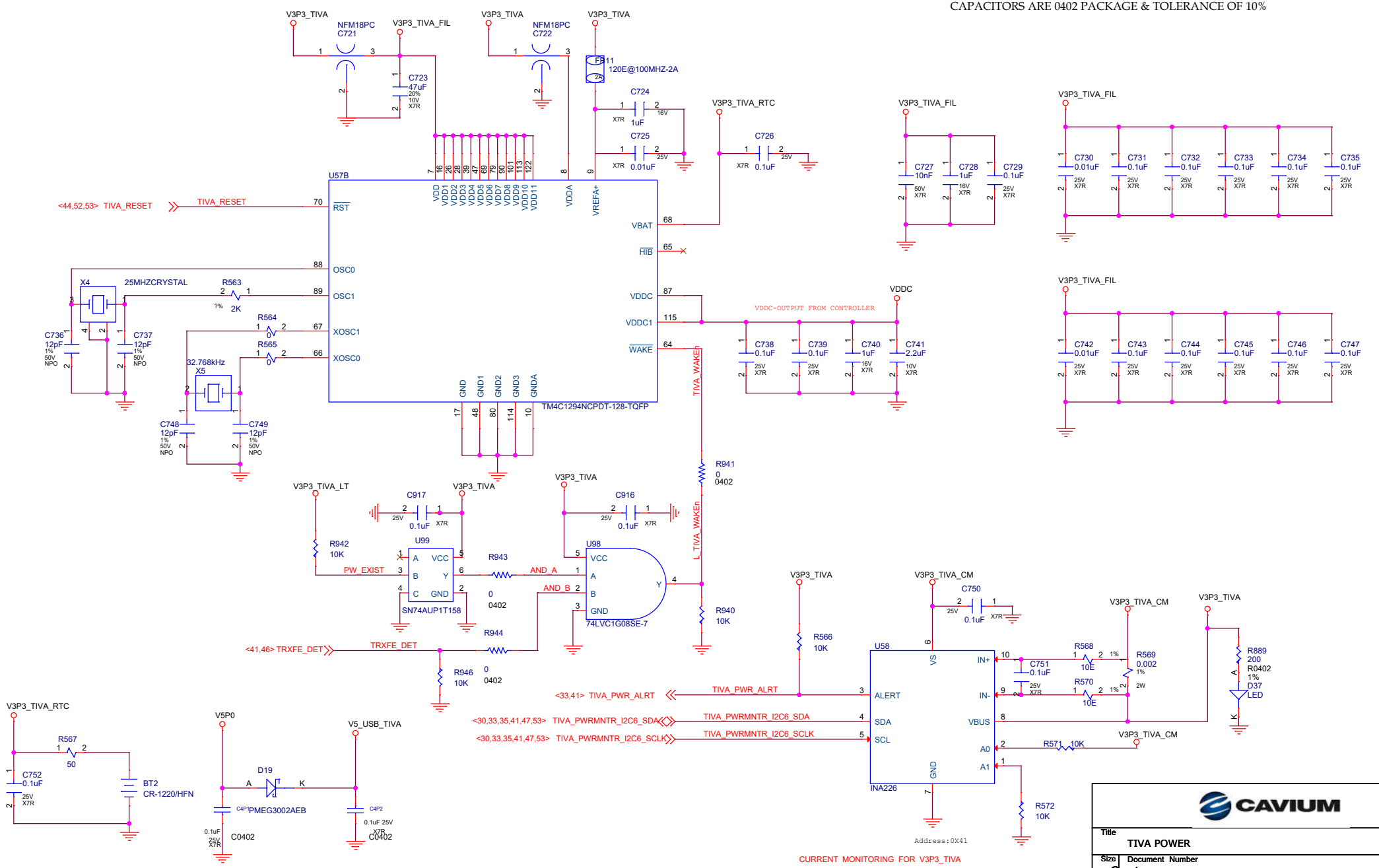
UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 0402 PACKAGE, POWER RATING < 0.5W & TOLERANCE > 1%
CAPACITORS ARE 0402 PACKAGE & TOLERANCE OF 10%



CAVIUM

Title: TIVA POWER		
Size: Custom	Document Number	Rev: 1.0
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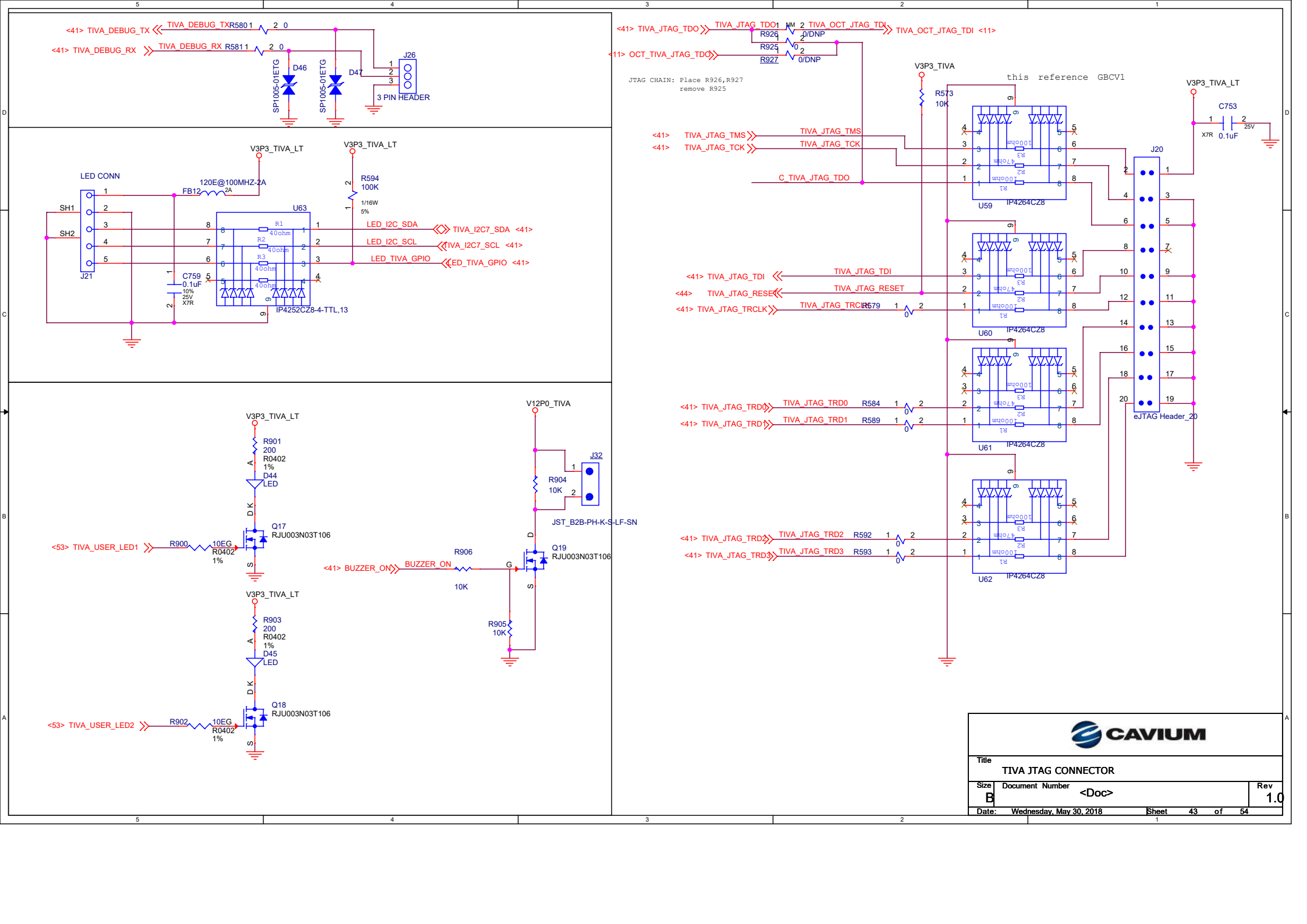
TIVA_DEBUG_TX
TIVA_DEBUG_RX
R580
R581
D46
D47
SP1005-01ETG
J26
3 PIN HEADER
LED CONN
SH1
SH2
J21
FB12
120E@100MHZ-2A
V3P3_TIVA_LT
R594
100K
U63
IP4252CZ8-4-TTL,13
C759
0.1uF
LED_I2C_SDA
LED_I2C_SCL
LED_TIVA_GPIO
TIVA_I2C7_SDA
TIVA_I2C7_SCL
LED_TIVA_GPIO
TIVA_JTAG_TDO
TIVA_OCT_JTAG_TDI
OCT_TIVA_JTAG_TDO
R926
R925
R927
0/DNP
JTAG CHAIN: Place R926,R927
remove R925
this reference GBCV1
R573
10K
C753
0.1uF
TIVA_JTAG_TMS
TIVA_JTAG_TCK
C_TIVA_JTAG_TDO
U59
U60
U61
U62
IP4264CZ8
J20
eJTAG Header_20
TIVA_JTAG_TDI
TIVA_JTAG_RESET
TIVA_JTAG_TRCLK
R679
TIVA_JTAG_TRD0
TIVA_JTAG_TRD1
TIVA_JTAG_TRD2
TIVA_JTAG_TRD3
R584
R589
R592
R593
R901
R903
D44
D45
LED
Q17
Q18
RJU003N03T106
R900
R902
10EG
R0402
TIVA_USER_LED1
TIVA_USER_LED2
V12P0_TIVA
J32
JST_B2B-PH-K-S-LF-SN
R904
10K
R905
10K
R906
Q19
BUZZER_ON
CAVIUM
Title
TIVA JTAG CONNECTOR
Size
B
Document Number
<Doc>
Rev
1.0
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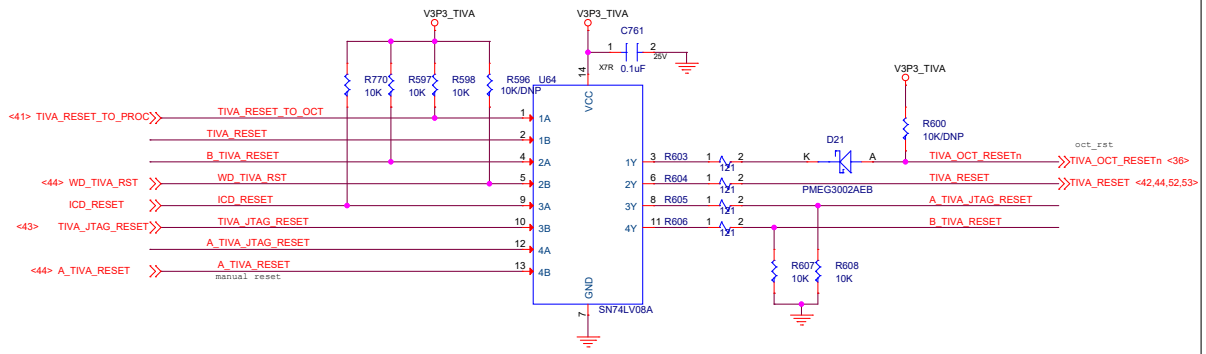
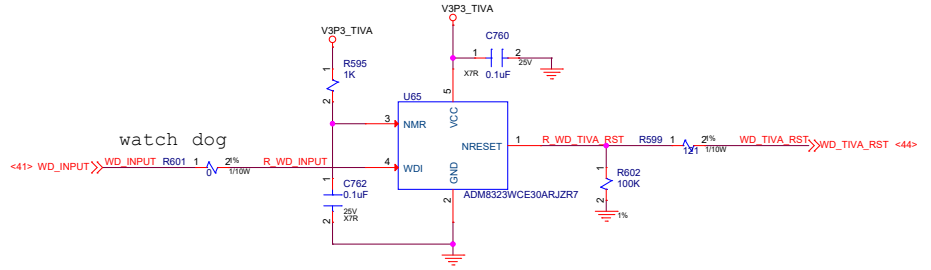
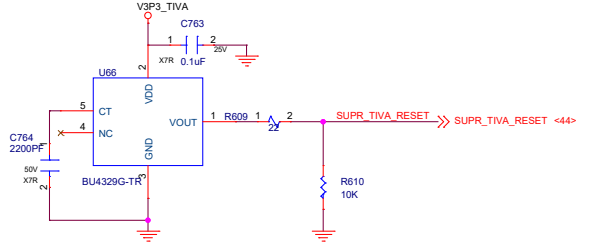
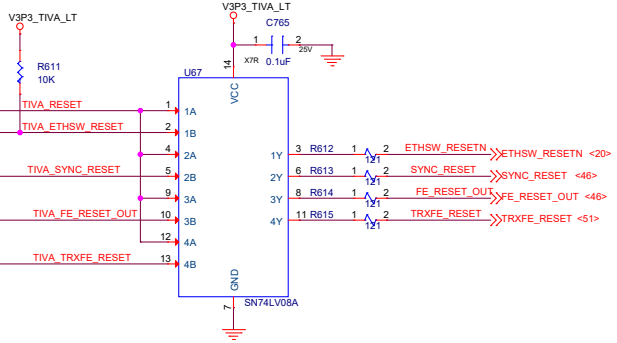
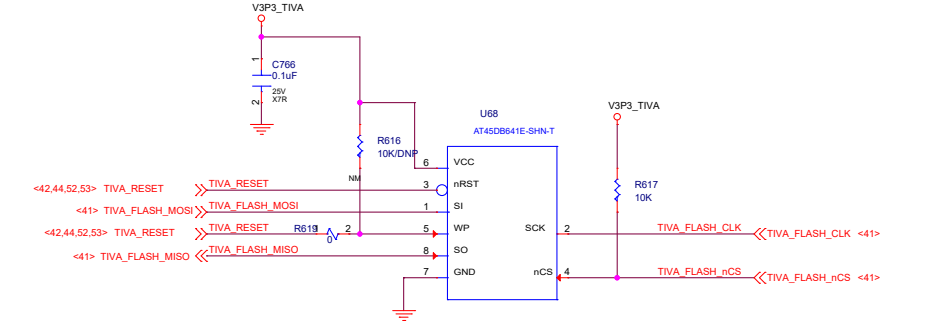
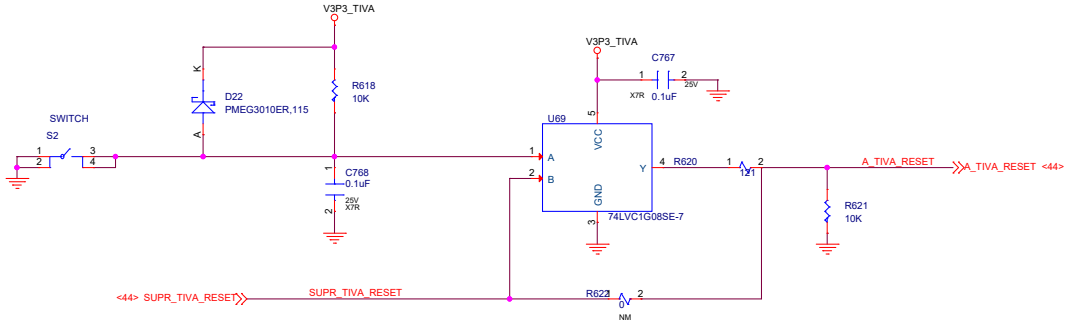






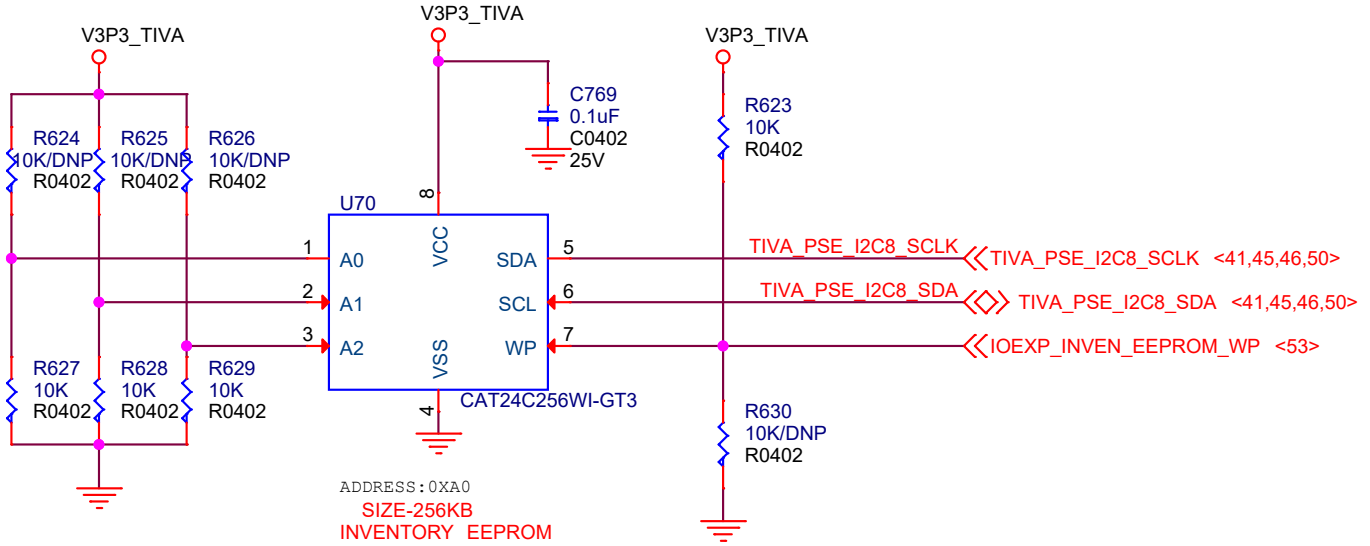


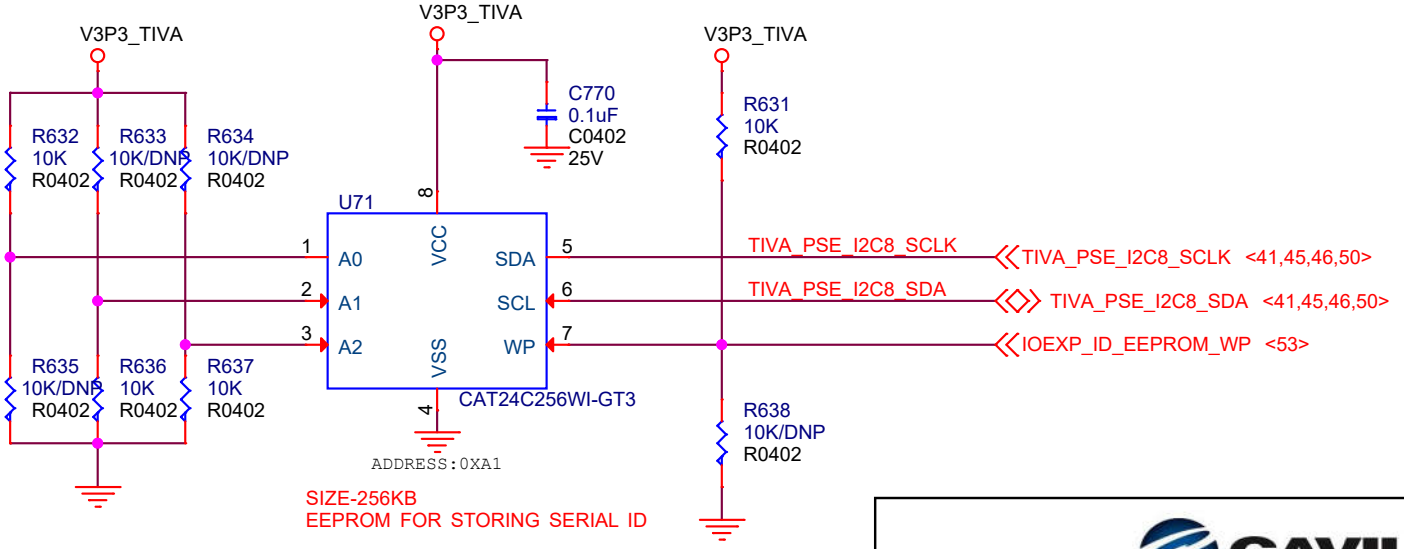




CAVIUM

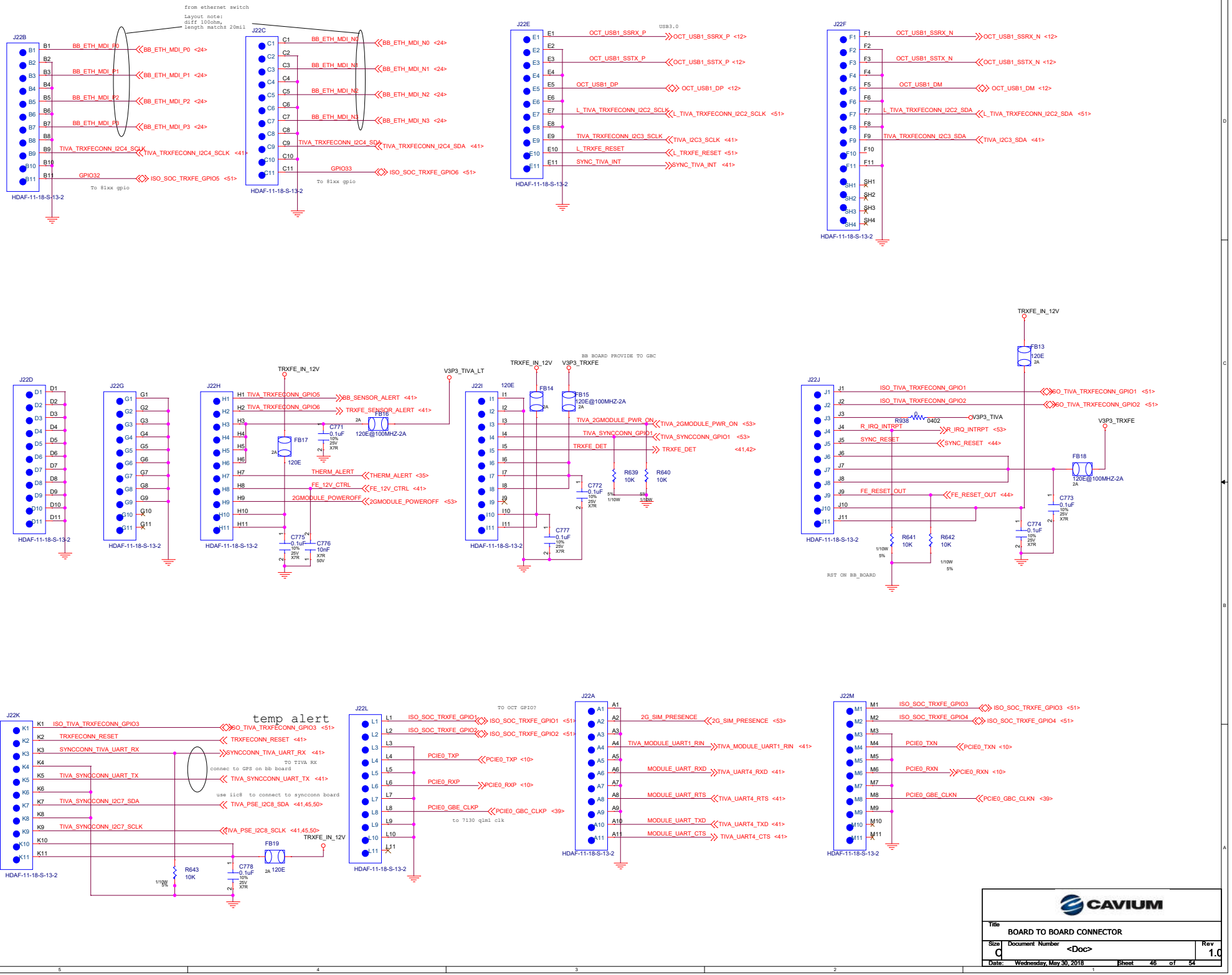
Title: TIVA FLASH & RESET		
Size: Custom	Document Number: <Doc>	Rev: 1.0
Date: Wednesday, May 30, 2018	Sheet 44 of 54	





CAVIUM

Title: TIVA EEPROM		
Size: A	Document Number: <Doc>	Rev: 1.0
Date: Wednesday, May 30, 2018	Sheet 45 of 54	


from ethernet switch
Layout note:
diff 100ohm,
length match± 20mil
J22B
J22C
J22E
J22F
HDAF-11-18-S-13-2
BB_ETH_MDI_P0 <24>
BB_ETH_MDI_P1 <24>
BB_ETH_MDI_P2 <24>
BB_ETH_MDI_P3 <24>
BB_ETH_MDI_N0 <24>
BB_ETH_MDI_N1 <24>
BB_ETH_MDI_N2 <24>
BB_ETH_MDI_N3 <24>
TIVA_TRXFECONN_I2C4_SCLK
TIVA_TRXFECONN_I2C4_SCLK <41>
TIVA_TRXFECONN_I2C4_SDA <41>
GPIO32
ISO_SOC_TRXFE_GPIO5 <51>
GPIO33
ISO_SOC_TRXFE_GPIO6 <51>
To 81xx gpio
USB3.0
OCT_USB1_SSRX_P
OCT_USB1_SSRX_P <12>
OCT_USB1_SSTX_P
OCT_USB1_SSTX_P <12>
OCT_USB1_DP
OCT_USB1_DP <12>
L_TIVA_TRXFECONN_I2C2_SCLK
L_TIVA_TRXFECONN_I2C2_SCLK <51>
TIVA_TRXFECONN_I2C3_SCLK
TIVA_I2C3_SCLK <41>
L_TRXFE_RESET
L_TRXFE_RESET <51>
SYNC_TIVA_INT
SYNC_TIVA_INT <41>
OCT_USB1_SSRX_N
OCT_USB1_SSRX_N <12>
OCT_USB1_SSTX_N
OCT_USB1_SSTX_N <12>
OCT_USB1_DM
OCT_USB1_DM <12>
L_TIVA_TRXFECONN_I2C2_SDA
L_TIVA_TRXFECONN_I2C2_SDA <51>
TIVA_TRXFECONN_I2C3_SDA
TIVA_I2C3_SDA <41>
J22D
J22G
J22H
J22I
J22J
TRXFE_IN_12V
V3P3_TIVA_LT
V3P3_TRXFE
BB BOARD PROVIDE TO GBC
TIVA_TRXFECONN_GPIO5
BB_SENSOR_ALERT <41>
TIVA_TRXFECONN_GPIO6
TRXFE_SENSOR_ALERT <41>
THERM_ALERT
THERM_ALERT <35>
FE_12V_CTRL
FE_12V_CTRL <41>
2GMODULE_POWEROFF
2GMODULE_POWEROFF <53>
TIVA_2GMODULE_PWR_ON
TIVA_2GMODULE_PWR_ON <53>
TIVA_SYNCCONN_GPIO1
TIVA_SYNCONN_GPIO1 <53>
TRXFE_DET
TRXFE_DET <41,42>
ISO_TIVA_TRXFECONN_GPIO1
ISO_TIVA_TRXFECONN_GPIO1 <51>
ISO_TIVA_TRXFECONN_GPIO2
ISO_TIVA_TRXFECONN_GPIO2 <51>
R_IRQ_INTRPT
R_IRQ_INTRPT <53>
SYNC_RESET
SYNC_RESET <44>
FE_RESET_OUT
FE_RESET_OUT <44>
RST ON BB_BOARD
J22K
J22L
J22A
J22M
temp alert
ISO_TIVA_TRXFECONN_GPIO3
ISO_TIVA_TRXFECONN_GPIO3 <51>
TRXFECONN_RESET
TRXFECONN_RESET <41>
SYNCCONN_TIVA_UART_RX
SYNCCONN_TIVA_UART_RX <41>
TIVA_SYNCCONN_UART_TX
TIVA_SYNCCONN_UART_TX <41>
TIVA_SYNCCONN_I2C7_SDA
TIVA_PSE_I2C8_SDA <41,45,50>
TIVA_SYNCCONN_I2C7_SCLK
TIVA_PSE_I2C8_SCLK <41,45,50>
connec to GPS on bb board
TO TIVA RX
use iic8 to connect to syncconn board
TO OCT GPIO?
ISO_SOC_TRXFE_GPIO1
ISO_SOC_TRXFE_GPIO1 <51>
ISO_SOC_TRXFE_GPIO2
ISO_SOC_TRXFE_GPIO2 <51>
PCIE0_TXP
PCIE0_TXP <10>
PCIE0_RXP
PCIE0_RXP <10>
PCIE0_GBE_CLKP
PCIE0_GBC_CLKP <39>
to 7130 qlm1 clk
2G_SIM_PRESENCE
2G_SIM_PRESENCE <53>
TIVA_MODULE_UART1_RIN
TIVA_MODULE_UART1_RIN <41>
MODULE_UART_RXD
TIVA_UART4_RXD <41>
MODULE_UART_RTS
TIVA_UART4_RTS <41>
MODULE_UART_TXD
TIVA_UART4_TXD <41>
MODULE_UART_CTS
TIVA_UART4_CTS <41>
ISO_SOC_TRXFE_GPIO3
ISO_SOC_TRXFE_GPIO3 <51>
ISO_SOC_TRXFE_GPIO4
ISO_SOC_TRXFE_GPIO4 <51>
PCIE0_TXN
PCIE0_TXN <10>
PCIE0_RXN
PCIE0_RXN <10>
PCIE0_GBE_CLKN
PCIE0_GBC_CLKN <39>
FB13
FB14
FB15
FB16
FB17
FB18
FB19
120E@100MHZ-2A
120E
R938
0402
R639
R640
R641
R642
R643
10K
C771
C772
C773
C774
C775
C776
C777
C778
0.1uF
10nF
Title
BOARD TO BOARD CONNECTOR
Size
C
Document Number
<Doc>
Rev
1.0
Date:
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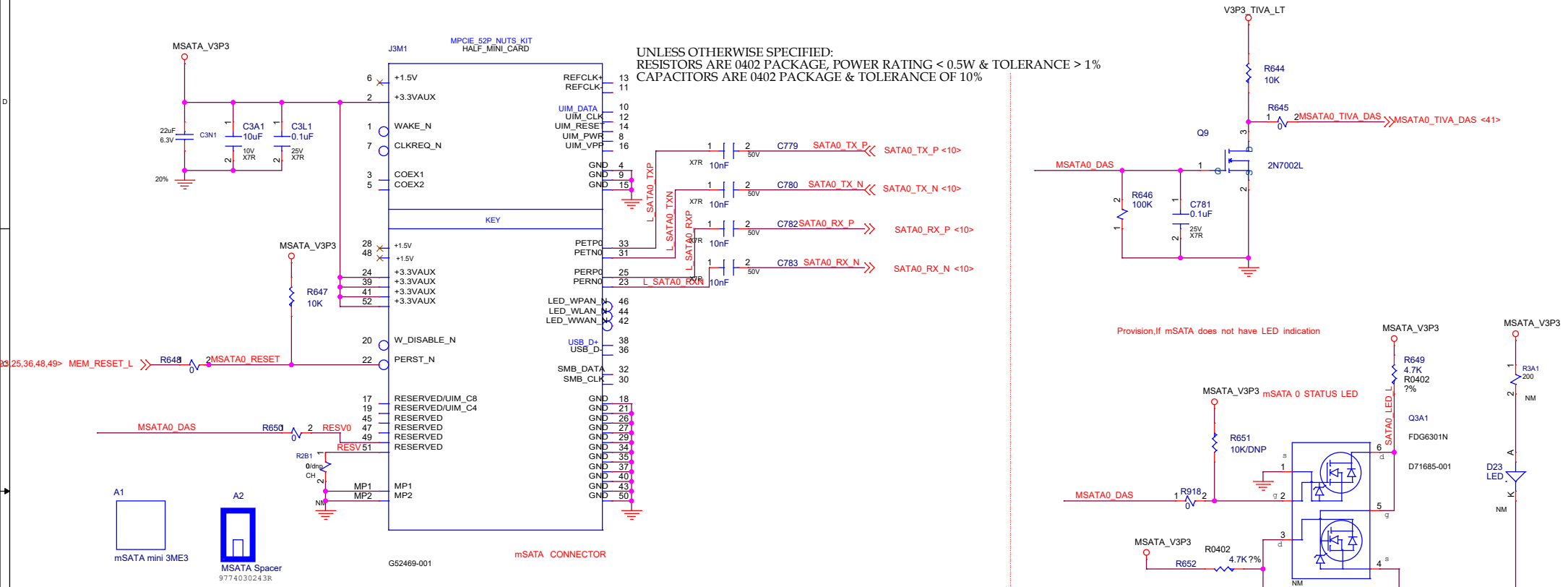
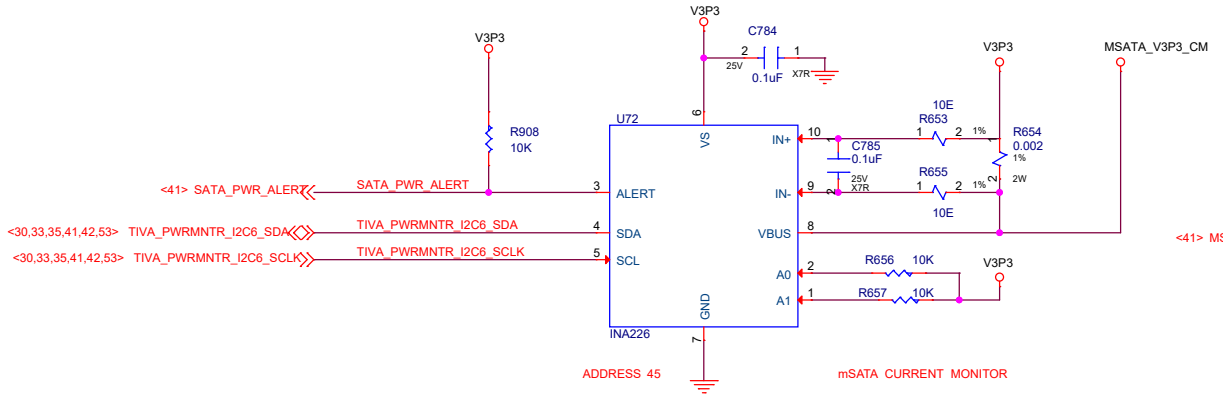
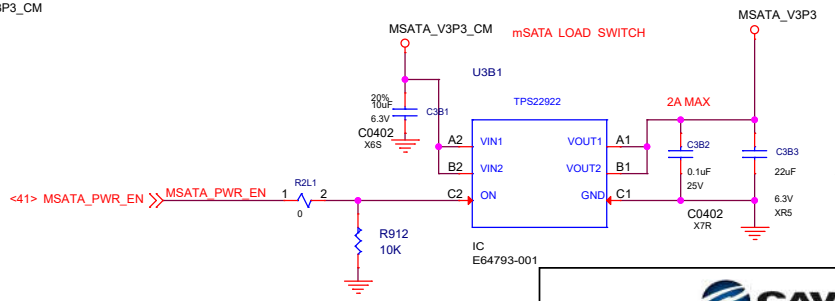
46
of
54

UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 0402 PACKAGE, POWER RATING < 0.5W & TOLERANCE > 1%
CAPACITORS ARE 0402 PACKAGE & TOLERANCE OF 10%

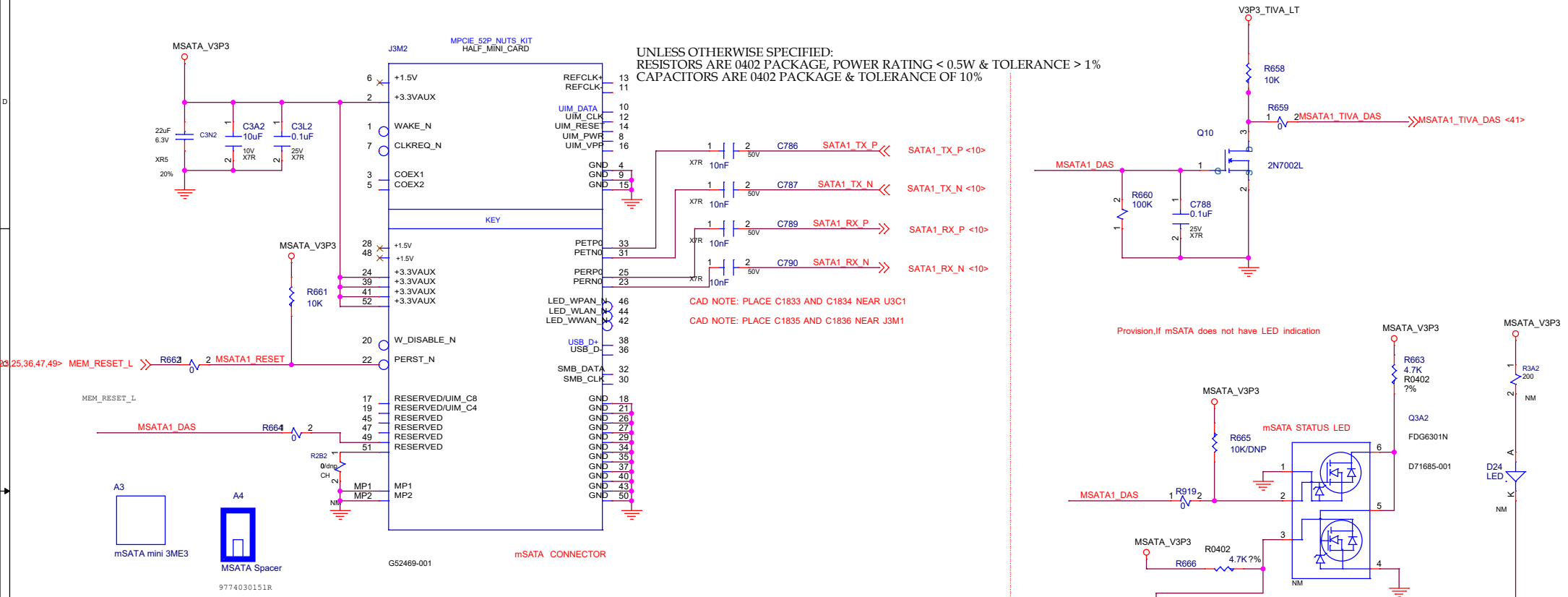






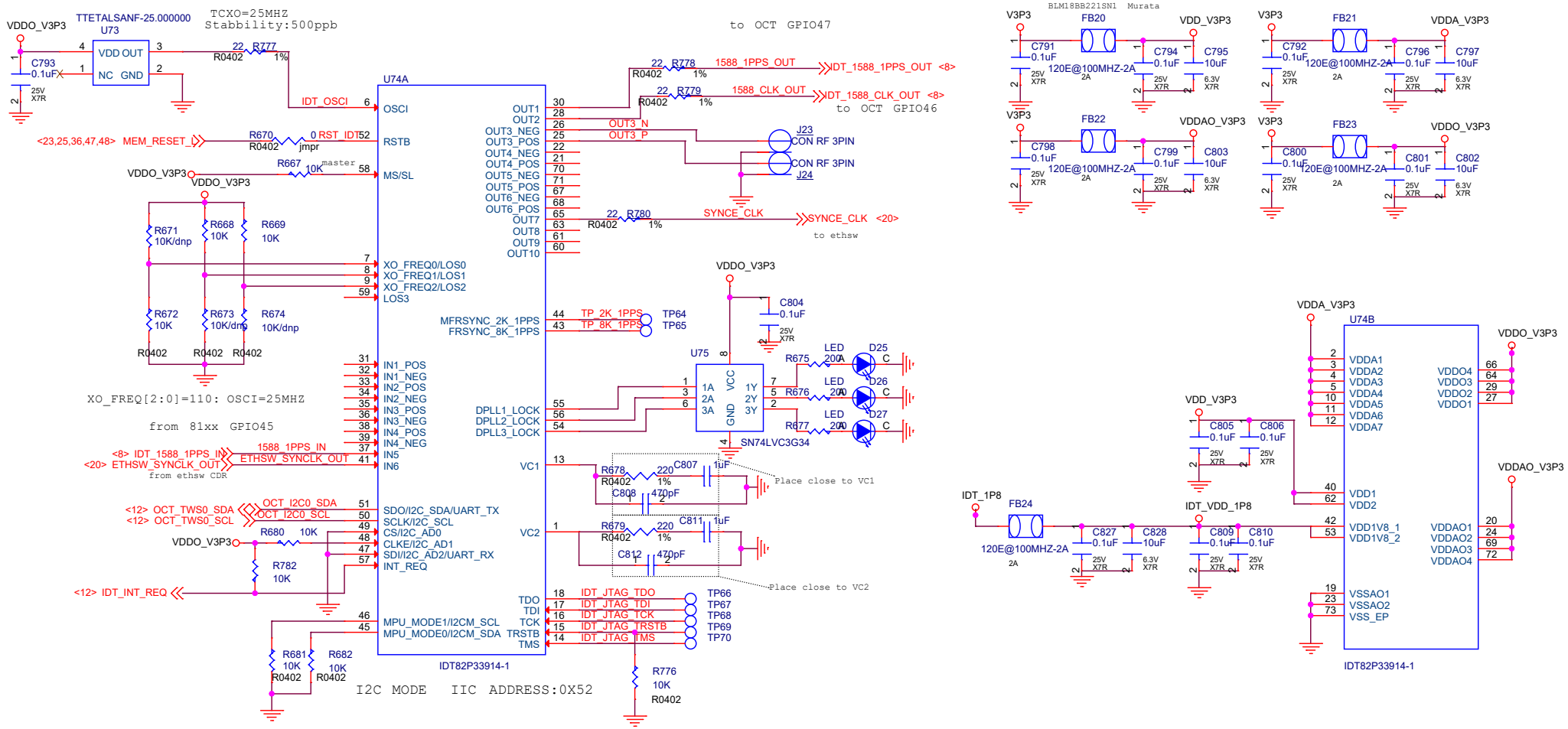
CAVIUM

Title: mSATA connector0		
Size	Document Number: Custom	Rev: 1.0
Date: Wednesday, May 30, 2018	Sheet 47 of 54	



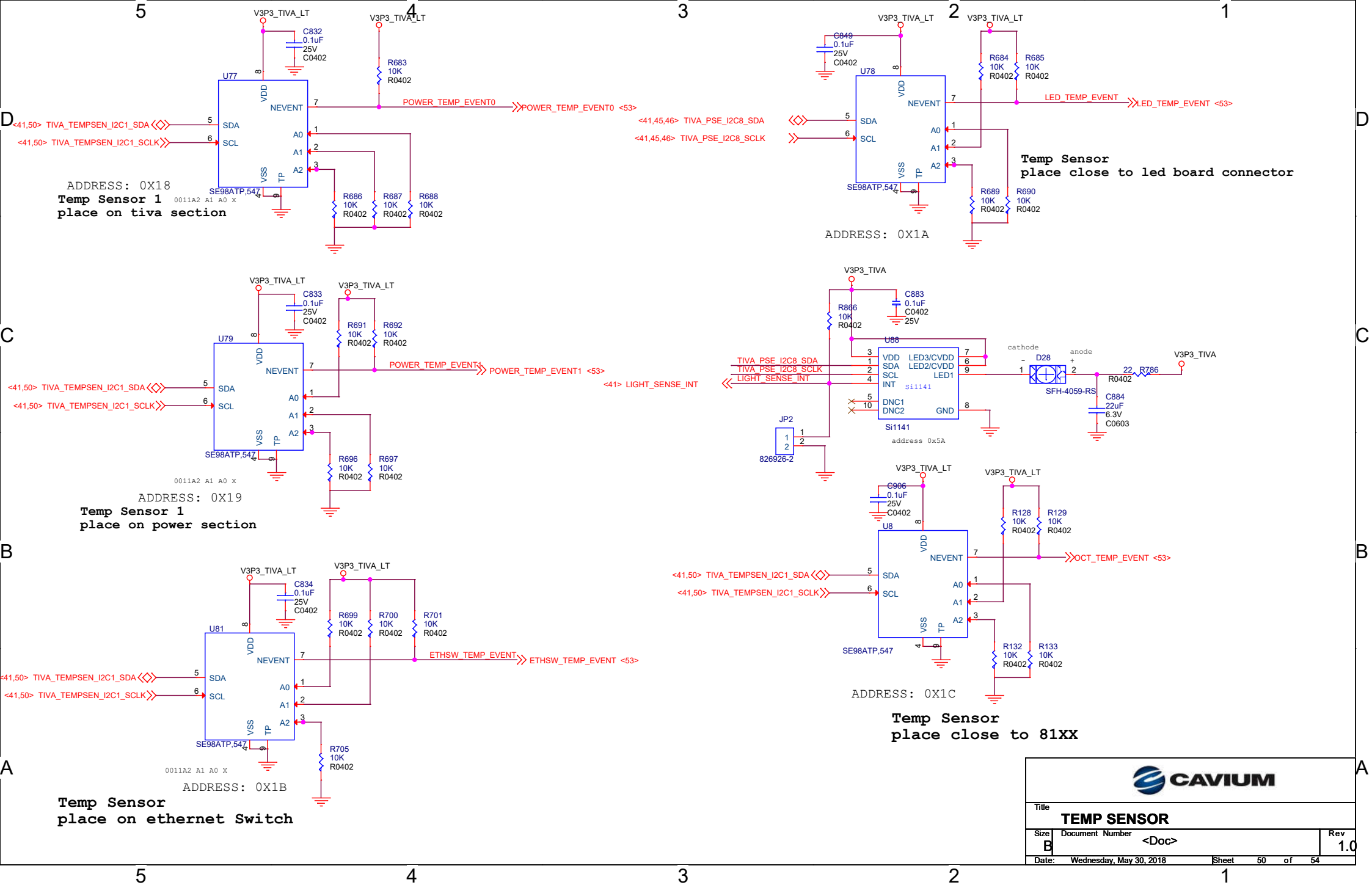
UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 0402 PACKAGE, POWER RATING < 0.5W & TOLERANCE > 1%
CAPACITORS ARE 0402 PACKAGE & TOLERANCE OF 10%

Title	mSATA connector1	
Size	Document Number Custom	Rev 1.0
Date: Wednesday, May 30, 2018	Sheet 48 of 54	



CAVIUM

Title	PTP Moduel	
Size B	Document Number <Doc>	Rev 1.0
Date: Wednesday, May 30, 2018	Sheet 49 of 54	


V3P3_TIVA_LT
C832 0.1uF 25V C0402
R683 10K R0402
U77
VDD
NEVENT
SDA
SCL
A0
A1
A2
VSS
TP
SE98ATP,547
POWER_TEMP_EVENT0
POWER_TEMP_EVENT0 <53>
<41,50> TIVA_TEMPSEN_I2C1_SDA
<41,50> TIVA_TEMPSEN_I2C1_SCLK
R686 10K R0402
R687 10K R0402
R688 10K R0402
ADDRESS: 0X18
Temp Sensor 1
place on tiva section
0011A2 A1 A0 X
C849 0.1uF 25V C0402
U78
R684 10K R0402
R685 10K R0402
LED_TEMP_EVENT
LED_TEMP_EVENT <53>
<41,45,46> TIVA_PSE_I2C8_SDA
<41,45,46> TIVA_PSE_I2C8_SCLK
R689 10K R0402
R690 10K R0402
ADDRESS: 0X1A
Temp Sensor
place close to led board connector
C833 0.1uF 25V C0402
U79
R691 10K R0402
R692 10K R0402
POWER_TEMP_EVENT1
POWER_TEMP_EVENT1 <53>
<41> LIGHT_SENSE_INT
R696 10K R0402
R697 10K R0402
ADDRESS: 0X19
Temp Sensor 1
place on power section
V3P3_TIVA
C883 0.1uF 25V C0402
R866 10K R0402
U88
TIVA_PSE_I2C8_SDA
TIVA_PSE_I2C8_SCLK
LIGHT_SENSE_INT
VDD
SDA
SCL
INT
LED3/CVDD
LED2/CVDD
LED1
DNC1
DNC2
GND
Si1141
address 0x5A
JP2
826926-2
cathode
anode
D28
SFH-4059-RS
R786 22 R0402
C884 22uF 6.3V C0603
C834 0.1uF 25V C0402
U81
R699 10K R0402
R700 10K R0402
R701 10K R0402
ETHSW_TEMP_EVENT
ETHSW_TEMP_EVENT <53>
R705 10K R0402
ADDRESS: 0X1B
Temp Sensor
place on ethernet Switch
C906 0.1uF 25V C0402
U8
R128 10K R0402
R129 10K R0402
OCT_TEMP_EVENT <53>
R132 10K R0402
R133 10K R0402
ADDRESS: 0X1C
Temp Sensor
place close to 81XX
CAVIUM
Title
TEMP SENSOR
Size B
Document Number <Doc>
Rev 1.0
Date: Wednesday, May 30, 2018
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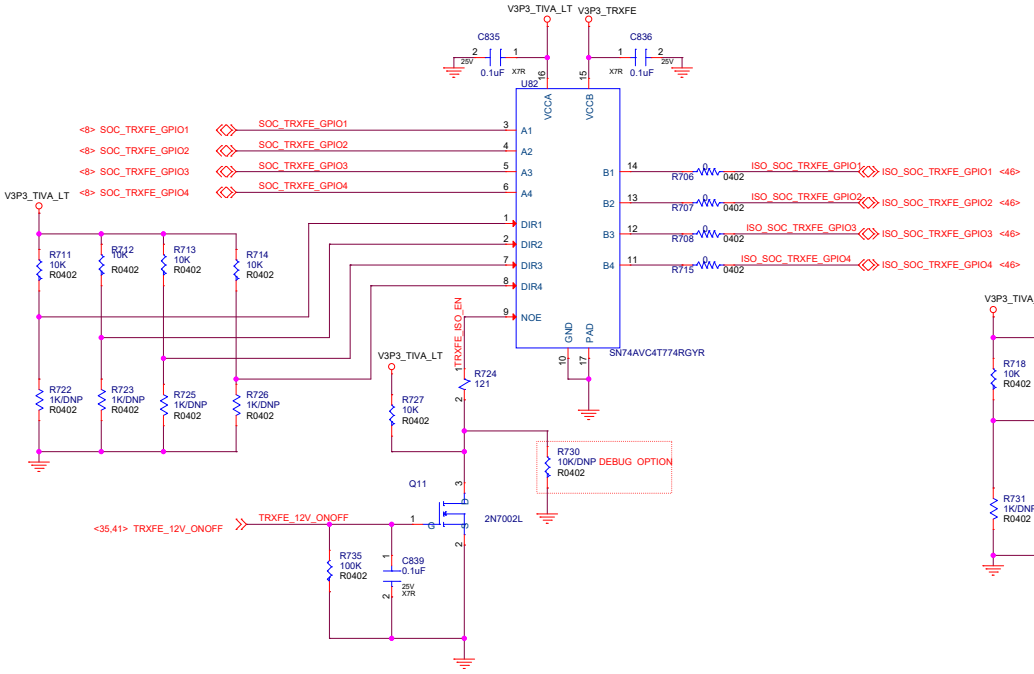
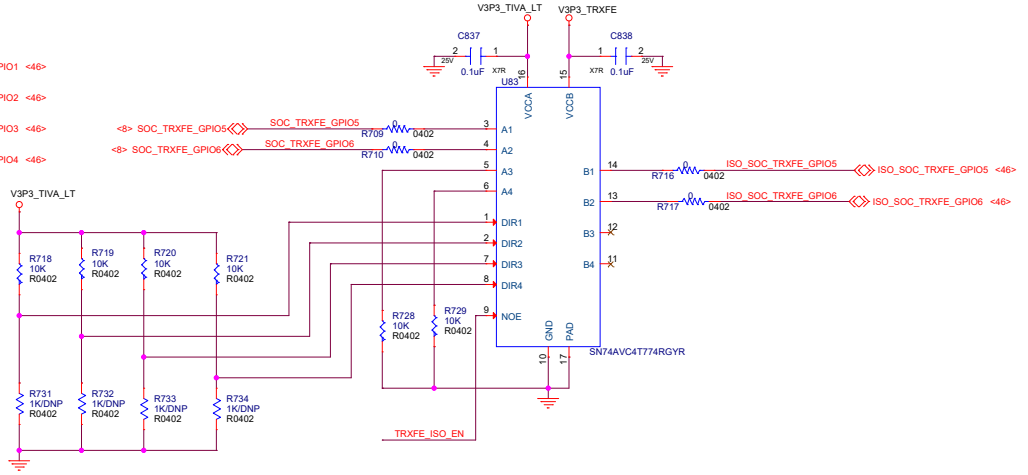
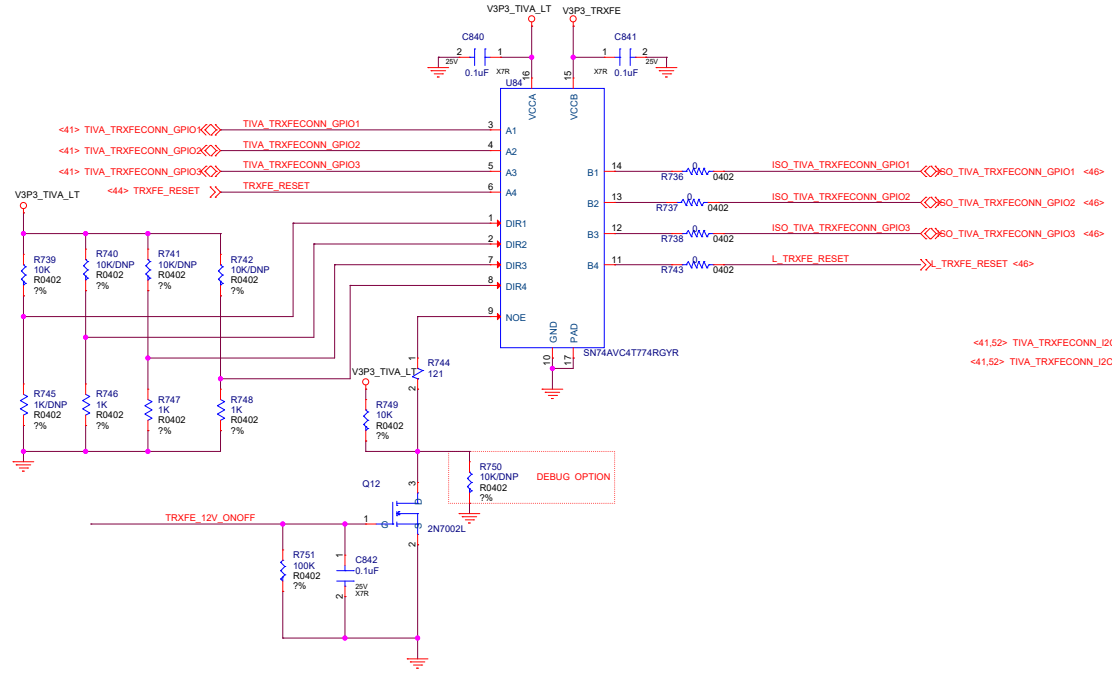
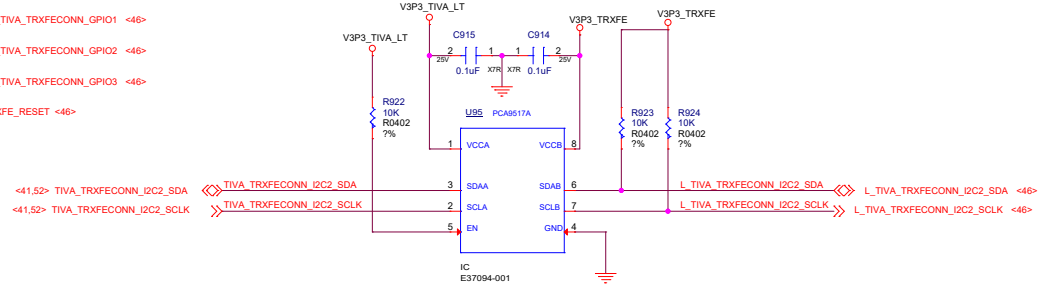
UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 0402 PACKAGE, POWER RATING < 0.5W & TOLERANCE > 1%
CAPACITORS ARE 0402 PACKAGE & TOLERANCE OF 10%









CAVIUM

Title: TIVA OCT-IO ISOLATION

Size	Document Number	Rev
C	<Doc>	1.0

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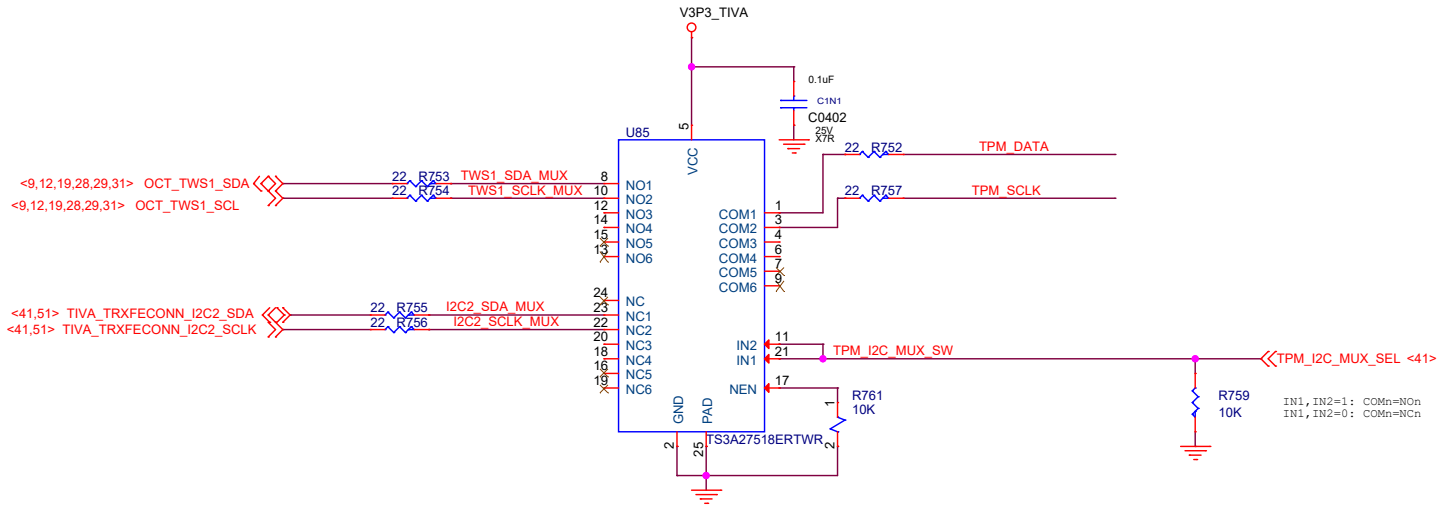
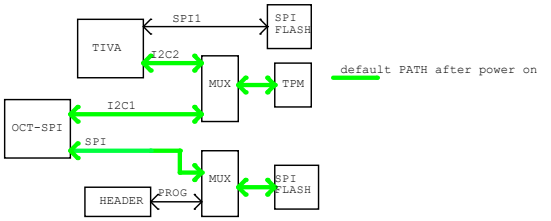
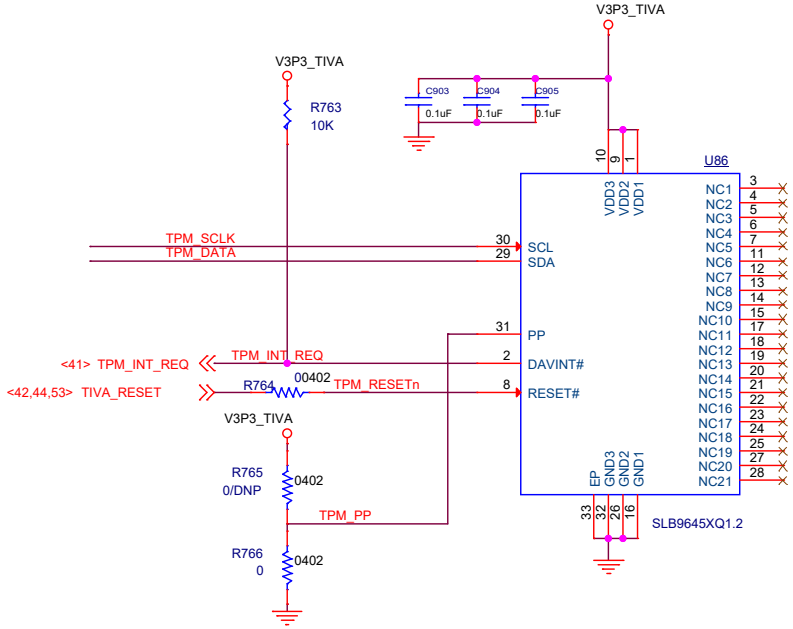
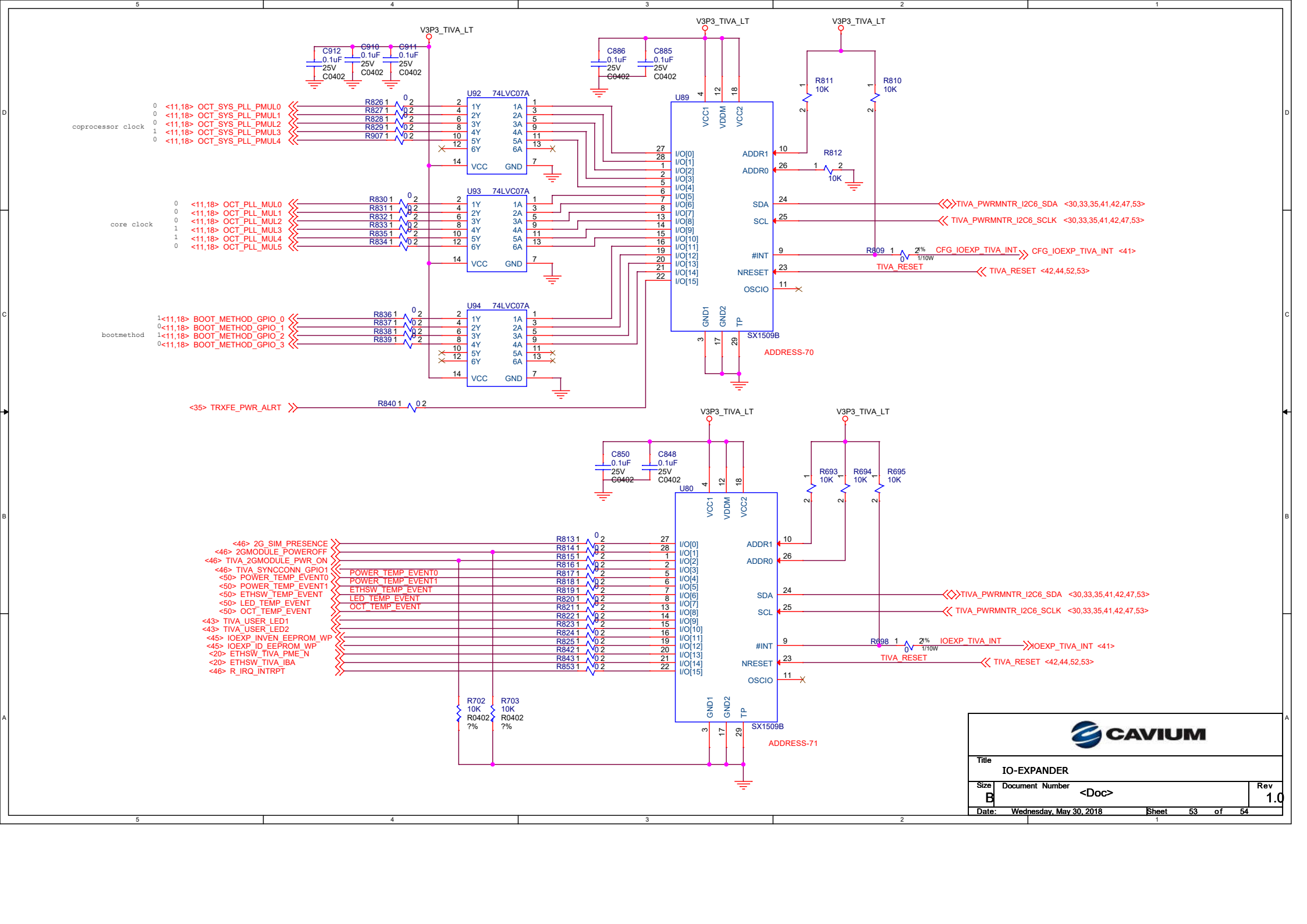






CAVIUM

Title: Trusted Platform Modul		
Size: B	Document Number: <Doc>	Rev: 1.0
Date: Wednesday, May 30, 2018	Sheet 52 of 54	


V3P3_TIVA_LT
C912 0.1uF 25V C0402
C910 0.1uF 25V C0402
C911 0.1uF 25V C0402
C886 0.1uF 25V C0402
C885 0.1uF 25V C0402
U92 74LVC07A
U93 74LVC07A
U94 74LVC07A
U89
SX1509B
ADDRESS-70
R811 10K
R810 10K
R812 10K
R826 R827 R828 R829 R907
R830 R831 R832 R833 R835 R834
R836 R837 R838 R839
R840
coprocessor clock
core clock
bootmethod
<11,18> OCT_SYS_PLL_PMUL0
<11,18> OCT_SYS_PLL_PMUL1
<11,18> OCT_SYS_PLL_PMUL2
<11,18> OCT_SYS_PLL_PMUL3
<11,18> OCT_SYS_PLL_PMUL4
<11,18> OCT_PLL_MUL0
<11,18> OCT_PLL_MUL1
<11,18> OCT_PLL_MUL2
<11,18> OCT_PLL_MUL3
<11,18> OCT_PLL_MUL4
<11,18> OCT_PLL_MUL5
<11,18> BOOT_METHOD_GPIO_0
<11,18> BOOT_METHOD_GPIO_1
<11,18> BOOT_METHOD_GPIO_2
<11,18> BOOT_METHOD_GPIO_3
<35> TRXFE_PWR_ALRT
TIVA_PWRMNTR_I2C6_SDA <30,33,35,41,42,47,53>
TIVA_PWRMNTR_I2C6_SCLK <30,33,35,41,42,47,53>
CFG_IOEXP_TIVA_INT
CFG_IOEXP_TIVA_INT <41>
TIVA_RESET
TIVA_RESET <42,44,52,53>
C850 0.1uF 25V C0402
C848 0.1uF 25V C0402
U80
R693 10K
R694 10K
R695 10K
R813 R814 R815 R816 R817 R818 R819 R820 R821 R822 R823 R824 R825 R842 R843 R853
<46> 2G_SIM_PRESENCE
<46> 2GMODULE_POWEROFF
<46> TIVA_2GMODULE_PWR_ON
<46> TIVA_SYNCCONN_GPIO1
<50> POWER_TEMP_EVENT0
<50> POWER_TEMP_EVENT1
<50> ETHSW_TEMP_EVENT
<50> LED_TEMP_EVENT
<50> OCT_TEMP_EVENT
<43> TIVA_USER_LED1
<43> TIVA_USER_LED2
<45> IOEXP_INVEN_EEPROM_WP
<45> IOEXP_ID_EEPROM_WP
<20> ETHSW_TIVA_PME_N
<20> ETHSW_TIVA_IBA
<46> R_IRQ_INTRPT
POWER_TEMP_EVENT0
POWER_TEMP_EVENT1
ETHSW_TEMP_EVENT
LED_TEMP_EVENT
OCT_TEMP_EVENT
R702 10K R0402 ?%
R703 10K R0402 ?%
R698
IOEXP_TIVA_INT
IOEXP_TIVA_INT <41>
ADDRESS-71
CAVIUM
Title
IO-EXPANDER
Size B
Document Number <Doc>
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when V1 fall to 3.0V ,V2 on
when V1 raise to 3.2V ,V2 off

V3P3_TIVA_LT

R783
267K
1%

C879
10uF
C0603
6.3V

U87

IN1_1
IN1_2
OUT1_2
OUT1_1
LTC4415
EN1
EN2
WARN1
WARN2
STAT2
STAT1
CLIM1
CLIM2
IN2_1
IN2_2
OUT2_2
OUT2_1
EGND

LTC4415IMSE

V3P3_TIVA_CM

C881
10uF
C0603
6.3V

C882
10uF
C0603
6.3V

calculate the resistor

R784
7.5K
?%
R0402

LT4415_EN
LT4415_EN2n

R785
100K
1%
R0402

R854
1M
1%

R855
1M
1%

TP73
TP72

J28
91601-306LF

SuperCap_VCC

C880
10uF
C0603
6.3V

MH13 should place 1.5inch away from J28

J28
MH13

MH13
Mounting_Hole

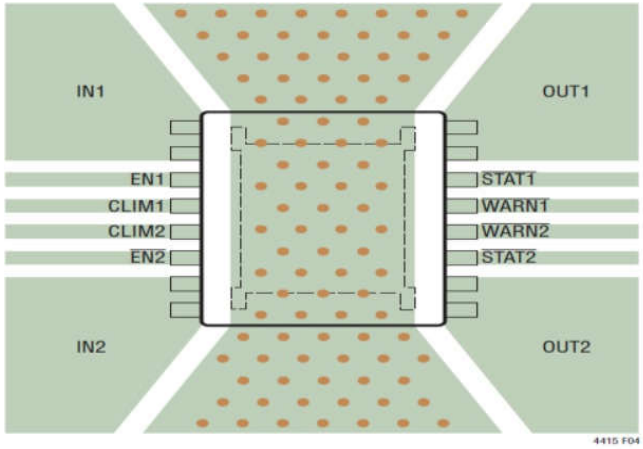
A5
Custom Board Spacer
9774070243R

MH6 Mounting_Hole
MH5 Mounting_Hole
MH8 Mounting_Hole
MH3 Mounting_Hole

MH10 Mounting_Hole
MH1 Mounting_Hole
MH2 Mounting_Hole

C843
1000PF
X7R
3KV
10%

CHASIS_GND
SHIELD_GND_B
CHASIS_GND



CAVIUM

Title
TIVA BackUp Power

Size	Document Number	Rev
A	<Doc>	1.0

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