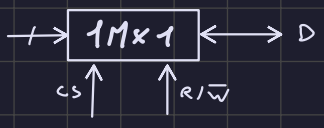
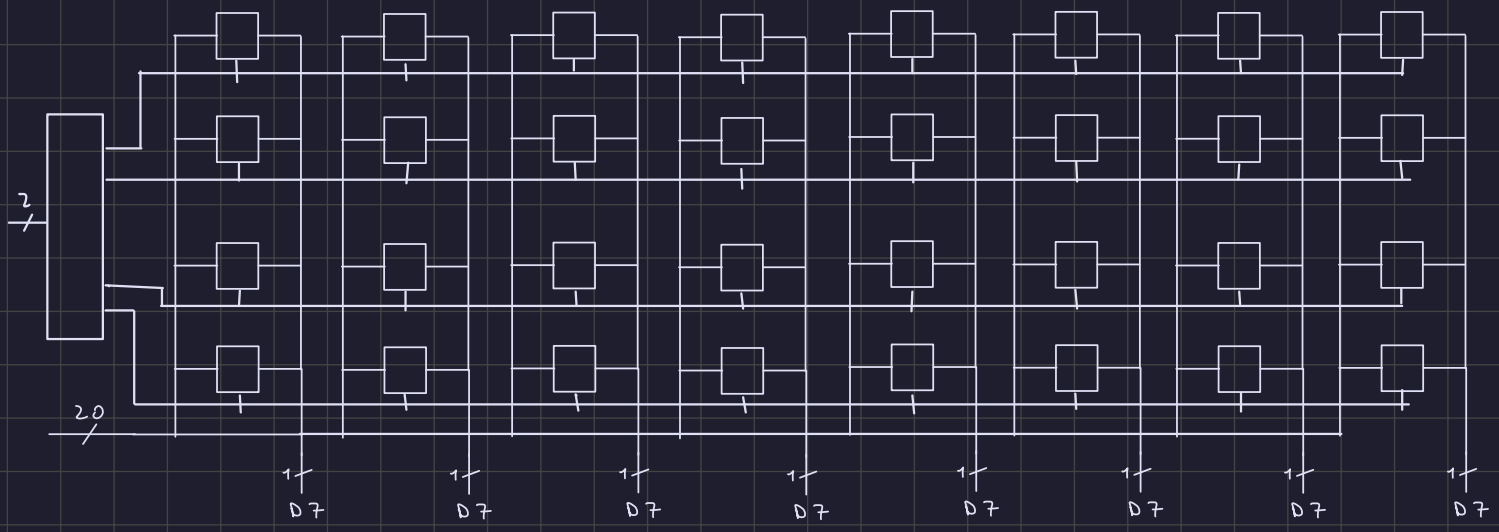
Esercitazione

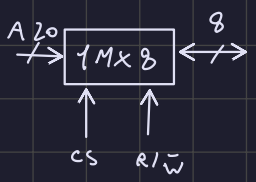
Progetta una SRAM di 4MByte indirizzabile al byte utilizzando chip 1M×1



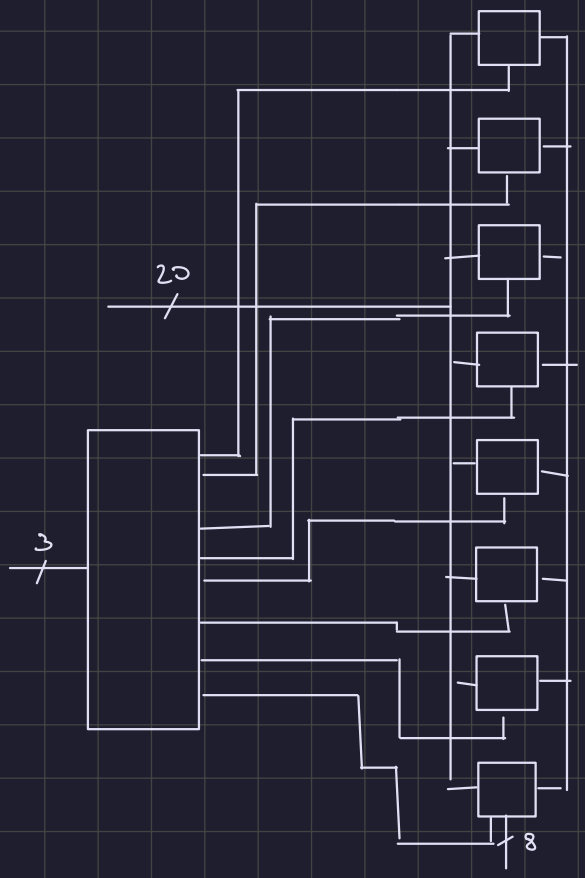
1M parole ⇒ 20 bit indirizzo

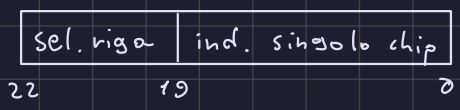


Si realizzi una SRAM di 8 MB indirizzata al byte con chip da 1M x 8



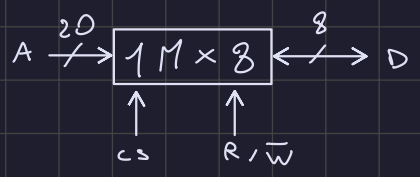
$8M = 2^{23}$ → ind 23 bit





Sram $2M \times 32 \mapsto \frac{32}{8} = 4 \rightarrow 2MB \cdot 4B = 8MB$

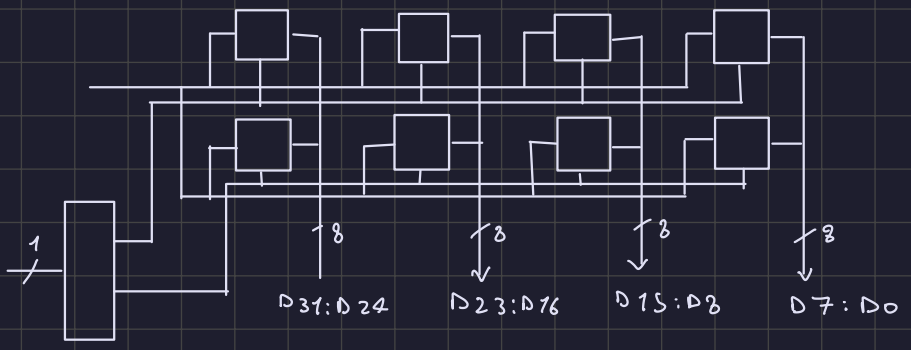
chip $1M \times 8$ indirizzabile a 32 bit



indirizzo per 2M parole → 21 bit

32/8 = 4 colonne

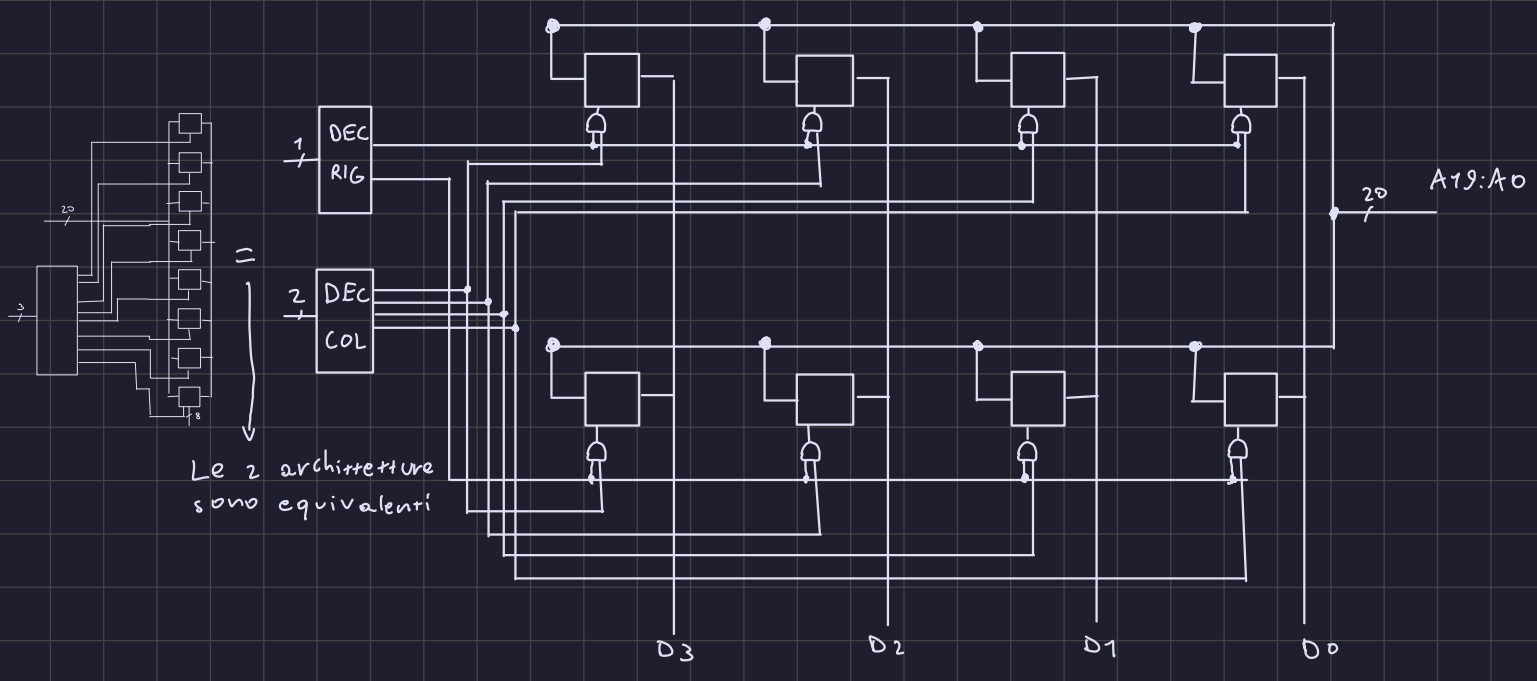
21 − 20 = 1 bit indirizza 2 righe



Con i dati del precedente indirizzare al byte

Indirizzo per 8M parole: 23 bit

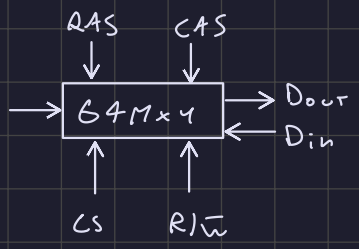
Indirizzo 23−20 3 bit per le righe: 8 righe



DRAM 256M x 8 → 256 M = 2^{28} 28 bit di indirizzo

indirizzabile al byte

chip da 64M x 1 → 64 M = 2^{26} 26 bit di indirizzo



8 colonne (1 x 8)

WMFC

$\frac{256\,M}{64\,M}$ = 4 righe