TI Designs: TIDA-01622
30-W/in^3, 92% Efficiency, 65-W USB Type-C™ PD AC/DC Adapter Reference Design

Description

This fully-tested, USB power delivery reference design is a high-efficiency, high-power-density, AC/DC adapter solution with a wide input voltage range (85- to 265-V AC) for laptop adapters and smartphone charger applications. The design adopts active-clamp-flyback topology controlled by TI's newest ACF controller UCC28780 as the primary power supply stage. This design uses TPS25740B, TI's PD source controller, to achieve a full PD 2.0 function. The design achieves a peak efficiency of 92% at a very-high switching frequency. The power density of the design has been increased to 30 W/in^3, which is much higher than traditional solutions.

Resources

TIDA-01622	Design Folder
UCC28780	Product Folder
UCC24612	Product Folder
TPS25740B	Product Folder
ATL431	Product Folder
ISO7710	Product Folder
CSD17578Q3A	Product Folder
TPD1E05U06-Q1	Product Folder

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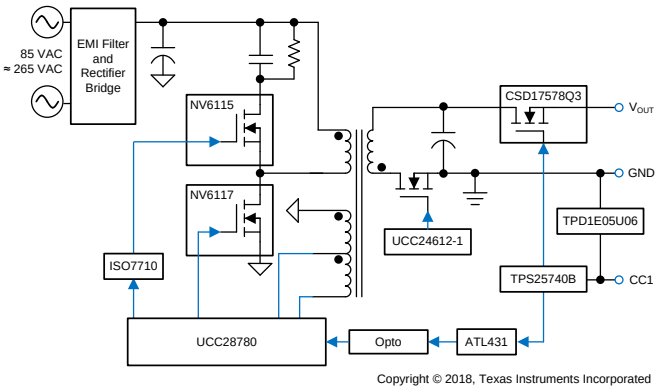
Features

- High Efficiency (92% Peak Value)
- High Power Density (30 W/in^3)
- Low Power Consumption at No Load (60 mW)
- Low Input Power at Light Load (0.5 W) at 20-V_{OUT}, 0.25-W Output
- Fully Compatible With USB PD 2.0 Standard With 5-V/3-A, 9-V/3-A, 15-V/3-A, 20-V/3.25-A Output
- Active-Clamp Flyback + SR Topology
- Small Size (62 mm × 26.8 mm × 20 mm)

Applications

- Consumer AC/DC
- Industrial AC/DC



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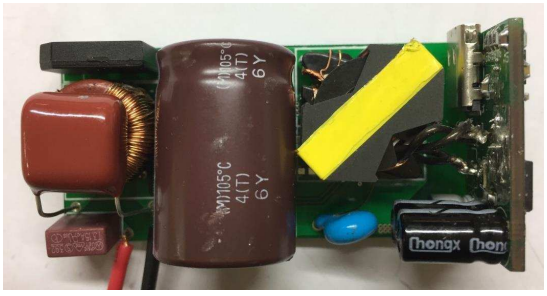

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1 System Description

Smartphones and notebook PCs need adapters to charge their batteries. A USB-PD function makes charging convenient because the smartphone charger and notebook PC adapter are combined to one converter. High efficiency and high power density are required for the adapter to save power and make the device easier to carry. A smartphone charger or notebook adapter is an AC/DC converter. Figure 1 shows a typical diagram of this converter. When the output power is lower than 75 W, a PFC stage is not required.

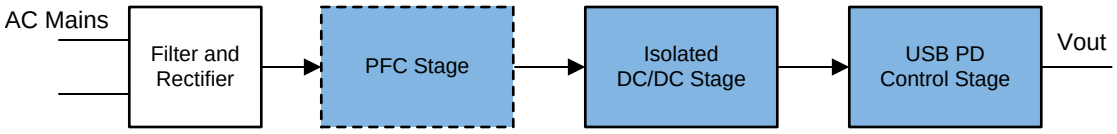

Figure 1. Typical Diagram of USB-PD Adapter

This adapter reference design operates over a wide input voltage range from 85-V to 265-V AC and must be able to power different equipment with different voltage demands automatically. When faults such as over-current, over-power, and over-voltage happen, the adapter reacts quickly to protect the terminal device.

This reference design is a high efficiency, high power density, 65-W output power USB-PD 2.0 AC/DC adapter that achieves a peak efficiency of 92% and a 30-W/in^3 power density. The input voltage ranges from 85-V to 265-V AC and the output is fully compatible with USB PD2.0 standard with 5-V/3-A, 9-V/3-A, 15-V/3-A, and 20-V/3.25-A outputs. When an over-current, short-circuit, or over-power event occurs, this adapter reference design can cut off the output and recovery automatically. With over-voltage, the adapter is latched to avoid further damage to the terminal devices. Also, this adapter meets low no-load power consumption, which is less than 60 mW.

This converter operates at a high switching frequency of 600 kHz (max), which helps decrease the size of the transformer and capacitors. Furthermore, the EMI filter is much simpler and smaller than low frequency converters.

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1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
Input voltage (V_{INAC})		85	230	265	V AC
Frequency (f_{LINE})		47	50	63	Hz
Brown-in voltage			75		V AC
Brownout voltage			70		V AC
OUTPUT CHARACTERISTICS					
Output voltage	5-V sink attached	4.95	5	5.05	V
	9-V sink attached	8.95	9	9.05	V
	15-V sink attached	14.9	15	15.1	V
	20-V sink attached	19.85	20	20.15	V
Output current	5-V sink attached		3		A
	9-V sink attached		3		A
	15-V sink attached		3		A
	20-V sink attached		3.25		A
Load regulation	5-V sink attached		0.2	0.5	%
	9-V sink attached		0.3	0.5	%
	15-V sink attached		0.6	1.0	%
	20-V sink attached		0.8	1.0	%
Ripple and noise	5-V sink attached			130	mV
	9-V sink attached			140	mV
	15-V sink attached			156	mV
	20-V sink attached			204	mV
Maximum output power				65	W
SYSTEM CHARACTERISTICS					
Peak efficiency	Low line		91.3		%
	High line		91.2		%
Operating ambient temperature			64.5		°C
Standards and norms	EMI	IEC 61000-2-3 Class D, EN 55022 class B			
Board form factor		60 mm × 28.6 mm × 20 mm			

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2 System Overview

2.1 Block Diagram

Figure 2 shows the high-level block diagram of the circuit. The main topology of this reference design is active clamp flyback (ACF), which is controlled by TI's new ACF controller UCC28780. The synchronize rectifier controller UCC24612-1 controls the synchronize rectifier MOSFET for better efficiency performance. The main switching devices are NV6115 and NV6117 GaN devices from Navitas Semiconductor, Inc. The TI USB-PD source controller TPS25740B controls the output fully compatible with the USB-PD 2.0 standard with 5-V/3-A, 9-V/3-A, 15-V/3-A, 20-V/3.25-A outputs.

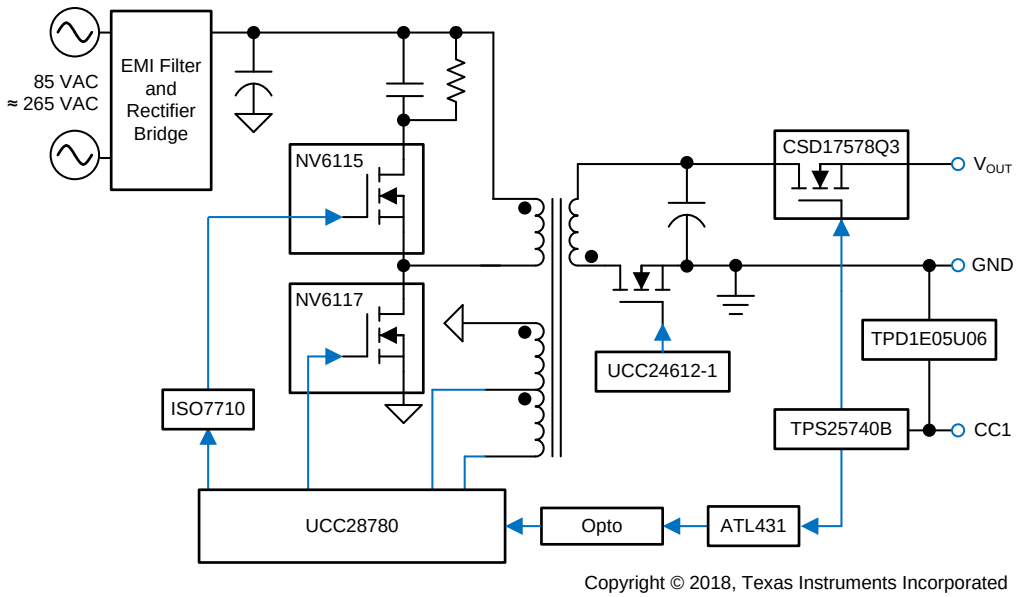

Figure 2. Block Diagram of TIDA-01622

2.2 Highlighted Products

2.2.1 UCC28780

The UCC28780 is a high-frequency active-clamp flyback controller that enables high-density AC/DC power supplies that comply with stringent global efficiency standards. Zero voltage switching (ZVS) is achieved over wide operating range with an advanced auto-tuning technique, adaptive dead time optimization, and variable switching frequency control law. Along with multimode control that changes the operation based on input and output conditions, the UCC28780 controller enables high efficiency without the risk of audible noise. The controller has a variable switching frequency of up to 1 MHz and accurate programmable OPP, which provides consistent thermal design power across a wide line range. This consistent power means passive components can be further reduced and enable high power density.

Key features for this device include the following:

- Configurable with external Si or GaN FETs
- Adaptive burst control for light-load efficiency with low output ripple and no audible noise
- Secondary-side regulation allows for dynamically scalable output voltage
- Internal soft start
- Brownout detection without direct line sensing
- Fault protections: Internal overtemperature, output overvoltage, overcurrent, short circuit, and pin fault
- NTC resistor interface with external enable

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2.2.2 UCC24612

The UCC24612 is a high-performance controller and driver for standard and logic-level N-channel MOSFET power devices used for low-voltage, secondary-side synchronous rectification. The combination of controller and MOSFET emulates a near-ideal diode rectifier. This solution not only directly reduces power dissipation of the rectifier, but also indirectly reduces primary-side losses as well due to compounding of efficiency gains. Using drain-to-source voltage sensing, the UCC24612 is ideal for ACF power supplies. This device is available in a 5-pin SOT-23-5 package.

Key features for this device include the following:

- Up to 1-MHz operating frequency
- V_{DS} MOSFET sensing
- 4-A sink, 1-A source gate-drive capability
- Micro-power sleep current for 90+ designs
- Automatic light-load management
- Synchronous wake-up from sleep and light-load modes
- Adaptive minimum off time for better noise immunity
- 16-ns typical turnoff propagation delay
- 9.5-V gate drive clamp levels for minimum driving loss

2.2.3 TPS25740B

Without any firmware configuration, the TPS25740B implements a source that is certified for USB-PD 2.0 version 1.2 and Type-C revision 1.2 designed to minimize time to market. The device offers four different voltages using USB-PD. The voltages and currents advertised are easily configured and the device can select the voltage from the power supply based on the voltage requested by the attached sink. The device automatically handles discharging the VBUS output per USB-PD requirements.

Key features for this device include the following:

- Pin-selectable voltage advertisement:
  - 5 V, 9 V, 12 V, and 15 V
  - 5 V, 9 V, 15 V, and 20 V
- Pin-selectable peak power settings:
  - Eight options 18 W to 100 W
- High voltage and safety integration:
  - OVP, OCP, OTP, and VBUS discharge
  - IEC 61000-4-2 protection on CC1 and CC2
  - Input pin for fast shutdown under fault
  - Control of external N-channel MOSFET
  - Three-pin external power supply control
  - Wide V_{IN} supply: 4.65 V to 25 V
- Below 10-µA quiescent current when unattached
- Port attachment indicator
- Self-directed port power management for dual-port applications

2.2.4 ATL431

The ATL431 is a three-terminal adjustable shunt regulator with specified thermal stability over applicable automotive, commercial, and industrial temperature ranges. The output voltage can be set to any value between V_{REF} (approximately 2.5 V) and 36 V with two external resistors. The regulator has a typical output impedance of 0.05 Ω. The operation current is as low as 35 µA (min), keeping the power loss at a quite low value.

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2.2.5 ISO7710

The ISO7710 device is a high-performance, single-channel digital isolator with 5000-V_{RMS} (DW package) and 3000-V_{RMS} (D package) isolation ratings per UL 1577. This device is also certified by VDE, TUV, CSA, and CQC. The ISO7710 device provides high EMI and low emissions at a low power consumption while isolating CMOS or LVCMOS digital I/Os. The isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO2) insulation barrier. In the event of input power or signal loss, default output is high for a device without suffix F and low for a device with suffix F.

2.2.6 CSD17578Q3A

The CSD17578Q3A is a 30-V NexFET™ Power MOSFET with a very low R_{DSon} of 6.3 mΩ and a SON 3.3-mm×3.3-mm package. In this reference design, this device is used as a PD function switch for its low cost and R_{DSon}.

2.2.7 TPD1E05U06-Q1

The TPD1E05U06-Q1 is a one-channel ESD protection diode for speeds up to 6 Gbps. The ultra-low loading capacitance makes this device ideal for protecting any high-speed signal applications including USB 2.0 or 3.0, HDMI 1.4 or 2.0, SIM cards, and so on.

2.3 System Design Theory

This reference design operates over a wide input voltage ranges from 85-V to 265-V AC and is fully compatible with the USB-PD 2.0 standard with 5-V/3-A, 9-V/3-A, 15-V/3-A, and 20-V/3.25-A outputs. The power supply operates as ACF topology controlled by the UCC28780. And the output voltage is selected by TPS25740B based on the voltage requested by the attached sink. The peak efficiency achieves 92% at a 230-V AC input and 93% at a 115-V AC input. The high switching frequency helps to decrease the transformer and EMI filter size to achieve a high power density.

2.3.1 ACF Converter Design

ACF is a two-switch topology that achieves soft switching and recovers leakage inductance energy. Compared with traditional ACF in continuous conduction mode (CCM), ACF in critical conduction mode (CrCM) uses the magnetizing inductance instead of leakage inductance to store ZVS energy. As magnetizing inductance is much larger than leakage inductance, only a small amount of negative magnetizing current is required to achieve full ZVS soft switching. By controlling the amount of negative magnetizing current, ZVS can easily be achieved from zero to full load. With proper design, the output rectifier achieves zero current switching (ZCS) during turnoff. All these features make ACF successful at high power density and efficiency adapter applications.

Table 2. ACF Design Goal Parameters

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
Input voltage (V_{INAC})		85	230	265	V AC
Brown-in voltage			75		V AC
Brownout voltage			70		V AC
OUTPUT CHARACTERISTICS					
Output voltage		5		20	V
Maximum output power				65	W
Burst mode load threshold			60		%
Peak efficiency	Low line		91.3		%
	High line		91.2		%
Load regulation				1.0	%

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2.3.1.1 Bulk Capacitor Calculation

The minimum value of a bulk capacitor is determined by the hold-up time (T_{hold_up}). A larger bulk capacitor value means a larger capacitor size; therefore, to maintain a high power density, the bulk capacitor value is determined by the hold-up time.

$$C = \frac{\frac{2 \times P_{out\_max}}{\eta} \times T_{hold\_up}}{V_{BULK\_RUN}^{2} - V_{Brownout}^{2}} \quad (1)$$

Where:

- P_{OUT_max} is the maximum output power
- V_{BULK_RUN} is the typical DC voltage on a bulk capacitor
- $V_{Brownout}$ is the DC brownout voltage

2.3.1.2 Transformer Turns Ratio Calculation

The transformer turns ratio is determined by the voltage rating of GaN and synchronous rectification MOSFET. The voltage stress of GaN NV6117 is 650 V and the SR MOSFET is a 150-V Si device. Therefore, the maximum and minimum turns ratio can be calculated separately using Equation 2 and Equation 3, respectively.

$$N_{PS\_max} = \frac{(1 - K_{dera}) \times V_{DS\_GaN} - V_{BULK\_max}}{V_{OUT\_max}} = 6.87 \quad (2)$$

Where:

- K_{dera} is the GaN voltage derating
- V_{DS_GaN} is the maximum GaN drain-to-source voltage rating
- V_{BULK_max} is the maximum bulk voltage
- V_{OUT_max} is the maximum output voltage

$$N_{PS\_min} = \frac{V_{BULK\_max}}{(1 - K_{dera}) \times V_{DS\_SR} - V_{OUT\_max} - V_{spike}} = 4.68 \quad (3)$$

Where:

- V_{DS_SR} is the SR MOSFET drain-to-source voltage rating
- V_{spike} is the spike voltage on SR MOSFET

A larger turns ratio means a larger main switch duty cycle and smaller secondary RMS current. In this reference design, the turns ratio is designed as 6 to maintain the minimum secondary RMS current, which does better to the efficiency and thermal.

2.3.1.3 Primary Magnetic Inductance Calculation

After N_{PS} is chosen, the primary magnetic inductance (L_m) can be determined based on the minimum switching frequency (f_{SW_min}) at the minimum bulk voltage (V_{BULK_min}), maximum duty cycle (D_{max}), and maximum output power (P_{OUT_max}). When selecting the minimum switching, consider the impact on full-load efficiency and EMI filter design.

Calculate the maximum duty cycle and primary inductance using Equation 4 and Equation 5.

$$D_{max} = \frac{N_{PS} \times V_{OUT\_max}}{V_{BULK\_min} + N_{PS} \times V_{OUT\_max}} = 0.67 \quad (4)$$

$$L_m = \frac{D_{max}^{2} \times V_{BIULK\_min}^{2} \times \eta}{2 \times f_{SW\_min} \times P_{OUT\_max}} = 79\ \mu H \quad (5)$$

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2.3.1.4 Auxiliary-to-Secondary Turn Ratio Design

The UCC28780 and both GaN devices are all powered by auxiliary winding at run mode. Two windings are designed to make sure that VDD will not be lower than the turnoff voltage and to minimize the power consumption. Figure 3 shows the auxiliary power diagram.

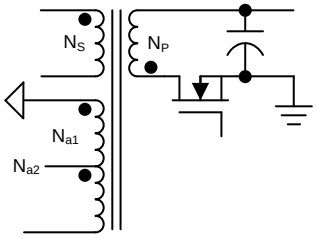

Figure 3. Auxiliary Power Diagram

The N_{a1} winding is designed to power the devices at 5-V and 9-V outputs. Considering the voltage derating at a light load, there should be enough margin on V_{DD_min}. Then at a 9-V output, the VDD is equal to the TVS diode voltage of 18 V. N_{a1} must stay a small value to decrease the power consumption on the transistor.

The N_{a2} winding is designed to power the devices at 15-V and 20-V outputs. Calculate the auxiliary-to-secondary turn ratio using Equation 6, Equation 7, and Equation 8.

$$\frac{N_{a1\_min}}{N_S} = \frac{1.8V_{DD\_min}}{5} = 3.78 \tag{6}$$

$$\frac{N_{a2\_min}}{N_S} = \frac{1.8V_{DD\_min}}{15} = 1.26 \tag{7}$$

$$\frac{N_{a2\_max}}{N_S} = \frac{0.9V_{DD\_max}}{20} = 1.35 \tag{8}$$

2.3.1.5 Clamp Capacitor Calculation

Consider the design trade-off between conduction loss reduction and turnoff switching loss of the high-side switching device (Q_H). A higher clamp capacitor (C_{clamp}) results in less RMS current flowing through the transformer windings and switching devices; therefore, the conduction loss can be reduced. However, a higher C_{clamp} design results in Q_H turning off before the clamp current returns to zero. The condition of non-ZCS increases the turnoff switching loss of Q_H. Therefore, C_{clamp} needs to be fine tuned based on the loss attribution. For best results, design the resonance between leakage inductance (L_k) and C_{clamp} to be completed by the time between resonant current is zero and Q_H is turned off. In this setup, the demagnetization time must be equal to around three quarters of the resonant period. Use Equation 9, Equation 10, and Equation 11 to design C_{clamp} for obtaining ZCS at a minimum bulk voltage, minimum output voltage, and full load. A low-ESR clamp capacitor is required to minimize the conduction loss.

$$C_{clamp\_max} = \frac{1}{L_k} \times \frac{2L_m i_{m+}}{3\pi \times N_{PS} \times V_{OUT\_min}}^2 \tag{9}$$

$$i_{m+} = \sqrt{\frac{2 \times P_{OUT\_max}}{\eta \times L_m \times f_{SW\_min}} + i_{m-}^2} \tag{10}$$

$$i_{m-} = -\sqrt{\frac{C_{SW}}{L_m}} \times V_{BULK\_min} \tag{11}$$

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2.3.1.6 Bleed Resistor Calculation

A large bleed resistor (R_{Bleed}) is used to discharge clamp capacitor voltage to a residual voltage ($V_{residual}$) during the 1.44-s fault delay recovery time (t_{FDR}). After the converter recovers from the fault mode, the lower $V_{residual}$ reduces the maximum current flowing through Q_H and SR within their respective safe operating areas, even if the output voltage is shorted. The target $V_{residual}$ can be calculated based on the maximum pulse current of Q_H or the SR current reflected to the primary side, depending on which is lower.

$$R_{Bleed} = \frac{t_{FDR}}{C_{clamp} \ln\left(\frac{N_{PS} \times V_{OUT\_max}}{V_{residual}}\right)} \quad (12)$$

2.3.1.7 Output Capacitor Calculation

Output capacitance (C_{OUT}) is determined by evaluating several factors and choosing the largest of the results.

1. The minimum output capacitor value must be enough to meet transient specification of output voltage due to a given load step until the voltage-control loop can respond to restore regulation.

   Where:

   - ΔI_{load} is maximum load-step magnitude for transient response
   - ΔV_{trans_max} is the maximum transient voltage deviation for transient response
   - Δt_{trans} is the transient response time
2. The maximum ESR of output capacitor is often limited by the maximum output peak-to-peak voltage ripple ($V_{pk\text{-}pk}$), where the worst-case output ripple is considered at maximum load (I_{OUT_max}). If the high-frequency switching ripple at the output is mainly dominated by the ESR ripple, a sinusoidal approximation of the secondary current waveform of the ACF is made to calculate the ESR requirement based on the target output ripple specification.

$$V_{residual} = \min\left(i_{max\_QH}, i_{max\_SR}\right) \times \sqrt{\frac{L_k}{C_{clamp}}} \quad (13)$$

$$C_{OUT\_min} = \frac{\Delta I_{load} \times \Delta t_{trans}}{\Delta V_{trans\_max}} \quad (14)$$

$$R_{Co\_max} = \frac{2\left(1 - D_{max} - f_{SW\_min} \times \pi \times \sqrt{L_m C_{SW}}\right) \times V_{pk-pk}}{\pi \times I_{OUT\_max}} \quad (15)$$

2.3.2 USB-PD Design

The USB-PD source controller TPS25740B is used in this reference design to achieve USB-PD 2.0 functions. The device can control an external voltage regulator by three digital PINs (CTL1, CTL2, and CTL3) to select the voltage from the power supply based on the voltage requested by the attached sink. Table 3 summarizes the control relationship between the CTL1, CTL2, and CTL3 statuses and VBUS.

Table 3. PD Control Relationship

VOLTAGE CONTAINED IN PDO REQUESTED BY UFP	CTL3 STATE	CTL2 STATE	CLT1 STATE
5 V	High-z	High-z	High-z
9 V	High-z	Low	High-z
15 V	High-z	Low	Low
20 V	Low	Low	Low

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The USB-PD control resistors can be calculated from Equation 16, Equation 17, and Equation 18 based on Table 3.

$$R_{CTL2} = \frac{V_{REF}}{\frac{(9\ V - V_{REF})}{R_{D1}} - \frac{V_{REF}}{R_{D2}}} \quad (16)$$

$$R_{CTL1} = \frac{V_{REF}}{\frac{(15\ V - V_{REF})}{R_{D1}} - \frac{V_{REF}}{R_{D2}} - \frac{V_{REF}}{R_{CTL2}}} \quad (17)$$

$$R_{CTL3} = \frac{V_{REF}}{\frac{(15\ V - V_{REF})}{R_{D1}} - \frac{V_{REF}}{R_{D2}} - \frac{V_{REF}}{R_{CTL2}} - \frac{V_{REF}}{R_{CTL1}}} \quad (18)$$

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3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

- Isolated AC source
- Single-phase power analyzer
- Digital oscilloscope
- Multimeters
- Electronic load
- USB Type-C™ UFP Load Board PMP20413

3.2 Testing and Results

3.2.1 Test Setup

1. Connect input terminals of the reference board to the AC power source.
2. Connect output terminals to the PMP20413 input terminals.
3. Connect the PMP20413 output terminals to electronic load, maintaining correct polarity.
4. Set a minimum load of about 0 A and minimum voltage of 25 V.
5. Gradually increase the input voltage from 0 V to turn on voltage of 75-V AC.
6. Observe that the output voltage across the load terminals has risen to about 5 V.
7. Increase the load to maximum load smoothly and observe the switching waveforms.
8. Select different output voltages through the PMP20413 device.
9. Increase the load to maximum load smoothly and observe the switching waveforms.
10. Compare these results with those presented in the design guide.

3.2.2 Test Results

3.2.2.1 Efficiency

Table 4 through Table 7 list the efficiency data of the different voltages.

Table 4. 5 V at 115-V AC/60 Hz

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY
5	0.1498	1.07	70
4.996	0.3	1.99	75.31658
4.996	0.45	2.88	78.0625
4.994	0.6	3.79	79.06069
4.993	0.75	4.71	79.50637
4.993	0.9	5.63	79.81705
4.992	1.05	6.58	79.65957
4.991	1.2	7.54	79.43236
4.996	1.35	8.15	82.75583
4.993	1.5	9	83.21667
4.992	1.65	9.9	83.2
4.991	1.8	10.8	83.18333
4.993	1.95	11.7	83.21667
4.992	2.1	12.6	83.2

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Table 4. 5 V at 115-V AC/60 Hz (continued)

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY
4.993	2.25	13.4	83.83769
4.996	2.4	14.3	83.84895
4.996	2.55	15.1	84.36954
4.996	2.7	16	84.3075
4.996	2.85	16.9	84.25207
4.998	3	17.7	84.71186

Table 5. 9 V at 115-V AC/60 Hz

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY
9.02	0.15	1.87	72.35294
9.01	0.3002	3.38	80.02373
9.01	0.45	4.8	84.46875
9.01	0.6	6.29	85.94595
9.02	0.75	7.82	86.50895
9.02	0.9	9.3	87.29032
9.02	1.05	10.82	87.53235
9.02	1.2	12.3	88
9.01	1.35	13.8	88.1413
9.02	1.5	15.3	88.43137
9.01	1.65	16.8	88.49107
9.02	1.8	18.3	88.72131
9.01	1.95	19.8	88.73485
9.01	2.1	21.3	88.83099
9.02	2.25	22.8	89.01316
9.02	2.4	24.3	89.08642
9.03	2.55	25.8	89.25
9.03	2.7	27.3	89.30769
9.03	2.85	28.8	89.35938
9.03	3	30.3	89.40594

Table 6. 15 V at 115-V AC/60 Hz

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY
14.91	0.1499	2.73	81.86846
14.9	0.3001	5.17	86.48917
14.91	0.4503	7.66	87.64978
14.9	0.6	10.07	88.77855
14.9	0.75	12.5	89.4
14.9	0.9	15	89.4
14.89	1.05	17.4	89.85345
14.89	1.2	19.9	89.78894
14.89	1.35	22.3	90.14126
14.88	1.5	24.8	90
14.88	1.65	27.2	90.26471
14.88	1.8	29.7	90.18182
14.88	1.95	32.1	90.39252
14.89	2.1	34.5	90.63478

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Table 6. 15 V at 115-V AC/60 Hz (continued)

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY
14.9	2.25	37	90.60811
14.91	2.4	39.5	90.59241
14.9	2.55	42	90.46429
14.9	2.7	44.4	90.60811
14.9	2.85	46.9	90.54371
14.89	3	49.4	90.4251

Table 7. 20 V at 115-V AC/60 Hz

OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT POWER	EFFICIENCY
20.03	0.162	3.91	82.98875
20.03	0.325	7.53	86.45086
20.01	0.4872	11	88.62611
19.99	0.65	14.6	88.99658
19.98	0.8127	18.1	89.7113
19.96	0.9748	21.6	90.07874
19.95	1.1374	25.2	90.04417
19.94	1.2997	28.6	90.61545
19.93	1.4622	32.2	90.50201
19.9	1.6252	35.6	90.84685
19.89	1.7874	39	91.1574
19.84	1.9504	42.5	91.04926
19.87	2.1128	46	91.26377
19.92	2.2745	49.6	91.34685
19.96	2.4372	53.3	91.26925
19.98	2.5999	56.9	91.2935
19.99	2.7618	60.5	91.25352
19.98	2.9243	64	91.29299
19.97	3.0878	67.6	91.218
19.96	3.2498	71.1	91.23208

Figure 4 and Figure 5 show the efficiency curves.

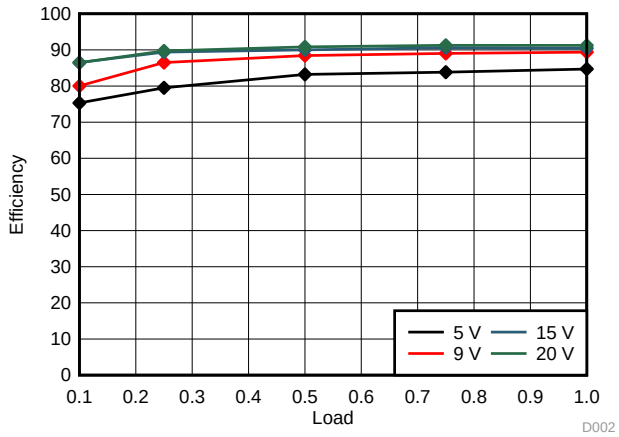

Figure 4. Efficiency Curve at 115-V AC

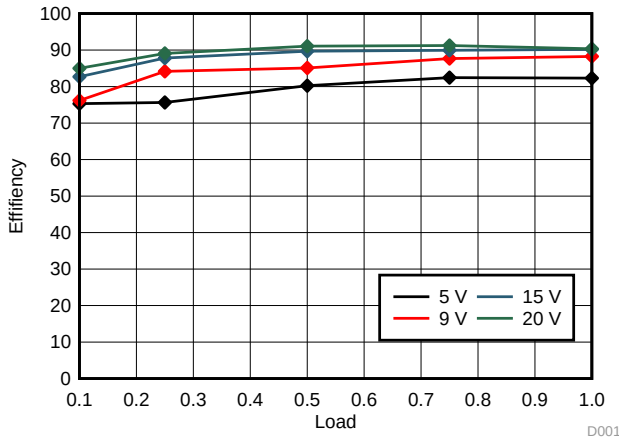

Figure 5. Efficiency Curve at 230-V AC

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3.2.2.2 Load Regulation

Figure 6 shows the load regulation at 115-V AC/60 Hz.

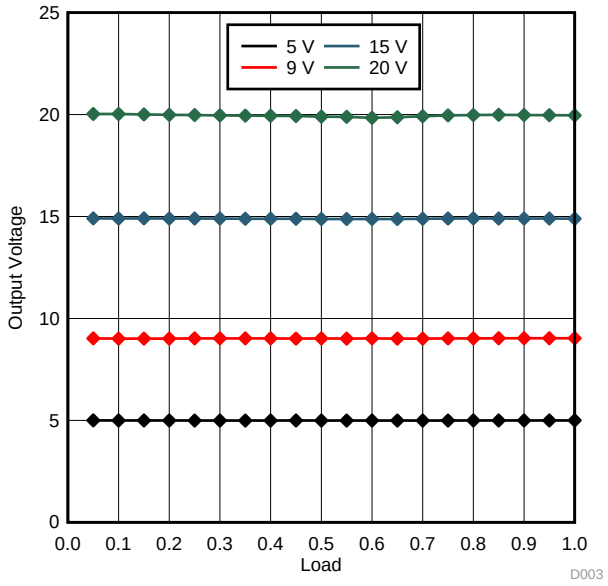

Figure 6. Load Regulation

3.2.2.3 Output Voltage Transitions

3.2.2.3.1 Start-up

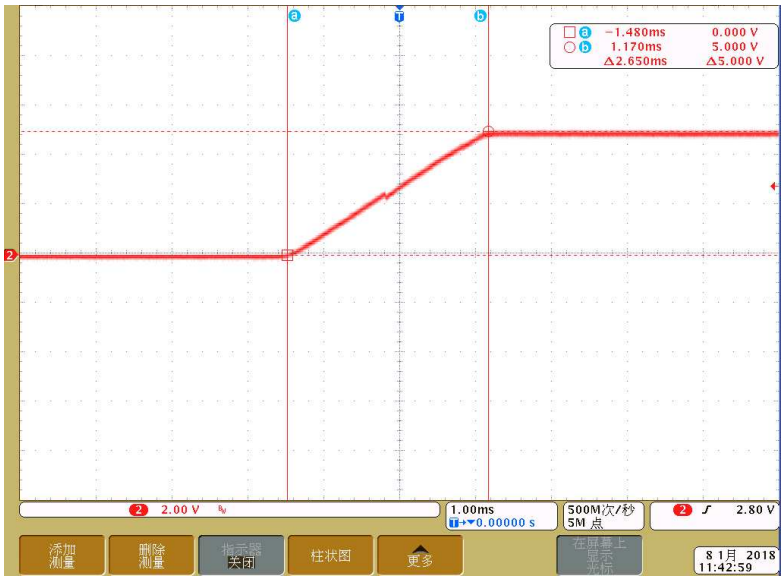

Figure 7. Start-up Waveform at 115-V AC and No Load

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3.2.2.3.2 5 V to 9 V

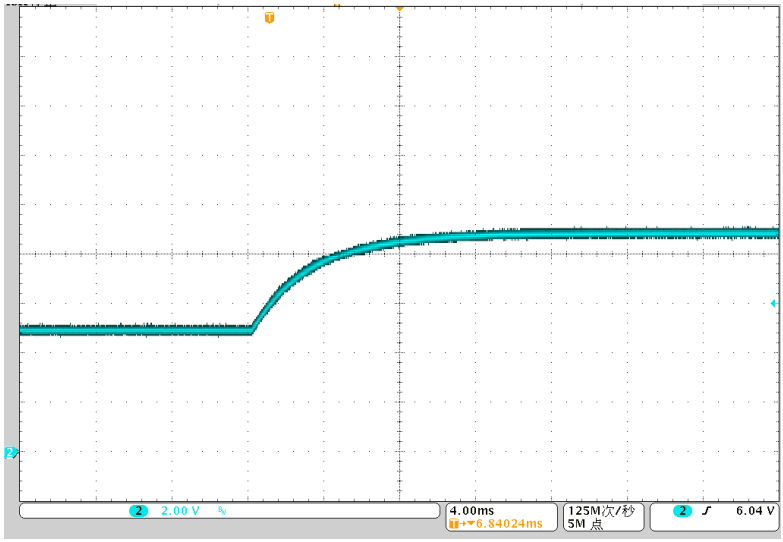

Figure 8. 5-V to 9-V Transition at 115-V AC and No Load

3.2.2.3.3 9 V at 15 V

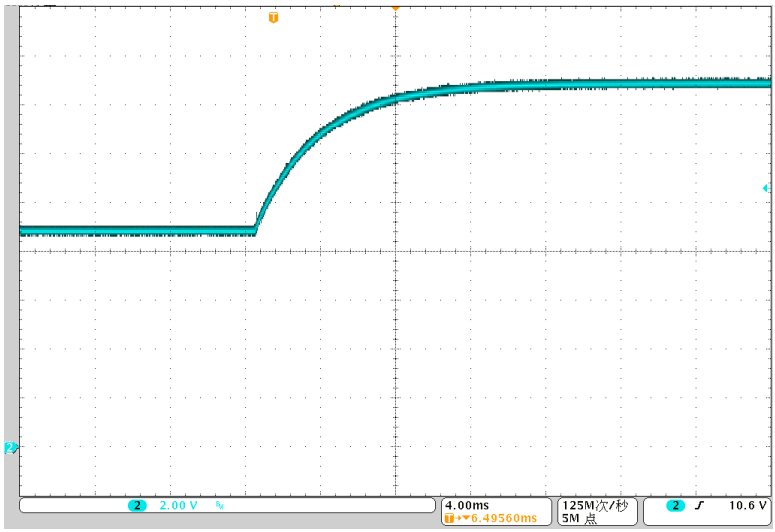

Figure 9. 9-V to 15-V Transition at 115-V AC and No Load

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3.2.2.3.4 15 V to 20 V

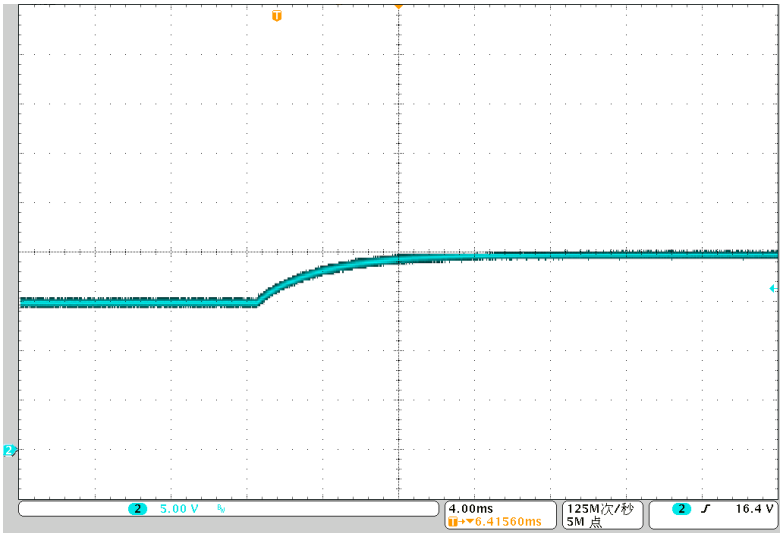

Figure 10. 15-V to 20-V Transition at 115-V AC and No Load

3.2.2.3.5 5 V to 15 V

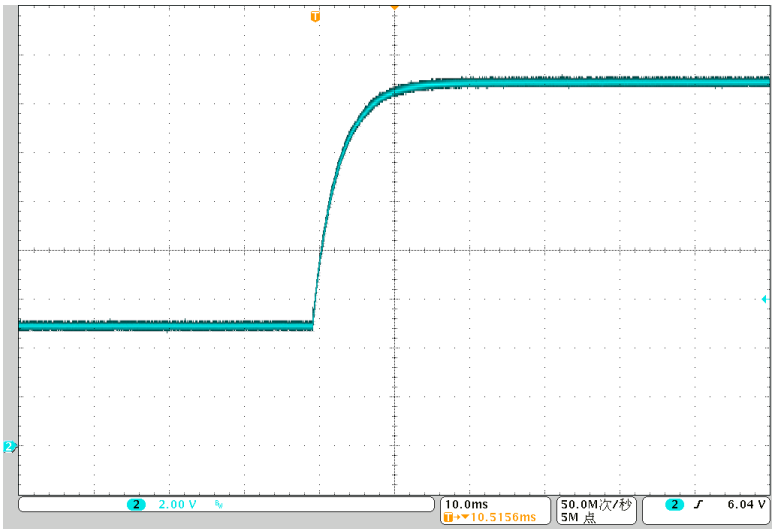

Figure 11. 5-V to 15-V Transition at 115-V AC and No Load

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3.2.2.3.6 5 V to 20 V

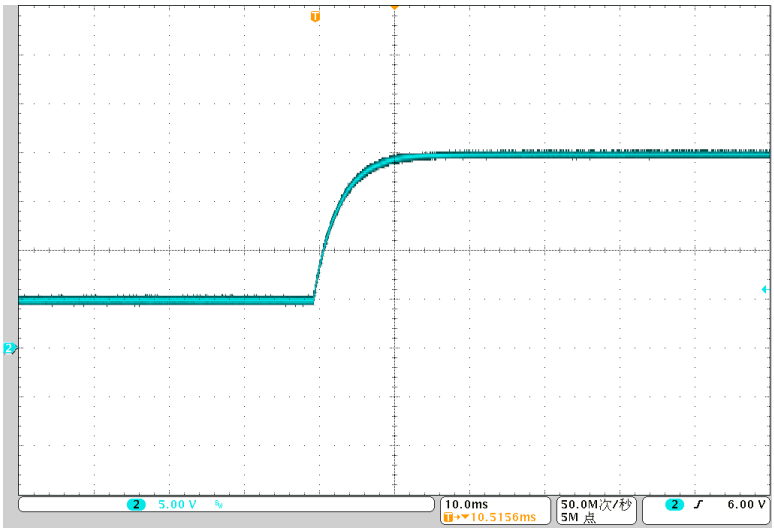

Figure 12. 5-V to 20-V Transition at 115-V AC and No Load

3.2.2.3.7 9 V to 20 V

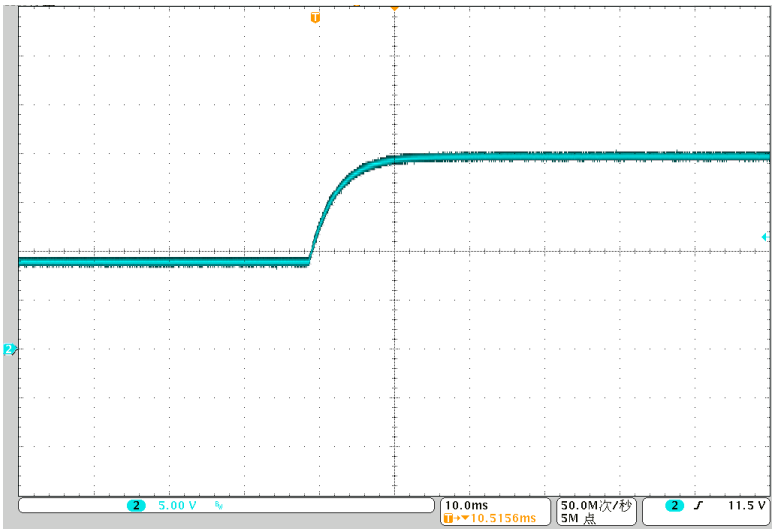

Figure 13. 9-V to 20-V Transition at 115-V AC and No Load

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3.2.2.4 Output Voltage Ripple

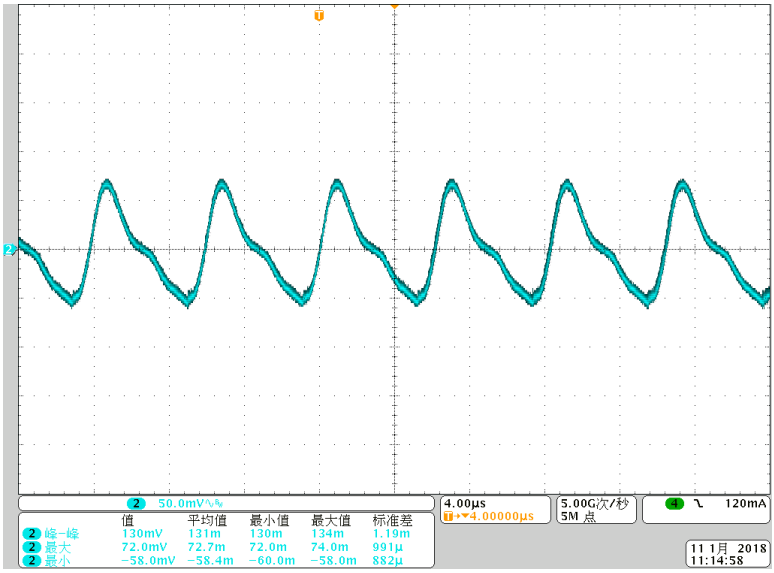

Figure 14. 115-V AC/60-Hz Input, 5-V/3-A Output

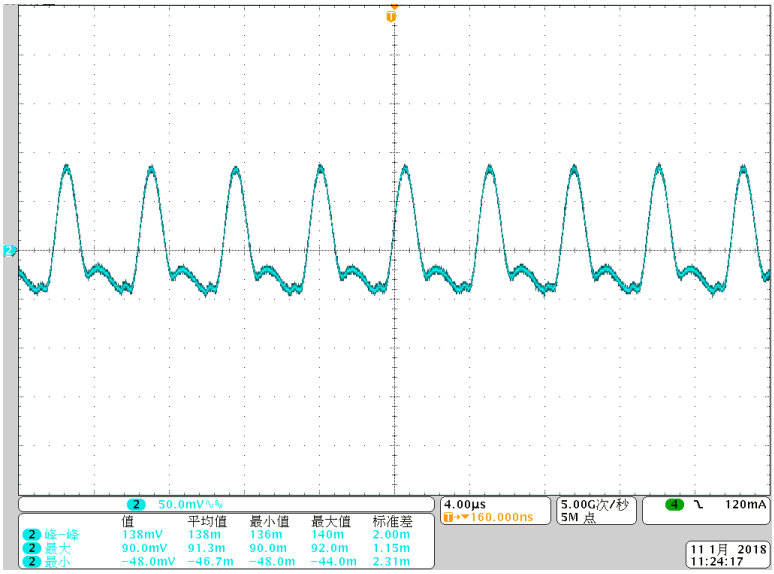

Figure 15. 115-V AC/60-Hz Input, 9-V/3-A Output

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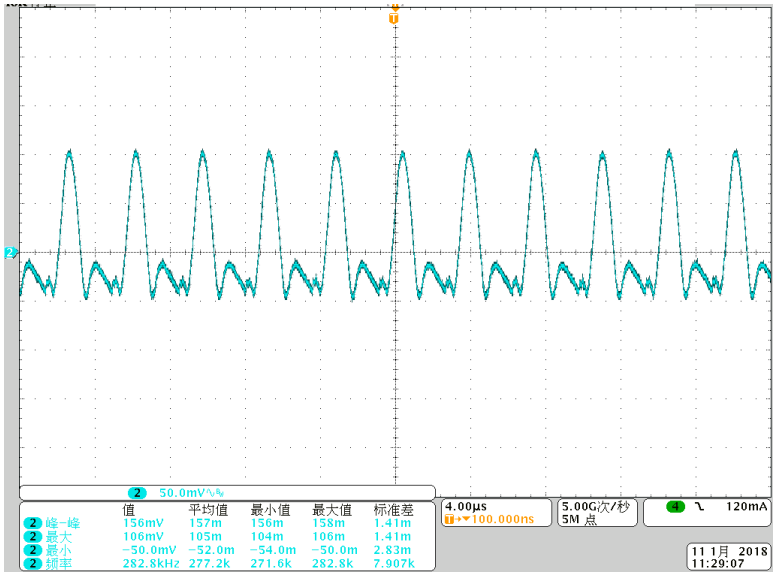

Figure 16. 115-V AC/60-Hz Input, 15-V/3-A Output

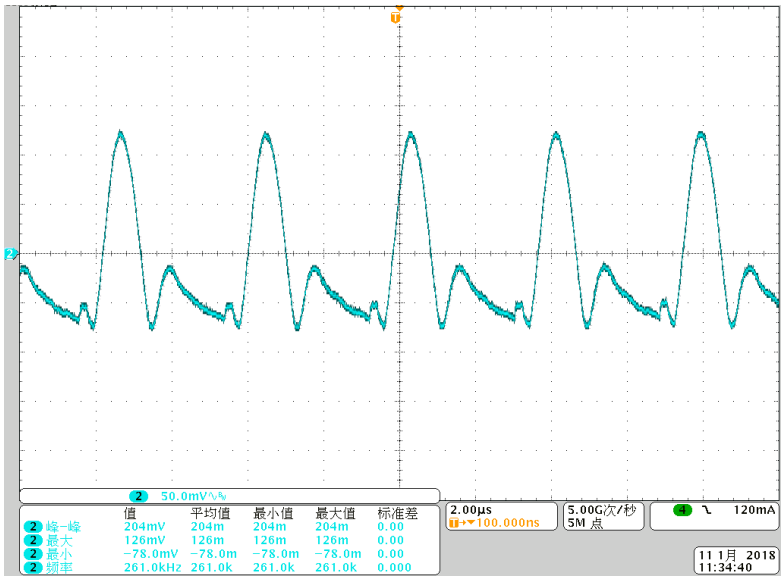

Figure 17. 115-V AC/60-Hz Input, 20-V/3.25-A Output

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3.2.2.5 CE Test Results

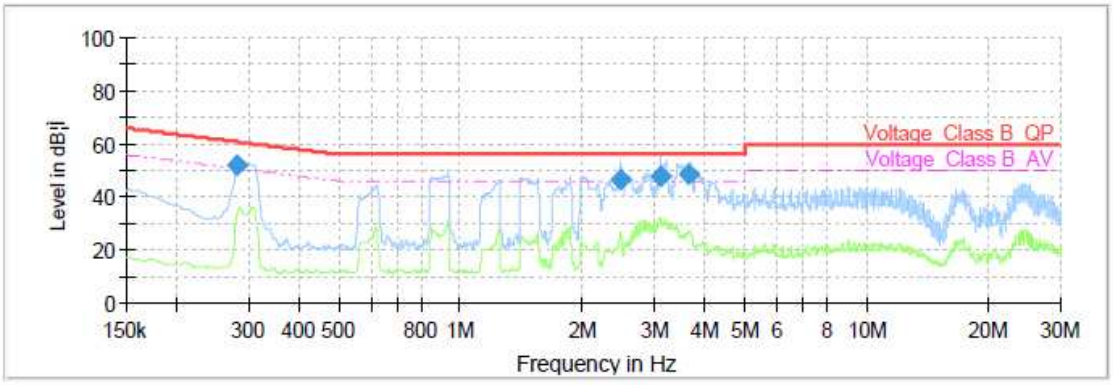

Figure 18. 115-V AC Input, 20-V/3.25-A Output

Table 8. Final Result for 115-V AC Input, 20-V/3.25-A Output

FREQ (MHz)	QUASIPEAK (dBµV)	AVERAGE (dBµV)	LIMIT (dBµV)	MARGIN (dB)	MEAS TIME (ms)	BANDWIDTH (kHz)	LINE	FILTER	CORR (dB)
0.280500	51.81	—	60.80	8.99	1000.0	9.000	L1	ON	19.6
2.483250	46.66	—	56.00	9.34	1000.0	9.000	L1	ON	19.6
3.099750	48.25	—	56.00	7.75	1000.0	9.000	L1	ON	19.6
3.653250	48.39	—	56.00	7.61	1000.0	9.000	L1	ON	19.6

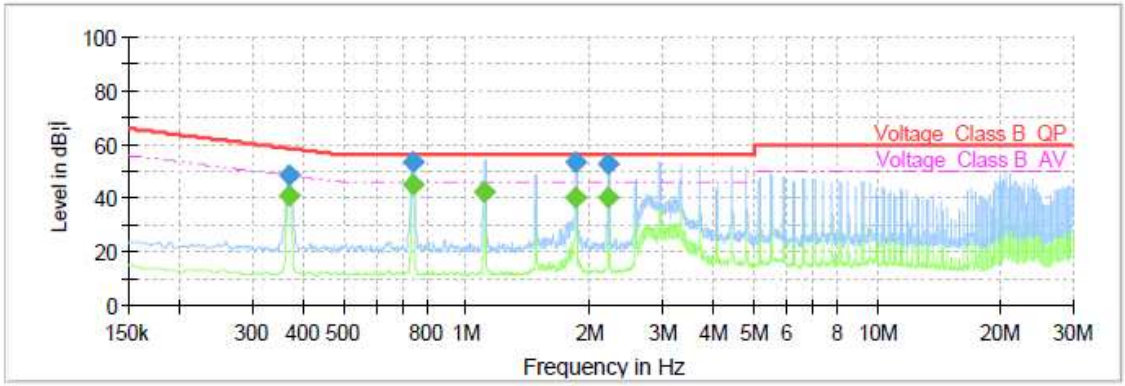

Figure 19. 230-V AC Input, 20-V/3.25-A Output

Table 9. Final Result for 230-V AC Input, 20-V/3.25-A Output

FREQ (MHz)	QUASIPEAK (dBµV)	AVERAGE (dBµV)	LIMIT (dBµV)	MARGIN (dB)	MEAS TIME (ms)	BANDWIDTH (kHz)	LINE	FILTER	CORR (dB)
0.368250	—	41.30	48.54	7.24	1000.0	9.000	N	ON	19.6
0.370500	48.52	—	58.49	9.97	1000.0	9.000	N	ON	19.6
0.737250	—	45.21	46.00	0.79	1000.0	9.000	N	ON	19.6
0.739500	53.59	—	56.00	2.41	1000.0	9.000	N	ON	19.6
1.106250	—	42.36	46.00	3.64	1000.0	9.000	N	ON	19.6
1.844250	—	40.59	46.00	5.41	1000.0	9.000	N	ON	19.6
1.844250	53.44	—	56.00	2.56	1000.0	9.000	N	ON	19.6
2.215500	—	40.21	46.00	5.79	1000.0	9.000	N	ON	19.6
2.217750	52.50	—	56.00	3.50	1000.0	9.000	N	ON	19.6

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3.2.2.6 Thermal Image

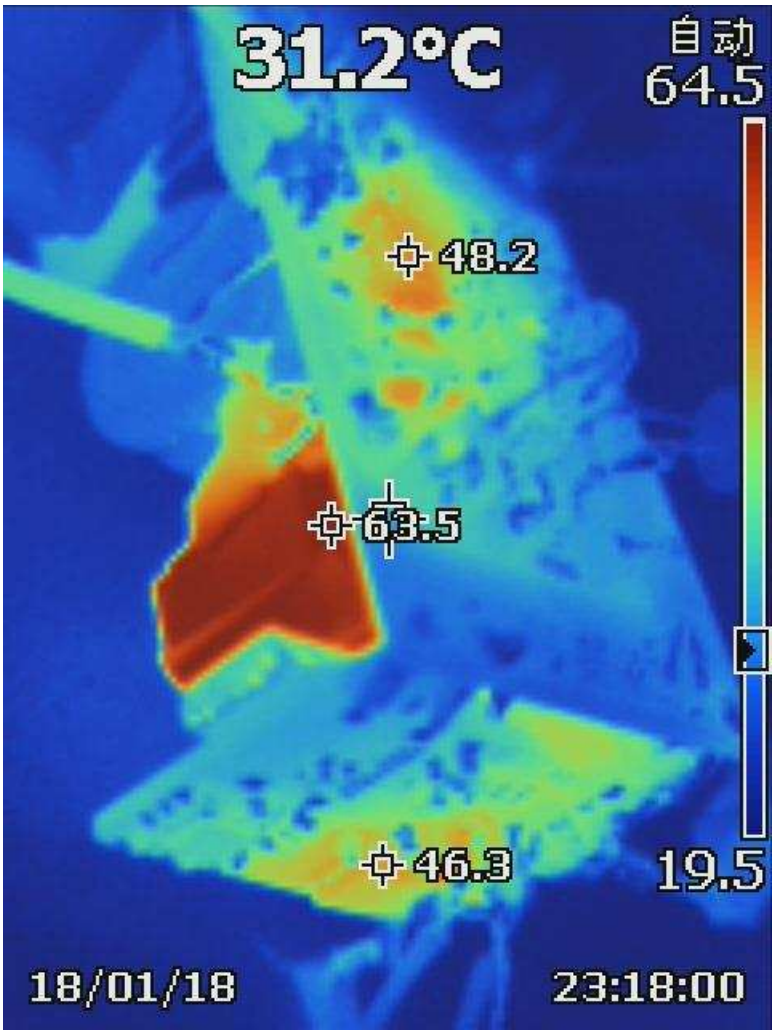

Figure 20. Thermal Image at 230-V AC/50-Hz Input, 20-V/3.25-A Output

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4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01622.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01622.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01622.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01622.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01622.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01622.

5 Software Files

To download the software files, see the design files at TIDA-01622.

6 Related Documentation

This reference design did not use any documentation.

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