Cmod A7 Horloge Demo

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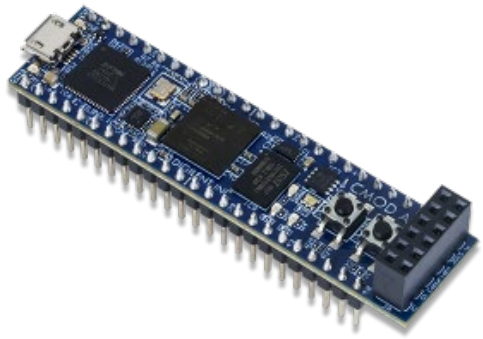

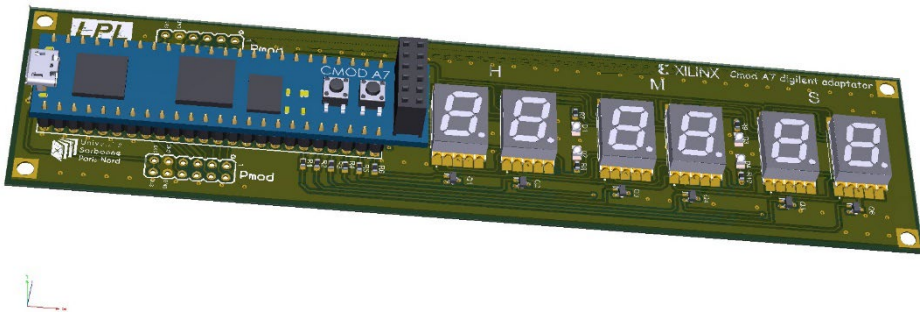

Overview

Description

This VHDL project demonstrates the basic digital clock of most of the Cmod-A7's

- The two user LEDs for digital clock
- The RGB LED is not use
- The UART bridge use to update the digital clock
- Features Used

	Not Used
2 user LEDs	
1 tri-color LEDs	

	Not Used
2 User Push Buttons	
48 GPIO Pins	
1 Pmod port	
Pins for XADC signals	
USB-UART Bridge	
512 kB SRAM	

Prerequisites

Hardware

- **Cmod A7 FPGA board**
- **Micro-USB cable**

Software

- **Vivado 2020.1**
  - *Newer versions can be used, but the procedure may vary slightly*
- **Digilent Board Support Files for Vivado**
  - Follow the Vivado Board Files for Digilent 7-Series FPGA Boards guide on how to install Board Support Files for Vivado.

Downloads

Cmod A7 35T GPIO Project Repository – https://github.com/fabzz60/Cmod-A7-Horloge-Demo- and ZIP project

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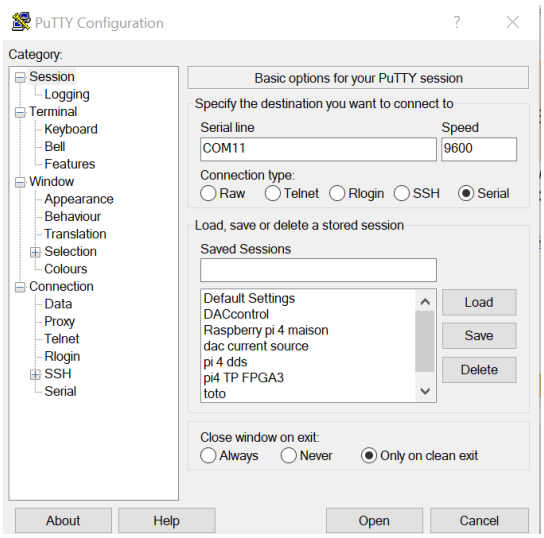
Download and Launch the Cmod A7 digital clock

1) Follow the Using Digilent Github Demo Projects Tutorial. This is an HDL design project, and as such does not support Vivado SDK, select the tutorial options appropriate for a Vivado-only design. Return to this guide when prompted to check for extra hardware requirements and setup.

Important

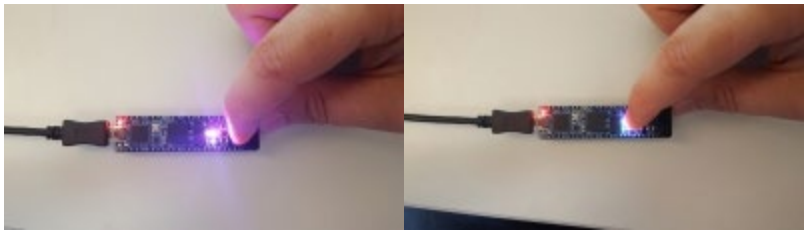
Make sure that between the 15T and 35T versions of the project, you download the version that applies to your Cmod A7.

2) In order to fully use the demo, you will need to connect a serial terminal to your Cmod A7. Plug your board into your computer with a Micro USB cable and make sure the board has power. Then open a serial terminal (such as putty) on your computer. In the terminal application setup the serial port to connect to the appropriate port for your board, with a baud rate of 9600.



Using the Cmod A7 digital clock Demo

1. LEDs and Buttons



2. UART Messages

Connect a terminal program with the settings 9600 baud rate, 8 bits, one stop bit, and no parity bit. update the clock by writing hour minute second and the enter key to validate