

# I2C FRU FAN SPECIFICATION

FOR FANS USED ON SELECT FACEBOOK SYSTEMS

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Daniel Xu, Facebook, Storage Hardware Engineer





## REVISION HISTORY

REVISION	AUTHOR(S)	DESCRIPTION	DATE
1.0.0	Daniel Xu	INITIAL RELEASE	07/14/2020
1.1.0	Daniel Xu	Removed requirement for GND pins to mate first. Changed to use one EEPROM per Dual Rotor Fan.	07/16/2020
1.1.1	Daniel Xu	Edited Multirecord header and Internal Use Area to conform with IPMI FRU Information Storage v1.2	08/21/2020
1.2.0	Daniel Xu	Corrected OEM Multirecord offsets. Made specification generic to all FB servers.	11/18/2020
1.3.0	Daniel Xu	Corrected Product Info Area size byte.	01/20/2021
1.4.0	Dan Zhang	Move FRU format spec to github	02/05/2021
1.5.0	Daniel Xu	Change I2C Series Resistor Value from 100 ohms to 22 ohms.	02/26/2021
1.6.0	Dan Zhang	Change FRU multi-record OEM record ID to 0xFB to avoid conflicts with OCP-NIC	04/14/2021



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## SCOPE

This document provides the technical specification for FRU Fans for use on Facebook rack-mounted and standalone data center equipment. As such, the information in this document should provide the information needed to create a fan conforming to the FRU Fan Specification. Additionally, this document provides examples of expected FRU Fan behaviors to help inform both fan manufacturers and system designers understand the fan's capabilities.

**Currently, FRU Fans are being introduced for certain products at Facebook.**



## INTRODUCTION

This specification describes both the electrical and command interfaces for I2C FRU Fans. I2C FRU Fans are designed for use in select Facebook servers. The decision to use FRU Fans is undertaken by the core team for a specific server product.

Traditional DC fans come in two, three and four-wire varieties. A two-wire fan consists of a wire for applying a voltage and a wire for ground. Control of the fan is done via pulse-width modulation (PWM) or via a variable power supply on the voltage wire. The three-wire fan adds a tachometer output which allows for the ability for a system to monitor the RPM of a fan. The four-wire fan adds a PWM input which removes the need for directly controlling the voltage line on the fans. Instead, a PWM duty cycle is given to the PWM input and the fan will automatically adjust the RPM.

The benefits of a FRU Fan are to provide traceability beyond what even a four-wire fan can provide.

- Serial number, model and date code.
- Voltage and Current Character
- SW and HW Revisions



## ELECTRICAL SPECIFICATION

Electrical specification for the FRU Fan interface.

### SYSTEM INTERFACE

The interface between the system and the FRU Fan will have the following signals. Note that the connector may include more pins due to power requirements.

#### DUAL ROTOR FAN

Signal Name	Description
V+	The supply voltage for the fan. Provides power for both the fan and associated circuitry. (Shared)
GND	Ground (Shared)
PWM_1	PWM Control (Server-side rotor)
PWM_2	PWM Control (Exhaust-side rotor)
TACH_1	Tachometer Reading (Server-side rotor)
TACH_2	Tachometer Reading (Exhaust-side rotor)
SDA	I <sup>2</sup> C Data Line (Shared)
SCL	I <sup>2</sup> C Clock Line (Shared)
PRES	Fan Presence Detect

### CONNECTOR

The exact connector between the system and the FRU Fan is left unspecified to allow for flexibility for system designers. However, for a dual rotor fan, there most likely needs to be a 12-pin connector due to needing two pins for the power and ground signals.

### VOLTAGE LEVELS

The V+ line's voltage is defined by the fan. The GND signal is the ground reference for the fan. All other signals are to operate at 3V3.

### I<sup>2</sup>C INTERFACE

Electrical specification follows the "Standard-mode" I<sup>2</sup>C device characteristics in the I<sup>2</sup>C specification. For FRU Fans, additional specifications for the interface are defined to allow for system compatibility. The I<sup>2</sup>C interface should operate at 3V3 (+/- 5%). In addition, the speed for communication should be 400KHz-capable.

No pull-ups resistors should be placed on the I<sup>2</sup>C signals (SDA, SCL) on the fan. It is the job of the system designer to appropriately select those resistors. To assist, the fan vendor should report the added capacitance of the FRU Fan on the I<sup>2</sup>C signals. To protect the system from high-voltage spikes, a series resistor (~22 ohms) should be placed on the FRU Fan circuitry for both the SCL and SCK lines as close as possible to the pins. The fan vendor should also report the total series resistance to the EEPROM.

System side considerations include proper selection of pull-up resistor. In addition, hot swap protection is not built into the FRU fan. For safe hot swapping of the fans, a I<sup>2</sup>C hot swap buffer like the Texas Instruments TCA4311A or the NXP PCA9511 along with protection diode is recommended on the system.

## FUNCTIONAL SPECIFICATION

This is expected to be compatible with future generations of Smart Fans.

(For Internal Use)



## PRESENCE DETECT ( $\overline{\text{PRES}}$ )

On the system, the presence detect should be pulled-up with a high-valued resistor (ex. 1M). When no fan is present, the system will see the presence detect signal high. When the fan is fully mated, the FRU Fan pull the signal down to ground.

## I<sup>2</sup>C ADDRESSING

The system should operate using 7-bit I<sup>2</sup>C addresses. The address should be 1010000.

## I<sup>2</sup>C PROTOCOL (SDA, SCL)

The FRU Fan will communicate to the system via an I<sup>2</sup>C EEPROM interface.

## GENERAL PROTOCOL SPECIFICATIONS

The system is the master and the FRU Fan is the endpoint device.

## EEPROM INTERFACE

The interface used will need to be compatible with the standard 24LCXX EEPROMs with **2-byte addressing** not 1-byte.

A list of 12LCXX series EEPROMs can be seen below (From Ref 3). Note that this shows both 1 and 2 byte addressed EEPROMs. In addition, the EEPROM must be 400KHz capable.

The fan vendor should report what EEPROM model(s) are being used on the fan.

SERIAL EEPROM CROSS REFERENCE GUIDE								
Size (bits)	MCHP Part #	Atmel Part #	Catalyst Part #	Fairchild Part #	Philips / Signetics Part #	Rohm Part #	ST Part #	Xicor Part #
128 to 512K I <sup>2</sup> C™ compatible Devices (Microchip's B revision devices do not use address pins A0, A1 and A2. These pins have no internal connection.)								
128	24AA00 T-t/p		CAT24C00 pt-v T					X24C00 pt-v
128	24C00 T-t/p							
128	24LC00 T-t/p							
1K	24AA01 T-t/p	AT24C01-10 pt-v T	CAT24C01B pt-v T			BR24C01A p-W T	M24C01-vptT	
1K	24C01B T-t/p				PCA8581C p			X24C01 pt-v
1K	24C01C T-t/p	AT24C01A-10 pt-v T	CAT24WC01 pt-v T		PCA8581 p		M24C01-vptT	X24C01 pt-v
1K	24LC014 T-t/p	AT24C01A-10 pt-v T	CAT24WC01 pt-v T		PCA8581C p		M24C01-vptT	X24012 pt-v
1K	24LC21A T-t/p	AT24C21-10 pt-v T	CAT24C21 pt-v T		PCB2421C p	BR24C21 p-T	ST24FC21-ptT	
1K	24LCS21A T-t/p						ST24FW21-ptT	
2K	24AA02 T-t/p	AT24C02ad-10 pt-v T	CAT24WC02 pt-v T			BR24C02 p-WT	M24C02-vptT	
2K	24C02B T-t/p			FM24C02U fvtp	PCF8582C-2 p			X24C02 pt-v
2K	24C02C T-t/p	AT24C02ad-10 pt-v T	CAT24WC03 pt-v T	FM24C03U fvtp	PCF8582C-2 p		M24C02-vptT	X24C02 pt-v
2K	24LC024 T-t/p	AT24C02ad-10 pt-v T	CAT24WC03 pt-v T		PCF8582C-2 p		M24C02-vptT	X24C02 pt-v
2K	24LC025 T-t/p							
2K	24LCS52 T-t/p						M34C02, M34C02-W	
4K	24AA04 T-t/p	AT24C04ad-10 pt-v T	CAT24WC04 pt-v T			BR24C04 p-T	M24C04-vptT	
4K	24LC04B T-t/p			FM24C04U fvtp	PCF8594C-2 p			X24C04 pt-v
8K	24AA08 T-t/p	AT24C08ad-10 pt-v T	CAT24WC08 pt-v T			BR24C08 p-WT	M24C08-vptT	
8K	24LC08B T-t/p			FM24C08U fvtp	PCF8598C-2 p			X24C08 pt-v
16K	24AA16 T-t/p	AT24C16ad-10 pt-v T	CAT24WC16 pt-v T			BR24C16 p-WT	M24C16-vptT	
16K	24LC16B T-t/p			FM24C16U fvtp	PCF85116-3 p			X24C16a pt-v
32K	24AA32A T-t/p	AT24C32ad-10 pt-v T	CAT24WC32 pt-v T			BR24C32 p-WT	M24C32-vptT	
32K	24LC32A T-t/p							X24320 pt-v
64K	24AA64 T-t/p	AT24C64ad-10 pt-v T	CAT24WC64 pt-v T			BR24C64 p-WT	M24C64-vptT	
64K	24LC64 T-t/p			FM24C64 fvtp T				X24645 pt-v
64K	24AA65 T-t/p							
64K	24LC65 T-t/p							
128K	24AA128 T-t/p	AT24C128ad-10 pt-v T	CAT24aC128 pt-v T				M24C128-avptT	
128K	24LC128 T-t/p			FM24C128 fvtp T				X24128 pt-v
128K	24FC128 T-t/p	AT24C128ad-10 pt-v T	CAT24aC128 pt-v T				M24C128-avptT	X24128 pt-v
256K	24AA256 T-t/p	AT24C256ad-10 pt-v T	CAT24WC256 pt-v T				M24C256-avptT	
256K	24LC256 T-t/p			FM24C256 fvtpT				X24C256 pt-v
512K	24AA512 T-t/p	AT24C512ad-10 pt-v T					M24512-vptT	
512K	24LC512 T-t/p							
512K	24FC512 T-t/p	AT24C512ad-10 pt-v T						
512K	24AA515 T-t/p							
512K	24LC515 T-t/p							
512K	24FC515 T-t/p							

## EEPROM DATA STRUCTURE

The FRU data on the EEPROM will be organized per the IPMI FRU Information Storage Definition v1.2.

## FRU INFORMATION FORMAT

The latest FAN FRU format please refer to: [Smartfan-fru.md at Facebook OpenBMC github](#)

(For Internal Use)



## REFERENCES

1. UM10204 I<sup>2</sup>C-bus specification and user manual <https://www.nxp.com/docs/en/user-guide/UM10204.pdf>
2. IPMI Platform Management FRU Information Storage Definition  
<https://www.intel.com/content/dam/www/public/us/en/documents/product-briefs/platform-management-fru-document-rev-1-2-feb-2013.pdf>
3. Microchip Serial EEPROM Cross Reference Guide <http://ww1.microchip.com/downloads/en/devicedoc/21621d.pdf>