Dual-channel bootstrapped switch for high-speed high-resolution sampling

L. Wang, W.J. Yin, J. Xu and J.Y. Ren

A novel low-voltage CMOS bootstrapped switch has been designed. In this switch, a PMOS-type bootstrapped circuit combining with an NMOS-type one forms a dual-channel sampling switch that transmits the input signals to the output. Because of this parallel structure, the variation of on-resistance, owing to the variation of the gate overdrive and the threshold voltage, is greatly reduced, exhibiting gain in the sample-and-hold accuracy and linearity. The design was realised in an SMIC 0.18 μm CMOS process and its greatly improved dynamic performance was measured.

Introduction: The bootstrapped switch can provide more constant on-resistance than the regular MOS switch by keeping the gate-source voltage of the sampling switches independent of input signals. They have often been used for sampling in S/H circuits to acquire higher precision and linearity.

Most high-speed S/H circuits are based on the conventional bootstrapped switch [1]. As shown in Fig. 1, it operates on a single phase clock, ck, that turns the sampling switch M11 on and off. During the 'on' phase, it provides an on-resistance of

$$R_{\mathrm{on},n} = \frac{1}{\mu_n C_{ox}(W/L)_n(V_{DD} - V_{thn})} \quad (1)$$

The conventional bootstrapped switch eliminates the distortion source of overdrive voltage, but it cannot eliminate the distortion induced by threshold voltage variation from body effect. Several methods have been proposed to overcome this problem [2–4]. The main idea behind [2] is to use direct connection from source to bulk of the sampling switch during 'on' state. This is a straightforward idea, but may not be desirable owing to large parasitic capacitances associated with the well; and for an NMOS bootstrapped switch with its bulk generally connected to its substrate, this method is not suitable, especially in a single-well CMOS technology. Other methods have either limited input bandwidth or introduced high design complexity, which may increase design cost. In this Letter, we present a bootstrapped switch which can eliminate nonlinear distortion and acquire a very low and constant on-resistance with low cost.

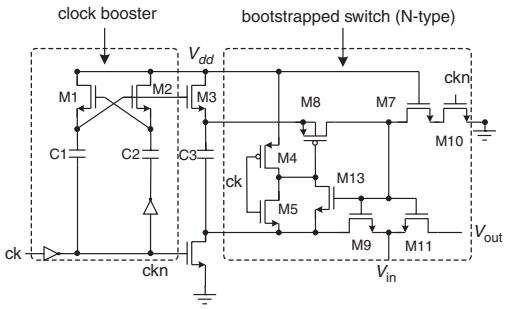

Fig. 1 *Conventional NMOS bootstrapped switch*

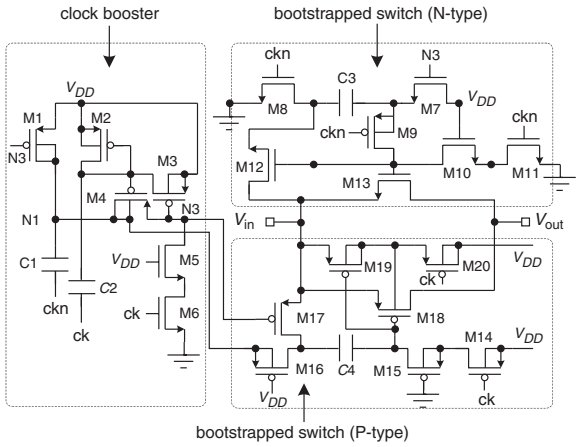

Fig. 2 *Proposed bootstrapped switch*

Proposed bootstrapped switch: Fig. 2 shows a schematic diagram of the proposed bootstrapped switch. It consists of three main elements: a clock booster, a PMOS-type and an NMOS-type bootstrapped switch. The clock booster is actually a charge pump. Its output signals N1 and N3 are used to control the two sampling switches. Both the NMOS-type and PMOS-type switch are bootstrapped. They were turned on or turned off simultaneously like a CMOS switch to transmit input signals to the V_{out} terminal. In addition, there is a clock generator to provide two matching non-overlapped clock signals and its reverse one.

During the off state, ck is low. Switch M11 discharges the gate of M13 to ground. M14 connects the gate of M18 to the supply voltage V_{dd}. At the same time, capacitors C3 and C4 are both charged to V_{dd}. They will act as floating batteries during the 'on' state. When ck goes high, M9 and M12 are turned on, allowing C3 to connect across the gate and source of M13. M17 allows C4 to connect across the gate and source of M18. Thus, floating batteries C3 and C4 enable the gates of M13 and M18 to track the input voltage V_{in} shifted by V_{dd}, keeping the gate-source voltage constant regardless of input signals. To reduce the variation in on-resistance of $P0$, we compensate for its body effect. By using switches M19 and M20, the bulk of M18 is connected to its source or V_{dd} during 'on' or 'off' state, respectively.

The on-resistance of this proposed circuit is

$$R_{on} = R_{on,N0} \| R_{on,P0} = \frac{1}{\mu_n C_{ox}(\frac{W}{L})_{N0}(V_{DD} - V_{thn}) + \mu_p C_{ox}(\frac{W}{L})_{P0}(V_{DD} - V_{th0,p})} \quad (2)$$

Comparing (1) and (2), a smaller on-resistance of the sampling switch can be acquired. The variations in it for the body effect of M13 can be reduced by increasing the values in the denominator of (2). This results in improved linearity of the switch. In the clock booster, feedback transistor M3 keeps the gate-drain voltage of transistor M4 to a reasonably low level and is subjected to a maximum source-gate voltage of $V_{DD} + |V_{th,p}|$, which is acceptable in this SMIC process. M5 and M6 are used to provide sufficient driving capability for N3 and discharge the gate of M17 to ground during 'on' state. The N-type bootstrapped part has a similar structure to the conventional one. Capacitors C3 and C4 are sufficiently large to supply charge to the gate of switching devices and address the charge sharing from all parasitic capacitances in the charging path. Devices in this path, such as M9, M12 or M17, have a small size, with the minimum length to reduce parasitic capacitances. In the P-type bootstrapped part, M16 has a small size to avoid large loading, which can present a substantial capacitance to the terminal N1. This ensures N1 reaches the high level of $2 \times V_{DD}$ during 'off' state.

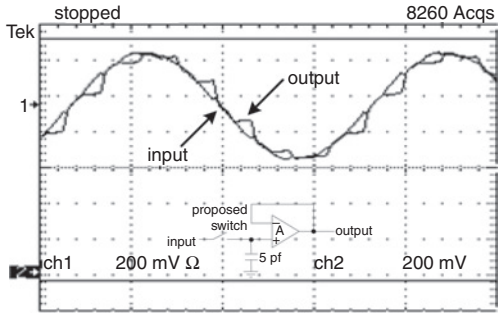

Fig. 3 *Measured switch behaviour of test chip*

Experiments and comparison: We manufactured the proposed circuit using an SMIC 0.18 μm CMOS process. The supply voltage V_{dd} is 1.8 V. The active area required for the implementation of the switch was less than 0.01 mm^2. Fig. 3 shows the measured input and output waveforms of the test chip with a sampling speed of 30.4 MHz and input frequency of 3.8 MHz. Fig. 4 shows the dynamic performance of S/H circuits based on the proposed bootstrapped switch and the conventional one with a sampling speed of 100 MHz and input frequency varying from 10 to 100 MHz. The test was carried out under the worst case where the sampling capacitor has a DC path to ground and charge injection and clock feed through both exist. The SNDR and SFDR are improved by about 15 and 17 dB, respectively. For input frequency up to the sampling frequency, the proposed switch can acquire SNDR and SFDR over 85 and 87 dB. Fig. 5

shows a comparison of the harmonic distortion between this work and others. Under the same conversion rate of 100 MS/s and 10 MHz input frequency, the proposed switch acquires total harmonic distortion (THD) of about −101 dB, second-harmonic distortion (HD2) of −102 dB and third-harmonic distortion (HD3) of −115.4 dB. The critical linearity characterisation is preferable to other reported structures.

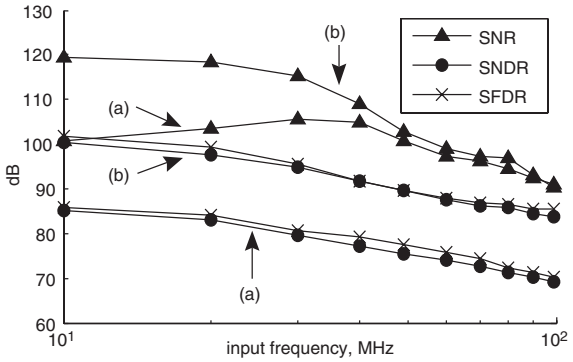

Fig. 4 *Dynamic performance against input frequency*
(a) conventional switch
(b) proposed switch

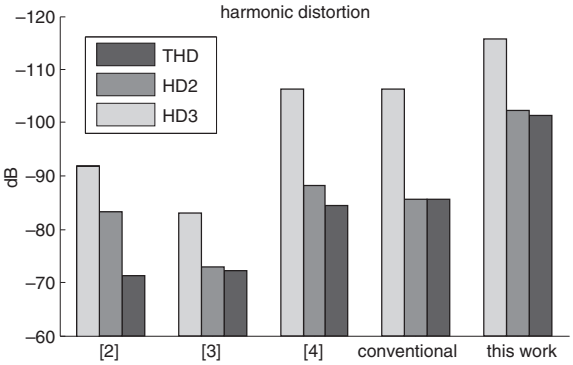

Fig. 5 *Comparison of harmonic distortion*

Conclusions: A new bootstrapped switch capable of operating with a very low and constant on-resistance is presented. A dual-channel structure was adopted to avoid the gate-source voltage of sampling devices varying with input signals. This ensures high SNDR, wide input bandwidth and low harmonic distortion with small device sizes and chip areas. The proposed switch can be applied in a high-speed high-resolution sampling circuit.

26 July 2006
Electronics Letters online no: 20062344
doi: 10.1049/el:20062344

L. Wang, W.J. Yin, J. Xu and J.Y. Ren (*Department of Microelectronics and Solid State Electronics, State Key Laboratory of ASIC & Systems, Fudan University, Shanghai, 201203, People's Republic of China*)

E-mail: 042021074@fudan.edu.cn

References

1 Abo, A.M., and Gray, P.R.: 'A 1.5-V 10-bit 14.3-MS/s CMOS pipeline analog-to-digital converter', *IEEE J. Solid-State Circuits*, 1999, **5**, pp. 599–606
2 Fayomi, C.J.B., Roberts, G.W., and Sawan, M.: 'Low-voltage CMOS analog bootstrapped switch for sample-and-hold circuit: design and chip characterization'. IEEE Proc. Int. Symp. Circuits and Systems, Kobe, Japan, 2005, Vol. 5, pp. 2200–2203
3 Ong, A.K., *et al*.: 'A method for reducing the variation in 'on' resistance of a MOS sampling switch'. IEEE Proc. Int. Symp. Circuits and Systems, 2000, Vol. 5, pp. 437–440
4 Yang, C.Y., and Hung, C.C.: 'A low-voltage low-distortion MOS sampling switch'. IEEE Proc. Int. Symp. Circuits and Systems, Kobe, Japan, 2005, Vol. 5, pp. 3131–3134