

# A 65-nm CMOS Continuous-Time Pipeline ADC Achieving 70-dB SNDR in 100-MHz Bandwidth

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**Abstract**—We describe the design principles and circuit details of a three-stage continuous-time pipeline (CTP) ADC that achieves 70-dB SNDR in a 100-MHz bandwidth while sampling at 800 MHz. Implemented in 65-nm CMOS, the ADC is easy to drive and incorporates an inherent anti-alias filter that achieves 60-dB rejection in the first Nyquist band. Each pipeline stage is realized using a second-order Rauch-filter-based residue amplifier that incorporates a 9-level resistive DAC and an RC-delay line. A dummy-switching scheme relaxes DAC reference-buffer requirements. The back-end ADC is a 4× time-interleaved 7-bit SAR converter. The Schreier and Walden FoMs of our ADC are 165.4 dB and 56.1 fJ/level, respectively.

**Index Terms**—Anti-alias, cancellation, continuous-time (CT) ADC, filtering, oversampling, pipeline, residue.

## I. INTRODUCTION

Achieving ADC resolution of 10–12 bits over a signal bandwidth in the hundreds of MHz range has traditionally been the forte of the discrete-time (DT) pipeline (or time-interleaved SAR) architecture. Since DT-pipes and SAR ADCs sample the input up front, they need an anti-alias filter preceding the ADC. To relax the design of this filter, they are typically operated with an oversampling ratio (OSR) of at least 2. Further, the switched-capacitor nature of their input makes them difficult to drive. An integrated buffer has to be designed, which often consumes more power than the ADC. The reference-buffer design is also a challenge due to the large signal-dependent current needed by these ADCs. Using a CTDSM is an approach to avoid these problems—it presents a resistive impedance that is easy to drive, and relaxes the design of the anti-alias filter due to the high OSR. However, technology limitations impose a fundamental limit on the sampling rate, thereby restricting its bandwidth. For instance, in a 65-nm CMOS process, achieving more than about 50–60-MHz bandwidth (in a power-efficient manner) with a single-loop CTDSM seems extremely difficult.

A continuous-time pipeline (CTP) converter is an emerging architecture [1], [2] that avoids the need to close the sampled-data feedback loop that is needed in a CTDSM. Thanks to this, a higher signal bandwidth can be obtained in a given process technology. Further, thanks to continuous-time (CT) operation, a resistive input impedance and low-power dissipation are achieved. While early development treated a CTP as a natural extension of a DT pipeline ADC, recent work [3] shows that a CTP can be approached as an attempt to realize an anti-alias filter and ADC in one unit.

This work describes a CTP that achieves about 70-dB SNDR over a 100-MHz bandwidth in a 65-nm CMOS technology, while sampling at 800 MS/s (OSR = 4). It features Rauch-biquad-based

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residue-generating stages that employ resistive DACs for low noise. A dummy-switching scheme reduces distortion due to the nonzero impedance of the reference path. The details form the rest of this letter, which is organized as follows. In Section II, we discuss the ADC architecture. Circuit implementation aspects are described in Section III. Section IV gives measurement results, compares our work with state-of-the-art, and concludes this letter.

## II. ARCHITECTURAL DETAILS

The block diagram of our CTP is shown in Fig. 1(a). It consists of three stages preceding a 7-bit 4× time-interleaved asynchronous SAR (ASAR) converter. The call-out shows the signal-processing equivalent of stage 1.<sup>1</sup> A 9-level quantizer samples the input  $u$  at  $f_s = 1/T_s = 800$  MHz, and creates a coarse version of it. The ADC and DAC are clocked on opposite edges of the clock to give enough time to the ADC to make a decision. This delay, along with the half-cycle delay due to the NRZ DAC pulse effectively delays the DAC output by  $T_s$  with respect to  $u$ . To generate the residue therefore,  $u$  is delayed by  $T_s$  [1], [4], [5] using a delay network [with transfer function  $H_d(s)$ ]. The residue  $v_r(t)$  is processed by a residue-amplifying filter with transfer function  $H_A(s)$ . The dc gain of  $H_A$  is chosen so that the filtered residue  $v_1(t)$  does not exceed the input range of the next stage due to practical nonidealities like offsets in the comparators of the flash ADC, and delay mismatch between the input and ADC-DAC path. In our design, for instance, the dc gain is only  $\approx 4$  even though a 9-level quantizer is used.  $H_A(s)$  is chosen to be a second-order Butterworth lowpass filter with a 3-dB bandwidth of 110 MHz. Like in [2], this is an improvement over earlier work that uses a first-order residue amplifier [1]. This is due to the following. The DAC produces images around multiples of  $f_s$ , which contribute to the swing at the residue-amplifier output. A second-order structure attenuates these images better. As seen in Fig. 1(a), a second-order  $H_A(s)$  attenuates images by more than 15 dB with respect to a first-order amplifier (for OSR = 4). Further, simulations show that increasing the order has virtually no effect on the peak-to-peak swing of  $v_1(t)$ .  $v_1(t)$  is further processed by two more pipeline stages before being digitized by a 7-bit ASAR ADC that uses 4× time interleaving. Thanks to the large gain  $\approx 64$  preceding the back-end ADC, its interleaving artifacts do not affect the performance of the CTP.

The system equivalent of the CTP can be determined by exciting it with a complex exponential  $u = e^{j2\pi ft}$ . Denoting the additive quantization error introduced by the ASAR ADC by  $e_4$ , analysis of Fig. 1(a) yields the block diagram of Fig. 1(b) which indicates that  $[H_d(j2\pi f)H_A(j2\pi f)]^3 e^{j2\pi fT_s n} + e_4 = D_4 + \sum_{i=1}^3 D_i * h_i$  where  $*$  denotes convolution and  $h_i$  ( $i = 1, 2, 3$ ) denotes the sampled pulse response from  $D_i$  to the ASAR input  $y_4$ . Dividing the above equation by the  $H_A^3(0)$  and rearranging, we obtain

$$\overbrace{(1/H_A^3(0))[(D_1 * h_1) + (D_2 * h_2) + (D_3 * h_3) + D_4]}^{\text{CTP output}}$$

<sup>1</sup>Stages 2 and 3 are similar, except for impedance scaling to save power.

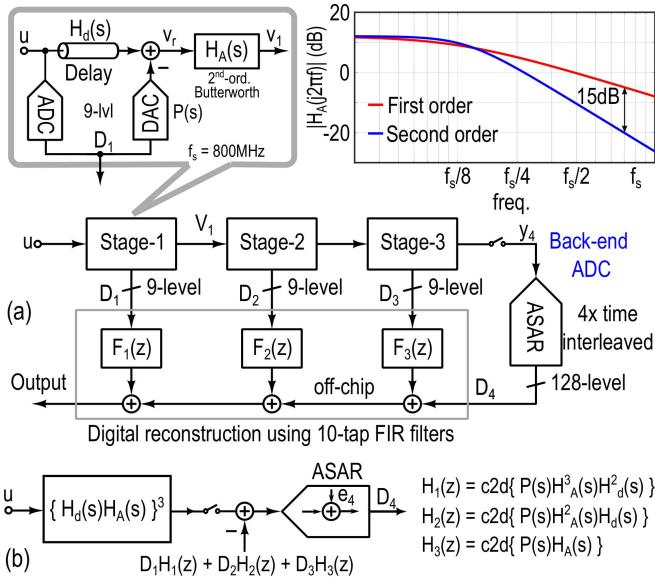


Fig. 1. (a) Architecture of the three-stage CTP. The call-out shows the architecture of each stage.  $H_d(s)$  and  $H_A(s)$  denote the transfer functions of the delay and residue-amplifying filters, respectively. (b) Equivalent block diagram of the CT-pipe illustrating its filtering effect on the input signals.

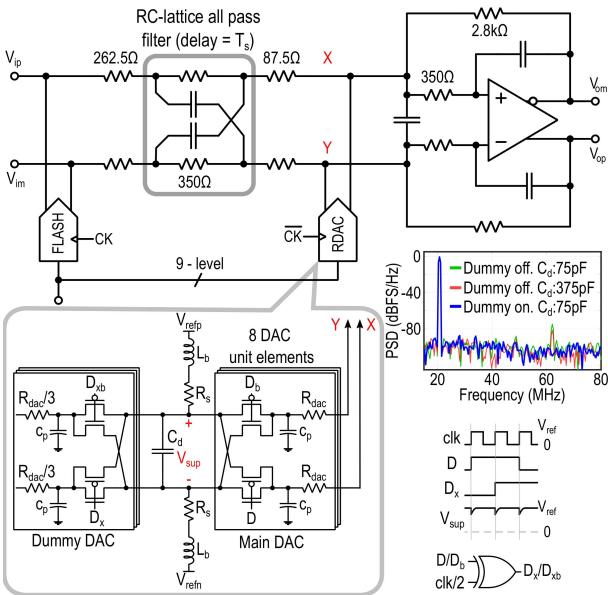


Fig. 2. Simplified schematic of the first stage. The resistor DAC along with the dummy DAC is shown.  $C_p$  is the parasitic capacitance of the DAC buffers and resistors.  $L_b$  and  $R_s$  are the reference line bond-wire inductance and resistance, respectively.  $C_d$  is the decoupling capacitor on the reference. The PSD plot shows the simulated output spectrum for different  $C_d$  with and without the dummy DAC.  $L_b = 1.5\text{nH}$  and  $R_s = 1\Omega$ .

$$= \underbrace{[H_d(j2\pi f)H_A(j2\pi f)/H_A(0)]^3 e^{j2\pi fT_s n}}_{= H_{eq}(j2\pi f)} + \underbrace{e_4/(H_A^3(0))}_{\text{quant. noise}}. \quad (1)$$

The left-hand side of (1), which is the output sequence of the CTP, is the sum of two parts. The first is the input, which is processed by a filter with response  $H_{eq}(j2\pi f) = [H_d(j2\pi f)H_A(j2\pi f)/H_A(0)]^3$  and then sampled. The dc gain of  $H_{eq}$  is unity. The second term on the right-hand side of (1), namely,  $e_4/H_A^3(0)$ , is the quantization error introduced by the CTP. From the above discussion, it is seen that our CTP is equivalent to a cascade of a sixth-order anti-alias filter

and a 13-bit ADC (7-bit ASAR ADC whose step size is divided by  $H_A^3(0) \approx 64$ ). The  $h_i$  are impulse responses of IIR filters, and are approximated by their 10-tap equivalents  $F_i(z)$ , as shown in Fig. 1(a).

### III. CIRCUIT DESIGN

Fig. 2 shows the simplified schematic of the CTP's first stage. It is basically a Rauch biquad realizing a Butterworth transfer function, modified to enable it to generate the filtered residue waveform. A coarse approximation of the input is created using the 9-level flash-DAC path, which incorporates a half-clock cycle delay between the ADC and DAC. This delay, along with the NRZ DAC pulse, creates an effective delay of one clock period between the input and DAC output. To reduce the peak-to-peak value of the residue, the input path incorporates a delay section based on an RC-lattice network. The dc gain of the residue transfer function is chosen to be four even though a 9-level quantizer is used—this over-ranging allows for delay mismatch between the input and ADC-DAC paths, as well as offsets in the comparators of the flash converter. The 3-dB bandwidth of the residue transfer function is 110 MHz. The comparators in the flash ADC are based on StrongArm latches. A resistive DAC, whose design is described in the next section, is chosen for low-noise operation. This is in contrast to prior art designs [1], [2], [6] that employ current-steering techniques, which necessitated an additional higher supply to achieve an adequately low noise.

#### A. DAC Design

The call-out in Fig. 2 shows the simplified schematic of the DAC. For the time being, ignore the dummy DAC. The main DAC consists of eight unit elements, each consisting of resistors  $R_{dac}$  switched between the references by the data-bit  $D$ .  $c_p$  denotes the parasitic capacitance at the junction of the switches.  $L_b$  and  $R_s$  model the (bond-wire) inductance and series resistance of the reference path, respectively.  $C_d$  is the on-chip capacitor used to bypass high frequencies on the reference nodes. The effective reference voltage seen by the main DAC is denoted by  $V_{sup}$ . Whenever  $D$  makes a transition, a charge  $c_p V_{sup}$  is drawn from the reference. Due to the nonzero reference-path impedance, this data-dependent switching current causes  $V_{sup}$  to vary in a signal-dependent fashion and results in distortion [7]. The dummy DAC addresses this problem [8]. Each element in the main DAC is associated with a corresponding dummy element that is driven by a sequence  $Dx = D \oplus (clk \div 2)$ .  $Dx$  makes a transition when  $D$  does not, and vice versa. The dummy consists of replica switches and floating resistors that are one-third the size of the resistors in the main DAC element. This choice of dummy results in an identical parasitic capacitance at the junction of the switches in the dummy element [7]. Thanks to the dummy, the reference current is data independent. Thus, the output impedance of the reference buffer is no longer a concern. Simulations (see the PSD plot in Fig. 2) show that using the dummy DAC greatly reduces the size of the capacitor  $C_d$  needed in the reference path.

#### B. OTA Design

Fig. 3 shows the simplified schematic of the OTA used in the Rauch filter of Fig. 2. It is a three-stage feedforward-compensated design that employs separate CMFB loops for the individual stages. An nMOS/pMOS input pair is used to achieve a higher transconductance for a given bias current. The negative resistance at the first-stage output increases the dc gain of the stage. The overall dc gain and unity-gain bandwidth (UGB) of the OTA are 54 dB and 2 GHz, respectively. The second and third stages of the CTP are similar to the first, except that they are impedance scaled by 4× to save power.

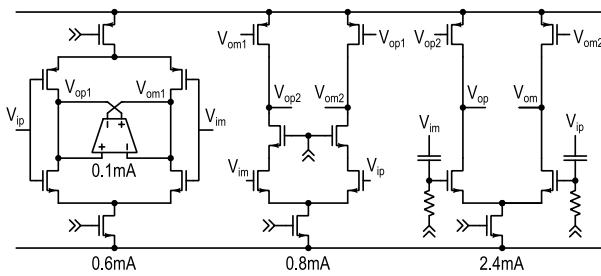


Fig. 3. Simplified schematic of three-stage OTA.

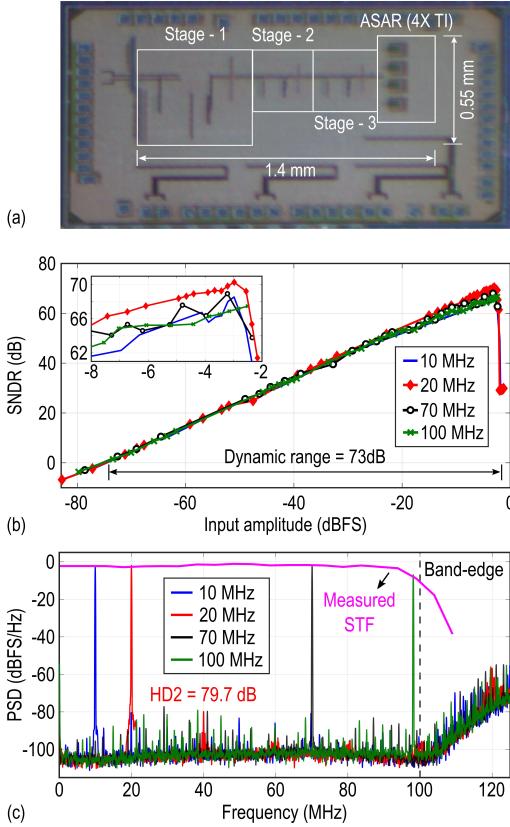
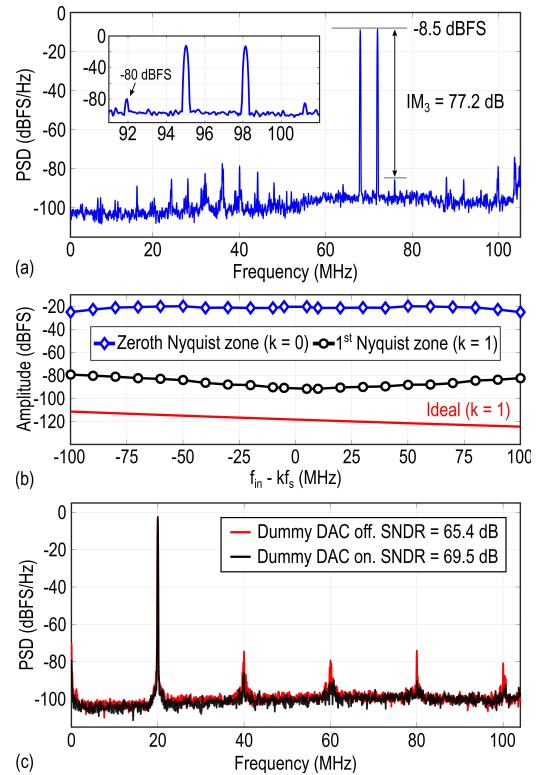


Fig. 4. (a) Chip micrograph. (b) Measured SNDR as a function of input amplitude for 10, 20, and 70 MHz input signals. (c) PSD for the case of peak SNDR for 10, 20, 70, and 100 MHz input signals. The measured STF is also shown.

### C. Back-End SAR ADC

The output of the third stage is digitized by four time-interleaved 7-bit ASAR slices, each operating at 200 MHz. Each ADC slice operates with a monotonic switching procedure [9]. The 6-fF unit capacitor in the SAR DAC array is realized as a multimetal sandwich. Interleaving artifacts are attenuated by the gain of the front-end ( $\approx 64$ ) and are inconsequential for the targeted performance level.

The ADC output is reconstructed by filtering the stage outputs with 10-tap FIR filters  $F_1$ ,  $F_2$ , and  $F_3$  [see Fig. 1(a)]. These tap weights are foreground calibrated in the following manner. The ADC is excited by a sinusoid, and the stage outputs  $D_1, \dots, D_4$  are captured. The in-band noise power of the sequence  $[D_1(z)F_1(z) + D_2(z)F_2(z) + D_3(z)F_3(z) + D_4(z)]$  is minimized in the least-squares sense. These frequency-domain calculations are implemented off-chip. Once calibrated, these tap weights are frozen, and used for all other input

Fig. 5. (a) Measured IM<sub>3</sub> distortion with two  $-8.5$  dBFS input tones at 68 and 72 MHz. The inset shows the output spectrum when the input tones are applied around 100 MHz. The measured IIP<sub>3</sub> is 27.3 dBFS. (b) Measured alias rejection of the ADC for a  $-20$  dBFS input. (c) PSD of the ADC output for a 20-MHz input signal with the dummy DAC off/on.

amplitudes/frequencies. A possible way of implementing an on-chip calibration engine is given in [2].

### IV. MEASUREMENT RESULTS AND CONCLUSION

The micrograph of the prototype, fabricated in a 65-nm CMOS process, is shown in Fig. 4(a). The active area is about  $0.77 \text{ mm}^2$ . Fig. 4(b) gives the measured dynamic range plots for 10, 20, 70, and 100 MHz inputs. The peak SNR/SNDR (for a 20-MHz input) is 70.4 dB/70 dB. Fig. 4(c) shows the PSD of the ADC's output for varying input frequencies. The measured signal transfer function (STF) is also given. The filtering nature of the ADC is apparent.

Fig. 5(a) shows the response of the ADC to two closely spaced tones at 68/72 and 95/98 MHz. From the IM<sub>3</sub> of 77.2 dB, the IIP<sub>3</sub> is calculated to be 27.3 dBFS. The measured alias rejection of the CT-pipe for a  $-20$ -dBFS input is shown in Fig. 5(b). It is seen that the ADC provides greater than 60-dB alias rejection in the first Nyquist zone. Fig. 5(c) compares the PSD of the ADC output with the dummy DAC off/on for a  $-2.94$ -dBFS input. The benefit of using the dummy DAC is apparent. The CTP consumes 29 mW. Of this, 10 mW is dissipated in the OTAs while the SAR array in the backend consumes 9 mW. The Schreier and Walden FoMs of our ADC are 165.4 dB and 56.1 fJ/level, respectively. The digital filters needed for reconstruction are estimated to consume about 15 mW.<sup>2</sup>

Table I compares the performance of our design with that of state-of-the-art works realized in 65/40-nm CMOS. The area occupied by our design is higher than that of the Nyquist converters [10]–[13]. This makes sense due to the following. Nyquist converters will need anti-alias filters up front. Practical considerations, therefore,

<sup>2</sup>This power is not included in FoM calculations.

TABLE I  
PERFORMANCE SUMMARY AND COMPARISON WITH  
STATE-OF-THE-ART 40/65 NM DESIGNS

	This work	[10]	[11]	[14]	[12]	[13]	[15]	[16]
Architecture	CT Pipe	Pipe SAR	DT Pipe	CT $\Delta\Sigma$	Pipe SAR	Pipe SAR	VCO $\Delta\Sigma$	CT $\Delta\Sigma$
Anti-alias	Yes	No	No	Yes	No	No	Yes	Yes
Tech (nm)	65	40	65	45	65	65	65	40
BW (MHz)	100	125	125	60	165	100	50	75
$f_s$ (MHz)	800	250	250	6000	330	210	1500	3200
SNR (dB)	70.4	-	-	61.5	-	-	76.1	66.8
SNDR(dB)	70	56	65.7	60.6	63.5	60.1	73.5	65.5
Power(mW)	29	1.7	49.7	20	6.23	5.3	51.8	22.8
Area(mm <sup>2</sup> )	0.77	0.07	0.53	0.49	0.08	0.48	0.35	0.07
FoM <sub>s</sub> (dB) <sup>†</sup>	165.4	164.7	159.7	155.4	167.7	163.1	163.3	161

<sup>†</sup> FoM<sub>s</sub> (dB) = SNDR + 10 log (BW/Power)

dicate that they be operated with OSR > 2, limiting their application bandwidth to  $f_s/4$ . They will also need buffers to drive the switched-capacitor impedance that they present to the external world. Our design, being an anti-alias filter and an ADC rolled into one, should be expected to have an increased area due to the inherent embedded filtering.<sup>3</sup> (Recall that the area of a filter is dictated by its input-referred thermal noise spectral density and cutoff frequency.) The anti-alias filters preceding [10]–[13] would need to be at least as large as the filter in our design. Further, our work achieves a power efficiency which is comparable to that of state-of-the-art works, while being easy to drive.

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<sup>3</sup>Our prototype chip has a 50-MHz bandwidth mode, which resulted in an area increase by about 30%.