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LETTER

Bootstrapped switch with improved linearity based on a negative-voltage bootstrapped capacitor

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Abstract This study introduces a new bootstrapped switch for improving sampling linearity. In this technology, the introduction of a negative-voltage bootstrap capacitor reduces the parasitic capacitance at the critical signal node, thus improving its linearity. The proposed circuit is simulated using 0.18-μm complementary metal-oxide-semiconductor technology. The parasitic capacitance of the proposed scheme is approximately 30% lower than that of the conventional structure. In the case of rail-to-rail input, the proposed switch achieves a signal-to-noise-plus-distortion ratio (SNDR) of 83.3 dB and a spurious-free dynamic range (SFDR) of 82.3 dB from a 1.2-V supply at a 50-MHz sampling rate. The SFDR and SNDR of the proposed bootstrapped switch increase by 11.7 and 12.7 dB, respectively, compared with those of conventional bootstrapped switches.

Keywords: bootstrapped switch, linearity, low voltage
Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Sensors are ubiquitous devices that include audio, temperature, light, magnetic, and capacitive sensors as well as biopotential acquisition and biometric identification sensors for wearable devices. In various sensor applications, the analog-to-digital converter (ADC) is a key block, and the core circuit of an ADC is the sample-and-hold (S/H) circuit. The performance of the S/H circuit largely determines the ADC performance. The S/H circuit of a conventional metal-oxide-semiconductor (MOS) switch is adversely affected by problems, such as low linearity and channel charge injection, clock feedthrough, kT/C noise, and other nonideal factors that limit its accuracy and speed.

To address these problems, researchers have proposed bootstrapped-switch technology [1] including various optimization-compensation techniques for bootstrapped switches such as body-effect compensation of analog switches to improve linearity [2, 3, 4], couple-effect compensation of bootstrapped switches to improve the high frequency performance [5, 6, 7, 8, 9], and other improvements [10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32]. These bootstrapped switches have demonstrated improved performance. Although these various compensation techniques have improved the linearity of the bootstrap switch, the parasitic capacitance of key nodes has not been reduced, and the size of these parasitic capacitances affects the nonlinearity of the bootstrap switch. To address this, a bootstrapped switch with improved linearity based on a negative-voltage bootstrapped capacitor is proposed in this study. In this technology, the introduction of a negative-voltage bootstrap capacitor causes the gate-source voltage of the PMOS switch on a signal link to be equal to $2V_{DD}$. That is, in the case of the same on-resistance, the size of the PMOS can be designed to be smaller to reduce the parasitic capacitance, which increases the linearity of the bootstrapped switch. Compared with the conventional bootstrapped switch, the number of transistors connected to the gate of the sampling transistor is smaller, which reduces the parasitic capacitance of the gate of the sampling transistor, thus improving the linearity of the bootstrapped switch.

2. Analysis of conventional bootstrapped switch

The conventional bootstrapped switch [5] is shown in Figure 1. When CLK = 0 and CLKB = 1, transistors M1, M3, M4, M9, and M10 are turned on, and transistors M2, M5, M6, M7, and M8 are turned off. Furthermore, the voltage across the bootstrapped capacitor C_1 is charged to V_{DD} and discharged to the ground. Because the sampling switch M8 is turned off, the output terminal voltage is in a holding state. When CLK = 1 and CLKB = 0, transistors M1, M3, M4, M9, and M10 are turned off, and transistors M2, M5, M6, M7, and M8 are turned on. The bootstrap capacitor C_1 charges the sampling switch M8; thus, the gate-source voltage of the sampling switch is fixed near V_{DD}. In this state, the output voltage follows the input signal. Because of the node parasitic capacitance in the bootstrapped-switch circuit, its gate voltage after sampling switch M8 is turned

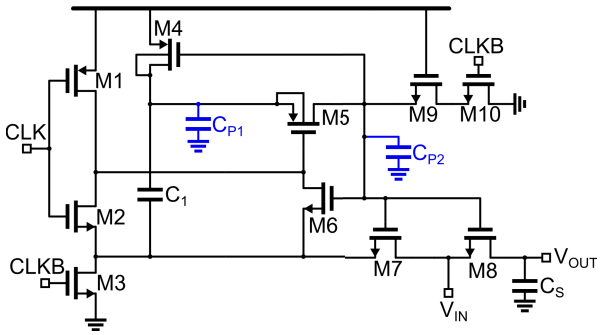

Fig. 1 Conventional bootstrapped switch circuit.

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on can be expressed as

$$V_{G8} = \frac{C_1 + C_{P1}}{C_1 + C_{P1} + C_{P2}} V_{DD} + \frac{C_1}{C_1 + C_{P1} + C_{P2}} V_{IN} \quad (1)$$

where C_{P1} and C_{P2} are the parasitic capacitances of the upper plate node of bootstrapped capacitor C_1 and the gate node of sampling switch M8, respectively. In the sampling phase, the gate-source voltage of M8 can be expressed as

$$V_{GS8} = \frac{C_1 + C_{P1}}{C_1 + C_{P1} + C_{P2}} V_{DD} + \left(\frac{C_1}{C_1 + C_{P1} + C_{P2}} - 1 \right) V_{IN} \quad (2)$$

$$R_{ON8} = \frac{1}{\mu_n c_{ox} \left(\frac{W}{L} \right)_8 (V_{GS8} - V_{TH8})} \quad (3)$$

The foregoing analysis illustrates that the gate-source voltage of sampling switch M8 is approximately equal to V_{DD} only when $C_{P1} + C_{P2} \ll C_1$. This phenomenon also reveals that the parasitic capacitance C_{P1} and C_{P2} are nonlinear sources of the bootstrapped switch. Therefore, parasitic capacitances C_{P1} and C_{P2} need to be reduced during the design process.

3. Proposed bootstrapped switch

Compared with the disadvantages of the conventional bootstrapped switch, the proposed bootstrapped switch primarily reduces the parasitic capacitance of C_{P1} and C_{P2} and fixes the gate-source voltage of the PMOS transistor to $2V_{DD}$. The proposed bootstrapped switch circuit is shown in Figure 2.

In the next step, we analyze the proposed bootstrap switch. For the sake of simplicity, we do not consider the influence of node parasitic capacitance. When CLK = 0 and CLKB = 1, the bootstrapped switch operates in the hold phase, and the input signal, V_{IN}, is sampled at the top plate of negative-voltage bootstrapped capacitor C_2 through transistors MN6 and MP6. The bottom plate of C_2 is discharged to the ground. Transistor M2 is turned off to isolate the gate-source voltage. Because the gate voltage of transistor MP5 is charged to V_{DD}, MP5 is turned off in the holding phase. The working state of the other transistors is the same as that of a conventional bootstrapped switch. In the holding phase, the gate voltage of MP5 and the voltage of the top and bottom plates of the

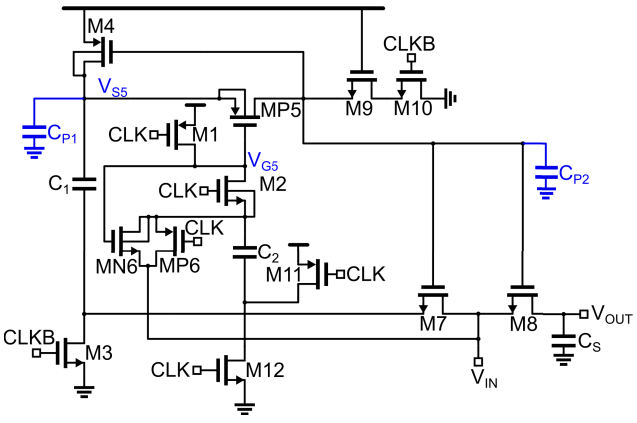


Fig. 2 Proposed bootstrapped switch circuit.

C_2 capacitor can be expressed as follows.

$$V_{G5} = V_{DD} \quad (4)$$

$$V_{TOP\text{-}PLATE} = V_{IN} \quad (5)$$

$$V_{BOTTOM\text{-}PLATE} = V_{DD} \quad (6)$$

When CLK = 1 and CLKB = 0, the bootstrapped switch operates in the sampling phase. Transistors MN6 and MP6 are turned off to isolate the input signal V_{IN}. Because transistor M12 is turned on, the bottom plate of C_2 is discharged to the ground, and the top-plate voltage of capacitor C_2 is bootstrapped to $V_{IN} - V_{DD}$. The connection between the NMOS MN6 substrate and the gate potential requires attention because it is critical in realizing a negative-voltage bootstrap capacitor. The potential of each node can be expressed as follows.

$$V_{BOTTOM\text{-}PLATE} = 0 \quad (7)$$

$$V_{TOP\text{-}PLATE} = V_{IN} - V_{DD} \quad (8)$$

$$V_{GS7} = V_{IN} + V_{DD} - V_{IN} = V_{DD} \quad (9)$$

$$V_{G5} = V_{TOP\text{-}PLATE} = V_{IN} - V_{DD} \quad (10)$$

$$V_{GS5} = V_{IN} + V_{DD} - (V_{IN} - V_{DD}) = 2V_{DD} \quad (11)$$

$$V_{GS8} = V_{IN} + V_{DD} - V_{IN} = V_{DD} \quad (12)$$

The main switching transistors in the signal link are M5 and M7. The ON resistance of the switching transistor and sampling transistor M8 can be expressed as follows.

$$R_{ON5} = \frac{1}{\mu_p c_{ox} \left(\frac{W}{L} \right)_5 (2V_{DD} - V_{TH5})} \quad (13)$$

$$R_{ON7} = \frac{1}{\mu_n c_{ox} \left(\frac{W}{L} \right)_7 (V_{DD} - V_{TH7})} \quad (14)$$

$$R_{ON8} = \frac{1}{\mu_n c_{ox} \left(\frac{W}{L} \right)_8 (V_{DD} - V_{TH8})} \quad (15)$$

In fact, according to formula (3), we must consider the parasitic capacitances C_{P1} and C_{P2}, the sizes of which will affect the sampling linearity of the bootstrap switch.

According to the aforementioned analysis, the proposed bootstrapped switch circuit successfully enables the gate-source voltage of PMOS MP5 to be fixed near $2V_{DD}$. That is, in the case of the same on-resistance, the size of the PMOS MP5 can be designed to be smaller to reduce the parasitic capacitance C_{P1} and C_{P2} so that the linearity of the bootstrapped switch is increased. In addition, compared with the traditional bootstrap switch circuit, the proposed circuit effectively reduces the gate capacitance of the sampling transistor because it removes the transistor M6, as shown in Figure 1. This improves the linearity of the bootstrap switch.

4. Simulation results

The proposed bootstrapped switch was simulated using 0.18-μm CMOS technology. The following main transistor sizes were used in the circuit simulation: M3 = 2 μm/180 nm, M4 = 4 μm/180 nm, M5 = 4 μm/180 nm, MP5 =

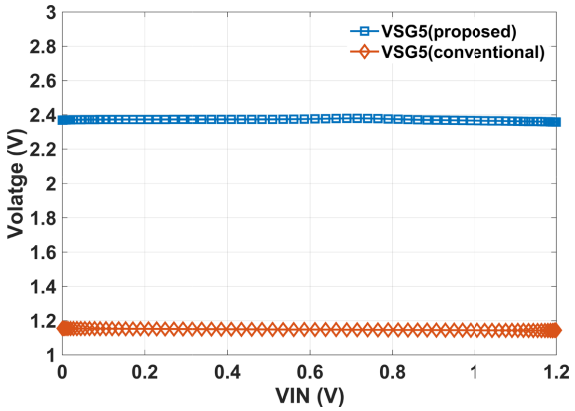


Fig. 3 Transient analysis of the gate-source voltage of the PMOS switch in the signal main link (rail-to-rail input).

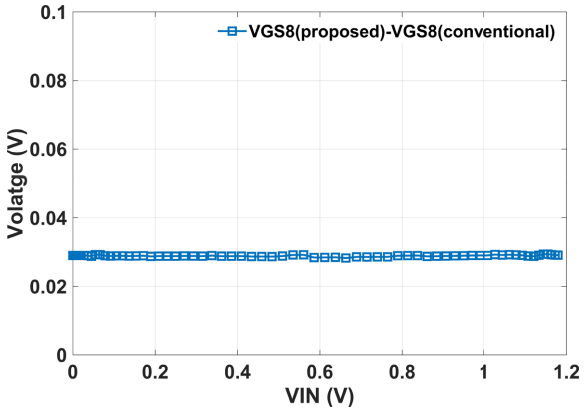


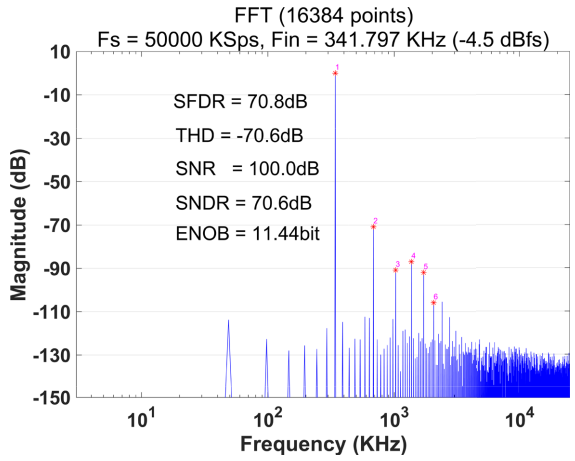
Fig. 4 Simulation of the difference in the gate-source voltage of the sampling switch.

2 µm/180 nm, M6 = 8 µm/180 nm, M7 = 2 µm/180 nm, M8 = 8 µm/180 nm, and M9 = 2 µm/180 nm. As random choices, a supply voltage of 1.2 V and a sampling frequency of 50 MHz with rail-to-rail input amplitude were applied. To detect the linearity improvement more effectively, the values of the bootstrapped capacitor C_1 and the sampling capacitor C_S of the conventional and proposed bootstrapped switches, respectively, were both 1 pF. In the sampling phase, the waveform of the gate-source voltage of the PMOS switch transistor M5 (MP5), shown in Figure 3, indicates that the proposed bootstrapped switch can achieve a gate-source voltage fixed at approximately $2V_{DD}$.

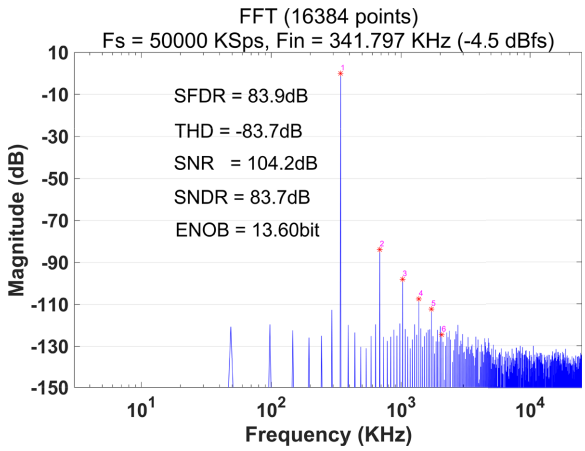
Figure 4 shows the gate-source voltage difference in the sampling transistors in the proposed and conventional bootstrapped switches. Because the proposed bootstrapped switch reduces the gate sampling capacitance, the conduction voltage of the sampling switch is closer to V_{DD}. Thus, the gate parasitic capacitance of the transistor M8 in the proposed bootstrap switch is smaller.

The simulation result shown in Figure 4 is related to the set transistor parameters; the parameters of the transistor can be amplified in equal proportions to obtain more obvious changes. In fact, there is no need to enlarge the size because the analysis of the dynamic characteristics of the bootstrap switch circuit enables a clear conclusion to be drawn.

As a random choice, a rail-to-rail input with an input frequency of 342 kHz and a sampling frequency of 50 MHz



(a)



(b)

Fig. 5 Output spectra of the (a) conventional and (b) proposed bootstrapped switches.

was used. The output spectra of the proposed and conventional bootstrapped switches are shown in Figure 5. The spurious-free dynamic range (SFDR) and the signal-to-noise-plus-distortion ratio (SNDR) of the conventional bootstrapped switch were 70.7 and 70.6 dB, respectively, whereas those of the proposed bootstrapped switch were 82.3 and 83.3 dB, respectively. The SFDR and SNDR of the proposed bootstrapped switch increased by 11.7 and 12.7 dB, respectively, compared with those of the conventional bootstrapped switches.

Figure 6 shows the SFDR and SNDR plots obtained at the differential output for input-signal amplitudes of 0.4, 0.6, 0.8, 1.0, and 1.2 V_{PP}. The proposed method clearly improved both the SFDR and SNDR over the input-signal amplitude.

5. Conclusion

A new bootstrapped switch is proposed to improve the sampling linearity. Simulation is conducted using the 0.18-µm CMOS process. Compared with the conventional sampling switch, the parasitic capacitance of the proposed scheme is approximately 30% lower than that of the conventional structure, which improves the linearity of the bootstrapped

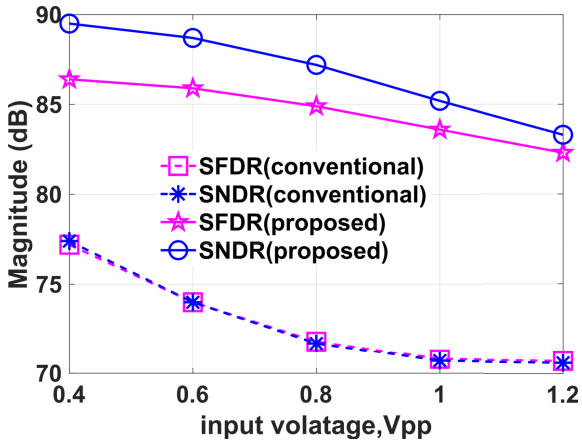


Fig. 6 Simulated dynamic performance versus sampling frequency.

sampling switch circuit. The simulation results show that the SFDR and SNDR of the proposed bootstrapped switch are improved compared with those of the conventional bootstrapped switch.

Acknowledgments

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