A Power Optimized Continuous-Time $\Delta\Sigma$ ADC for Audio Applications

Shanthi Pavan, Nagendra Krishnapura, Ramalingam Pandarinathan, and Prabu Sankar

***Abstract*—We present design considerations for low-power continuous-time $\Delta\Sigma$ modulators. Circuit design details and measurement results for a 15 bit audio modulator are given. The converter, designed in a 0.18 μm CMOS technology, achieves a dynamic range of 93.5 dB in a 24 kHz bandwidth and dissipates 90 μW from a 1.8 V supply. It features a third-order active-*RC* loop filter, a very low-power 4-bit flash quantizer, and an efficient excess-delay compensation scheme to reduce power dissipation.**

***Index Terms*—Analog-to-digital converter (ADC), continuous time, data converter, jitter, oversampling, sigma-delta modulation.**

I. Introduction

DELTA–SIGMA modulation is well suited for high-resolution analog-to-digital conversion since only modest demands are made on the accuracy of passive devices. Oversampling is used to shape the quantization noise from a coarse quantizer outside the signal band. Many such modulators have been reported over the years (see [1] and the references therein). Traditional modulators were discrete-time designs. Recently, there has been a tremendous interest in modulators built using continuous-time loop filters. The reasons why continuous-time delta-sigma modulators (CT-DSMs) are attractive are the following. The bandwidth requirements of the active elements are greatly reduced when compared with a switched-capacitor implementation, thereby resulting in significant power savings. CT-DSMs also offer implicit anti-aliasing.

Power reduction is a key motivator for using CT-DSMs for digitizing low-frequency analog signals. Several implementations targeting the audio range have been reported recently [2]–[6]. The first three of these designs use a single-bit quantizer. Single-bit CT-DSMs have several problems, which can be mitigated by using a multibit quantizer in the loop. In this study, we describe the design of a 15-bit CT-DSM for audio applications. Implemented in a 0.18 μm CMOS technology, the modulator consumes 90 μW from a 1.8 V supply and achieves a dynamic range of 93.5 dB for a signal bandwidth of 24 kHz. The modulator operates with an oversampling ratio (OSR) of 64. The DSM employs several strategies to reduce power consumption. A large input signal swing (3 V peak-to-peak differential) is used to reduce noise requirements of the opamps and offset requirements in the flash analog-to-digital converter (ADC). An appropriate choice of the loop noise transfer function (NTF) results in a performance that is tolerant of comparator offsets. The deleterious effect of extra poles in the loop filter (due to the finite bandwidth of the opamps) is mitigated using a novel excess-delay compensation technique. This enables the use of very low bias currents in the operational amplifiers.

The architectural and circuit details of the modulator form the subject of the remainder of this paper, which is organized as follows. In Section II, we justify the various design choices made in this study. Section III delves into the implementation issues of various circuit blocks used in the modulator. Experimental results from a prototype modulator designed in a 0.18 μm CMOS process are shown in Section IV [7]. Section V gives the conclusions.

II. Choice of Architecture

A single-loop topology was chosen over a MASH design to avoid the complexity resulting from the additional circuitry needed to match the NTF and the digital noise-canceling filter. A third-order NTF was chosen so that a peak signal-to-quantization-noise ratio (SQNR) well above the 92 dB SNR (in a 24 kHz bandwidth) required of the modulator could be achieved. This way, the performance of the design would be limited by thermal noise. We now justify the other architectural choices made in the converter.

A. Single-Bit Versus Multibit Modulation

The advantages of a multibit modulator over a single-bit design are the following.

- *Lower In-Band Quantization Noise*: This results from two factors. A multibit quantizer has inherently low quantization noise—so, for the same NTF, the in-band quantization noise would decrease by 6 dB for every extra quantizer bit. More importantly, a multibit quantizer allows a more aggressive NTF, resulting in a significant reduction of in-band quantization noise. For a third-order single-bit design, stability considerations restrict the out-of-band gain of the NTF to about 1.5 [8]. For an OSR of 64, this results in a peak SQNR of 78 dB. With a four-bit quantizer in the loop and an NTF out-of-band gain (OBG) gain of 2.5, the peak SQNR is about 118 dB.
- *Lower Noise Due to Clock Jitter*: Clock jitter influences the sampling instant of the quantizer, as well as the width of the feedback DAC pulse (assuming NRZ or RZ DACs). It can be shown [9], [10] that the modulation of the width of the DAC feedback pulse is the dominant cause of jitter noise. The effect of jitter can be modeled as an additive sequence

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The authors are with the Department of Electrical Engineering, Indian Institute of Technology (IIT), Madras, Chennai 600 036, India (e-mail: shanthi.pavan@iitm.ac.in).

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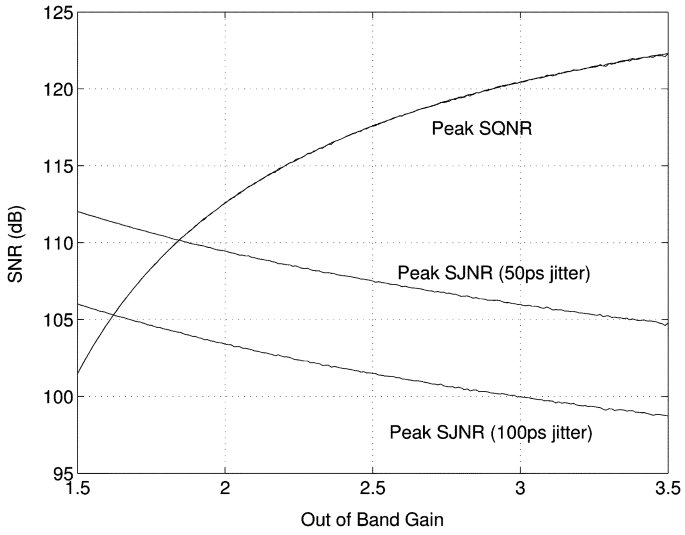

Fig. 1. NTFs with a systematic ±30% change in loop filter bandwidth.

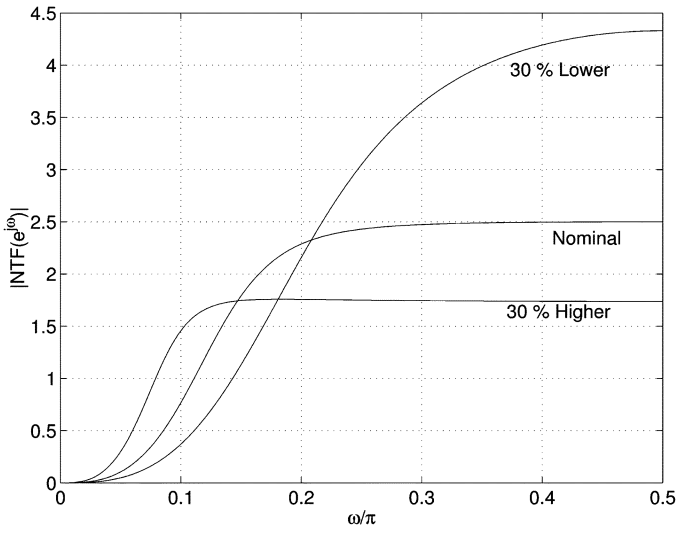

Fig. 2. NTFs with a systematic ±30% change in loop filter bandwidth.

at the input of a jitter-free modulator. For the case of NRZ feedback DACs, the error sequence is given by

$$e_j(n) = [y(n) - y(n-1)]\frac{\Delta T_s(n)}{T} \tag{1}$$

where $y(n)$ is the nth output sample of the modulator, T is the sampling time, and $\Delta T_s(n)$ is the clocking uncertainty of the nth edge of the DAC. Since the difference between successive outputs of the modulator are smaller with a multibit quantizer, the sensitivity to clock jitter is greatly reduced when compared with a single-bit design. A switched-capacitor DAC could also be used for reduced jitter sensitivity—however, this would necessitate a larger slew rate (bias currents) in the first opamp.

- *Lower Slew Rate Requirements in the Loop Filter*: The input to the loop filter is shaped quantization noise. The amplitude of this noise is much lower in a multibit design when compared with a single-bit modulator. It is thus seen that the loop filter opamps need to have a lower slew rate, which translates into a lower power dissipation for the entire modulator.

Based on the discussion above, a single-loop multibit architecture was chosen. A four-bit quantizer was chosen as a reasonable compromise between the benefits offered by multibit operation and the exponential complexity of implementation.

B. Choice of NTF

The NTF influences several aspects of the modulator performance. As discussed earlier, multibit operation enables NTFs with large out-of-band gains, which result in reduced in-band quantization noise. However, a large out-of-band gain results in increased noise due to clock jitter. It can be shown that there is a tradeoff between quantization and jitter noise [11], [12]. Fig. 1 shows the peak SQNR and the peak signal-to-jitter-noise ratio (SJNR) as a function of the out-of-band gain, for a maximally flat NTF. The tradeoff between SQNR and SJNR is clearly visible.

RC time constants in the loop filter vary due to process shifts and changes in ambient temperature. A decrease (increase) in time constants from the nominal value causes the in-band quantization noise to reduce (increase), while simultaneously increasing (decreasing) the out-of-band gain. It is thus seen that time-constant variations in the loop filter either result in a poor rejection of the in-band quantization noise or impact the stability of the modulator. To combat the increased quantization noise when the time constants become larger, the NTF can be chosen so that the in-band noise satisfies the specification under this worst case condition. Such a strategy obviates the need for an *RC* time-constant tuning loop (Fig. 2). A modulator with a large out-of-band gain is more sensitive to the *RC* component variations and excess loop delay. Based on the above conflicting considerations, an out-of-band gain of 2.5 was chosen. In this way, the quantization noise is dominated by the noise due to clock jitter, which in turn is dominated by the thermal noise of the loop filter.

The peak SQNR was simulated to be about 118 dB. The in-band noise due to 100 ps rms clock jitter was calculated to be −103 dBFS. The effect of a systematic *RC* time-constant variation on the in-band SQNR and the maximum stable amplitude (MSA) are shown in Fig. 3.

Fig. 4 shows the quantizer output when the loop-filter time constants are 30% lower than the nominal value. Simulations show that the worst case code-to-code jump is 4 LSB, though this happens infrequently. The SJNR is 98 dB for 100 ps rms jitter.

C. Loop Filter Architecture

A "cascaded integrators with feedforward summation" architecture was chosen to implement the loop filter. Such a structure has the following advantages when compared with the more common multiple-feedback approach.

- *Reduced DAC Area*: In our implementation, a resistive-feedback DAC was used. This occupies a large chip area (in spite of high-resistivity poly resistors with a sheet resistance of about 1 kΩ/square) due to the impedance

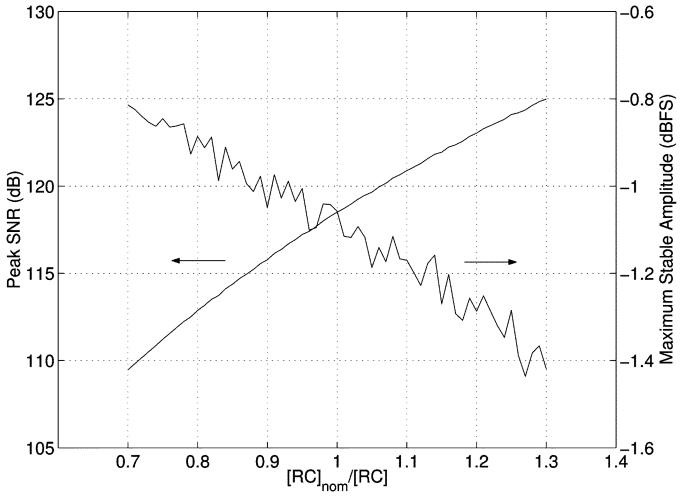

Fig. 3. Effect of systematic *RC* time-constant deviation on the in-band SQNR and MSA of a third-order NTF with a nominal OBG of 2.5.

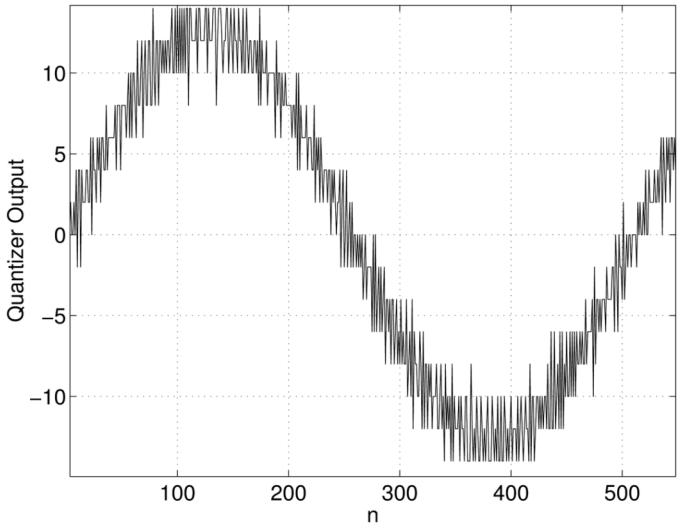

Fig. 4. Quantizer output when the loop-filter time constants are 30% lower than the nominal value. The LSB size of the quantizer is 2.

levels used in the modulator. A multiple-feedback loop filter would need three DACs. Typically, the impedance levels in the second and third integrators are chosen to be several times those in the first integrator to reduce power dissipation. This means that the feedback DACs feeding into the second and third integrators would be much larger and occupy a large area.

- *Capacitor Sizes* : Another issue with a multiple-feedback loop filter is explained with the help of Fig. 5, where the block diagrams of modulators with an OBG of 2.5 and a sampling rate of 1 Hz are shown. Part (a) of the figure shows a feedforward design, where the integrator unity gain frequencies are scaled so that the peak signal swing of the first integrator (the one with a unity gain frequency of ω_1) is one half that of the other two integrators. This way, the first integrator limits the last, thereby aiding recovery of the modulator from overload. No additional provisions were made to reset the integrating capacitors. Fig. 5(b) shows the unity gain frequencies for a multiple-feedback loop-filter design. The value of the integrating resistor in the first integrator in both designs is governed by thermal noise considerations. The second and third integrators can, in principle, be implemented with much larger resistors and the sizes of the corresponding capacitors can be reduced. Notice that the first integrator is the "fastest" in a feedforward design, while the first integrator is the "slowest" in the multiple-feedback modulator. Thus, the integrating capacitor of the first integrator in a feedforward loop filter will be much smaller than that in a multiple-feedback modulator.

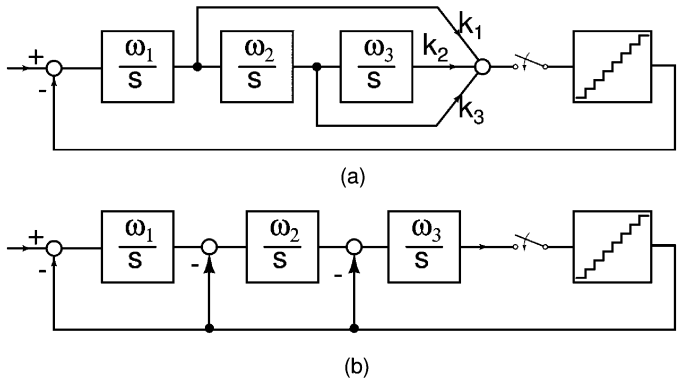

Fig. 5. Feedforward and distributed feedback modulators—the out-of-band gain is 2.5, and the sampling rate is 1 Hz. (a) $\omega_1 = 2.67, \omega_2 = 2.08, \omega_3 = 0.059$. (b) $\omega_1 = 0.34, \omega_2 = 0.71, \omega_3 = 1.225$.

Noise and distortion considerations necessitate the use of large bias currents in the first opamp. In the first integrator, therefore, poles resulting from the finite bandwidth of the opamp can be expected to be at high frequencies. This can be used to advantage in the feedforward design, since the first integrator has the highest unity gain frequency and needs to have the least "delay." In a multiple-feedback design, steps must be taken to ensure that the extra poles in the last integrator are not so low that loop stability is impacted. It is thus seen that the large bias currents in the first opamp, which are needed anyway for noise reasons, are more efficiently used in a feedforward loop filter. The resulting peaking in the signal transfer function (STF) was not an issue in this particular design.

III. Circuit Design

A. Loop Filter

A schematic of the loop filter is shown in Fig. 6. Weighted addition of the integrator outputs is performed using a summing amplifier. The first integrator uses an opamp with a pMOS input stage for low $1/f$ noise. The other integrators and the summing amplifier use operational amplifiers with nMOS input pairs, whose design is discussed in Section III-B. The input-referred noise of the loop filter is dominated by the thermal noise from the input and DAC resistors and the input-referred noise of the first opamp. The first integrator uses (polysilicon) resistors of 100 kΩ, while larger resistors are used in subsequent integrators. The third integrator has the largest time constant, and using a large integrating resistor has the additional benefit of reducing the area of the third capacitor.

The poles in the opamps introduce excess delay in the loop filter, which can potentially cause instability in the modulator.

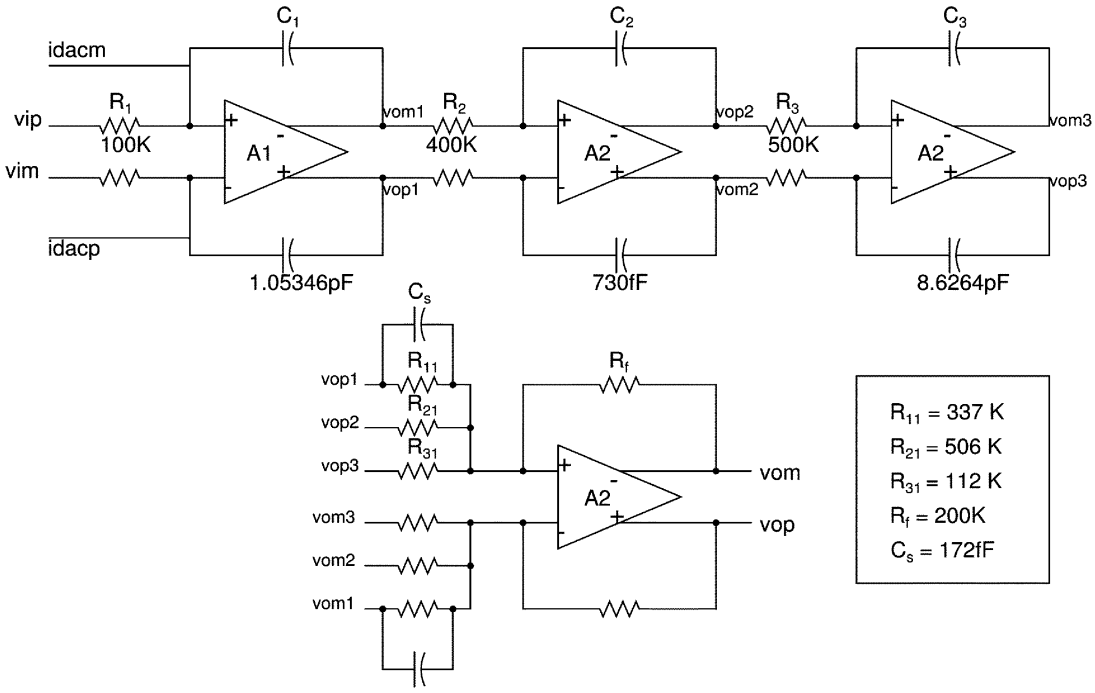

Fig. 6. Loop filter.

One way of mitigating this problem (at the expense of power dissipation) is to use wideband opamps. An alternative approach is to use low-speed (power) opamps and compensate for the delay introduced by the loop filter. A conventional way of combating excess delay is to have a direct path around the quantizer using a second DAC, as shown in Fig. 7(a). This needs an extra DAC, which occupies a large area. In this study, we use a feed-in capacitor C_x [Fig. 7(b)] to accomplish the same task. With ideal opamps, the equivalent gain of the direct path around the quantizer is seen to be $R_f C_x / R_i C_1$.

A CAD routine and methodology were developed to determine the relative weighting factors and C_x required in the summing amplifier to realize the desired NTF. The routine accounts for the frequency response of the operational amplifiers and the (small) excess delay introduced by the ADC and the DEM logic.

B. Operational Amplifiers

The first integrator determines the overall noise and linearity of the modulator. The circuit schematic of the opamp used in the first integrator is shown in Fig. 8 [13]. It is a two-stage design, with a first stage using a pMOS input pair with long channels to lower input-referred $1/f$ noise, and a class-AB second stage. The opamp is Miller-compensated using R_z and C_c, as shown in Fig. 8(a). The value of C_c is chosen to be 150 fF. It can be shown that a two-stage design is more effective in reducing the in-band noise arising from opamp nonlinearity when compared with a single-stage opamp [14].

The CMFB circuit that stabilizes the output level of the first stage is shown in Fig. 8(b). The quiescent output voltage at nodes $o1p$ and $o1m$ (which is also the gate–source voltage of *M6–M61* and *M8–M81*) sets the quiescent currents in the second stage. To set the output quiescent currents accurately, the common-mode reference *vref* is derived from a diode-connected transistor biased with a fixed current. Since the signal swings

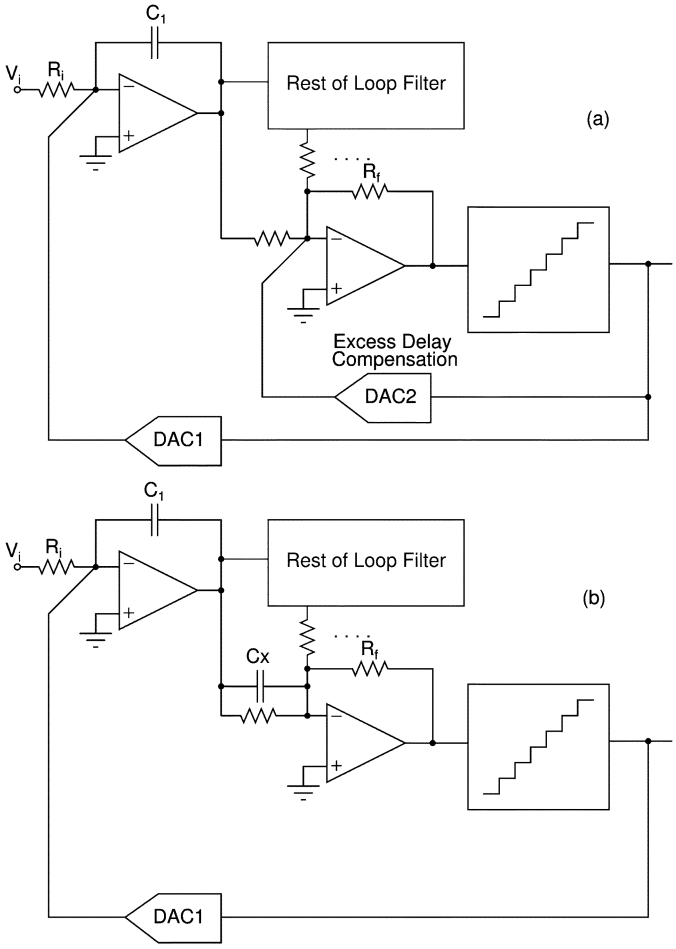

Fig. 7. Excess delay compensation. (a) Conventional. (b) Proposed.

at $o1p$ and $o1m$ are modest, the linearity of the common-mode detector is not critical. The 70 fF capacitors bypass the active

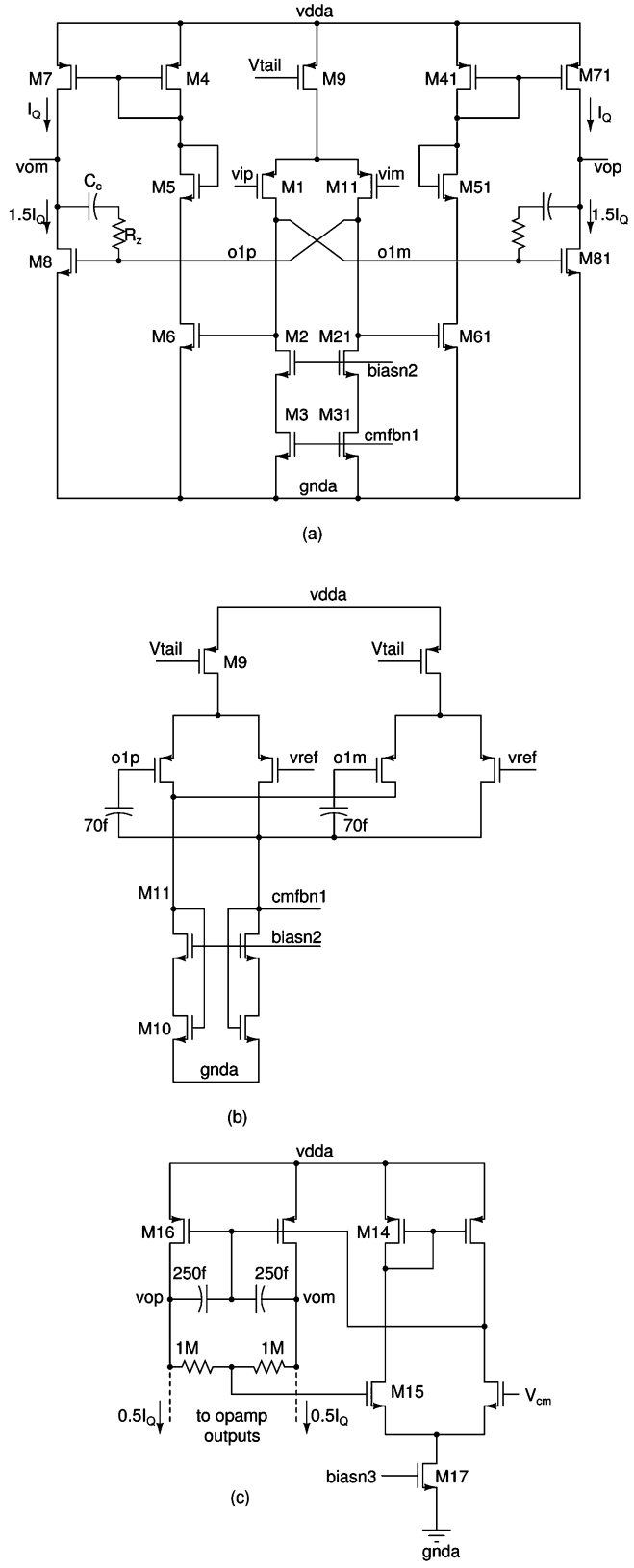

Fig. 8. Operational amplifier used in the first integrator. (a) Main amplifier. (b) Common-mode feedback (CMFB) for the first stage. (c) Second-stage CMFB circuit.

common-mode detector for high frequencies and help stabilize the loop. The first stage uses a 4 μA tail current.

Since the output swings of the opamp are large, linear operation of the CMFB mechanism is ensured by using resistive averaging to detect the output common mode [Fig. 8(c)]. The 250 fF capacitors provide a fast high-frequency path, bypassing the resistive common-mode detector and the error amplifier.

At high frequencies, where the compensation capacitors C_c can be considered as shorts, the common-mode output impedance of the opamp in Fig. 8(a) consists of the parallel combination of the positive resistance of the diode-connected (through C_c) transistors *M8* and *M81* and the negative resistance formed by the loop *M6-M4-M7* and *M61-M41-M71*. If equal quiescent currents are used in *M8* and *M7*, this impedance is infinite. In the presence of mismatches, it is possible for the common-mode output impedance to have a negative real part and lead to instability. To prevent this, quiescent currents in the lower transistors *M8* and *M81*, which contribute to the positive resistance, are made 1.5 times larger than quiescent currents in the upper transistors *M7* and *M71*. The remainder of the quiescent current is provided by the CMFB circuitry. This technique ensures stability and reliable operation of the CMFB loop. Quiescent current through each output branch (*M8* and *M81*) is 1.2 μA.

The schematic of the operational amplifier used in the second and third integrators and the summing block is shown in Fig. 9. An nMOS input pair design is used to reduce power dissipation. The tail current in the input pair is 750 nA. It is thus seen that the power dissipation in this opamp is much smaller than that in the opamp of Fig. 8. $C_c = 100$ fF. The first-stage CMFB circuit is shown towards the left of the figure. An arrangement similar to the circuit of Fig. 8(c) is used to stabilize the output common-mode voltage of the second stage.

C. Flash ADC

The block diagram of the 4-bit flash ADC used in this study is shown in Fig. 10. It consists of 15 differential comparators, a resistor ladder, and a digital backend. The input range of the converter is [−1.5 V, 1.5 V] differential, resulting in a nominal step size of 187.5 mV. This greatly relaxes the offset requirements of the comparators. The circuit diagram of the comparator and the corresponding clock waveforms are shown in Fig. 11(a) and (b), respectively. The comparator operates as follows.

When *LC* is high, the nodes X and Y are connected to ip and im through two coupling capacitors C_b, which have been charged to $V_{\rm refp} - V_{\rm cm}$ and $V_{\rm refm} - V_{\rm cm}$, respectively. Thus, the differential voltage between nodes X and Y at the end of the on-phase of *LC* is $(V_{\rm ip} - V_{\rm im}) - (V_{\rm refp} - V_{\rm refm})$. L goes high after *LC* goes low. In this phase, the back-to-back inverters formed by *M1, M2, M3,* and *M4* are activated, thereby regenerating the difference between the voltages at nodes X and Y. After allowing for some regeneration time, the decision made by the latch is held on C^{2}MOS inverters, which are clocked by Ld , which goes low before L goes low. Even after L goes low, the nodes X and Y will remain at $V_{\rm dd}$ or ground. Hence, a small reset phase LR is necessary to clear the latch of its prior decision. At the end of this phase, the absolute potentials at X and Y are brought to $V_{\rm dd}/2$. Note that, when L is high, the coupling capacitors C_b are charged to $V_{\rm refp} - V_{\rm cm}$ and $V_{\rm refm} - V_{\rm cm}$.

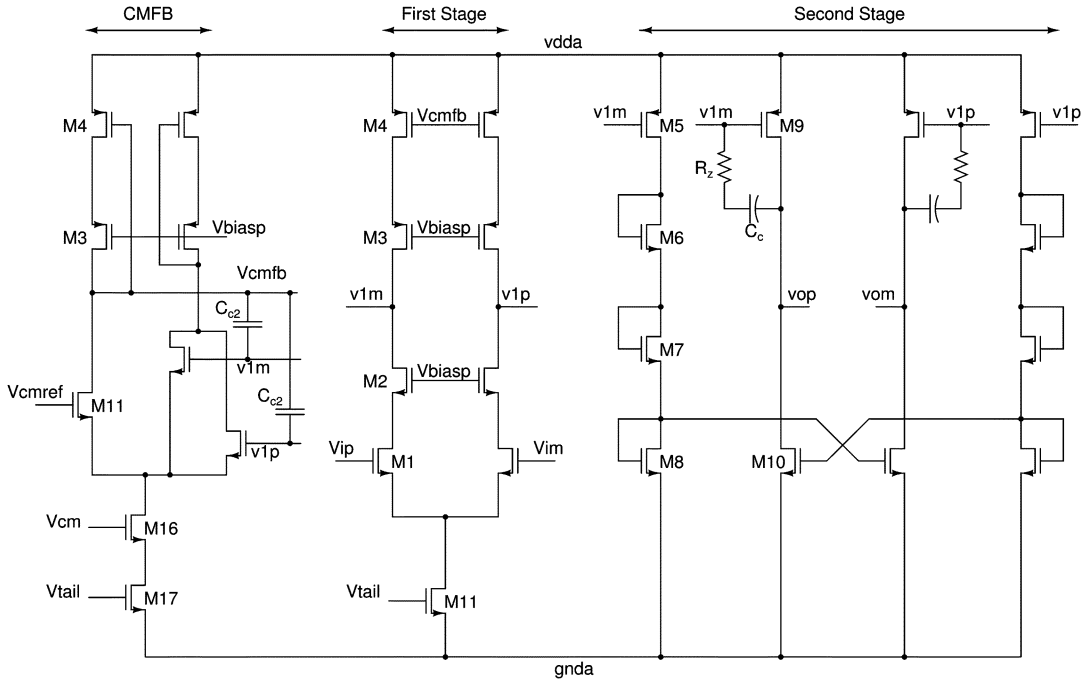

Fig. 9. Schematic of the operational amplifier used in the second and third integrators and the summing amplifier.

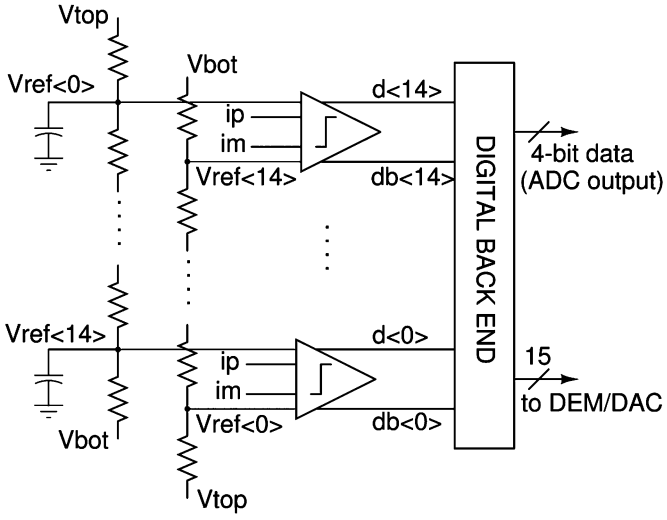

Fig. 10. Block diagram of the flash quantizer.

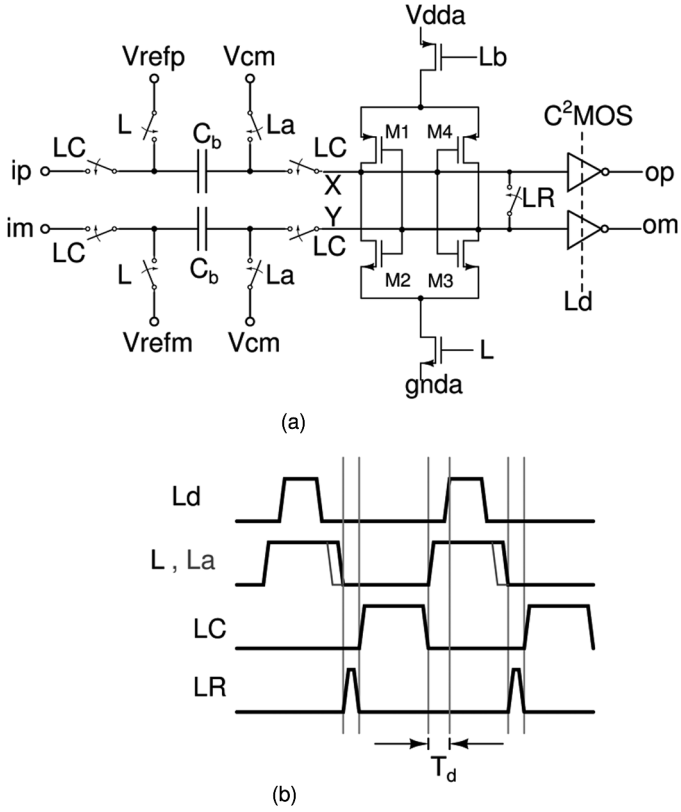

Fig. 11. (a) Comparator schematic. (b) Clock waveforms.

To prevent reference-dependent charge injection on to the coupling capacitors, their "bottom" plate is turned off first, using a slightly advanced version of L, denoted by La. The sampling instant of the ADC is the falling edge of *LC*, and the output is available at the rising edge of Ld. The latency of the ADC is denoted as $\mathrm{T_d}$ in Fig. 11(b). The estimated 3σ random offset of the comparator was about 50 mV.

The comparator of Fig. 11(a) has several advantages, making it an appropriate choice in the context of a $\Delta\Sigma$ modulator. Note that it consumes no static power. The dynamic offset of the latch is also small, since nodes X and Y are biased at midsupply. During the *LC* phase, the coupling capacitors C_b share their charge with the small parasitic capacitances at nodes X and Y. Hence, only this small amount of charge has to be replenished when L is high. Thus, large resistors can be used in the resistor ladder, reducing power dissipation. Many flash converters used in $\Delta\Sigma$ modulators use offset-cancelled preamplifiers to reduce latch offset. This strategy increases area and power dissipation.

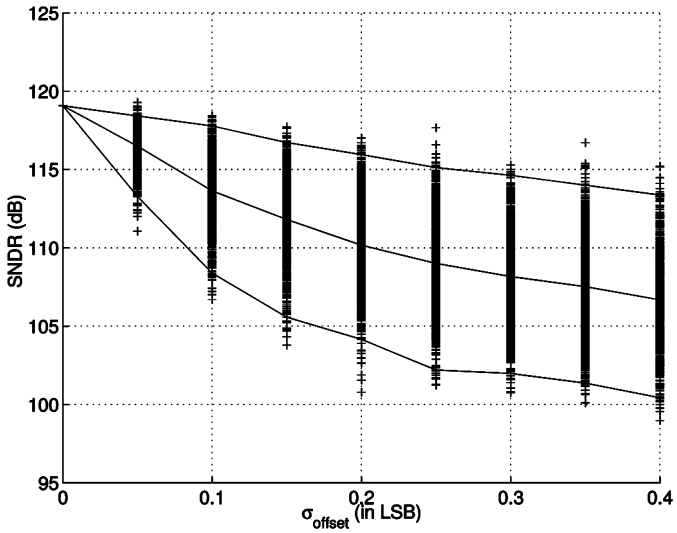

Fig. 12. Effect of comparator random offset on in-band SNDR—for each level of offset, 1000 trials were simulated. The lines show the modulators with the best 1% SNDR, mean SNDR, and the worst 1% SNDR, respectively.

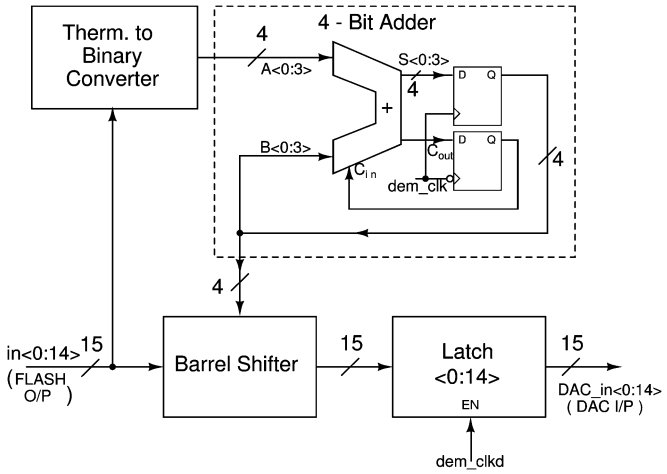

Fig. 13. Digital back-end of the flash ADC and DEM logic.

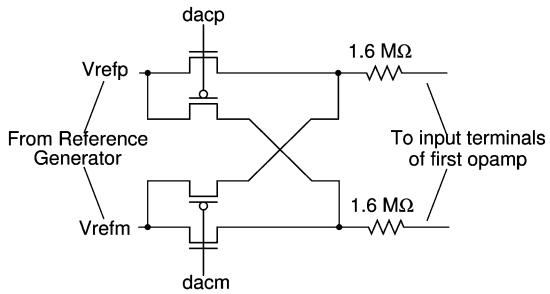

Fig. 14. DAC unit element.

Cancelling the offset in every clock cycle also necessitates large bias currents in the preamplifiers. In this study, we eliminate the preamplifier by using a large LSB size. Further, the 4-bit ADC output code is generated from the thermometer code by summing the number of 1's in the thermometer code. This makes the quantizer characteristic inherently monotonic.

The predominant nonideality in the flash converter is the deviation in quantizer thresholds from the ideal values due to device mismatch in the comparators. It is usually assumed that this is not a serious issue since nonidealities in the flash ADC are noise shaped by the loop. However, ADC threshold deviations increase the mean square error introduced by the quantizer, so it should be expected that the performance of the modulator will be degraded by comparator offsets. To study this effect, the modulator was simulated for various levels of Gaussian distributed offsets in the comparators. One thousand trials for each level of offset were run. Fig. 12 shows the results. The lines represent the mean, the best, and the worst 1% of the SNDRs. It is thus seen that, to achieve a 15 bit performance from the modulator, random offsets in the comparator with a standard deviation of up to 0.4 LSB can easily be tolerated, as long as the characteristic of the quantizer is monotonic.

D. Digital Back-End and Dynamic Element Matching (DEM) Logic

A block diagram of the digital back-end of the flash ADC and the DEM logic is shown in Fig. 13. The thermometer coded output of the flash ADC is converted into a binary code, which is also the modulator output. As mentioned in the previous subsection, the binary code is generated by summing the number of ones in the thermometer output of the flash ADC. The summing is done by tree-structured combinational logic.

In this study, data weighted averaging (DWA) [15] is used to shape mismatch noise from the feedback DAC away from the signal band. The DWA algorithm is implemented using the accumulator (shown in dotted lines in the figure), whose outputs control a barrel shifter, which in turn drive the DAC unit elements. To prevent distortion due to data-dependent delays in the combinational logic, the DAC control signals are synchronized with the clock.

E. Feedback DAC and Reference Generation

The feedback DAC consists of resistive unit elements, each with a value of 1.6 MΩ. The width of these resistors is chosen to be as small as possible to reduce parasitic capacitance which causes excess delay in the loop. Matching requirements are greatly relaxed, thanks to DEM. Fig. 14 shows the unit element of the DAC. The resistors are driven by differential reference voltages $V_{\rm refp}$ and $V_{\rm refm}$. The other ends of the resistors are connected to the virtual ground terminals of the first integrator. The polarity of the current flowing into the loop filter is determined by the control bits.

The on-chip reference generation circuitry for the DAC is shown in Fig. 15. An external reference voltage referenced to ground is converted into a set of differential currents I as shown in Fig. 15(a). These currents converted into differential voltages using a transimpedance amplifier, as shown in Fig. 15(b). Note that the DC current drawn out of $V_{\rm refp}$ is $(15/R)(V_{\rm refp} - V_{\rm cm})/R_{\rm dac}$. To compensate for this, a fixed current of the same value is pumped into the $V_{\rm refp}$ node. Similarly, a sink that draws a current of $(15/R)(V_{\rm cm} - V_{\rm refm})/R_{\rm dac}$ is connected to $V_{\rm refm}$. Thus, the DC current supplied by the opamp becomes very small (the mismatch between the fixed current and the current drawn by the DAC). This current causes a small DC drop across R_x

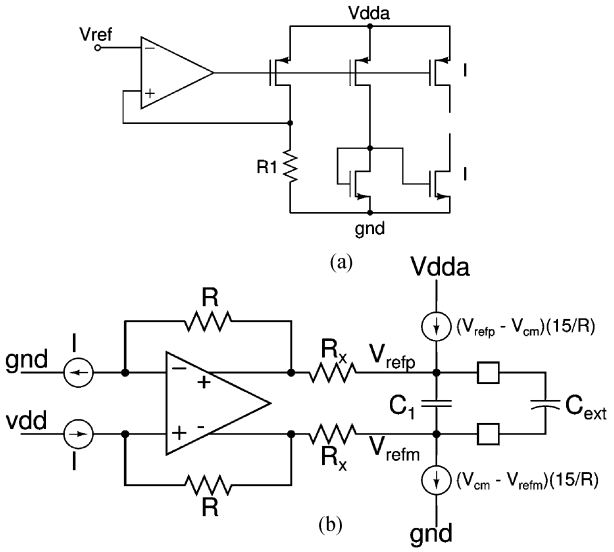

Fig. 15. Simplified schematic of the reference generation circuitry.

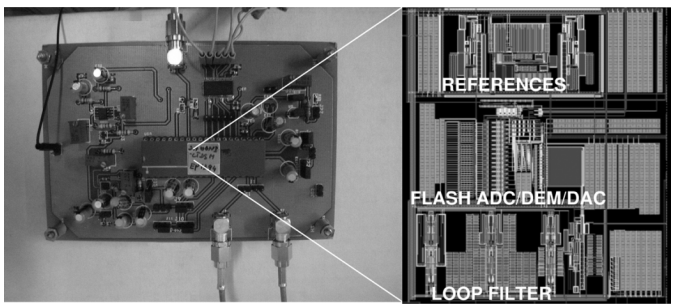

Fig. 16. Test board and chip layout.

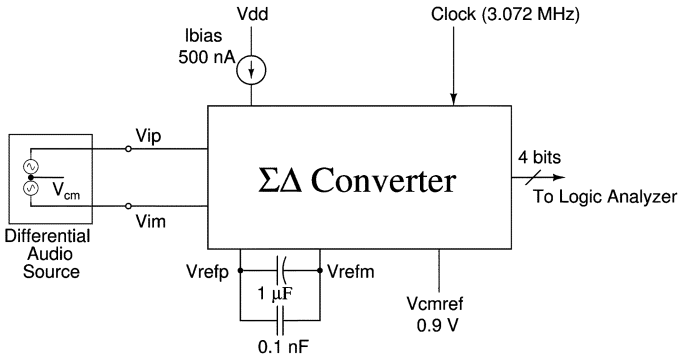

Fig. 17. Modulator test setup.

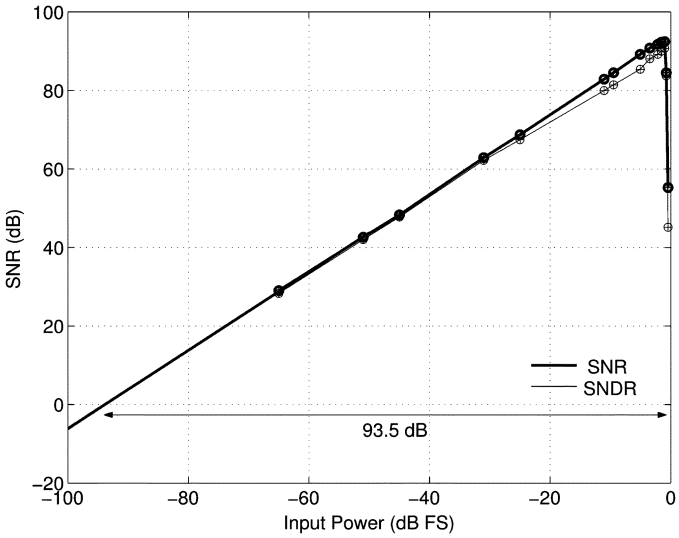

Fig. 18. Measured SNR and SNDR—the dynamic range is 93.5 dB.

and can result in a gain error in the converter. The $1/f$ and thermal noise of the reference path is filtered by a low-pass filter formed by R_x and $C_{\text{ext}}+C_1$. In our design, C_{ext} was a 1 μF external capacitor. R_x and C_1 were chosen to be 5 KΩ and 55 pF, respectively.

The reference ladder in the flash ADC is driven by an arrangement similar to that in Fig. 15(b). An external capacitor is not necessary, since the performance of the modulator is insensitive to noise in the flash converter. The DAC and flash reference generation circuits are kept separate to prevent any potential corruption of DAC reference voltages.

IV. Measurement Results

The third-order continuous-time $\Delta\Sigma$ ADC was fabricated in a 0.18 μm CMOS process through Europractice. Fig. 16 shows the two-layer test board used for characterization and the layout of the integrated circuit. The die area is about 0.72 mm^2.

An Audio Precision (SYS-2722) differential signal source and a Tektronix AWG2021 clock source were used to characterize the ADC as shown in Fig. 17. It was not possible to synchronize the clock source with the input sinewave. Five million samples from the modulator output were captured using an Agilent 16500C Logic Analyzer. The data were processed offline on a PC. Thanks to the large number of samples captured, leakage effects during power spectral density estimation (due to the source and clock not being in sync) can be minimized by an appropriate choice of the data window. In this study, a 16 K Blackman–Harris window was used. The side-lobes due to this window are much lower than those due to (the more commonly used) Hann window. The main-lobe width is larger, but this is not a problem due to the large number of bins in the frequency range of interest.

No idle tones were seen for small DC inputs. Fig. 18 shows the measured SNR and SNDR of the modulator. The peak SNR and SNDR are 92.5 dB and 90.8 dB, respectively. The measured dynamic range of the modulator is 93.5 dB. Thanks to the 4-bit quantizer employed in the loop, the modulator is stable for signals as large as −0.7 dBFS. The authors believe the effects of

TABLE I
Summary of Measured ADC Performance

Signal Bandwidth/Clock Rate	24 kHz / 3.072 MHz
Quantizer Range	3 $V_{pp,diff}$
Input Swing for peak SNR	-1 dBFS
Dynamic Range/SNR/SNDR	93.5 dB/92.5 dB/90.8 dB
Active Area	0.72 mm^2
Process/Supply Voltage	0.18 μm CMOS/1.8 V
Power Dissipation (Modulator)	90 μW
Power Dissipation (Modulator and Reference Buffers)	121 μW
Figure of Merit	0.049 pJ/level

TABLE II
COMPARISON WITH OTHER CONTINUOUS-TIME ΣΔ MODULATORS

Reference	Bandwidth	OSR	Dynamic Range	Peak SNR	Power	Technology	Supply Voltage	$\mathrm{FOM_{DR}}$ (pJ/level)	$\mathrm{FOM_{SNR}}$ (pJ/level)
[2]	25 kHz	48	80 dB	73 dB	135 μW	0.35 μm	1.5 V	0.33	0.74
[3]	25 kHz	48	81 dB	66 dB	250 μW	0.35 μm	1.5 V	0.55	3.07
[5]	20 kHz	128	106 dB	99 dB	18 mW	0.35 μm	3.3 V	2.76	6.18
[6]	20 kHz	300	95 dB	77 dB	2.2 mW	0.065 μm	1.5 V	1.20	9.51
[16]	3.4 kHz	64	80 dB	80 dB	210 μW	0.50 μm	2.2 V	3.78	3.78
This work	24 kHz	64	93.5 dB	92.5 dB	90 μW	0.18 μm	1.8 V	0.049	0.054

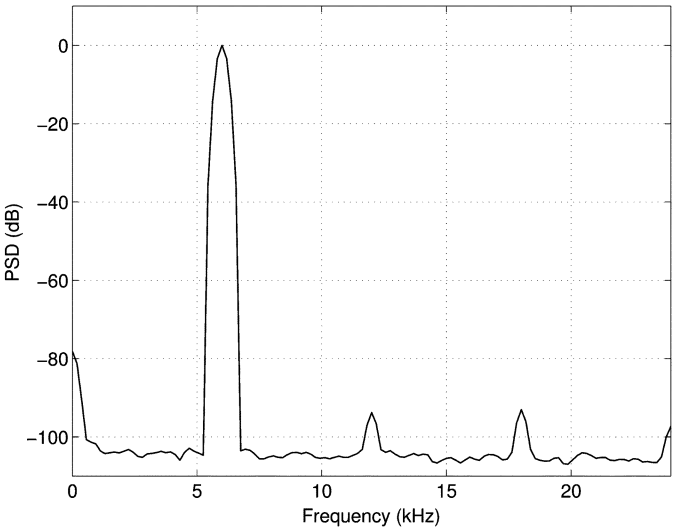

Fig. 19. In-band spectrum for a 6 kHz input. The amplitude is that which results in the maximum SNR.

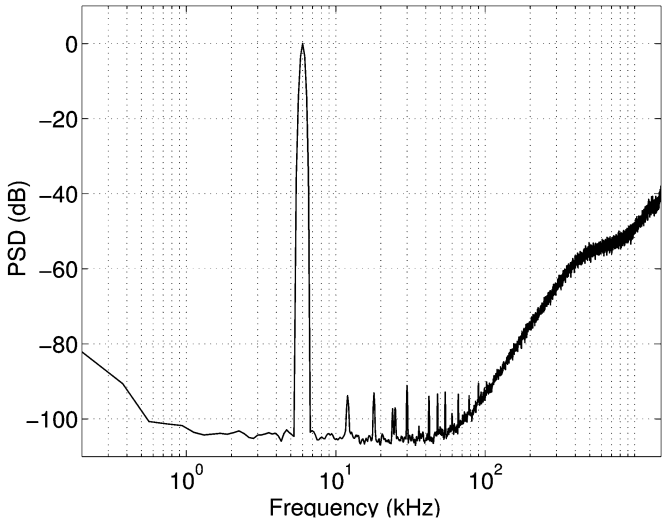

Fig. 20. Complete spectrum for a 6 kHz input.

quantization noise and noise due to clock jitter are completely dominated by the circuit noise. There was no provision in the test chip to turn off the DEM logic. The distortion seen in measurements is most likely due to the switching of the feedback DAC.

The in-band spectrum when the modulator is excited by a 6 kHz tone at the maximum stable amplitude is shown in Fig. 19. It is seen that the harmonics are about 94 dB below the fundamental, and no nonharmonic tones are observed above the noise floor. Fig. 20 shows the complete spectrum. A summary of measured performance is given in Table I. The figures of merit of the converter are determined as [2]

$$\mathrm{FOM_{DR}} = \frac{P}{2 \times f_B \times 2^{(\mathrm{DR}-1.76)/6.02}} \tag{2}$$

$$\mathrm{FOM_{SNR}} = \frac{P}{2 \times f_B \times 2^{(SNR-1.76)/6.02}} \tag{3}$$

where P, f_B, DR, and SNR denote the power dissipation, signal bandwidth, dynamic range (in dB), and peak SNR (in dB), respectively. Our converter achieves $\mathrm{FOM_{DR}} = 0.049$ pJ/level and $\mathrm{FOM_{SNR}} = 0.054$ pJ/level, making it the most power-efficient audio modulator to be reported.

A. Comparison With Other Works

Table II compares the performance of several continuous-time modulators presented in the literature with the ADC presented in this work. They are designed in different technologies with varying supply voltages which makes a true comparison difficult, but we nevertheless use the FOM to assess power efficiency. The modulators presented in [2] and [3] are single-bit multiple feedback designs. The ADC presented in [5] employs a four-bit quantizer in the loop and has a hybrid continuous-time and switched-capacitor loop filter. Apart from the modulator, the chip also includes *RC* time-constant tuning loops and a "clock clean-up" loop that makes the performance insensitive to clock jitter. The work in [6] presents a design in a 65 nm CMOS process. It employs a "tracking ADC" to reduce the number of comparators in the 4-bit quantizer. Due to the high OSR, the power efficiency is low. The modulator in [16] employs a single-bit modulator and is intended for voice applications. When compared with the ADCs cited above, it is seen that the ADC in this work achieves a drastic reduction in power consumption, thanks to the architectural and circuit techniques employed.

V. CONCLUSION

We presented design considerations for low-power continuous-time delta-sigma converters. Use of a multibit quantizer along with a proper choice of NTF can result in a modulator performance that is relatively immune to loop-filter time-constant variations, clock jitter, and comparator offsets. A cascade of integrator structures with feedforward design was chosen to implement the loop filter. An active-*RC* implementation with class-AB opamps and a resistive-feedback DAC was chosen to reduce noise and power dissipation. The effect of parasitic poles

in the loop filter were mitigated by using a new excess-delay compensation technique. These techniques were applied to the design of an audio-frequency third-order CTDSM implemented in a 0.18 μm CMOS technology. The ADC has a measured dynamic range of 93.5 dB while dissipating 90 μW from a 1.8 V supply, achieving the lowest energy consumption per level resolved.

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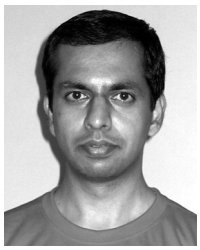
Shanthi Pavan was born in 1973. He received the B.Tech. degree in electronics and communication engineering from the Indian Institute of Technology (IIT), Madras, in 1995, and the M.S. and Sc.D. degrees from Columbia University, New York, in 1997 and 1999, respectively.

From 1997 to 2000, he was with Texas Instruments, Warren, NJ, where he was involved with high-speed analog filters and data converters. From 2000 to June 2002, he worked on microwave ICs for data communication with Bigbear Networks, Sunnyvale, CA. Since July 2002, he has been with the Electrical Engineering Department, IIT, Madras, where he is an Assistant Professor. His research interests are in the areas of high-speed analog circuit design and signal processing.

Dr. Pavan serves on the editorial board of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS. He has been an associate editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS, and is a recipient of the Young Engineer Award from the Indian National Academy of Engineering.



Nagendra Krishnapura received the B.Tech. degree from the Indian Institute of Technology (IIT), Madras, in 1996, and the Ph.D. degree from Columbia University, New York, in 2000.

He is an Assistant Professor with IIT, Madras. His research interests are analog and RF circuits. He has worked at Bell Laboratories, Celight Inc., Multilink Technology Corporation, and Vitesse Semiconductor on high-speed analog-to-digital converters, filters, adaptive equalizers, and high-speed serial links. He joined IIT, Madras, in 2005, where he is involved in teaching and researching analog circuits and systems.

Ramalingam Pandarinathan received the B.E. degree in electronics and telecommunications engineering from Mumbai University, Mumbai, India, in 2004, and the M.Tech. degree in microelectronics and VLSI design from the Indian Institute of Technology, Madras, in 2006.

He is currently with SiRF Technology India, Bangalore, where he is involved in the design of data converters. His interests are in the areas of analog-to-digital converters and signal processing.

Prabu Sankar received the B.Eng. degree from the College of Engineering, Guindy (Anna University), Chennai, India, in 2005. He is currently working toward the M.S. degree at the Indian Institute of Technology, Chennai.

His research interests are in the area of oversampling data converters.