Analog Integrated Circuits and Signal Processing (2020) 103:345–353
https://doi.org/10.1007/s10470-020-01641-w

Robust linear sampling switch for low-voltage SAR ADCs

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Received: 15 September 2019 / Revised: 16 January 2020 / Accepted: 20 March 2020 / Published online: 4 April 2020

Abstract
This paper presents a linear sampling switch for low-voltage successive-approximation register (SAR) analogue-to-digital converters (ADCs) operating at a frequency of tens of MHz. The proposed switch employs a bootstrapped transmission gate, where the bulk voltages are generated internally to minimize variations in the threshold voltage of transistors with input signal amplitude. Thus, ensuring almost constant and low ON-resistance (R_{ON}) over complete input signal range without using wide transistors, charge pumps, or both, at low supply voltages. The proposed switch was designed using standard 65 nm CMOS technology. The post-layout simulations have shown a signal to noise and distortion ratio (SNDR) of 87.81 dB, a spurious-free dynamic range (SFDR) of 90 dB and a total harmonic distortion (THD) of −91.5 dB at a sampling frequency and supply voltage of 100 MHz and 0.8 V, respectively. In addition, the switch has shown a maximum variation of 1% in R_{ON} over input signal amplitude at different process corners and temperature, which is low compared to other sampling switches reported in the literature.

Keywords Robust sampling switch · Linear on-resistance · Low-voltage SAR ADCs

1 Introduction

SAR ADCs operating at a sampling frequency of tens of Mega-Hertz and with moderate resolutions (up to 10-bits), are widely employed in wireless receivers [1–3] due to its high-energy efficiency and switching intensive nature. The sampling switch is one of the important blocks of the SAR ADC since it samples the input analog signal (V_{IN}) and holds the sampled value for the quantization process. However, the ON-resistance (R_{ON}) of the switch is a function of over-drive voltage (for constant device parameters and aspect ratio) of the MOS (metal-oxide semiconductor) transistor, which varies with the amplitude of V_{IN} and therefore, leading to non-linear errors. As the technology scales down, the threshold voltage (V_{TH}) of transistors does not scale proportionately with the supply voltages, which yields to small over-drive voltage. Therefore, wider devices are employed to minimize R_{ON}. However, wide transistors limit the operating speed of the switch, as they have large parasitics. In addition, they promote charge injection [4] when MOS transistor changes the state from ON to OFF, thus, degrading the signal-to-noise ratio (SNR) of the switch at low supply voltages. The effect of R_{ON} variations, charge injection, clock feed-through are critical factors, which degrade the performance of the switch [5].

The overdrive voltage of a MOS transistor is expressed as the difference between the gate to source voltage (V_{GS}) and V_{TH}. Both these voltages are a function of V_{IN}. Since R_{ON} is a function of overdrive voltage, its variations with V_{IN} are unavoidable. Bootstrapped switches, presented in [6, 7], are meant to boost the gate voltage of MOS transistors and makes V_{GS} constant but, the variations of V_{TH} with V_{IN} are not compensated. Besides, charge injection becomes critical at low supply voltages, which degrades the performance. To minimize these limitations, a bootstrapped transmission gate (TG) switch was proposed in [8, 9]. This switch minimizes charge injection, variation in R_{ON} due to V_{GS} as it compensates for V_{TH} variations with

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V_{IN}, only for the p-channel metal-oxide-semiconductor (PMOS) devices. In addition, all these switches employ clock booster/ charge pumps for their operation, which adds to power consumption and elevate the active area. N-channel metal-oxide semiconductor (NMOS) transistor bootstrapped switch without charge pumps had been presented in [10]. However, the problems of V_{TH} variations with V_{IN} and charge injections are not addressed. Therefore, this paper proposes a bootstrapped TG switch, which minimizes the variations of V_{TH} with V_{IN}, for both PMOS and NMOS devices, hence, ensuring almost constant R_{ON} over complete input signal amplitude, without employing either charge pumps or boosters and any additional switches.

The rest of the paper is organized as follows: Sect. 2 describes the operation and limitations of the TG bootstrapped switch. Section 3 presents the details of the proposed switch. The simulation results are summarized in Sect. 4, and conclusions are drawn in Sect. 5.

2 TG bootstrapped sampling switch

The circuit schematic of the TG bootstrapped switch ($M1$,$M2$) is shown in Fig. 1, and its operation is described in [9]. The R_{ON} of the switch is defined as $R_{ON,M1} \parallel R_{ON,M2}$, where $R_{ON,M1}$ and $R_{ON,M2}$ represent the ON-resistances of NMOS ($M1$) and PMOS ($M2$) transistors in the switch, respectively, defined as:

$$R_{ON} = \frac{1}{\mu_{M1,2} C_{OX} \frac{W_{M1,2}}{L_{M1,2}} \left(|V_{GS,M1,2}| - |V_{TH,M1,2}|\right)} \tag{1}$$

where, μ, C_{OX} and $\frac{W}{L}$ are the mobility, oxide capacitance and aspect ratios of the transistors, respectively. The effect

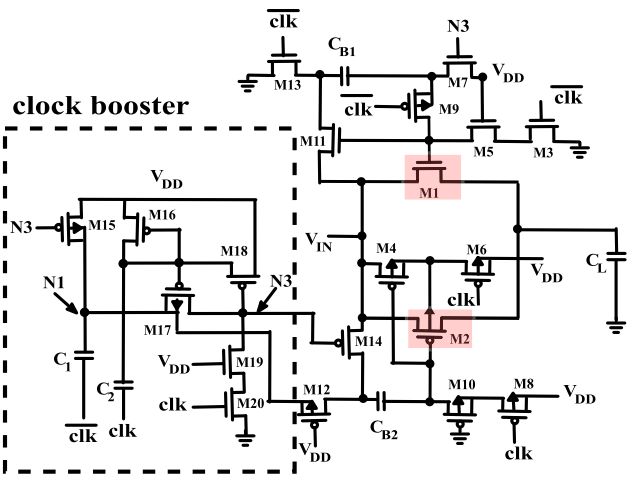

Fig. 1 Circuit schematic of bootstrapped transmission gate based sampling switch [9]

of the source-to-bulk voltage, V_{SB}, variations on V_{TH} of a p-type or n-type MOS transistor is defined in [11] as:

$$|V_{TH}| = |V_{TH,0}| + \gamma\left(\sqrt{|2\phi_f| + |V_{SB}|} - \sqrt{|2\phi_f|}\right) \tag{2}$$

where, $V_{TH,0}$, γ, and $2\phi_f$ are the threshold voltage (when $|V_{SB}| = 0$ V), body-effect coefficient and surface potential of the transistor, respectively.

In this switch, the gate of $M1$ and $M2$ are bootstrapped to nullify the variation of $|V_{GS}|$ with the amplitude of the input analog signal (V_{IN}). However, for bootstrapping the gate of $M2$, a clock booster circuit had been employed, which drains more power. On the other hand, two transistors $M4$ and $M6$ are used as switches to switch the bulk of $M2$ between V_{IN} and V_{DD}, during sampling and hold phase, respectively, to compensate its V_{TH} variations with V_{IN}. However, variation in V_{TH} of $M1$ with the amplitude of V_{IN} had not been compensated. The bulk of $M1$ is connected to ground, and the voltage at its source terminal is V_{IN} . As a result, V_{TH} varies with V_{IN} in accordance with (2). Therefore, R_{ON} variation with V_{IN} is not completely eliminated.

3 Proposed sampling switch

The circuit schematic of the proposed switch ($M1$, $M2$) is shown in Fig. 2(a). This circuit does not employ a charge pump or clock booster to bootstrap the gate voltage of the PMOS transistor. In addition, no additional switches are used to minimize the V_{TH}, variations as the voltages used for this purpose are generated internally.

Here, the sampling clock, clk, oscillates between 0 V and supply voltage, V_{DD}. The signal $\overline{clk}$ is obtained from clk using an inverter I_1. C_L and $C_{B1,2}$ are the load and bootstrapping capacitors, respectively. The operation of the proposed switch can be understood in two phases:

Hold Phase ($clk = 0$ V) In this phase, $M3$, $M4$, $M7$, $M10$, $M11$, $M12$ are ON, and $M5$, $M6$, $M8$, $M9$ are OFF. Therefore, capacitors, C_{B1} and C_{B2} are charged to V_{DD}. As a result, voltages at node x (V_x) and y (V_y) are at V_{DD} and 0V, respectively. Moreover, the output of inverters I_1 and I_2 are at V_{DD} and 0 V, respectively. Therefore, $M11$ and $M12$ set the gate of $M1$ and $M2$ to 0 V and V_{DD}, respectively, to turn them OFF. In addition, the bulk of $M1$ is at 0 V ($= V_y$), and $M2$ is at V_{DD} ($= V_x$). Thus, C_L is isolated from the input signal, V_{IN}, and the switch is in hold phase. The equivalent circuit is shown in Fig. 2(b).

Track Phase ($clk = V_{DD}$): In this phase, $M5$, $M6$, $M8$, $M9$ are ON, and $M3$, $M4$, $M7$, $M10$, $M11$, $M12$ are OFF. As a result, V_x and V_y are defined as:

$$V_x = V_{IN} + V_{DD} \quad \text{and } V_y = V_{IN} - V_{DD} \tag{3}$$

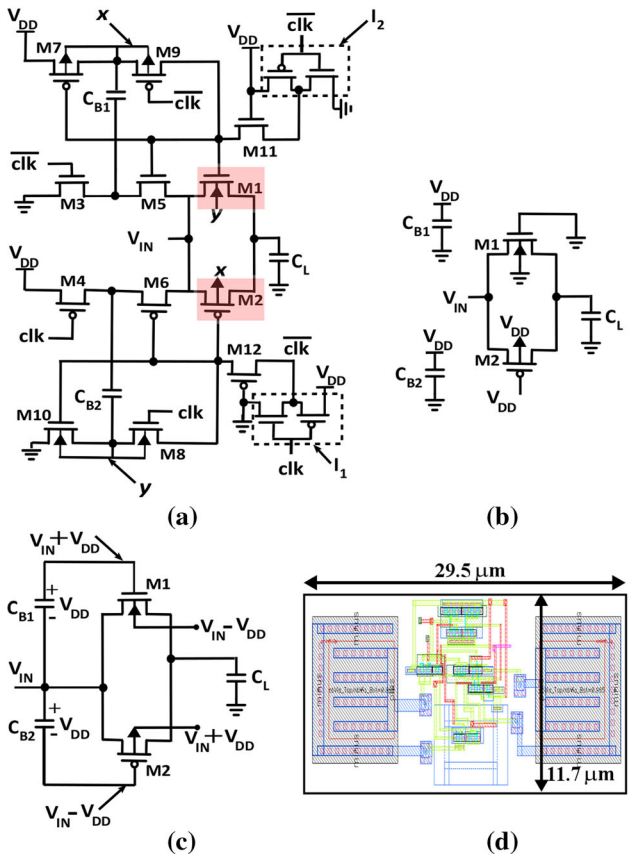

Fig. 2 Proposed robust linear bootstrapped TG switch **a** Circuit Schematic. **b** In hold phase ($clk = 0$ V). **c** In tracking phase ($clk = V_{DD}$) and **d** Layout showing active area occupied

Since V_{IN} is bounded by the power supply rails, V_y can never be a positive value. Therefore, the bulks of NMOS transistors, $M8$, and $M10$ are connected to node y. Similarly, bulks of PMOS transistors, $M7$, and $M9$ are connected to node x. These connections ensure the junction diode between source and bulk to be reversed biased. $M8$ and $M9$ connect the gates of $M2$ and $M1$ to node y and x, respectively. As a result, the gate-to-source voltages of $M1$ and $M2$ are at V_{DD} and $-V_{DD}$, respectively, which turn ON both the transistors. In addition, bulks of $M1$ and $M2$ are connected to nodes y and x, respectively, which ensures $|V_{SB}|$ of $M1$ and $M2$ to be a constant value equal to $|V_{DD}|$ (see (3)). Therefore, $M1$ and $M2$, in the proposed switch, provide a constant R_{ON} (from (1) and (2)) irrespective of the magnitude of V_{IN} while C_L is tracking it. Thus, the switch is in the track phase. The equivalent circuit is shown in Fig. 2(c).

Due to a constant R_{ON}, the proposed switch also ensures the desired performance without using wider transistors, thus, improving its speed of operation even at low supply voltages. In addition, no boosters or charge pumps are employed. Moreover, there are no reliability issues noticed with the proposed circuit.

4 Simulation results and discussions

4.1 Sampling switch

The proposed switch has been designed in STM 65 nm CMOS technology, and post-layout simulations are performed using Spectre. Since SAR ADC completes digital conversion serially, the duty cycle of the sampling clock is always kept much less than 50%. As a result, a small-time interval is available for the sampling switch to track the input analog signal. Therefore, in this work, the ON-time of the sampling clock for testing the sampling switch is taken as 5ns. Hence, simulations are performed at a sampling frequency of 100 MHz (considering 50% duty cycle), a nominal supply voltage of 0.8 V and load capacitance, $C_L = 1$pF.

The layout of the proposed switch is shown in Fig. 2(d). Deep n-well (DNW) layer is used in the layout to isolate the bulk of the NMOS transistors, $M1$, $M8$, and $M10$ (see Fig. 2(a)) from other devices. The layout occupies an active area of only 345.15μm^2. As a first step, transient simulations were performed to plot V_{TH} of NMOS transistor $M1$ and PMOS transistor $M2$ (in Fig. 2(a)) as a function of V_{IN}. The plots were obtained for two cases:

Case-1: When bulk voltages of $M1$ and $M2$ ($V_{B,M1}$ and $V_{B,M2}$) are at 0 V and V_{DD}, respectively.

Case-2: When $V_{B,M1} = V_y$ and $V_{B,M2} = V_x$ as shown in Fig. 2(a).

The obtained results are shown in Fig. 3. It can be observed from the figure that a variation of 5% in V_{TH} of $M1$ and $M2$ have been noticed for case-1. On the other hand, only 0.05% of variations are observed in V_{TH} of $M1$

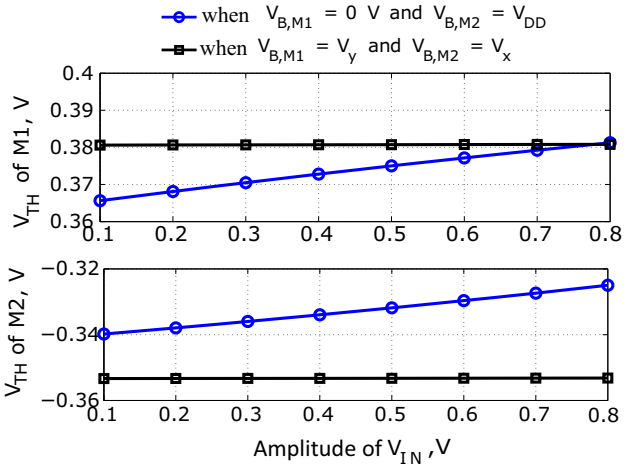

Fig. 3 Variations in V_{TH} of $M1$ and $M2$ with V_{IN}

and $M2$ for case-2. Therefore, the proposed design ensures almost constant V_{TH} over the complete input signal amplitude range, as explained in the previous section. Post-layout transient simulations of the proposed sampling switch are performed with a full-scale (FS) input sinusoidal signal with a frequency of 10 MHz. The gate voltages (V_G) of $M1$ and $M2$ (see Fig. 2(a)) are presented in Fig. 4, which shows that during tracking phase, $V_{G,M1} = V_{IN} + V_{DD}$ and $V_{G,M2} = V_{IN} - V_{DD}$. As a result, the gate-to-source voltages of $M1$ and $M2$ are at V_{DD} and $-V_{DD}$, respectively. The FFT is plotted for 4096 bins and is shown in Fig. 5. The plot has shown SNDR, SFDR, and THD of 87.81 dB, 90 dB and − 91.5 dB, respectively, under typical conditions.

The performance of the proposed design is compared with four sampling switches reported in [6, 7, 9, 10]. These switches have been designed with the same technology (STM 65 nm), and post-layout simulations are performed under the same conditions ($V_{DD} = 0.8$ V) as that of the proposed sampling switch. The aspect ratios of all the transistors in different switches are kept the same to have a fair comparison of the performance metrics. R_{ON} of the proposed and other switches from literature were calculated at the different amplitude of V_{IN} using transient simulations at a *clk* frequency of 100 MHz. Simulation results are presented in Fig. 6. It can be observed that the proposed switch provides almost constant and least value of R_{ON} (=560 Ohms) compared to other designs. The proposed switch has shown the least value of R_{ON} because it is defined as the parallel connection of the R_{ON} of PMOS and NMOS transistors compared to the NMOS

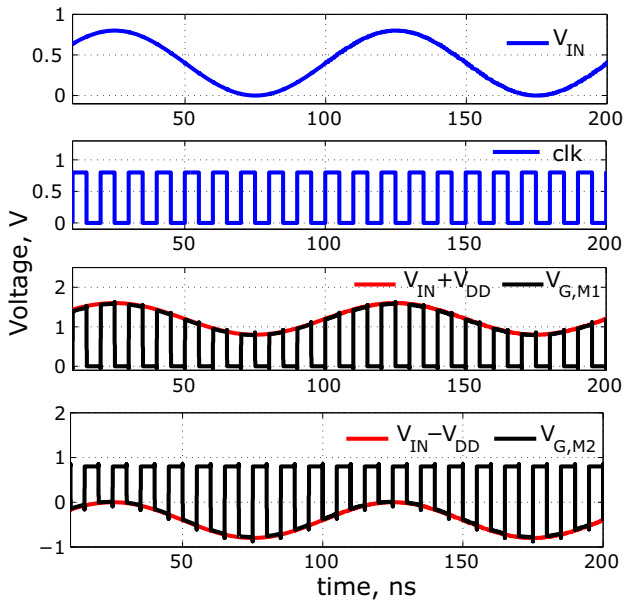

Fig. 4 Timing diagram showing the gate voltages of $M1$ ($V_{G,M1}$) and $M2$ ($V_{G,M2}$) in the proposed sampling switch

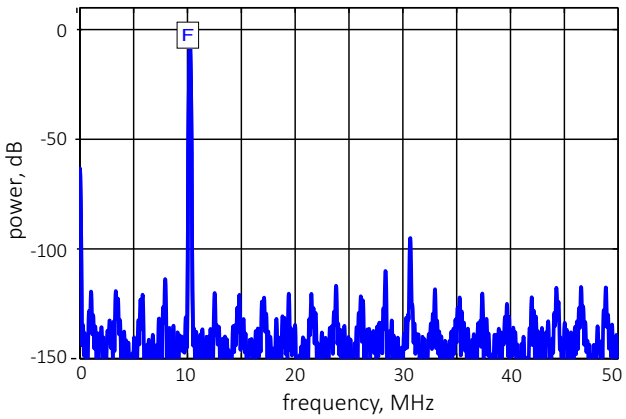

Fig. 5 FFT plot of proposed linear switch for 4096 points with FS input at 10 MHz

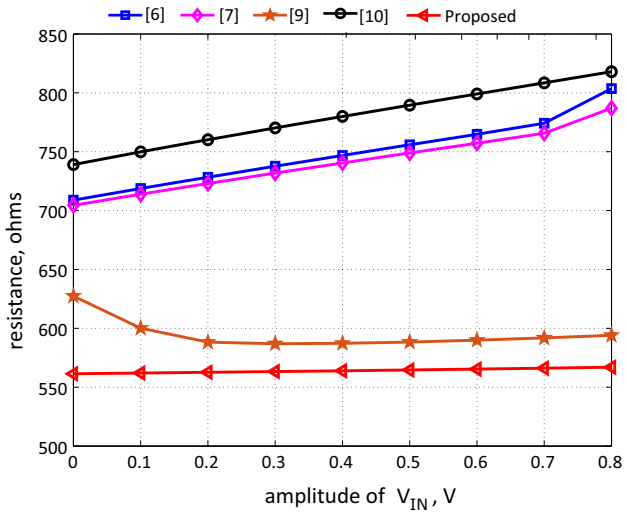

Fig. 6 Comparison of R_{ON} of proposed switch with state of art work

bootstrapped switches [6, 7, 10], where the resultant R_{ON} is the ON-resistance of NMOS transistor only. On the other hand, R_{ON} of the TG bootstrapped sampling switch [9] is defined in the same manner as that of the proposed sampling switch. However, the R_{ON} of the TG bootstrapped switch is higher due to the degraded gate voltages of $M1$ and $M2$ compared to the proposed design. The degradation is due to the parasitics contributed by continuously ON transistors M5 and M10 (see Fig. 1). Besides, in the tracking phase, the PMOS transistor $M14$ turns OFF, when the magnitude of V_{IN} falls below the magnitude of the threshold voltage of $M14$ and prevents the bootstrapping operation of $M2$. However, no such degradation is observed in the proposed switch, as shown in Fig. 4. In the proposed switch, the parasitics at the gate of $M1$ and $M2$ due to $M11$ and $M12$ (see Fig. 2(a)) are compensated by turning them ($M11$ and $M12$) OFF using inverters $I1$ and $I2$. To make this point more clear, $V_{G,M1}$ (when $V_{IN} = V_{DD}$) and $V_{G,M2}$

(when $V_{IN} = 0$ V) of the TG bootstrapped and proposed sampling switch in tracking phase, is shown in Fig. 7. It is observed from the plot that the proposed sampling switch reaches the desired voltage faster than the TG bootstrapped switch. In addition, no degradation in gate voltages of the proposed sampling switch has been observed.

The SNDR, SFDR, and THD of the proposed switch and switches reported in the literature are calculated at different input signal frequencies, and the results are presented in Fig. 8. It can be observed from the figure that the proposed switch delivers the highest SNDR, SFDR, and least THD compared to other switches. The performance metrics of the proposed switch are compared with other reported switches, and the results have been summarized in Table 1. From the table, it has been observed that the proposed switch has shown excellent performance compared to others, at a supply voltage of 0.8 V. Again, it is worth to mention that the superior performance from the proposed design is obtained without employing any charge pumps or clock boosters.

Next, the amount of variations in R_{ON} with the amplitude of V_{IN}, ΔR_{ON}, has been calculated using the following equation:

$$\Delta R_{ON} = 2 * \frac{R_{ON,max} - R_{ON,min}}{R_{ON,max} + R_{ON,min}} \tag{4}$$

Here, $R_{ON,max}$ and $R_{ON,min}$ are defined as the maximum and minimum values of R_{ON}, respectively, which are obtained from Fig. 6. The values of ΔR_{ON} of the proposed switch and the switches from the literature, are evaluated at different process corners (*ss*, *sf*, *tt*, *fs* and *ff*) and temperature (−40 °C, 27 °C and 125 °C) at a $V_{DD} = 0.8$ V. The results are presented in Fig. 9. It can be observed from the figure that the proposed switch has shown a maximum variation of 1% against different process corners and

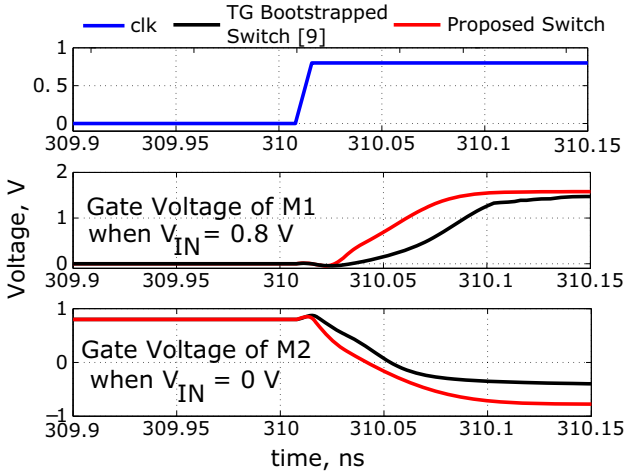

Fig. 7 Transient Simulations showing $V_{G,M1}$ and $V_{G,M2}$ of proposed and TG bootstrapped sampling switch

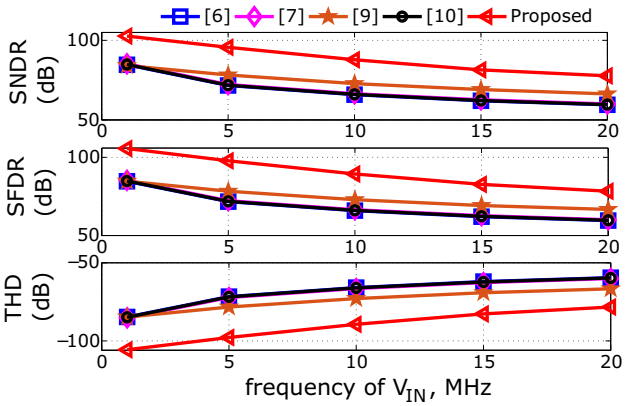

Fig. 8 Dynamic performance comparison at different frequencies of input signal

temperature, which is very low compared to other works reported in the literature. In addition, the dynamic performance metrics of the proposed switch and the switches form the state of the art work is also obtained at different process corners, and temperature condition at a V_{DD} of 0.8 V and the plot is presented in Fig. 10. It can be observed from the plot that the proposed switch delivers the highest SNDR and SFDR and least THD compared to other switches. The robust performance of the proposed switch can be attributed to the fact that it makes R_{ON} almost independent of the input signal amplitude, as explained in the preceding section.

4.2 10-bit SAR ADC

A 10-bit SAR ADC with MCS switching scheme [12] is designed in CMOS 65 nm technology. The capacitance of the DAC unit capacitor is kept five times higher than the minimum value of the capacitance, which is calculated from [13] considering the effect of noise. It should be noted that for moderate to high frequency *clk* signal, the available acquisition time (T_{AQ}) (time during which the sampling switch is in ON state and tracks the input signal) is small due to the serial conversion process of the SAR ADC. T_{AQ} depends on R_{ON} of the sampling switch and the total DAC capacitance, C_{DAC} of the SAR ADC [14].

$$T_{AQ} \propto R_{ON} C_{DAC} \tag{5}$$

It should be noted that various switching schemes have been reported [15–18] to reduce the value of C_{DAC}. However, the value of C_{DAC} is limited by $\frac{KT}{q}$ noise. As a result, R_{ON} of the sampling switch should be kept small to deliver the desired performance of the SAR ADC. Semi-behavioral transient simulations of the SAR ADC, with proposed and the sampling switches reported in [6, 7, 9, 10] at layout level, are performed at a *clk* frequency of 20 MHz, input signal frequency close to 10 MHz, and V_{DD} of 0.8 V. The

Table 1 Performance comparison of proposed switch with state of art work

Metrics*	JSSC-1999 [6]	JSSC-2018 [7]	EL-2006 [9]	SSCM-2015 [10]	Proposed
SNDR (dB)	65.86	66.45	72.8	66	87.81
SFDR (bits)	66.4	67	74	66.5	90
THD (dB)	−66.8	−67.8	−74.5	− 67.2	− 91.5
Power consumption (μW)	2	2.3	8.35	1	1.3
Employs boosters	Yes	Yes	Yes	No	No

*The metrics are obtained by simulating all the switches under same conditions at a $V_{DD} = 0.8$V and with CMOS 65 nm technology

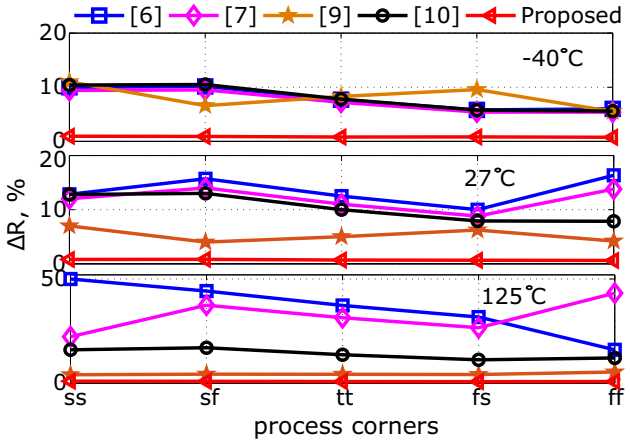

Fig. 9 Comparison of ΔR_{ON} of proposed switch with state of art work at different process corners and temperatures

obtained results are summarized in Table 2. It can be observed from the table that the performance of the SAR ADC with the proposed sampling switch is much superior compared with the sampling switches reported in the literature as the proposed sampling switch provides least and almost constant R_{ON} compared to others. The FFT plot of the SAR ADC with a proposed sampling switch for 2048 bins is shown in Fig. 11.

Next, the transient simulation of SAR ADC is performed with the proposed sampling switch by varying the number of bits of the ADC from 6 to 14 in a step size of 2 bits. The stimulus is kept the same as mentioned before. Here, the capacitance of the DAC unit capacitor is kept five times higher than the minimum value of the capacitance, which is calculated from [13] for a particular bit size of the ADC. The obtained results are summarized in Fig. 12. It can be noticed that the performance of the ADC is degraded when the resolution (n) of the ADC becomes greater than 12 bits at 20 MHz sampling frequency. At higher values of n, the value of C_{DAC} increases exponentially. As a result, the sampling switch does not get sufficient time to track the input signal. Therefore, the operating frequency of the ADC should decrease to accommodate adequate time for tracking the input signal at higher targeted bits.

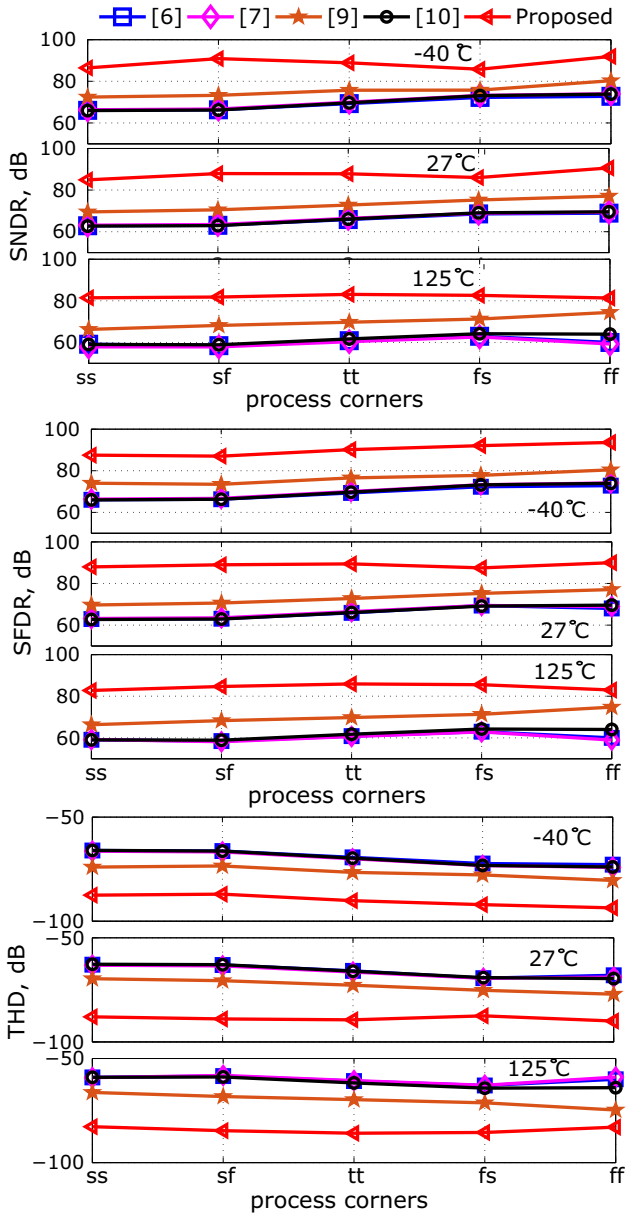

Fig. 10 Comparison of dynamic performance of proposed switch with state of art work at different process corners and temperatures for a FS input signal with a frequency of 10 MHz

Table 2 Performance comparison of different switches when simulated with 10-bit SAR ADC

ADC Metrics	JSSC-1999 [6]	JSSC-2018 [7]	EL-2006 [9]	SSCM-2015 [10]	Proposed
SNDR (dB)	52.47	52.6	56.93	51.9	59.43
ENOB (bits)	8.42	8.44	9.16	8.3	9.6
SFDR (dB)	53.5	53.6	60	52.84	68.72

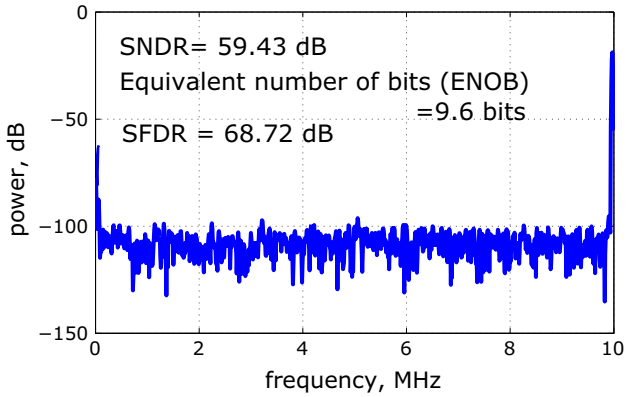

Fig. 11 FFT plot of 10-bit SAR ADC with proposed sampling switch

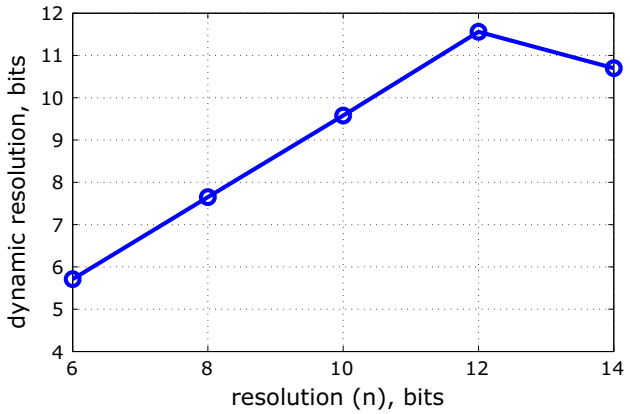

Fig. 12 Dynamic resolution of the *n*-bit SAR ADC with proposed sampling switch

5 Conclusion

A linear robust sampling switch is proposed in this paper without any boosters. This switch has shown a maximum variation of 1% in R_{ON} over FS input signal at different process corners and temperatures, which is very low compared to the state of art work. In addition, the proposed switch provides around 87.8 dB SNDR, 90 dB SFDR and − 91.5 dB THD at a sampling frequency of 100 MHz and a supply voltage of 0.8 V. The proposed switch is suitable for low-voltage moderate resolution SAR ADCs.

Acknowledgements This work is supported by early career research grant with Project Ref. ECR/2017/000931. This publication is also an outcome of the R & D work undertaken project under the Visvesvaraya PhD Scheme of Ministry of Electronics & Information Technology, Government of India, being implemented by Digital India Corporation.

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