Continuous-Time Pipelined Analog-to-Digital Converters: A Mini-Tutorial

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***Abstract*—The continuous-time pipelined (CTP) ADC is an emerging analog-to-digital converter that combines anti-alias filtering and quantization in a single unit. It presents a resistive input impedance making it easy to drive, and places relaxed requirements on amplifiers used in the ADC. The CTP ADC attempts to address many of the challenges of discrete-time pipelined analog-to-digital conversion. This brief is a first-principles introduction to this recent architecture.**

***Index Terms*—Pipeline, filter, aliasing, analog to digital conversion, oversampling.**

I. Introduction

MEDIUM-RESOLUTION analog-to-digital converters pushing the speed limits of process technology have largely been realized using the discrete-time pipelined architecture. Pipelined ADCs in CMOS have been investigated since the mid-1980's [1] and have been improved upon for the past 35 years – see for example [2], which uses time-interleaving and extensive digital calibration to achieve 12-bit resolution at 18 GS/s in 16 nm CMOS.

Discrete-time pipelined converters sample the input signal up front, and process these samples using switched-capacitor techniques. This means that such ADCs need to be preceded by an anti-alias filter, whose design becomes increasingly difficult as the digitization bandwidth approaches half the sampling frequency. In practice, therefore, a signal chain incorporating a Nyquist converter operates with an OSR of 2 or higher to relax the design of the filter up front. Driving a discrete-time pipelined ADC is a significant challenge due to the switched-capacitor impedance presented by such a converter to the external world. This has prompted many designers to include a buffer on chip. The design of this buffer is no easy task, often requiring a higher supply than the ADC core. Switched-capacitor ADCs also complicate the design of the reference buffer due to the data-dependent charge drawn from it. On-chip reference buffers are, therefore, complex to design, particularly at high resolutions/speeds. Finally, achieving the desired settling and linearity in the inter-stage gain amplifier is yet another formidable difficulty. Time interleaving low-rate converters is a way to address speed problems, but this strategy is accompanied by interleaving artifacts. See [3] and the references therein for a recent tutorial describing the challenges associated with discrete-time pipelined ADCs.

A way of avoiding the problems above is to employ the continuous-time $\Delta\Sigma$ architecture. CT$\Delta\Sigma$Ms use oversampling and negative feedback to achieve the desired SNR, while possessing the feature of implicit anti-aliasing [4] and presenting a resistive input impedance. Unfortunately, the need to close a feedback loop restricts the maximum sampling rate at which a CT$\Delta\Sigma$M can be clocked. Together with the high oversampling ratio needed to achieve adequate noise-shaping, this restricts the maximum bandwidth achievable with such a modulator. For example, the maximum bandwidth reported in a single-loop CT$\Delta\Sigma$M in a 65 nm CMOS process is only about 100 MHz while sampling at about 1.5 GS/s [5] - compare this with [6], which is a discrete-time pipelined ADC that uses 16× time-interleaving to achieve a sampling rate of 4 GS/s in the same process technology.

The continuous-time pipelined (CTP) ADC, as the name suggests, is an architecture that attempts to combine pipelining with continuous-time operation. This way, a high sampling rate can be achieved in addition to inherent anti-alias filtering and a resistive input impedance. This brief is a first-principles introduction to continuous-time pipelined ADCs. The rest of this mini-tutorial is organized as follows. Section II introduces the one-stage CTP. We build it from the ground up, and show a one-to-one correspondence with a signal-processing chain consisting of an anti-alias filter followed by an ADC. Section III gives design considerations for an example single-stage CTP ADC that incorporates a first-order anti-alias filter. We place the continuous-time pipelined ADC in context with CT$\Delta\Sigma$Ms and discrete-time pipelined ADCs in Section IV. Section V describes design and implementation challenges with the CTP and concludes the brief.

II. The One-Stage Continuous-Time Pipeline ADC

Fig. 1(a) shows a signal-processing chain that incorporates an ADC. The input u is first processed by an anti-alias filter with frequency response $H_{aa}(f)$. The output of this filter is sampled by the ADC at a rate $f_s(= 1/T_s)$. The quantization error introduced by the ADC is denoted by q. If the bandwidth of the desired signal is B, the job of the anti-alias filter is to let through frequency components in the range $[0 - B]$ with a gain of unity, while significantly attenuating signals in the

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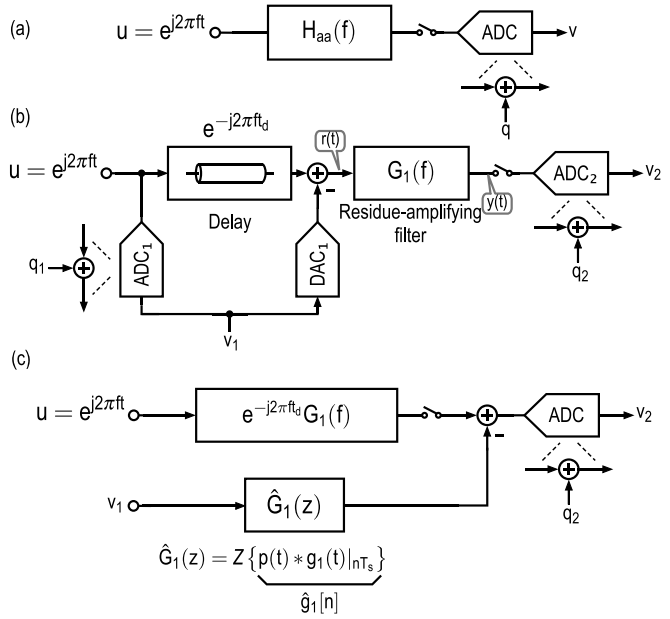

Fig. 1. (a) Signal-processing chain with an anti-alias filter followed by an ADC. (b) Equivalent method of realizing the signal chain with lower-resolution ADCs. (c) Signal-flow diagram of the structure of part (b).

range $[f_s - B, f_s + B]$. If $u = e^{j2\pi ft}$, the output sequence $v[n]$ is given by

$$v[n] = H_{aa}(f)e^{j2\pi fT_s n} + q[n]. \tag{1}$$

Consider an alternative (but not immediately obvious) way of implementing the same signal-processing chain, shown in Fig. 1(b). An approximate version of the input is formed by quantizing it coarsely using ADC_1 and DAC_1. This is subtracted from a delayed version of u, yielding the residue signal $r(t)$. This is low-pass filtered by a residue-amplifying filter with frequency response $G_1(f)$, whose output is quantized by ADC_2 (with a quantization error q_2), yielding v_2. The signal chain can be modeled as shown in Fig. 1(c) where $p(t)$ and $g_1(t)$ denote the DAC pulse shape and the impulse response corresponding to G_1 respectively. $\hat{G}_1(z)$ is the z-transform of $\hat{g}_1[n]$, which is the sampled pulse response of G_1. If $u = e^{j2\pi ft}$, straightforward analysis shows that

$$v_1[n] * \hat{g}_1[n] + v_2[n] = e^{-j2\pi ft_d}G_1(f)e^{j2\pi fT_s n} + q_2[n].$$

where $*$ denotes convolution. Dividing both sides of the equation above by the dc gain of G_1, namely $G_1(0)$, we have

$$\underbrace{\frac{1}{G_1(0)}\left\{v_1[n] * \hat{g}_1[n] + v_2[n]\right\}}_{v[n]} = \underbrace{\left\{\frac{1}{G_1(0)}e^{-j2\pi ft_d}G_1(f)\right\}}_{H_{aa}(f)} e^{j2\pi fT_s n} + \underbrace{\frac{q_2[n]}{G_1(0)}}_{q}. \tag{2}$$

Comparing (1) and (2), observe that the signal chains of Figs. 1(a) and (b) would be equivalent if

$$H_{aa}(f) = \frac{1}{G_1(0)}e^{-j2\pi ft_d}G_1(f), \quad q = q_2[n]/G_1(0)$$
$$v[n] = \frac{1}{G_1(0)}(v_1[n] * \hat{g}_1[n] + v_2[n]). \tag{3}$$

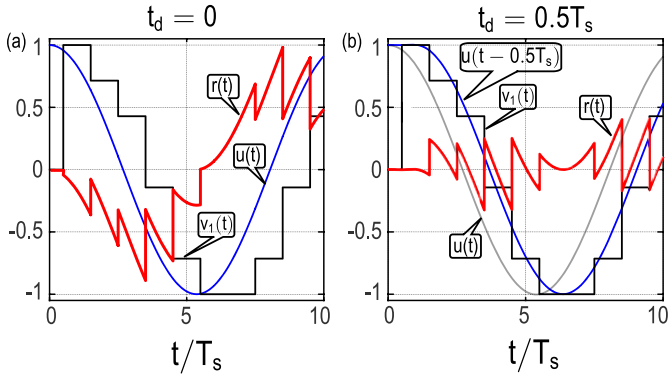

Fig. 2. Example input, DAC_1 and residue waveforms when (a) $t_d = 0$ and (b) $t_d = 0.5\,T_s$. DAC_1 is assumed to be clocked at the same instant as ADC_1.

The system of Fig. 1(b), which realizes a filter-ADC combination is called the continuous-time pipelined ADC. A few observations are in order.

(**a**) The transfer function of the equivalent anti-alias filter of the system of Fig. 1(b) is $e^{-j2\pi ft_d}G_1(f)/G_1(0)$. In $\Delta\Sigma$ parlance, this would be called the signal transfer function (STF). The dc gain of the STF is unity, like that of $H_{aa}(f)$.

(**b**) The "final" output of the structure of Fig. 1(b) is obtained by filtering v_1 with a discrete-time transfer function $\hat{G}_1(z)$, and adding the result to v_2.

(**c**) As seen from (2), the quantization noise of ADC_2 in Fig. 1(b) is attenuated by a factor of $G_1(0)$ when the final output of the system is reconstructed. In $\Delta\Sigma$ parlance, $1/G_1(0)$ would represent the noise transfer function (NTF). It is thus seen that making $G_1(0)$ very large without saturating the residue-amplifying filter can significantly simplify the design of ADC_2.

(**d**) The role of $\text{ADC}_1/\text{DAC}_1$ is to create a coarse approximation of u, so that the residue signal $r(t)$ is sufficiently small. This way, $G_1(0)$ can be made large, relaxing the design of ADC_2.

(**e**) The role of the delay t_d in the input path is to reduce the peak value of $r(t)$. The intuition behind the need for the delay[1] is the following. ADC_1 samples the input, and drives DAC_1 to result in $v_1(t)$. Assuming an NRZ pulse shape for the DAC, its output is going to be delayed by $0.5T_s$ with respect to the impulse sequence produced at ADC_1's output. If this delay is not compensated in the input path, the residue's peak value can become very large, as illustrated in Fig. 2(a). Choosing t_d to mimic the delay in the $\text{ADC}_1/\text{DAC}_1$ path results in a significant reduction in the peak-to-peak value of $r(t)$. This enables the use of a residue amplifier with a higher dc gain, thereby allowing one to use a larger quantization step in the back-end ADC. In practice, ADC_1 will need some time to resolve the input. Thus DAC_1 will have to be clocked some time later. This introduces excess delay in the flash-DAC path. It is apparent that the delay in the input path must be increased to account for excess delay to keep the peak-to-peak value of $r(t)$ in check. An alternative approach is to insert a "negative

[1]Initially recognized in the context of MASH CT$\Delta\Sigma$Ms in [7], [8], [9], and adapted in CTP's [10], [11], [12].

delay" before ADC_1 by using a predictive filter [13], [14]. As one might expect, a negative delay can only be achieved over a small bandwidth – and such an approach is less effective compared [15] to the one in Fig. 1(b), where the input is delayed (and can be accomplished passively).

(**f**) The amplified-and-filtered version of the residue, namely $y(t)$ will have a peak-to-peak swing that is lesser than that of $r(t)$, on account of the low-pass nature of $G_1(f)$. Lowering the bandwidth of G_1, or increasing its high-frequency roll off should be expected to reduce the peak-to-peak value of $y(t)$. $G_1(f)$, therefore, not only performs anti-alias filtering but also enables the use of a larger dc gain than would otherwise be possible.A similar problem also exists in MASH ADCs – see [16], for instance.

(**g**) The discussion so far assumed that ADC_1 is ideal. In practice, device mismatch will cause its thresholds to deviate from their ideal values, thereby increasing the peak-to-peak value of $r(t)$ (and $y(t)$). The dc gain of G_1 should be chosen so that $y(t)$ does not become so large that it saturates the stage, even with threshold-voltage deviations in ADC_1. Thus, with ideal circuit blocks, $G_1(0)$ is chosen so that $y(t)$ occupies a fraction (usually about 50%) of the output range of the stage, akin to what is done in discrete-time pipeline ADCs.

(**h**) Our analysis, which showed that the signal chains of Figs. 1(a) and (b) are equivalent, assumed a linear residue-amplifying filter. In practice, however, this stage will saturate. This limits the maximum input signal level that the CTP can handle at frequencies around multiples of f_s. This is best understood by examining the response of the system of Fig. 1(b) to a full-scale tone at f_s. v_1 will then be a dc sequence. Consequently, the residue $r(t)$ will be the sum of the input tone and the full-scale dc output produced by DAC_1. An appropriately chosen filtering characteristic for $G_1(f)$ will significantly attenuate the f_s component in $y(t)$. The full-scale dc output of DAC_1, however, which is gained-up by $G_1(0)$ will saturate the residue amplifying filter. Assuming that the peak-to-peak swing of $y(t)$ is restricted to the converter's full scale before saturation sets in, the maximum permissible amplitude of the input tone at f_s is seen to be $1/G_1(0)$ times the full scale. This is not restrictive if one is only concerned with rejection of noise in the first- and higher-Nyquist zones. If large blockers are present, however, some gentle prefiltering might be needed to avoid saturating the residue-amplifying filter.

To summarize, the one-stage continuous-time pipelined ADC of Fig. 1(b) combines anti-alias filtering with analog-to-digital conversion. Further, like in a discrete-time pipeline ADC, it employs two low-resolution ADCs to achieve a high resolution.

III. Example Design

Fig. 3 shows an example circuit realization of a one-stage CTP with a built-in first-order lowpass filter. The opamp is ideal, and DAC_1 (which produces a current) and ADC_2 are inverting. The input is converted into a delayed current using a transmission-line delay network, and a coarse approximation to that current, generated by DAC_1, is subtracted from it. For the time being, assume that the current i_{prbs} shown in red is

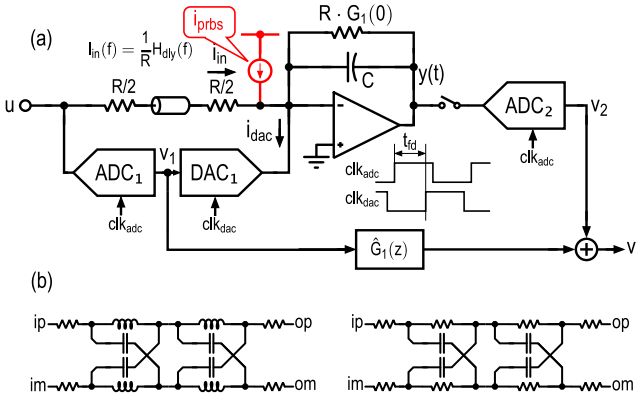

Fig. 3. (a) Single-ended equivalent of an example one-stage CTP incorporating a first-order anti-aliasing filter. (b) Two-section delay line based on the LC lattice. (c) Delay-line using RC-lattice sections.

zero. The residue, which we denoted by $r(t)$ in Fig. 1(b), is formed in the current domain and converted into a filtered-and-amplified voltage $y(t)$. ADC_2 digitizes $y(t)$, resulting in v_2. We denote the frequency response from u to i_{in} by $(1/R)H_{dly}(f)$, where $H_{dly}(f)$ depends on the details of the delay network used in the input path. Excess delay in the flash-DAC path is denoted by t_{fd}. It is instructive to analyze the various constituents of the filtered residue $y(t)$. Straightforward analysis of Fig. 3 indicates that $y(t)$ can be written in the frequency domain as follows.

$$Y(f) = \underbrace{-U(f)\left\{H_{dly}(f) - e^{-j2\pi f t_{fd}}P(f)\right\}\overbrace{\frac{G_1(0)}{1+j(f/f_0)}}^{\equiv G_1(f)}}_{\text{input leakage due to delay mismatch}} + \underbrace{G_1(f)P(f)e^{-j2\pi f t_{fd}}\sum_{k\neq 0}U(f-kf_s)}_{\text{filtered DAC images}} + \underbrace{G_1(f)P(f)e^{-j2\pi f t_{fd}}\sum_{k}Q_1(f-kf_s)}_{\text{quantization noise}} \quad (4)$$

where $P(f)$ and $Q_1(f)$ denote the Fourier transforms of the DAC pulse shape and ADC_1's quantization noise respectively, $f_0 = 1/(2\pi G_1(0)RC)$, and k is an integer. The first term represents the component of the input that leaks into $y(t)$ due to delay mismatch between the input and ADC_1-DAC_1 paths. The second term quantifies the strength of the filtered images of the DAC spectrum (centered around integral multiples of f_s), while the last term represents the filtered quantization noise of ADC_1.

From (4), we see that it is important that the delay between the input and ADC_1-DAC_1 paths be very well matched within the signal bandwidth to keep $y(t)$ small. The filtered DAC images are less problematic, and are easily addressed by choosing higher-order residue filtering. The contribution of quantization noise to $y(t)$ can be reduced by increasing the resolution of ADC_1 (and DAC_1). Note however, that the increasing the resolution of ADC_1 will not tame $y(t)$ if there is significant delay mismatch between the input and DAC paths.

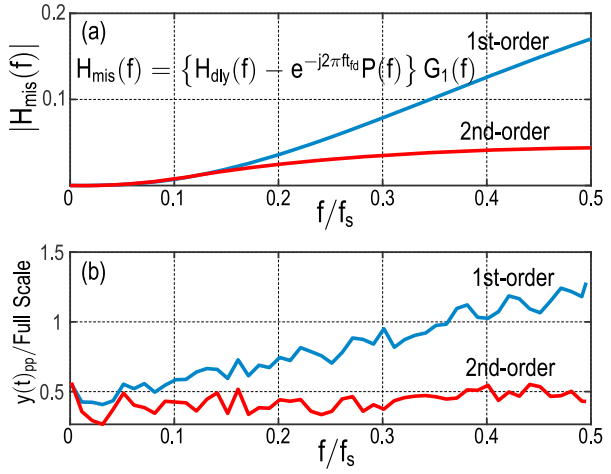

Fig. 4. (a) $|H_{mis}(f)|$ versus f/f_s for first- and second-order $G_1(f)$. $G_1(0) = 4$, bandwidth is $f_s/8$ and $t_{fd} = 0.5\,T_s$. 5-section LC-lattice delay lines are assumed, with a magnitude response tailored to mimic the sinc roll-off the NRZ DAC pulse. (b) Peak-to-peak value of $y(t)$ normalized to the full scale.

The discussion so far described a one-stage continuous-time pipelined ADC. Realizing ADC_2 in Fig. 3 with a single-stage pipeline ADC will result in a two-stage continuous-time pipelined ADC. Multi-stage pipelines are similarly derived. The order of the residue-amplifying filter can also be increased. The design process for a single stage of the pipeline typically proceeds as follows.

(a) *Choose the Delay Element:* As seen from (4), it is important that H_{dly} matches $e^{-j2\pi f t_{fd}} P(f)$ in the signal band, so that the peak-to-peak value of the filtered-and-amplified residue is kept as low as possible. Several types of delay networks have been used, and examples of lattice-based structures are shown in Figs. 3(b) and (c). Analysis shows that the LC network can achieve a flatter delay over a wider bandwidth when compared to the RC structure, at the expense of area.

(b) *Choose the Properties of the Residue-Amplifying Filter:* The simple-minded example of Fig. 3 used a first-order residue-amplifying filter. As seen from (4), a high-order $G_1(f)$ can better attenuate the DAC images. A second-order $G_1(f)$ is a good choice - increasing the order further has little (if any) effect on the peak of the amplified residue. A good starting point is to choose the dc gain $G_1(0)$ so that the peak-to-peak swing of $y(t)$ is about half the full-scale voltage. This gives enough margin for threshold-voltage deviations in ADC_1, and delay mismatch between the input and ADC_1/DAC_1 paths. A good way to quantify the effect of delay mismatch on y is to evaluate the mismatch frequency response given by (see (4))

$$H_{mis}(f) = \left\{H_{dly}(f) - e^{-j2\pi f t_{fd}} P(f)\right\} G_1(f).$$

A rule of thumb that has been used in industrial designs ([10], [11], [12]) is to keep the $|H_{mis}(f)| < 0.25$ in the signal bandwidth. This means that 25% of the output range of the residue-amplifying filter will be occupied by the input signal leaking due to delay mismatch. Fig. 4(a) shows $|H_{mis}(f)|$ for first- and second-order $G_1(f)$. $G_1(0) = 4$, a 3-dB bandwidth of $f_s/8$ (OSR $= 4$), and a flash-DAC delay $t_{fd} = 0.5T_s$ were used in both cases. The magnitude of $(H_{dly}(f) - e^{-j2\pi f t_{fd}} P(f))$ typically increases with frequency, and using a second-order $G_1(f)$ helps keep this problem in check, as it is more effective in attenuating high frequency inputs that leak due to delay mismatch. The beneficial effect of employing a second-order $G_1(f)$ is further evident in Fig. 4(b), which plots the peak-to-peak $y(t)$ when a 3-bit ADC_1 is used. We see that $y(t)_{pp}$ increases with frequency when a first-order $G_1(f)$ is used and exceeds the full-scale of the second stage when $f/f_s \approx 0.35$. This is due to inadequate attenuation of DAC images, and the leaked input. A second-order filter is free of this problem, as $y(t)_{pp}$ remains largely unchanged with frequency, indicating that $y(t)$ is dominated by quantization noise.

(c) *Choose the Resolution of ADC_1 and DAC_1:* In a high-speed application, realizing ADC_1 as a flash structure is perhaps the most appropriate. Practical considerations probably limit its resolution to four bits anyway, but a careful analysis based on H_{mis} as discussed above must be used to choose ADC_1's resolution. [17] demonstrates a converter that can be interpreted as a CTP with high OSR, where ADC_1 is a SAR converter, while ADC_2 is a CTΔΣM.

(d) *Final Verification:* Use transient simulations to confirm that the peak-to-peak swing at the stage output does not exceed the input full scale of the next stage.

A. Digital Reconstruction

Analysis of the block diagram of Fig. 1(b) showed that the output of the continuous-time pipelined ADC has to be constructed by combining v_1 and v_2 according to (4). In Fig. 3, the recombining filter is shown as $\hat{G}_1(z)$, which is the z-transform of the sampled pulse response from v_1 to $y[nT_s]$. $\hat{G}_1(z)$ is an IIR filter, which is difficult to implement at high speeds. One way to address this is to approximate it by an appropriate FIR transfer function. Since $\hat{G}_1(z)$ depends on the frequency response of the residue-amplifying filter, its transfer function will change with process, supply voltage, and temperature. It is therefore necessary to be able to estimate this transfer function. One way of doing this is to inject a pseudo-random bit source (PRBS) current (with bits derived from a maximal length sequence generator), shown as i_{prbs} in Fig. 3. The impulse response corresponding to $\hat{G}_1(z)$ can be determined by cross-correlating successively delayed versions of the PRBS sequence with v_2. This technique, which can also run in the background, has been borrowed from the continuous-time MASH literature [18] and successfully applied to continuous-time pipelined ADCs [12]. Related techniques [19] can possibly be applied.

IV. Architectural Comparisons

In this section, we compare continuous-time pipelined ADCs with two other architectures, namely CTΔΣMs and discrete-time pipelined converters. We assume a communication application, where there is a need to filter out-of-band signals. This necessitates operating the ADC with an oversampling ratio (OSR), so that the design of the anti-alias filter does not become unmanageably difficult. Table I compares the properties of CT-pipelined ADCs, CTΔΣMs and DT-pipelined ADCs (assuming all are realized in the same process technology). As we have discussed, CT-pipelines and CTΔΣMs

TABLE I
COMPARISON OF CTP ADCS, CTΔΣMS, AND DT-PIPELINED ADCS

	CT Pipeline	CTΔΣM	DT Pipeline
Anti-aliasing	Yes	Yes	No
Input interface	Resistive	Resistive	Switched capacitor
Max. f_s	10 GHz	10 GHz	3.2 GHz (no interleaving) >10 GHz (interleaved)
Min. OSR	4	16	1
BW	1.25 GHz	312 MHz	400 MHz (OSR=4, no interleaving) 1.6 GHz (OSR=1, no interleaving) 1.2 GHz (OSR=4, 3× interleaving)
P_{th}	1×	1×	4×
P_{sw}	1×	0.5×	1×

feature inherent anti-aliasing and a resistive input impedance. In contrast, DT-pipelines need an anti-alias filter up front, and present a switched-capacitive input impedance (which is a challenge to drive).

We first compare the converters on the basis of their digitization bandwidth, defined as $BW = f_s/(2 \cdot OSR)$. The maximum sampling frequency of CT-pipelines and CTΔΣMs is limited by the time taken for the flash ADC to resolve an input. In advanced process technologies (like the 16 nm CMOS process used in [12]), we assume that the maximum sampling frequency that can be reliably achieved is 10 GHz. A single-loop CTΔΣM needs an OSR of at least 16 to achieve sufficient noise shaping in a power-efficient manner. A CT-pipelined ADC, on the other hand, can operate with OSR as low as 4. OSRs lower than this will need the dc gain of the residue amplifier to be so low that the number of stages needed will become impractically large. From the discussion above, we see that a CT-pipelined ADC is capable of achieving 4× the digitization bandwidth of a CTΔΣM in the same process technology. The maximum f_S of non-interleaved DT ADCs are generally 1/3 of that of CT ADCs, as opamps used in the residue amplifiers need to settle to an adequate degree. However DT ADCs can achieve a larger digitization bandwidth by time interleaving.

We now discuss and compare power dissipation in the three ADC architectures under consideration. The total power consumption P_{tot} of an ADC can be expressed as $P_{tot} = P_{sw} + P_{th}$, where P_{sw} is the switching power (mostly due to digital blocks), and P_{th} denotes the power needed to achieve the desired input-referred noise-spectral density. P_{sw} is proportional to f_s and P_{th} is inversely proportional to the noise spectral density (NSD), in the sense that a 3 dB reduction in NSD will need P_{th} to increase by 2×. The question we wish to answer is the following. Suppose we have a CTP ADC that achieves a NSD denoted by NSD_{target} over a digitization bandwidth BW. Furthermore, assume that we know its switching and "thermal-noise" powers, denoted by $P_{sw,ctp}$ and $P_{th,ctp}$ respectively. How would these vary if we attempted to realize an ADC with the same NSD and BW in the same process technology, but by using a CTΔΣM or a discrete-time pipeline?

When the digitization bandwidth (BW) is small relative to the speed of the process technology, so that a CTΔΣM with sufficiently large OSR is realizable, the power spent on achieving NSD_{target}, namely $P_{th,\Delta\Sigma}$, must be about the same as $P_{th,ctp}$. The switching power $P_{sw,\Delta\Sigma}$, however, will be smaller than $P_{sw,ctp}$ due to the fewer number of quantizers needed in the CTΔΣM. Thus, for low bandwidths (up to about 200 MHz in a 16 nm technology), a CTΔΣM is more power efficient than the continuous-time pipeline. A discrete-time pipeline, however, will typically need about 4× higher power to achieve the same NSD. This is primarily because the amplifiers need to source/sink current spikes needed to (dis)charge capacitors. Thus, $P_{th,dtp} \approx 4P_{th,ctp}$. $P_{sw,dtp} \approx P_{sw,ctp}$ due to the following. The DTP has more switching in the analog section (due to the switched-capacitor circuitry), but lesser switching in the digital section (due to simpler calibration filters) when compared to the CTP. As BW increases, P_{sw} eventually dominates P_{tot} in every architecture. In that case, a CTP is more efficient than a CTΔΣM (if it is at all doable) as it operates at a much lower sampling rate. When compared to a discrete-time pipeline, the CTP is more power efficient for all bandwidths, thanks to the power-efficiency continuous-time signal processing. Note that the comparison above does not account for the increased calibration complexity in a CTP. The broad conclusions above are confirmed by observing the performance of CT- and DT-ADCs on the power efficiency versus BW chart (see Fig. 5). We see that CTΔΣMs dominate at low bandwidths, while CTP-ADCs are more power efficient at high BW.

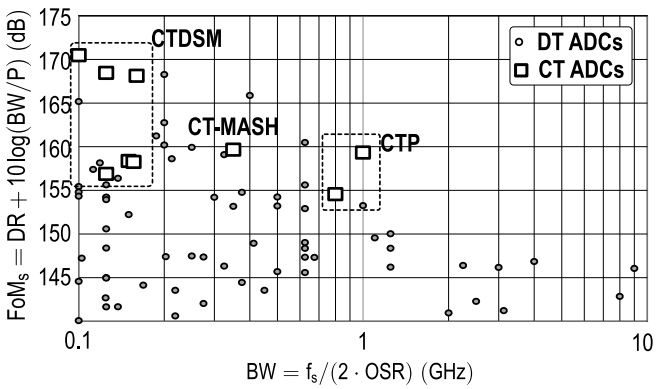

Fig. 5. Comparison of continuous- and discrete-time ADC families on the (Schreier) FoM-bandwidth chart. An OSR = 4 is assumed for Nyquist ADCs. Data from [20].

V. CHALLENGES, FUTURE DIRECTIONS AND CONCLUSION

This mini-tutorial derived the continuous-time pipeline ADC in a ground-up manner, and established its equivalence to an anti-alias filter followed by an ADC. When compared to the discrete-time pipelined ADC, which is a mature architecture that has been researched for almost four decades, the continuous-time pipelined ADC is in its infancy. The prospect of obtaining high-order anti-alias filtering and analog-to-digital conversion, coupled with a resistive input impedance makes the CTP ADC too attractive to ignore. While good progress has been made in understanding these converters, as exemplified by designs that push the envelop [10], [12], much challenging and interesting work remains.

A rethink of ADC building blocks, such as the delay lines, residue amplifiers, and DACs particular to the continuous-time pipelined architecture will improve the speed and efficiency of these converters. Rapid and efficient estimation of the digital reconstruction filters, as well as their power- and area-efficient implementation are important aspects that could benefit from further research. Mitigating the drawbacks such as the limited anti-aliasing and blocker tolerance also need attention. Another thread is the design of bandpass and quadrature continuous-time pipelined ADCs.

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