

8-bit • times

Commodore PET Video

How does it work?
A technical deep dive!

And why does it snow on the screen...???
And what about that killer poke...???



8-bit • times

Commodore PET Video – Part 1

How does it work?
A technical deep dive!

And why does it snow on the screen...???
And what about that killer poke...???



Commodore PET Video

Five different types of Video output



2001:

- 40x25 chars
- fixed timing
- 1k VRAM
- „snow“

2001N / 3032:

- 40x25 chars
- fixed timing
- 1k VRAM

4032

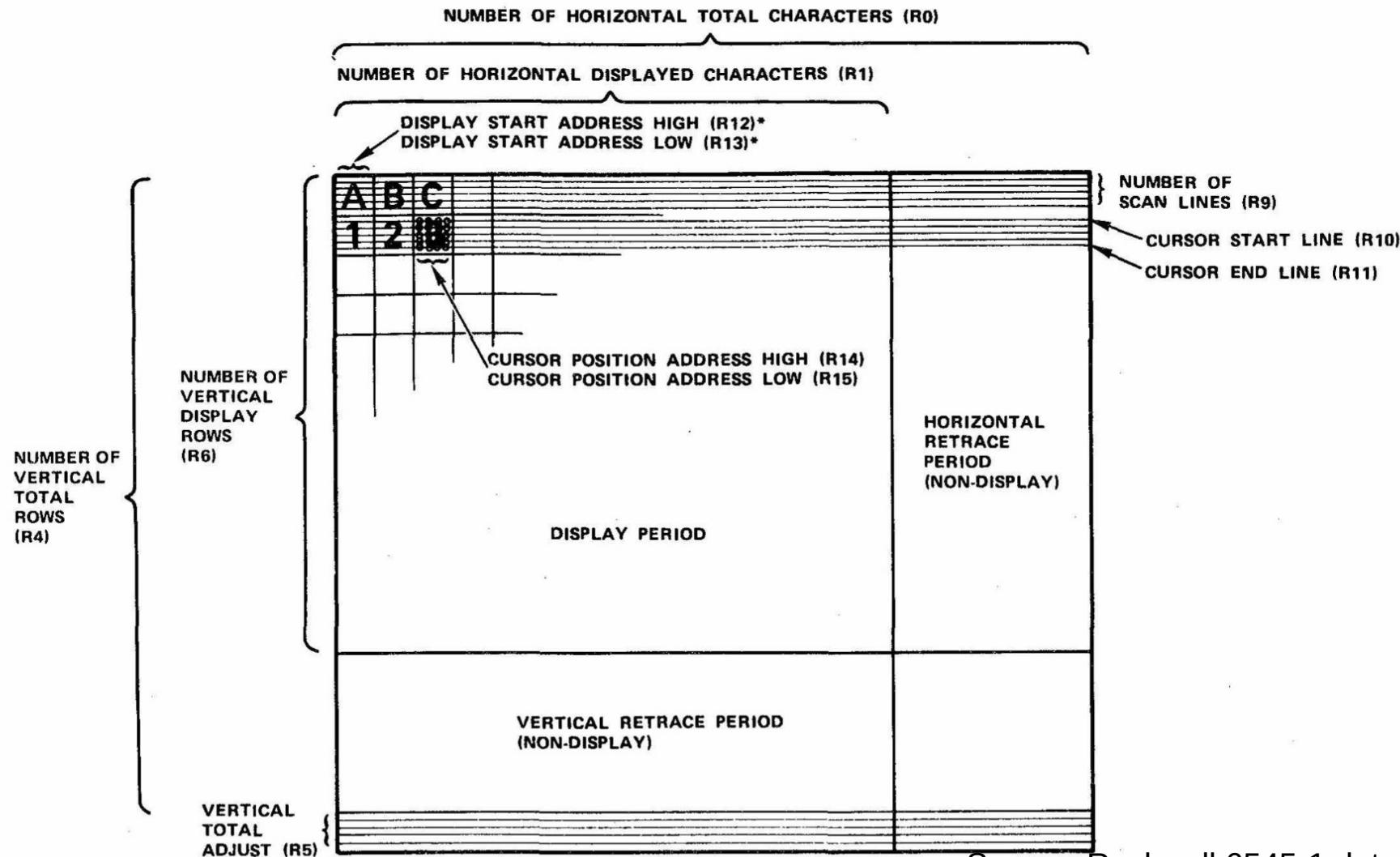
- 40x25 chars
- CRTC timing
- 1k VRAM

8032

- 80x25 chars
- CRTC timing
- 2k VRAM

8296

- 80x25 chars
- CRTC timing
- 4k(+) VRAM



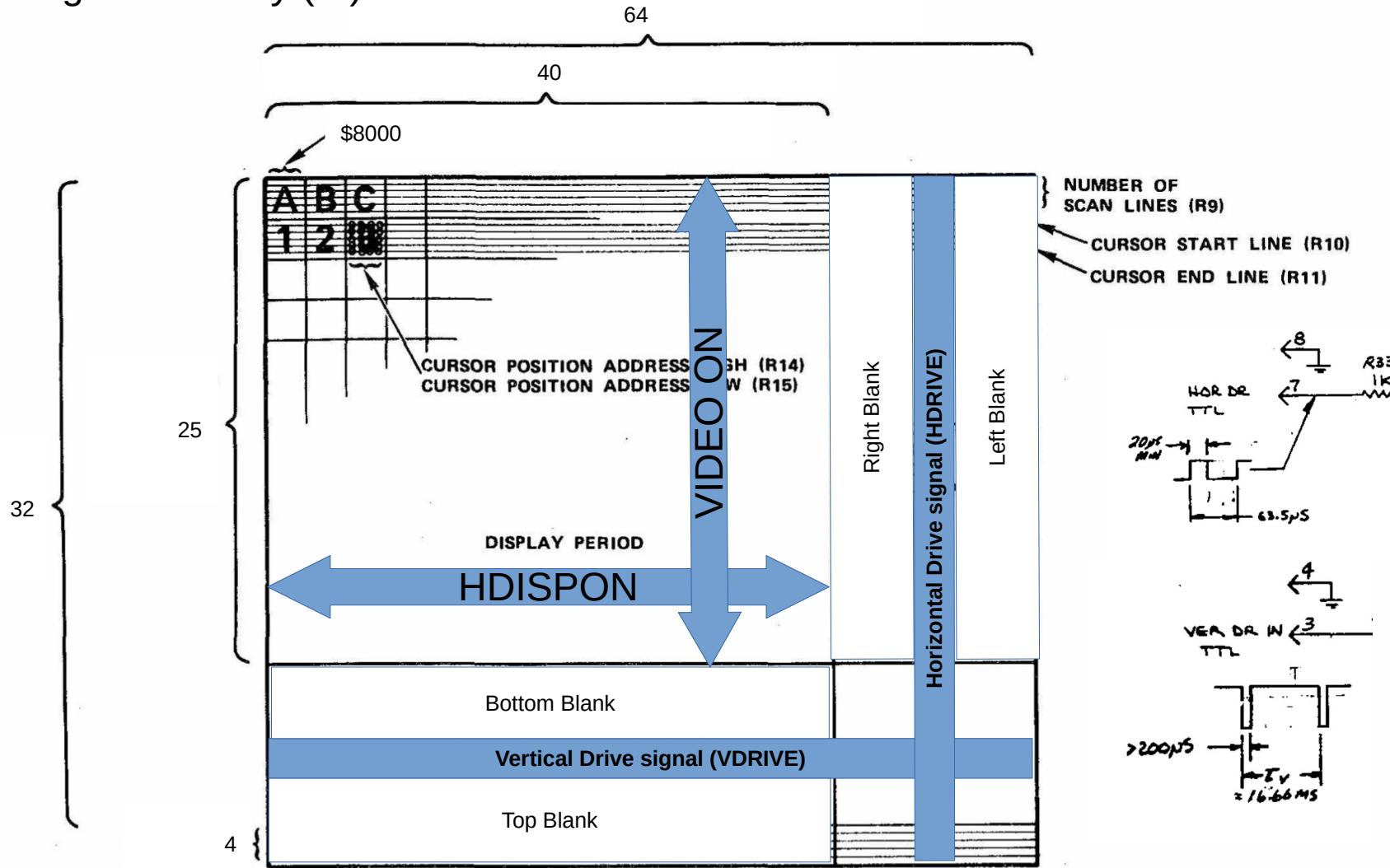
Source: Rockwell 6545-1 datasheet

Original PET

- All static RAM
 - 1k x 4 SRAM chips
 - 1 MHz access time
 - Video created by logic circuits, no „video chip“
-
- 40x25 character
 - B/W
 - Fixed character set
 - „snow“ on screen when accessing screen memory



Fixed video timing on an early (9") PET



Original PET

- All static RAM
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- 1 MHz access time
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- „snow“ on screen when accessing screen mem



Original PET

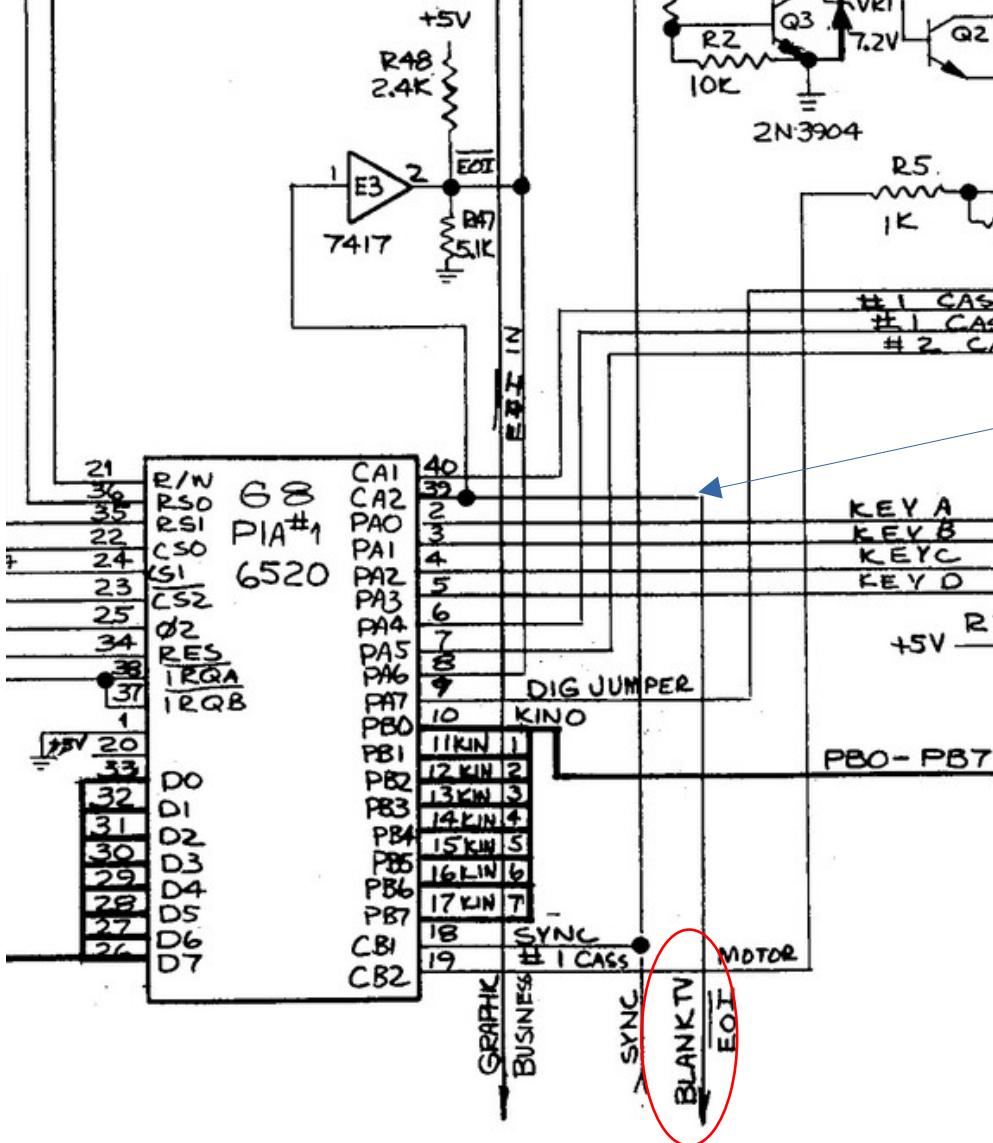
- All static RAM
- 1k x 4 SRAM chips
- **1 MHz access time**
- Video created by logic circuits, no „video chip“
- 40x25 character
- B/W
- Fixed character set
- „snow“ on screen when accessing screen mem



2001 intro and Snow demo

How did Commodore prevent snow?

.C:e35f	A6 FB	LDX \$FB	A:04 X:00 Y:0a SP:e1 ..-....Z.	27570413
.C:e361	F0 02	BEQ \$E365	A:04 X:00 Y:0a SP:e1 ..-....Z.	27570416
.C:e365	20 AC E7	JSR \$E7AC	A:04 X:00 Y:0a SP:e1 ..-....Z.	27570419
.C:e7ac	A8	TAY	A:04 X:00 Y:0a SP:df ..-....Z.	27570425
.C:e7ad	AD 40 E8	LDA \$E840	A:04 X:00 Y:04 SP:df ..-.....	27570427
(C:\$e7b0)	n			
.C:e7b2	D0 F9	BNE \$E7AD	- A:00 X:00 Y:04 SP:df ..-....Z.	27570433
(C:\$e7b2)				
.C:e7b4	98	TYA	- A:00 X:00 Y:04 SP:df ..-....Z.	27570435
(C:\$e7b4)				
.C:e7b5	A4 E2	LDY \$E2	- A:04 X:00 Y:04 SP:df ..-.....	27570437
(C:\$e7b5)				
.C:e7b7	91 E0	STA (\$E0),Y	- A:04 X:00 Y:0A SP:df ..-.....	27570440
(C:\$e7b7)				
.C:e7b9	60	RTS	- A:04 X:00 Y:0A SP:df ..-.....	27570446
(C:\$e7b9)				

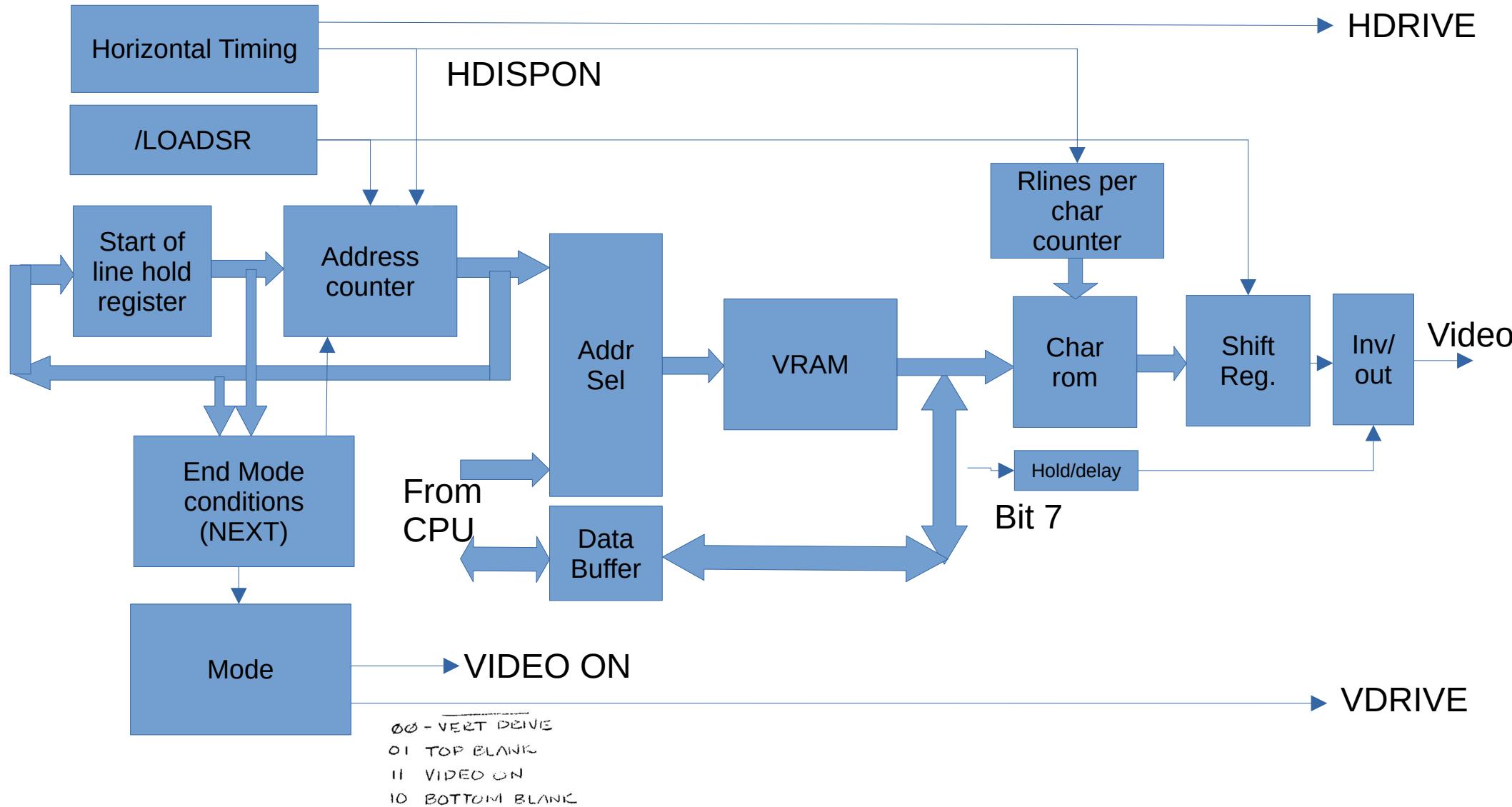


Original PET

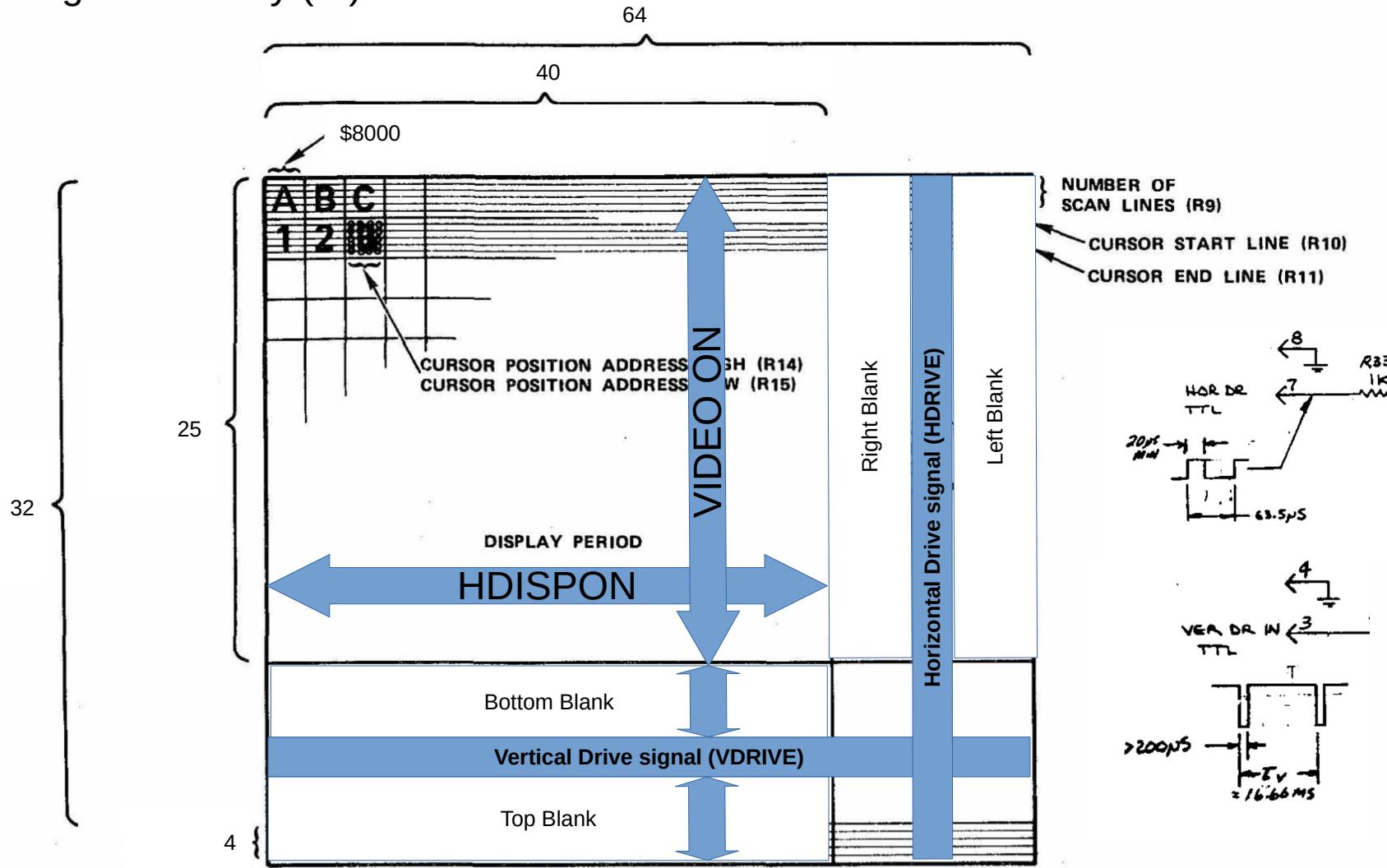
- All static RAM
 - 1k x 4 SRAM chips
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 - Video created by logic circuits, no „video chip“
-
- 40x25 character
 - B/W
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 - „snow“ on screen when accessing screen memory

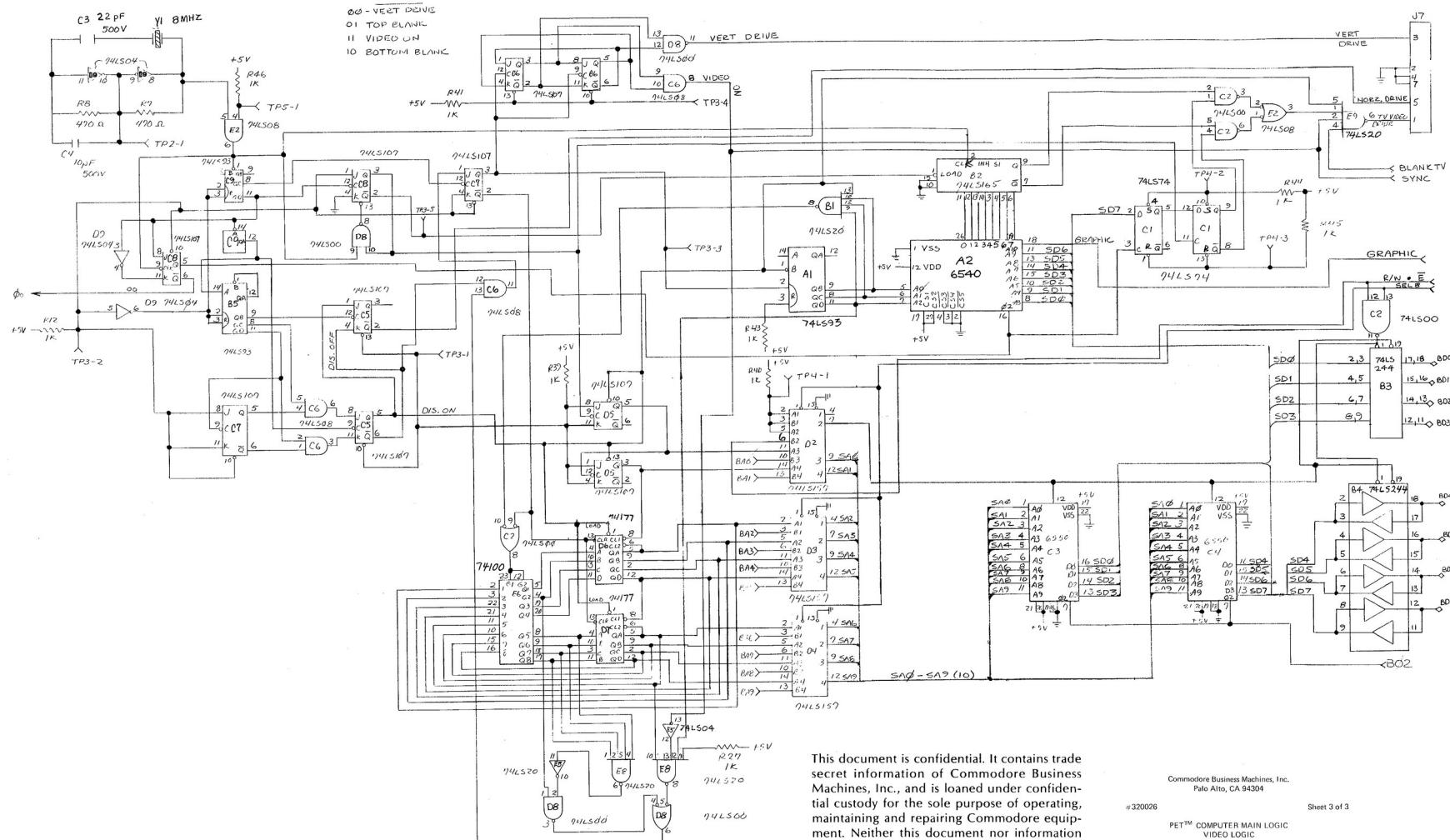


Theory of Operation



Fixed video timing on an early (9") PET





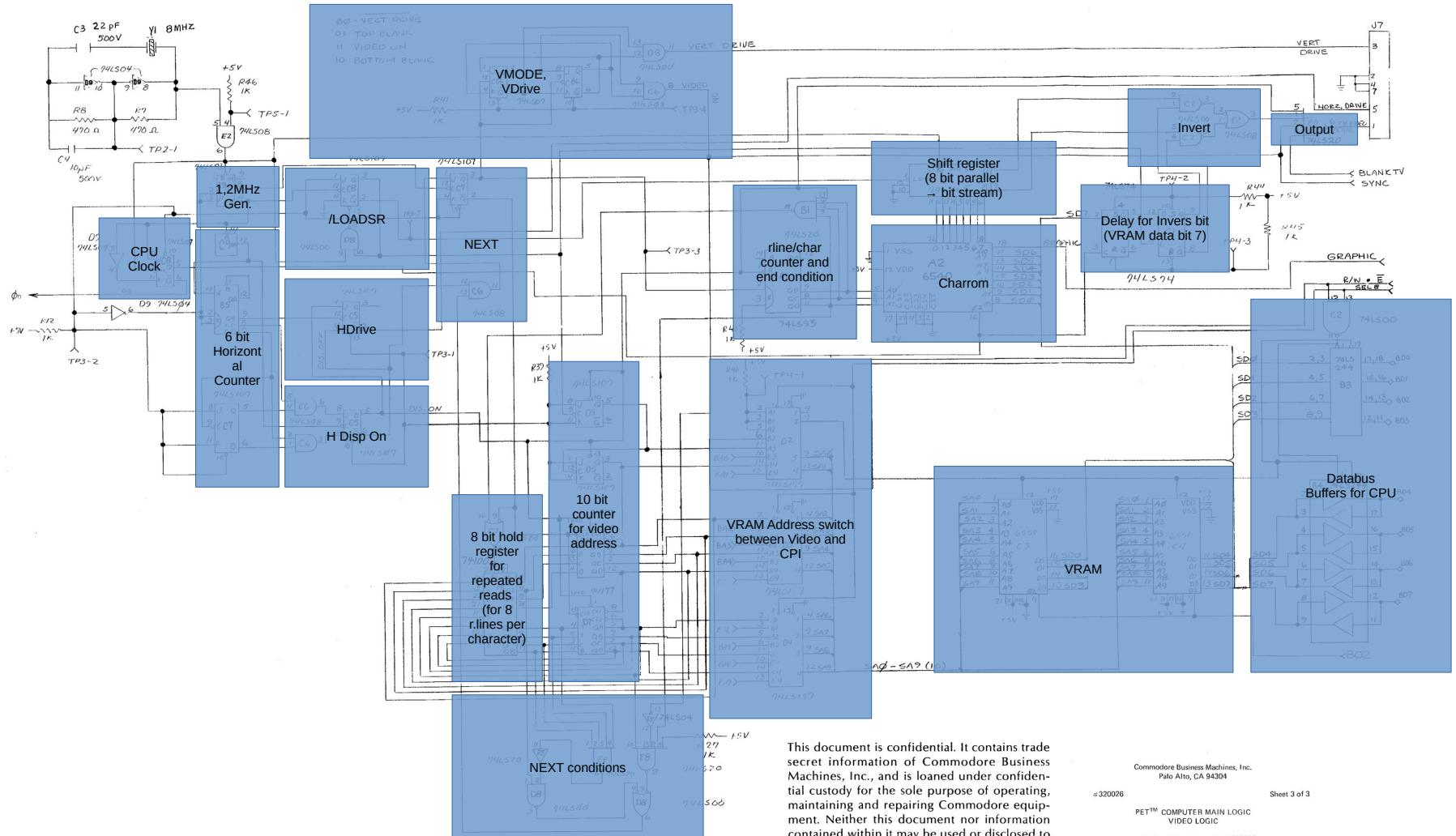
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PET™ COMPUTER MAIN LOGIC
VIDEO LOGIC

pertaining to board assembly #320008

NOTE: All locations are same on all boards; only the specific components will differ on boards numbered 320132, 320081, 3232008, 3232008B.



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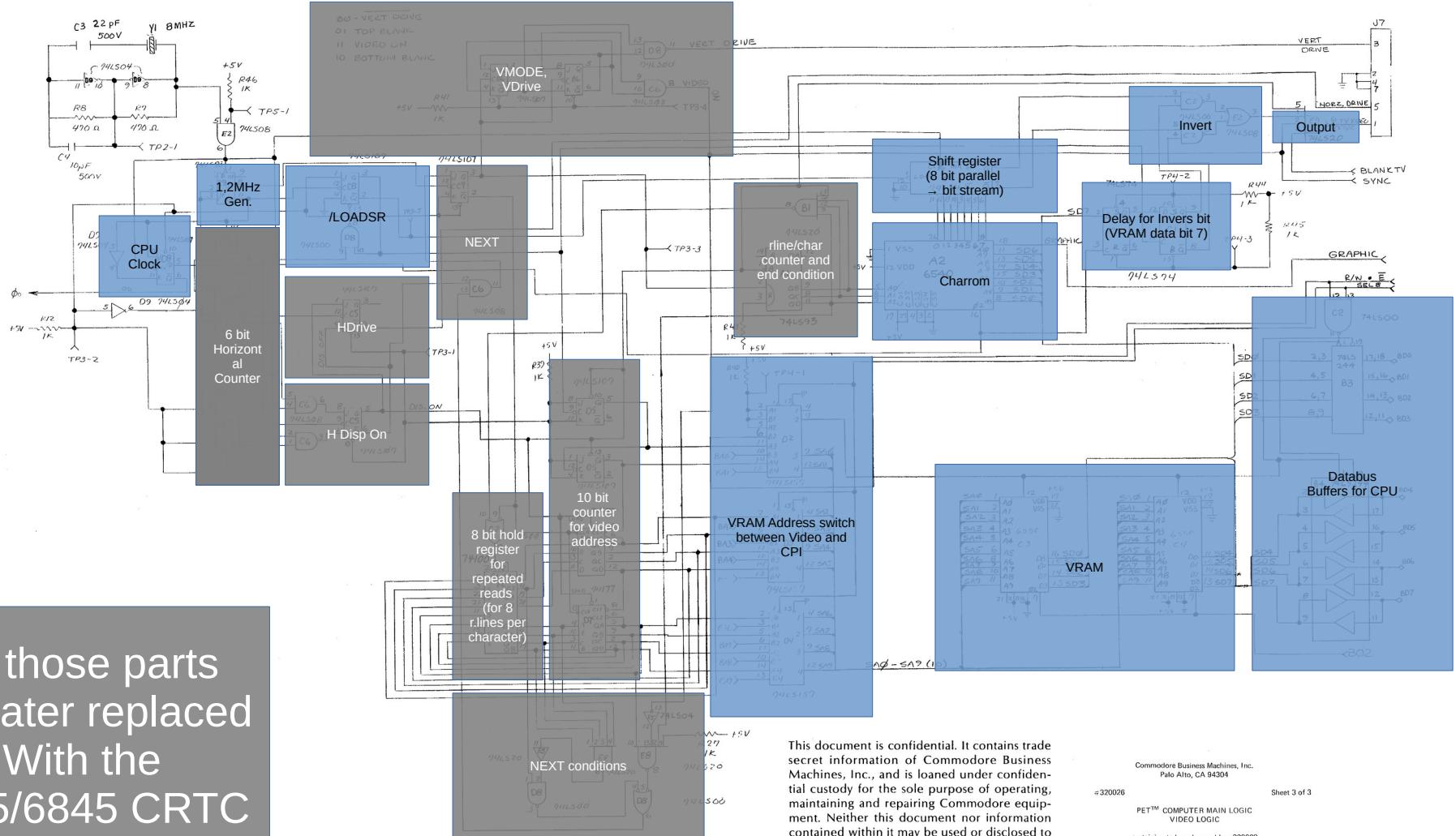
Sheet 3 of 3

PET™ COMPUTER MAIN LOGIC

pertaining to board assembly #320008

NOTE: All locations are same on all boards; only the specific components will differ on boards numbered 320132, 320081, 320133, 320008.

All those parts
Are later replaced
With the
6545/6845 CRTC



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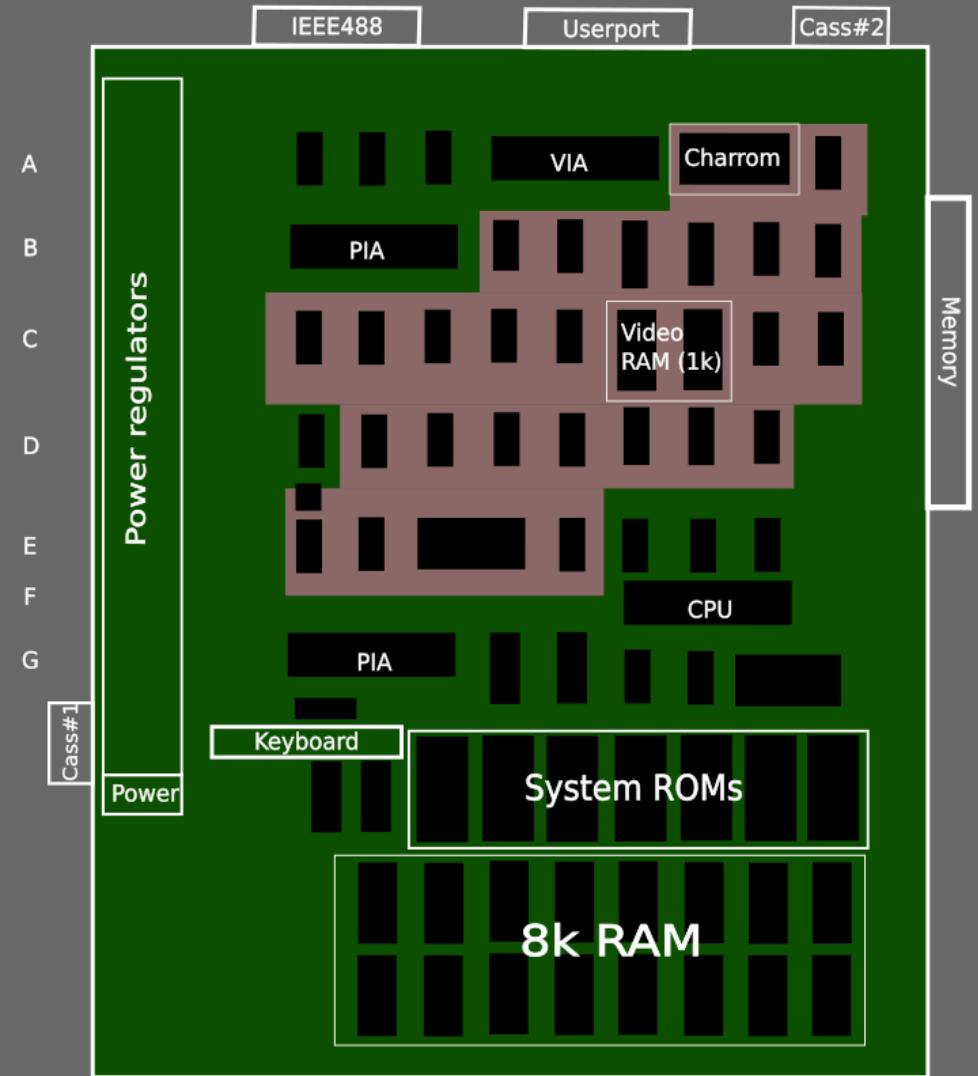
Commodore Business Machines, Inc.
Palo Alto, CA 94304

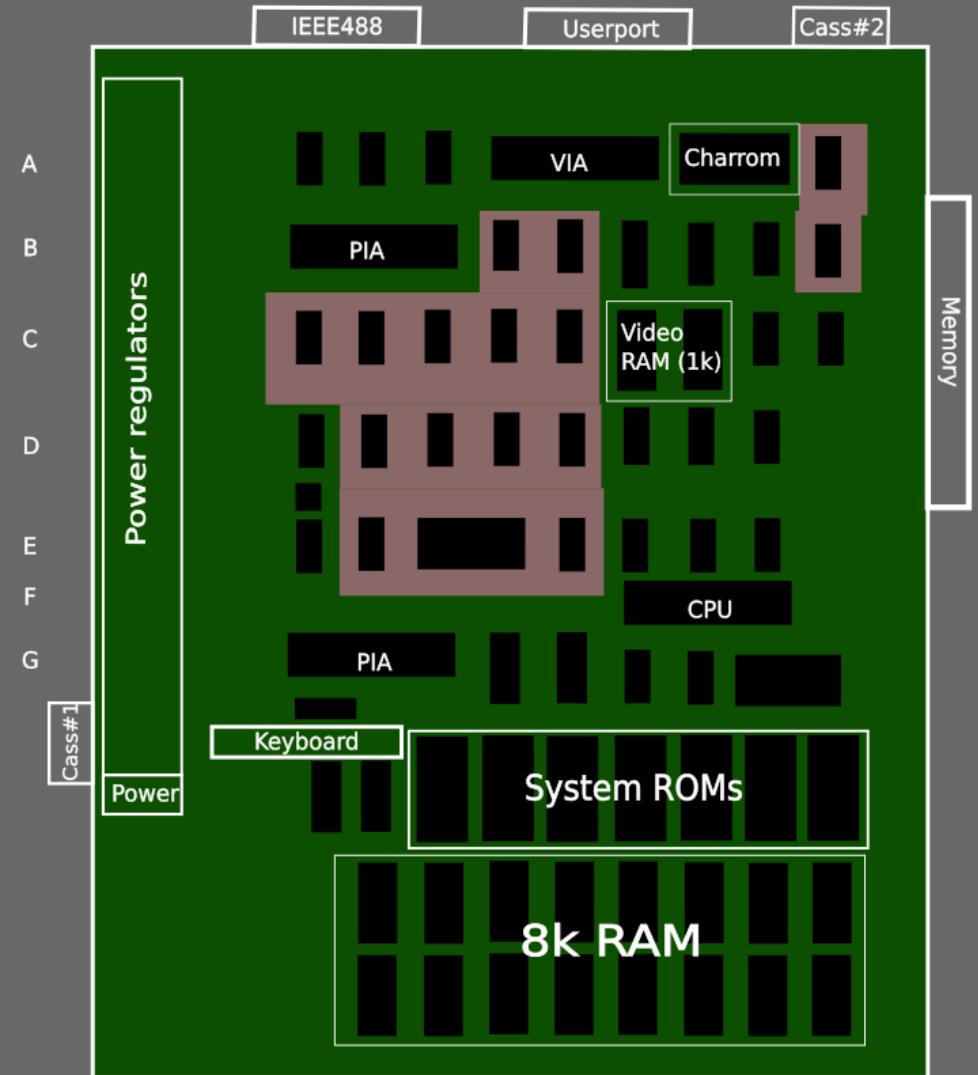
Sheet 3 of 3

PET™ COMPUTER MAIN LOGIC VIDEO LOGIC

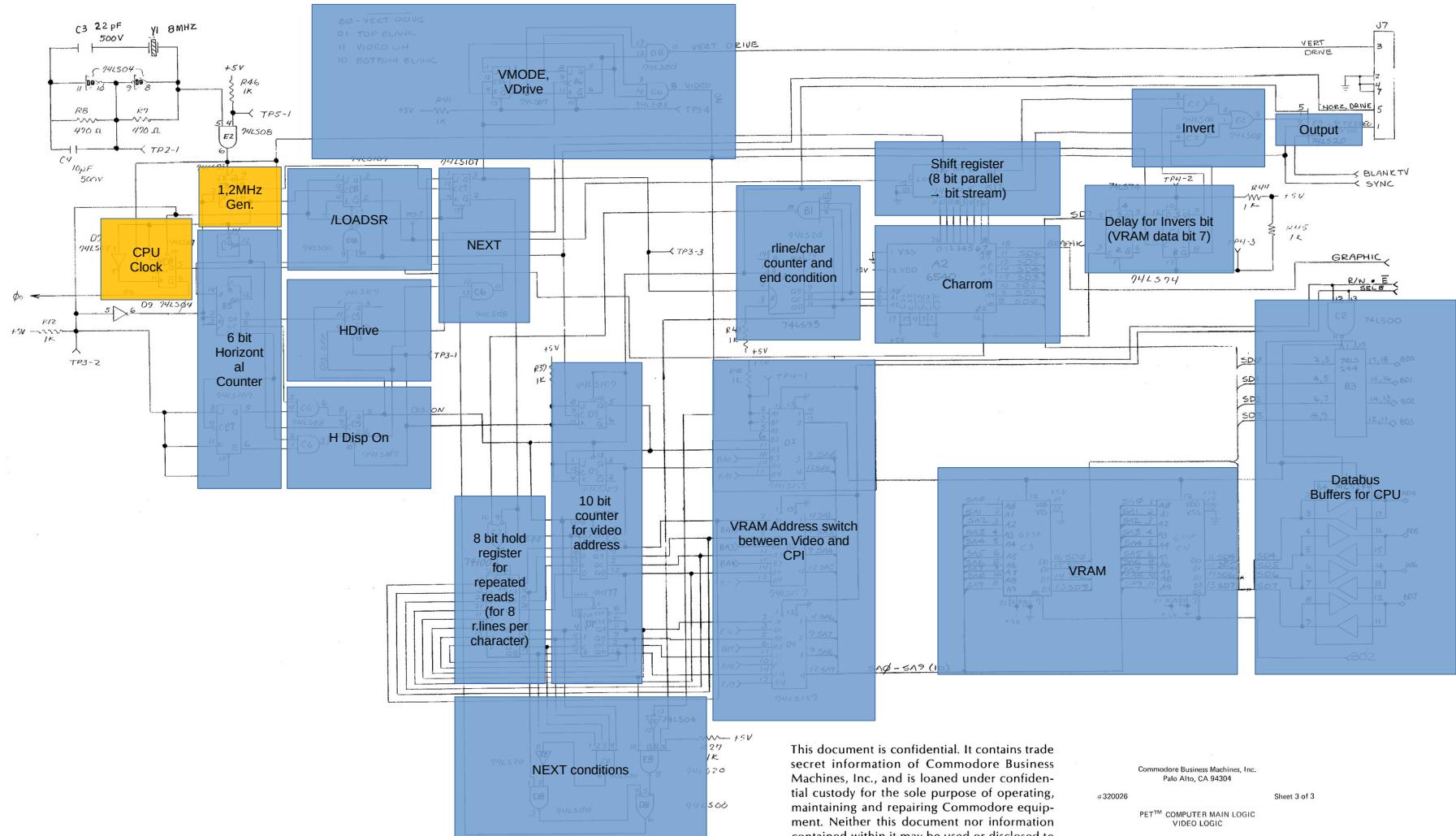
pertaining to board assembly #320008

NOTE: All locations are same on all boards; only the specific components will differ on boards numbered 320132, 320081, 320137, 320008.
The identifying board number is in upper left corner.





Clock gen



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#320026

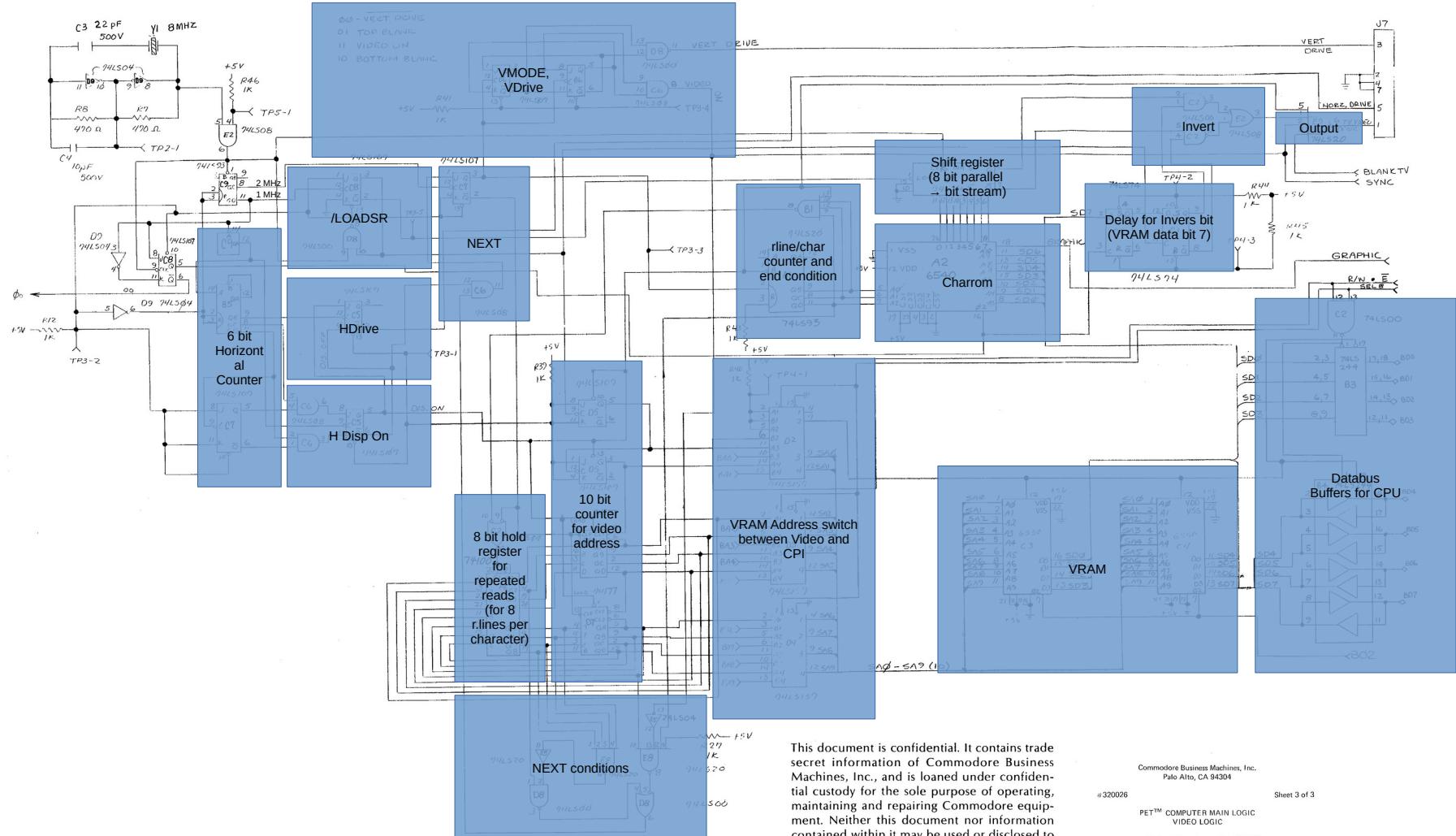
Sheet 3 of 3

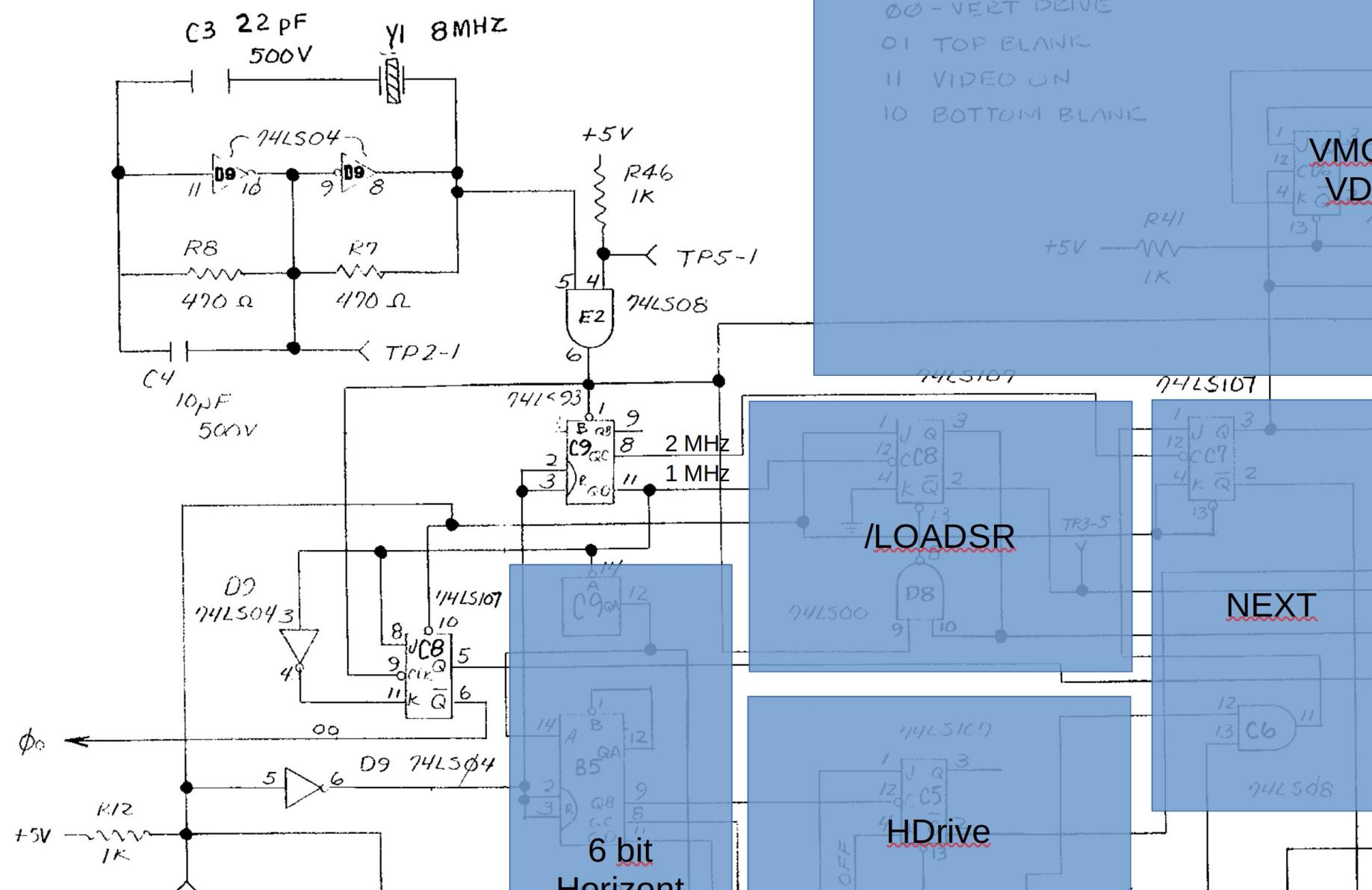
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VIDEO LOGIC

pertaining to board assembly #320008

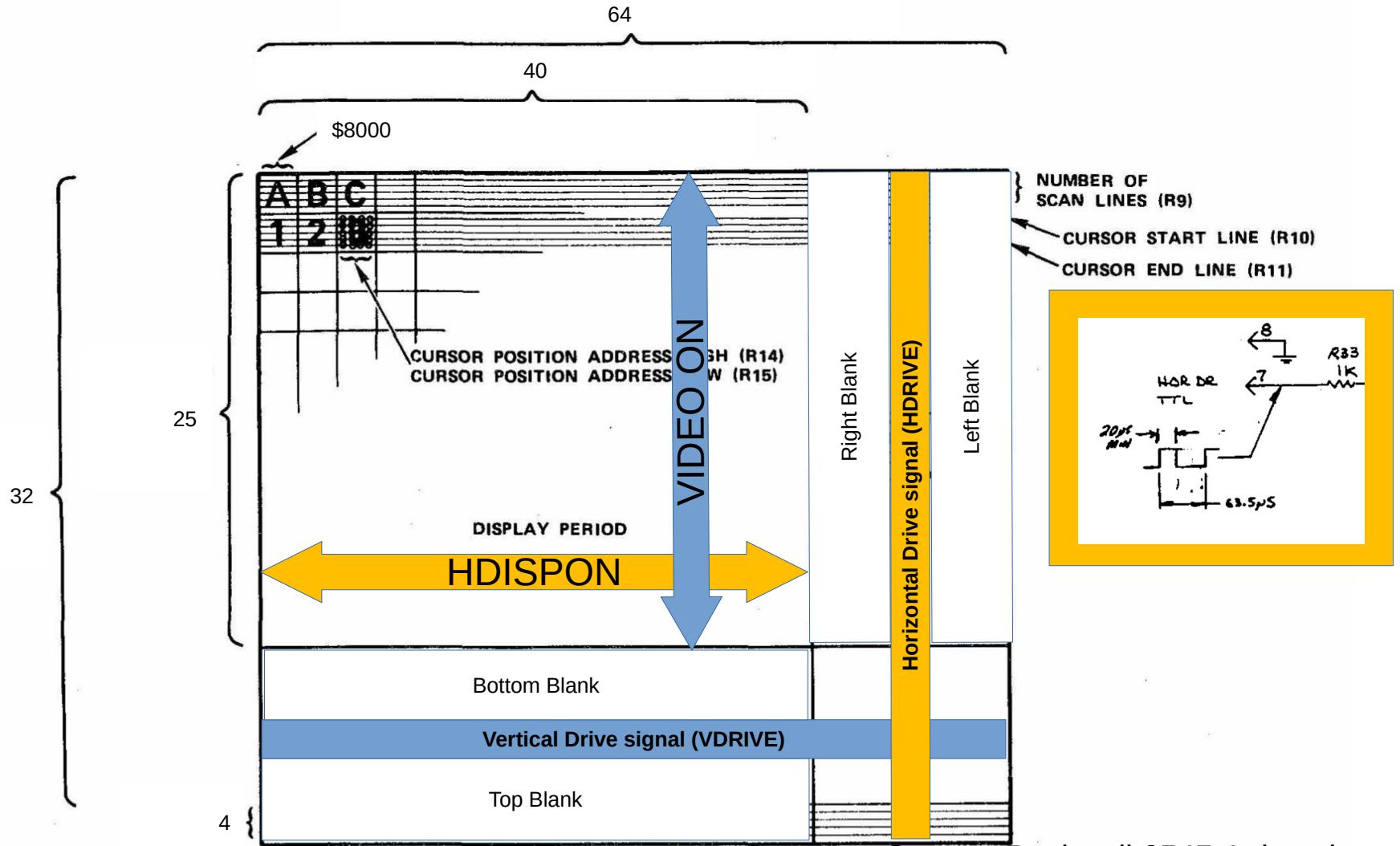
NOTE: All locations are same on all boards; only the specific components will differ on boards numbered 320132, 320081, 320137, 320008.

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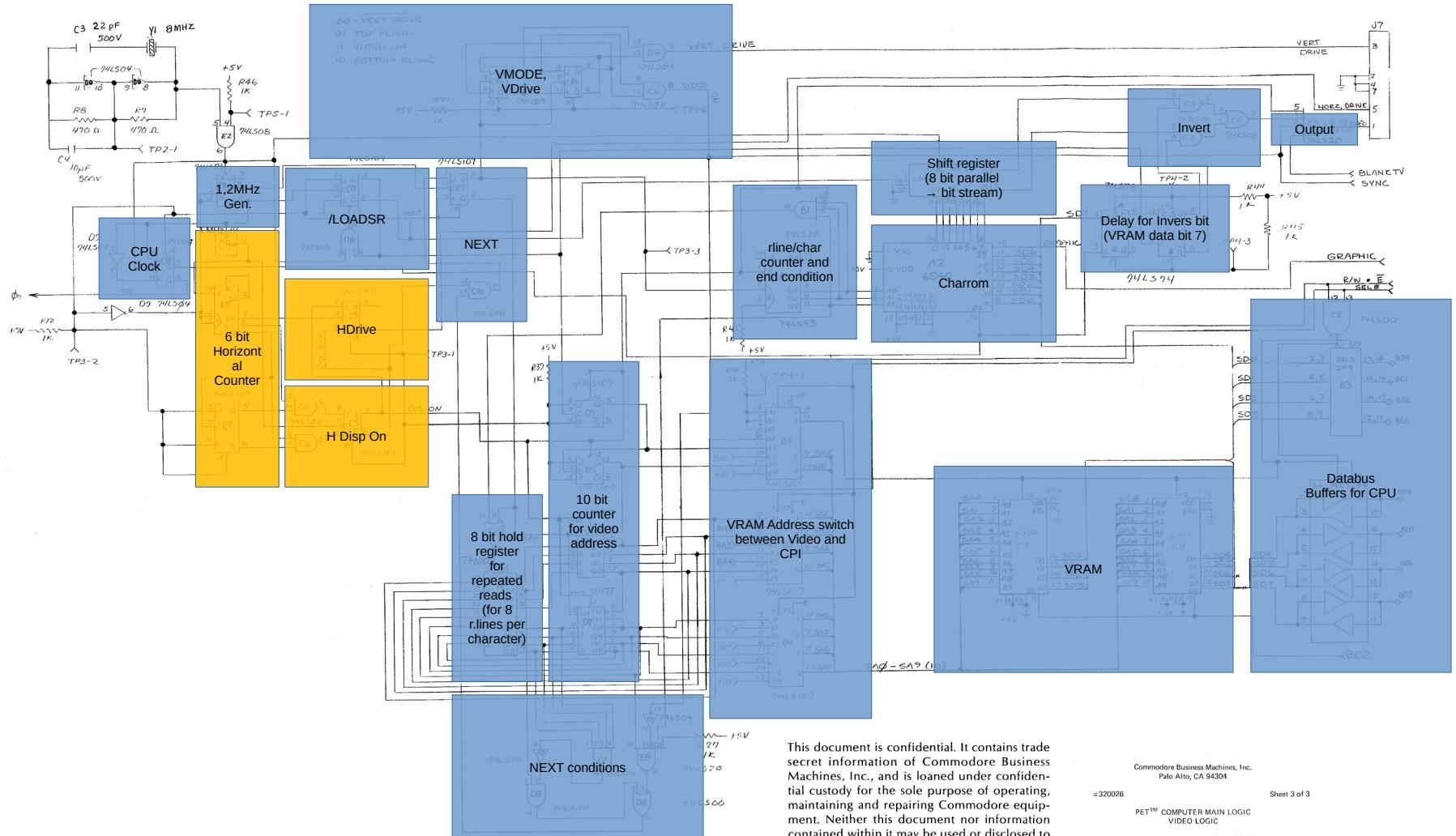




Horizontal timing



Source: Rockwell 6545-1 datasheet



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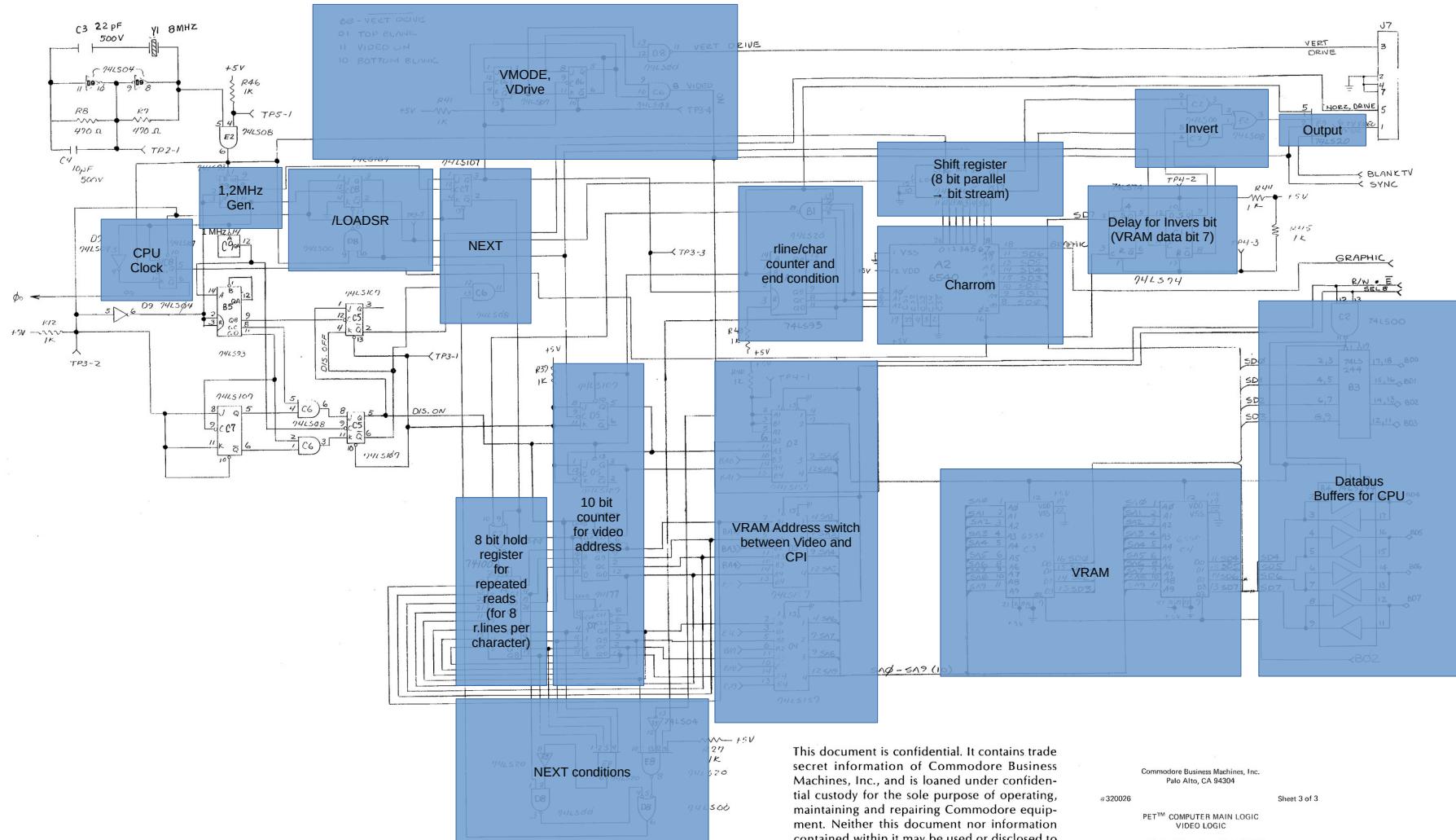
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pertaining to board assembly #320008

NOTE: All locations are same on all boards; only the specific components will differ on boards numbered 320132, 320081, 32032008.



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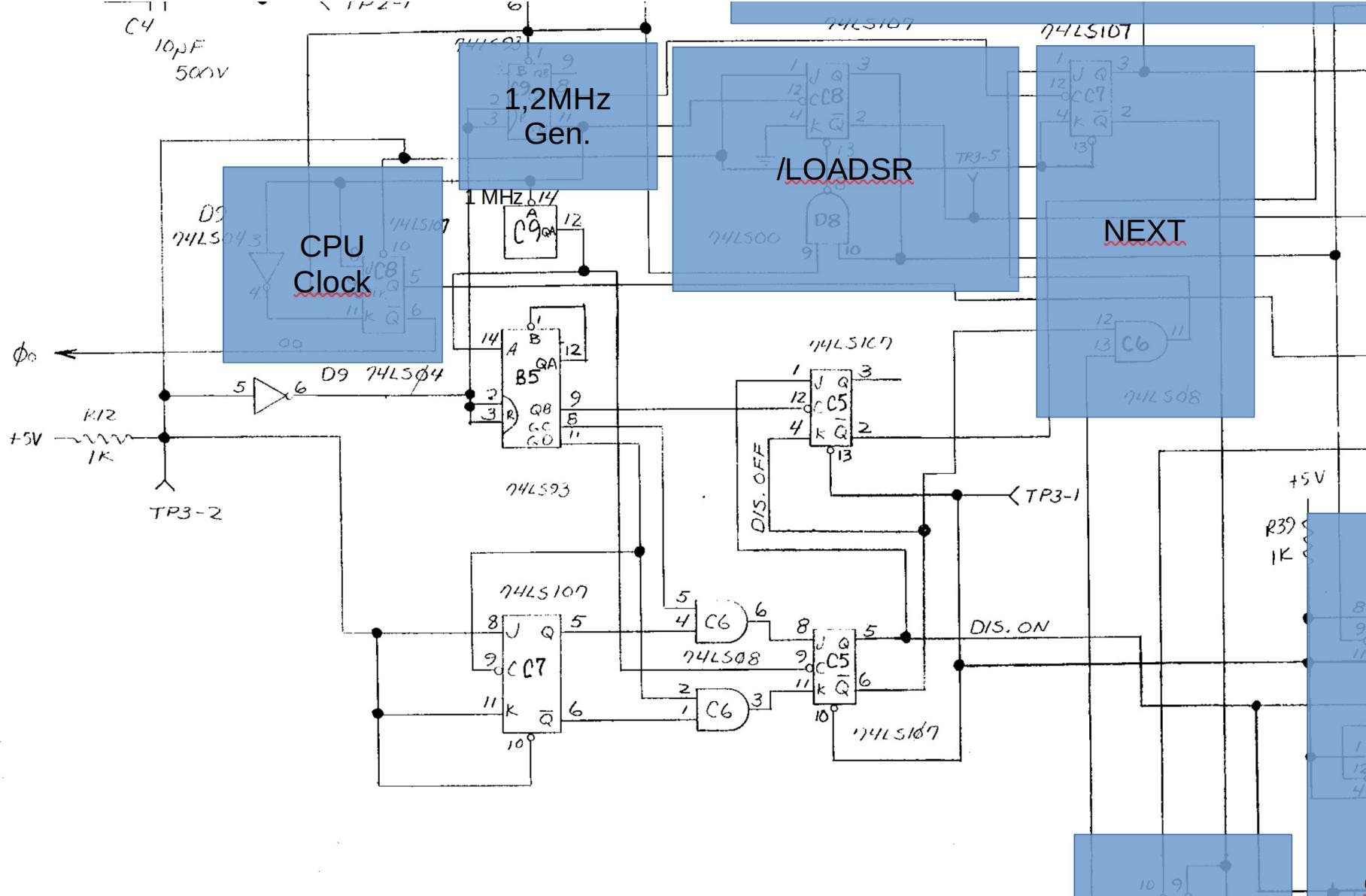
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pertaining to board assembly #320008

NOTE: All locations are same on all boards; only the specific components will differ on boards numbered 320132, 320081, 320137, 320008.



4 8 12 16 20 24 28 32 36 40 44 48 52 56 60 64

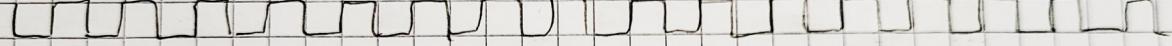
C9.11



C9.12



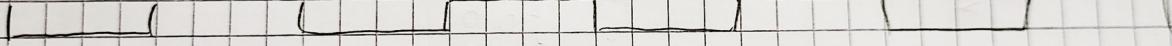
BS.12



BS.9



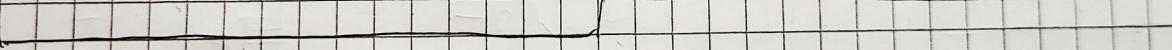
BS.8



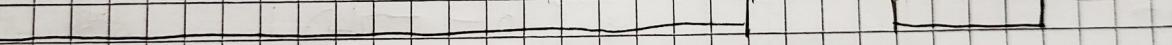
BS.11



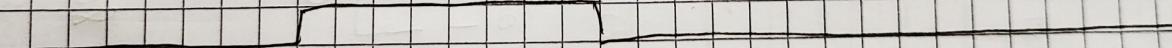
C7.5



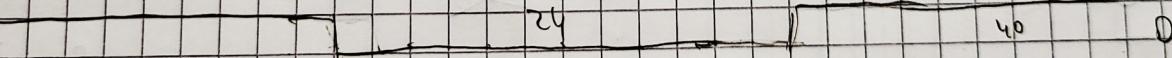
J6 = BS.8 & C7.5



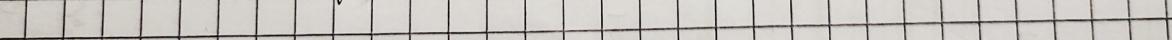
J5 = BS.11 & C7.5



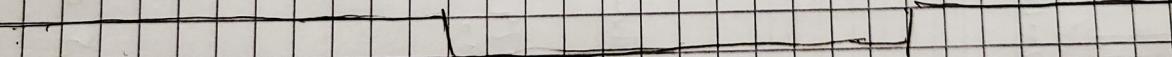
S.5
J=66
> C9.12



K=11



J3 -> D04
> BS.3

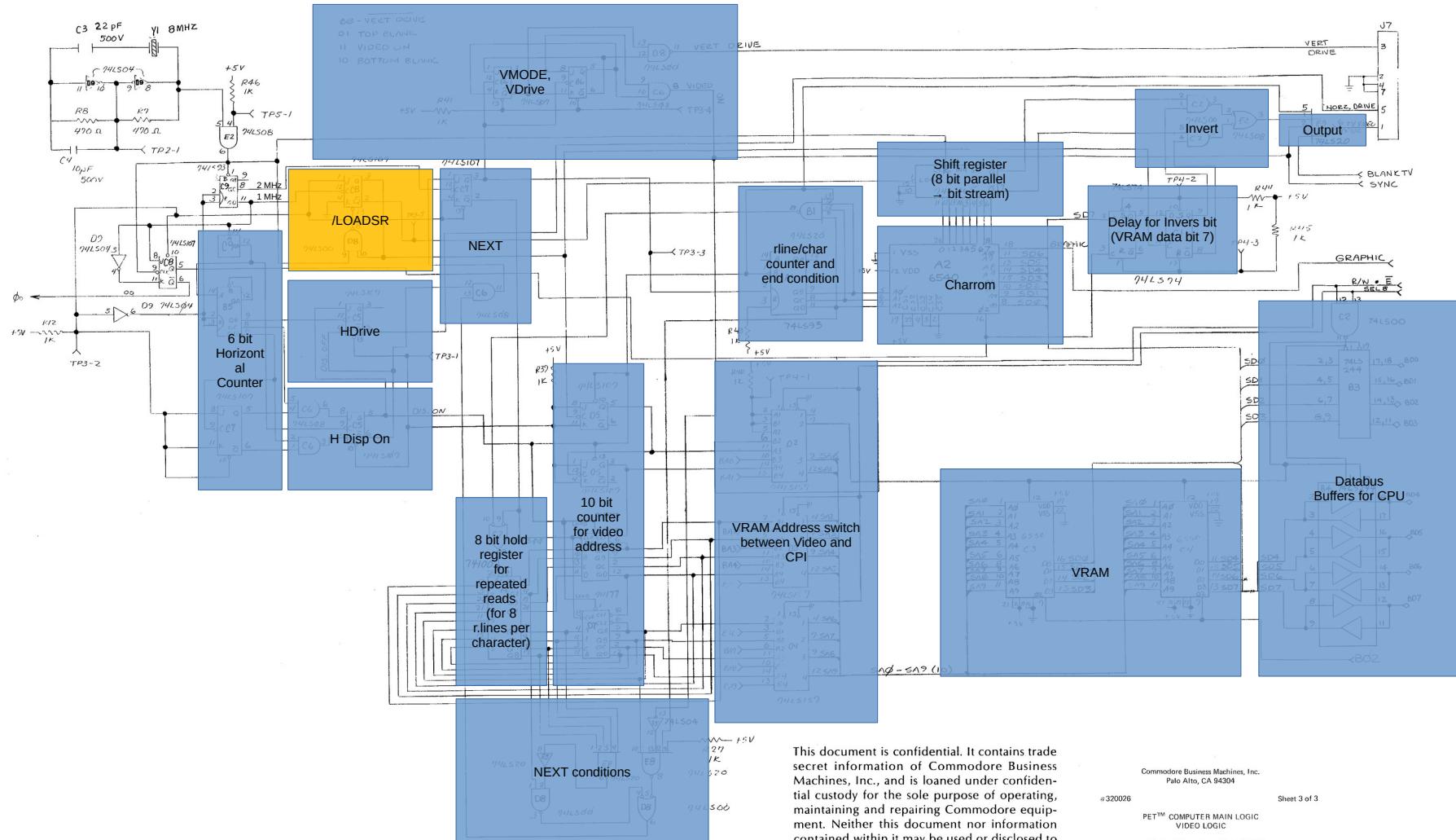


K=00FF

HDISPON

VDRIVE

Shift register control



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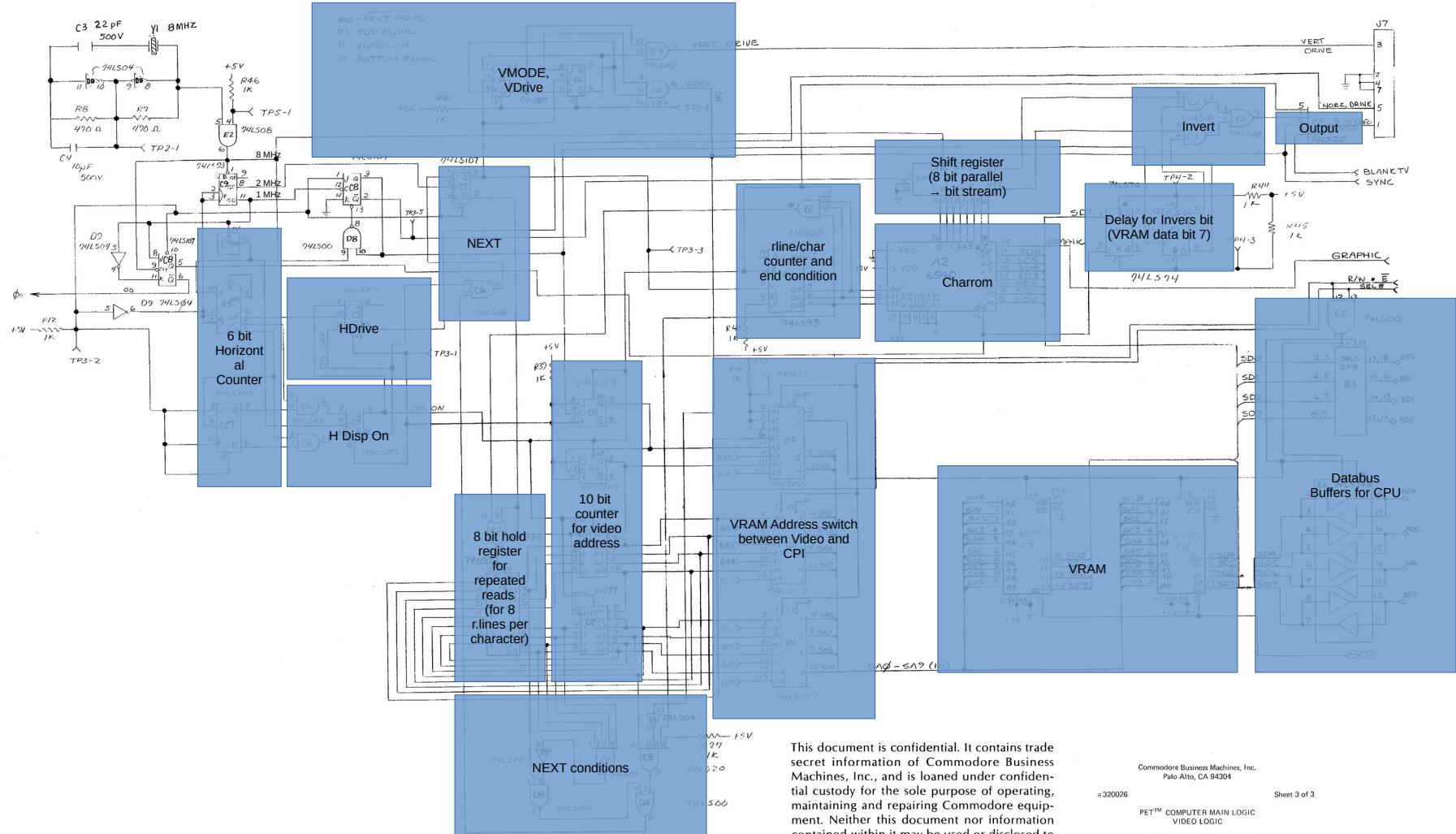
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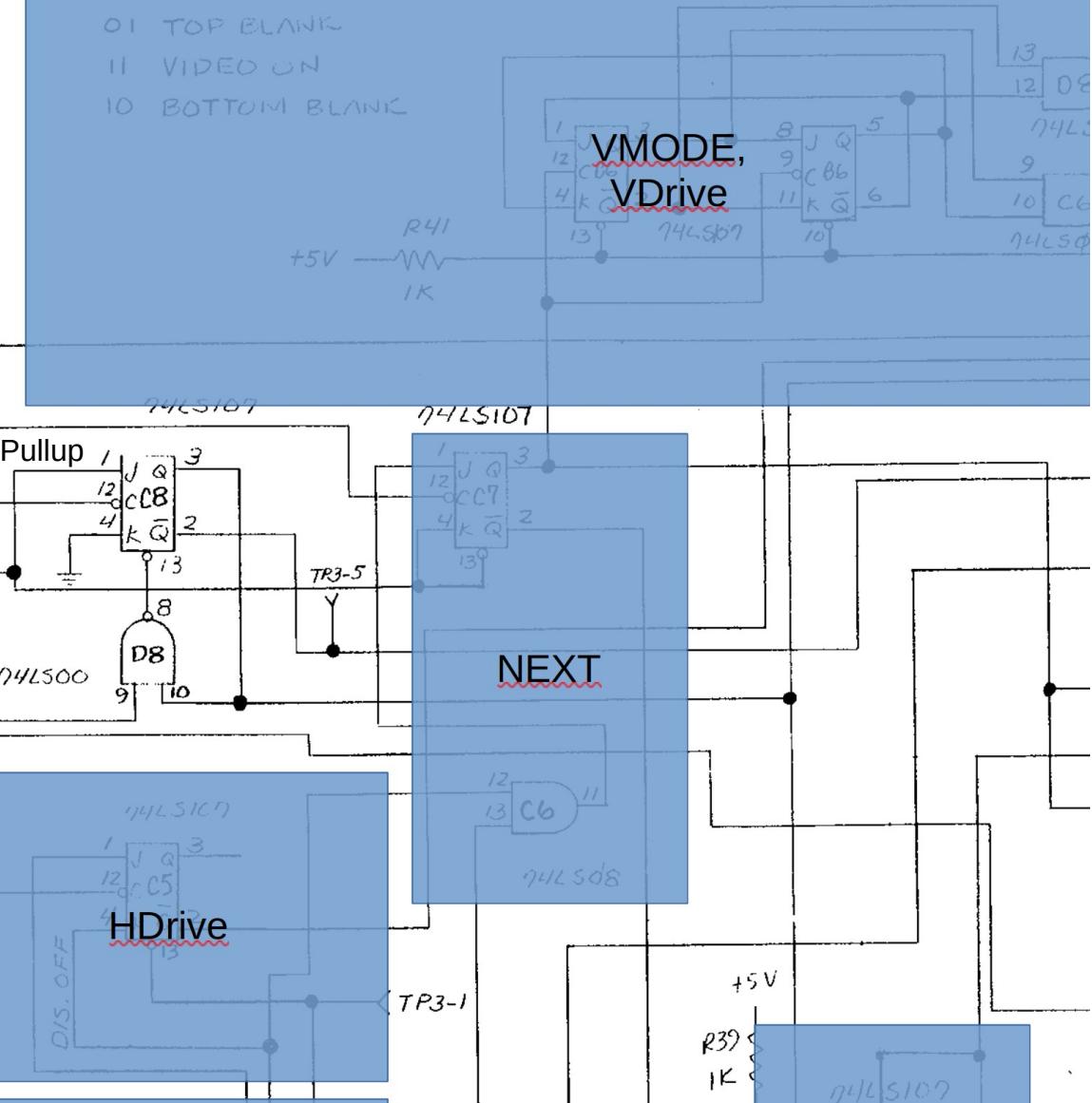
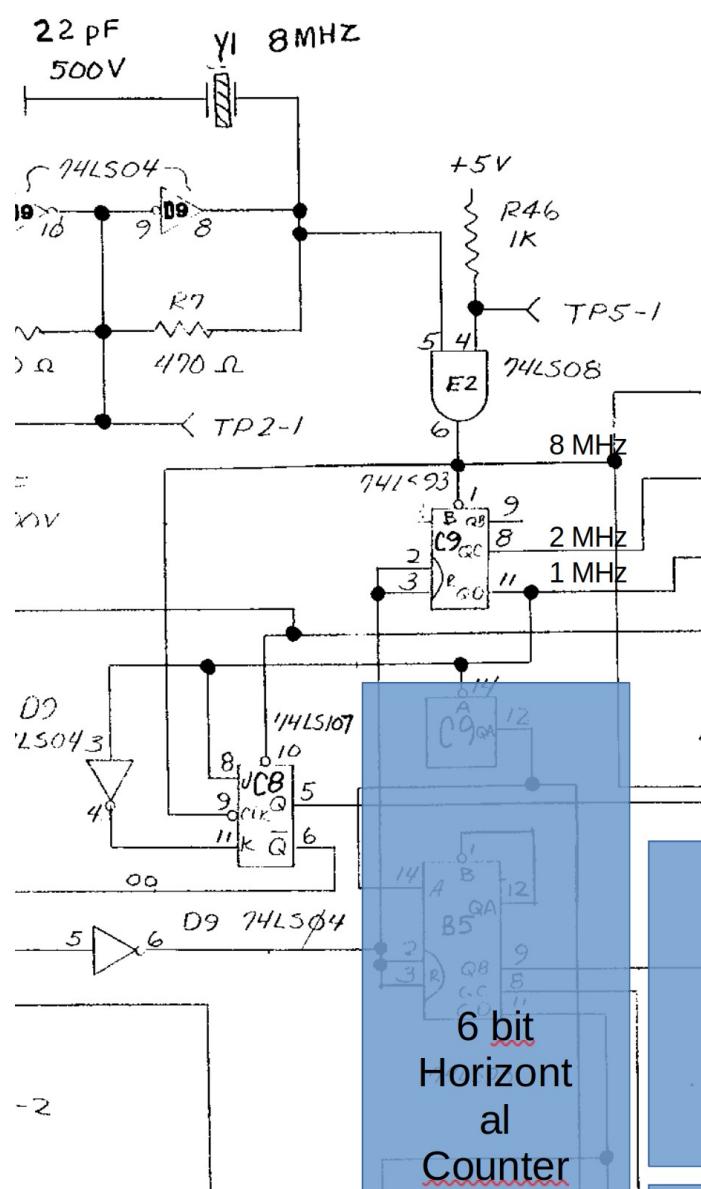
2186

PET™ COMPUTER MAIN LOGIC

pertaining to board assembly #32000

NOTE: All locations are same on all boards; only the spec





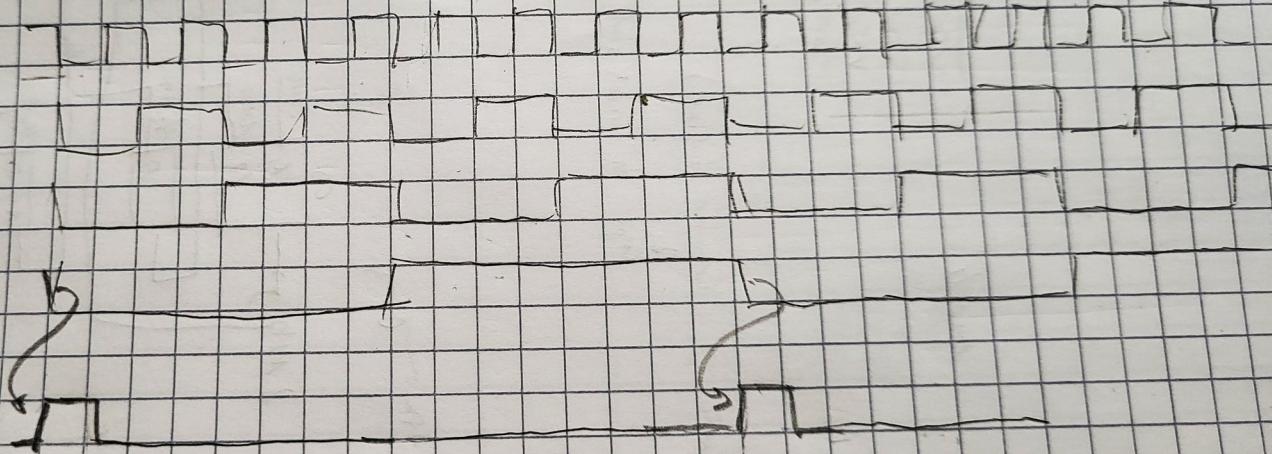
8M

C3S (4m)

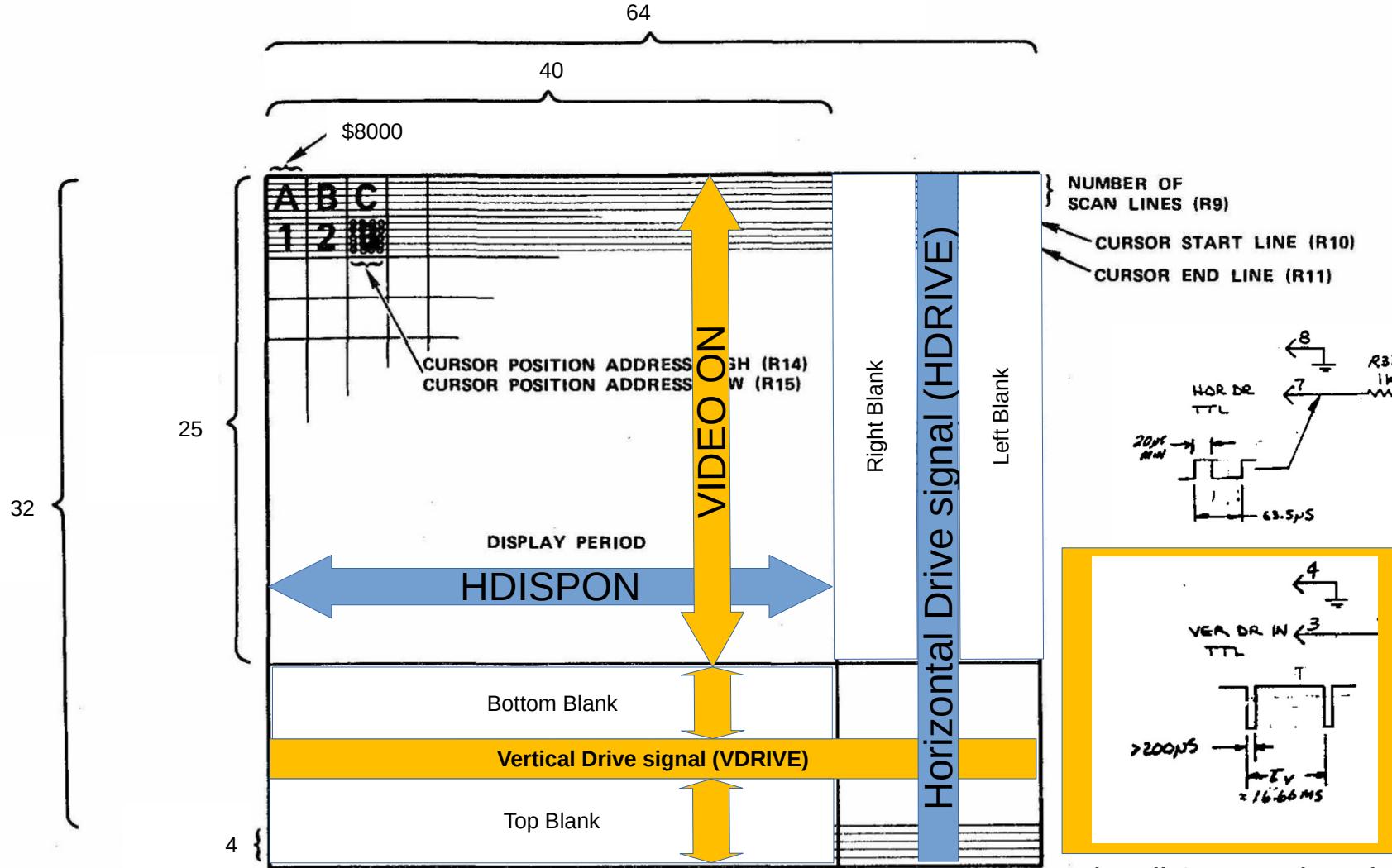
(58) (2m)

(9H) (1m)

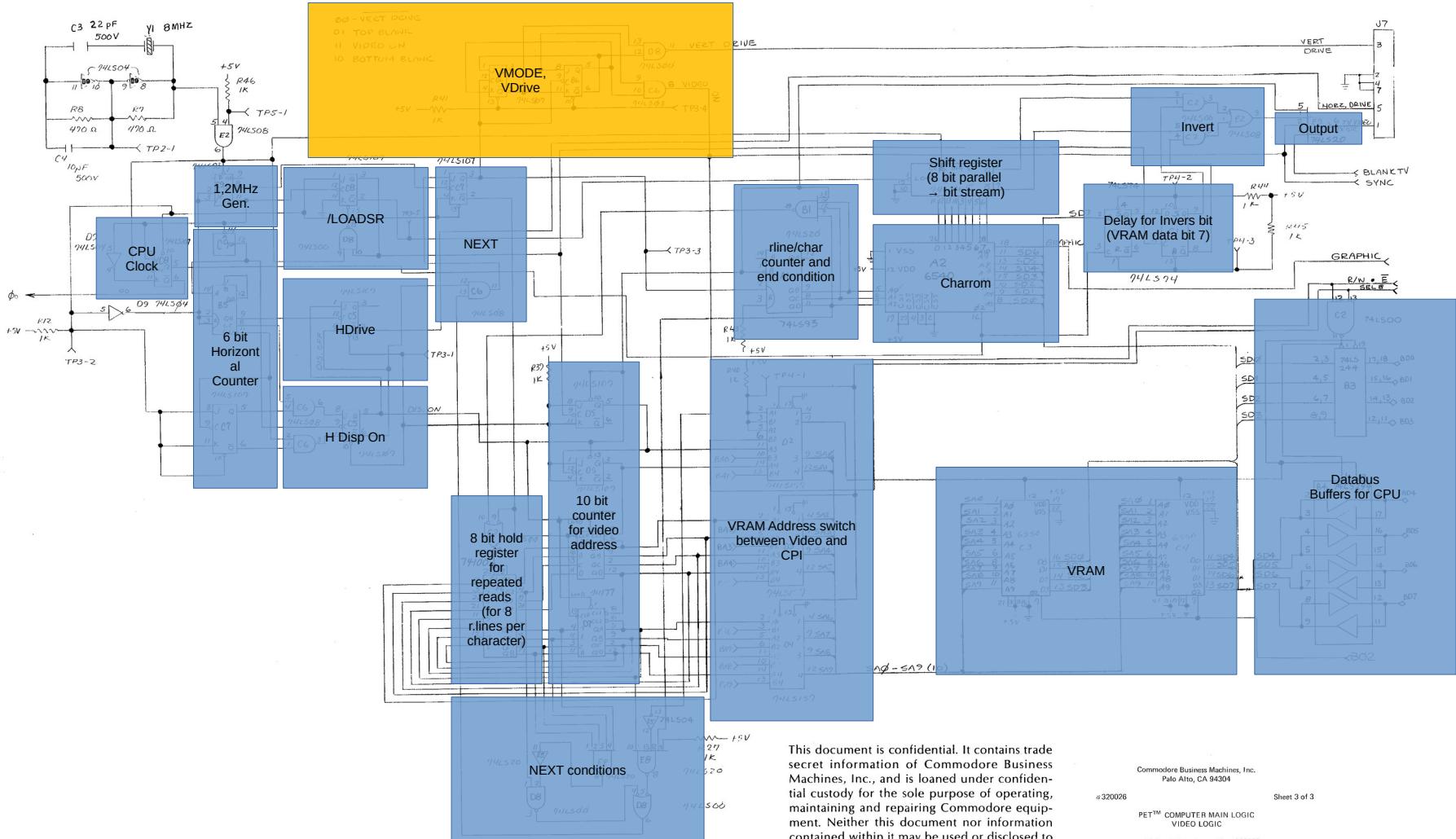
(8-3) ^{Am}



Mode



Source: Rockwell 6545-1 datasheet



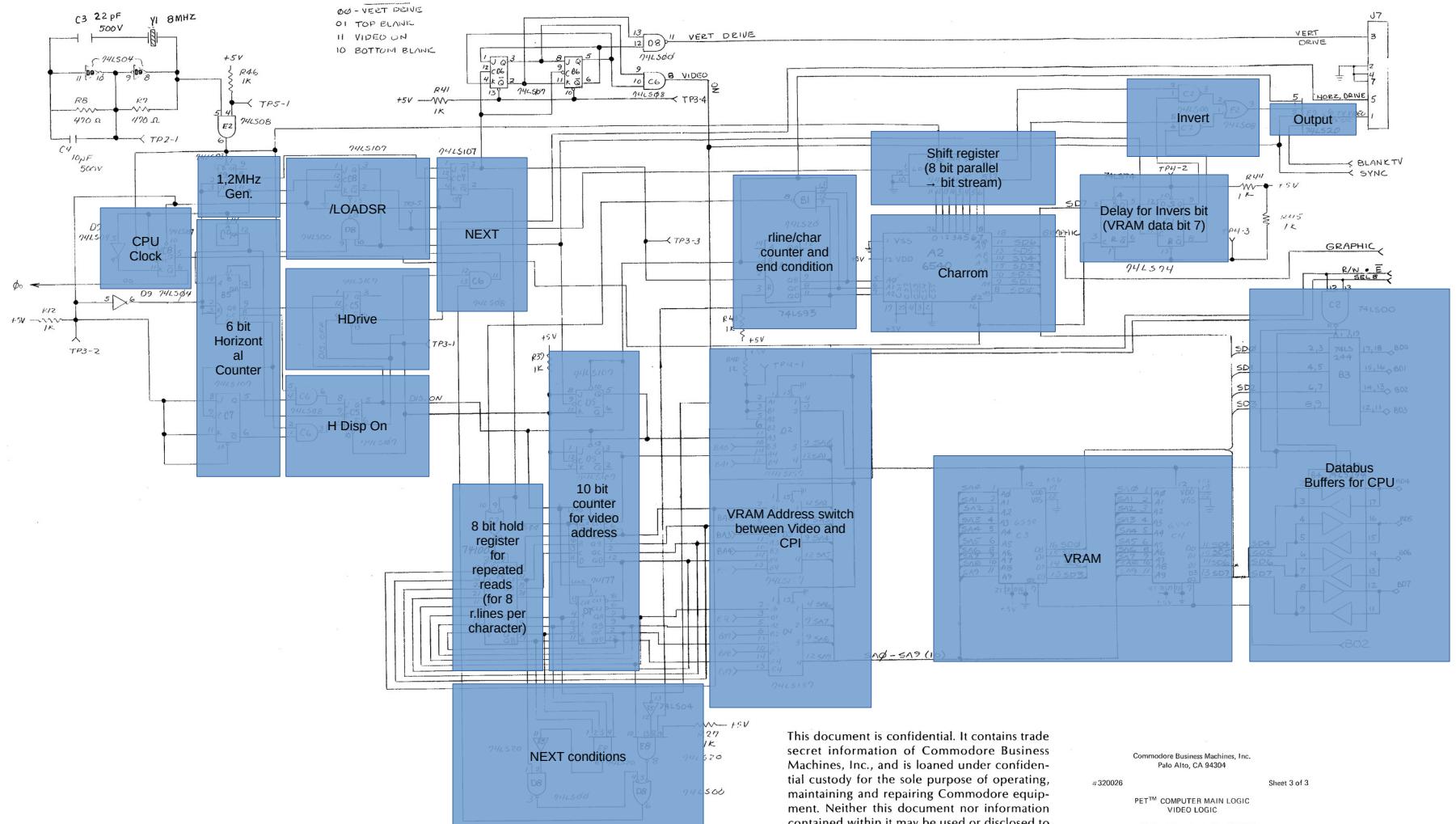
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#320026

Sheet 3 of 3

PET™ COMPUTER MAIN LOGIC
VIDEO LOGIC

pertaining to board assembly #320008



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Sheet 3 of 3

PET™ COMPUTER MAIN LOGIC
VIDEO LOGIC

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NOTE: All locations are same on all boards; only the specific components will differ on boards numbered 320132, 320081, 320137, 320008.

00 - VERT DRIVE

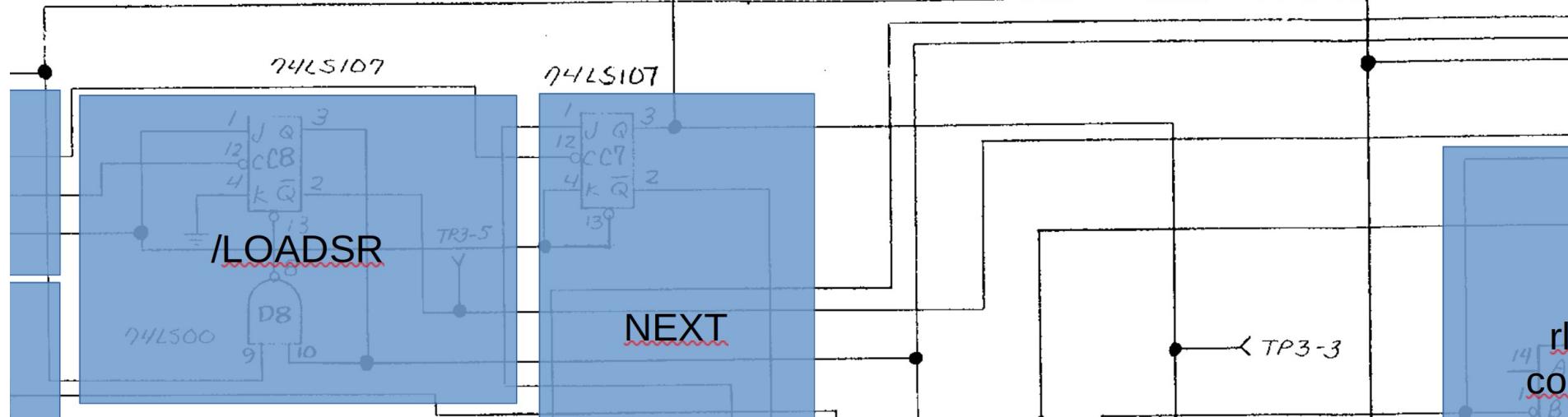
01 TOP BLANK

11 VIDEO ON

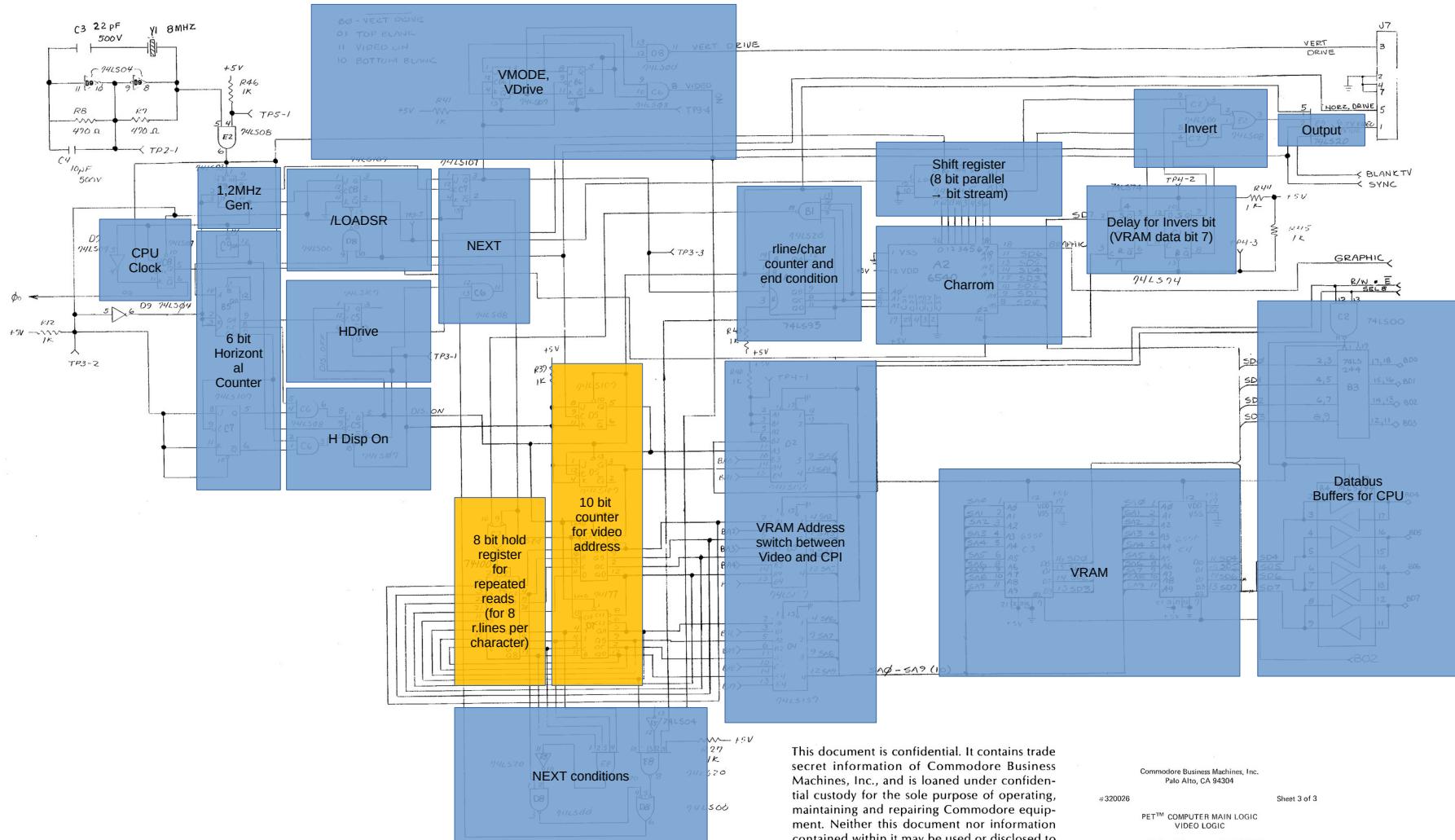
10 BOTTOM BLANK

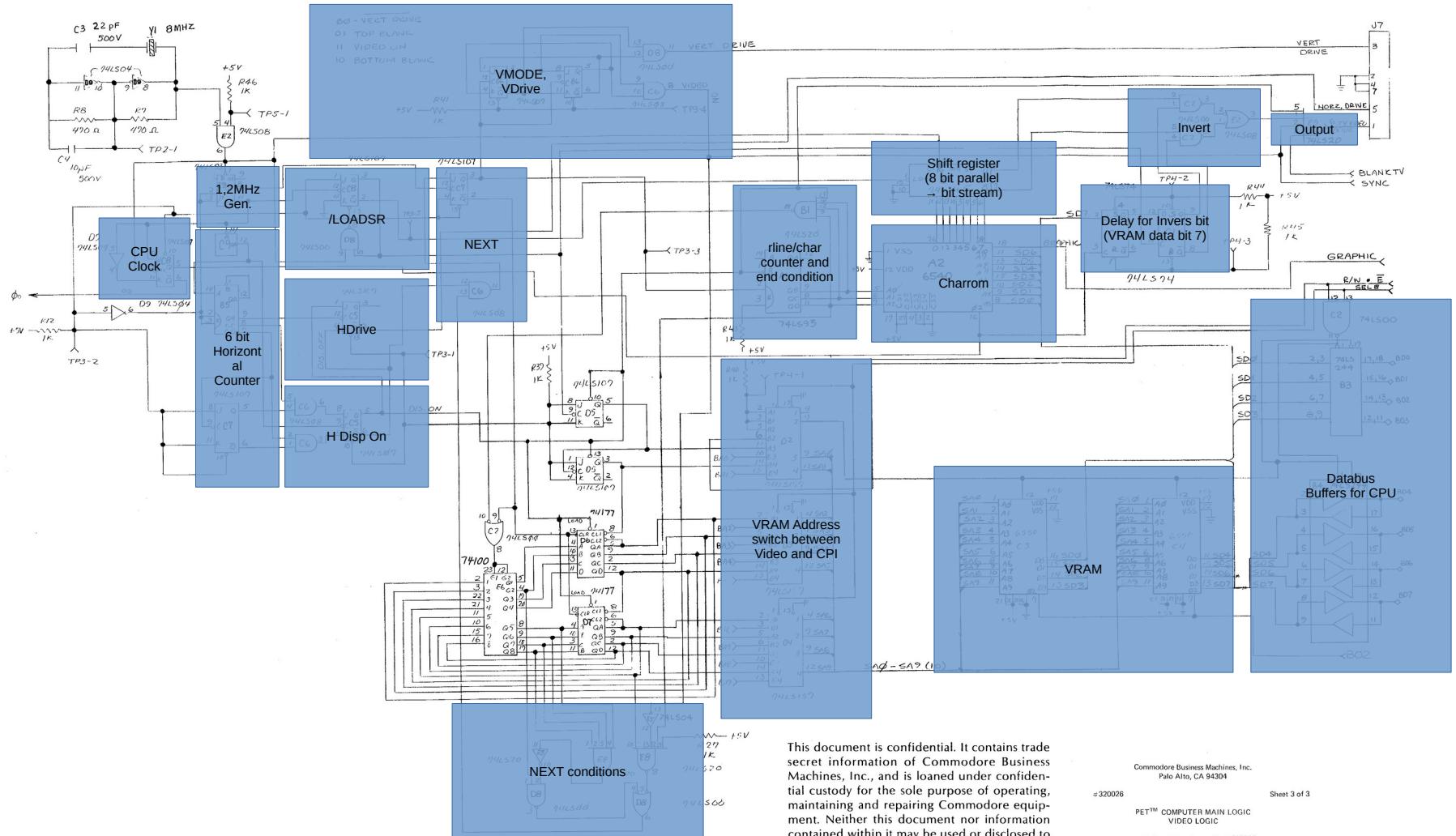
TP5-1

18



Address counter





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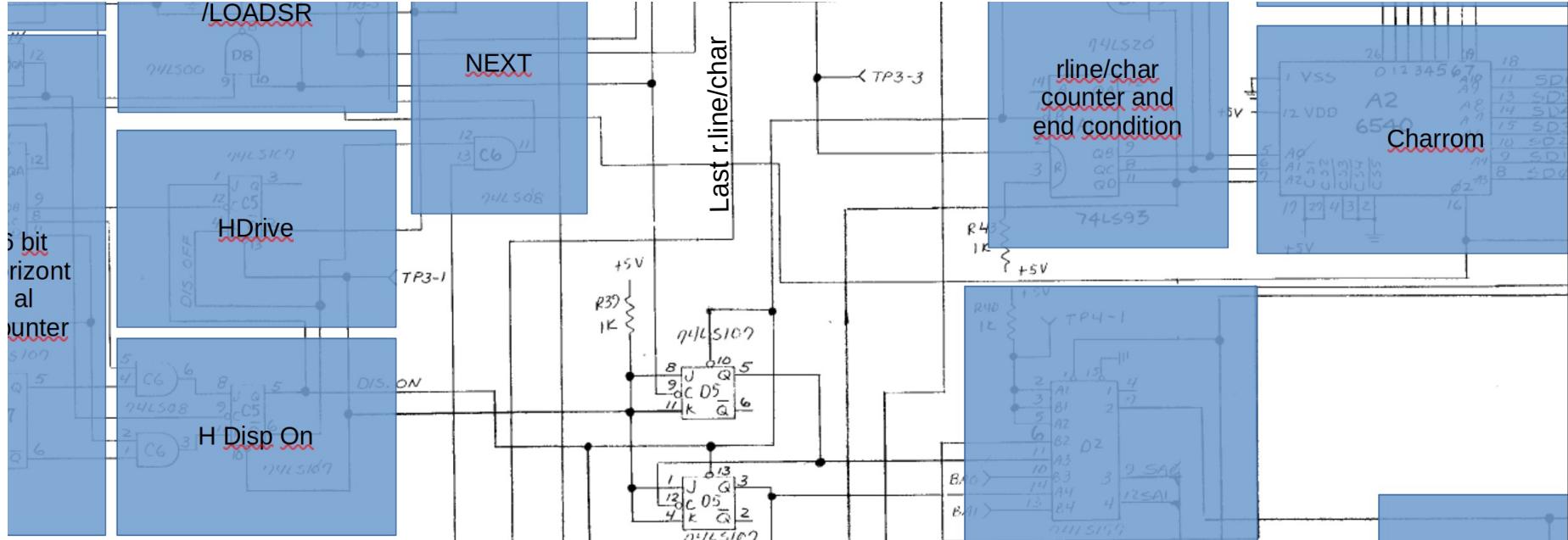
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2186

PET™ COMPUTER MAIN LOGIC

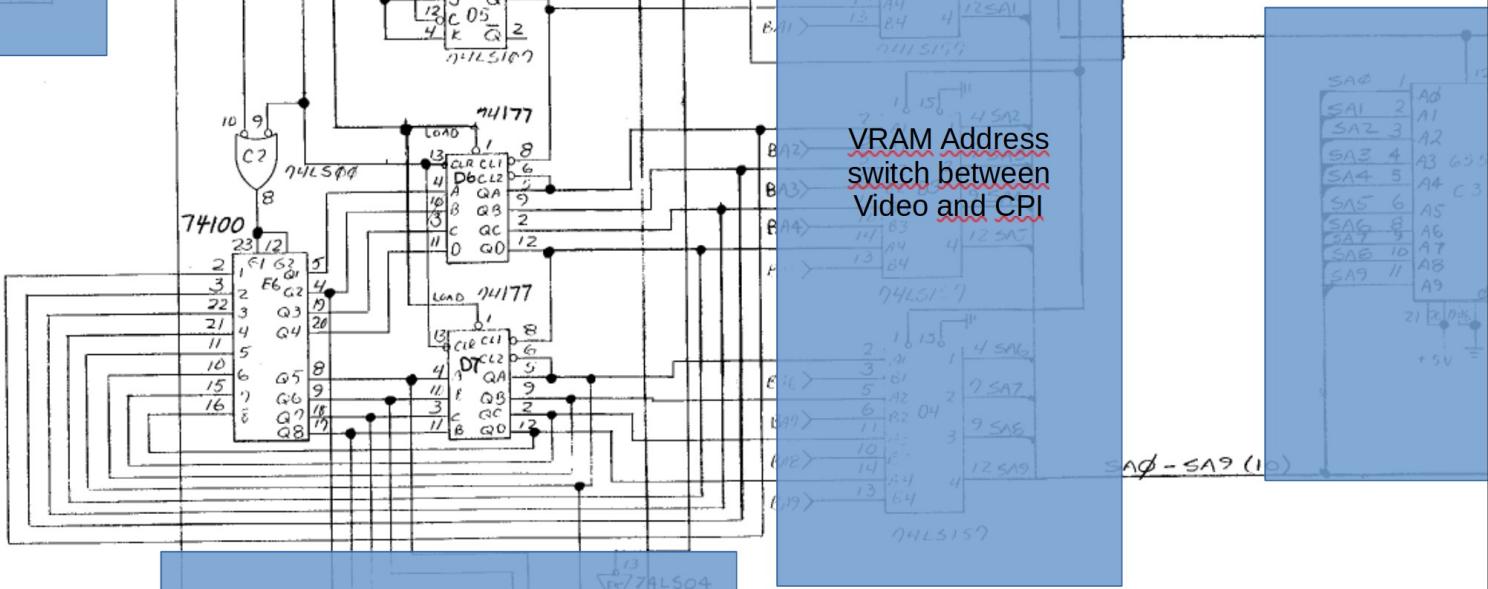
Page 200000

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Counter reloaded
At HDISPON=0

Hold Register
Transparent in
Last rasterline
For each char



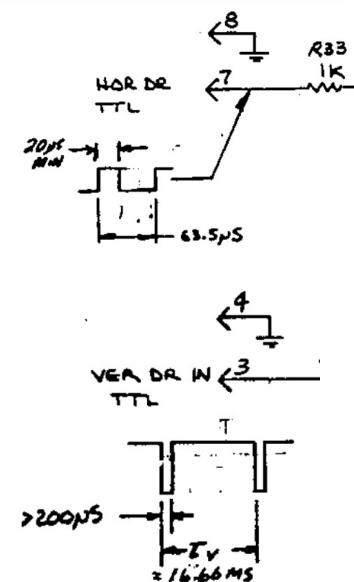
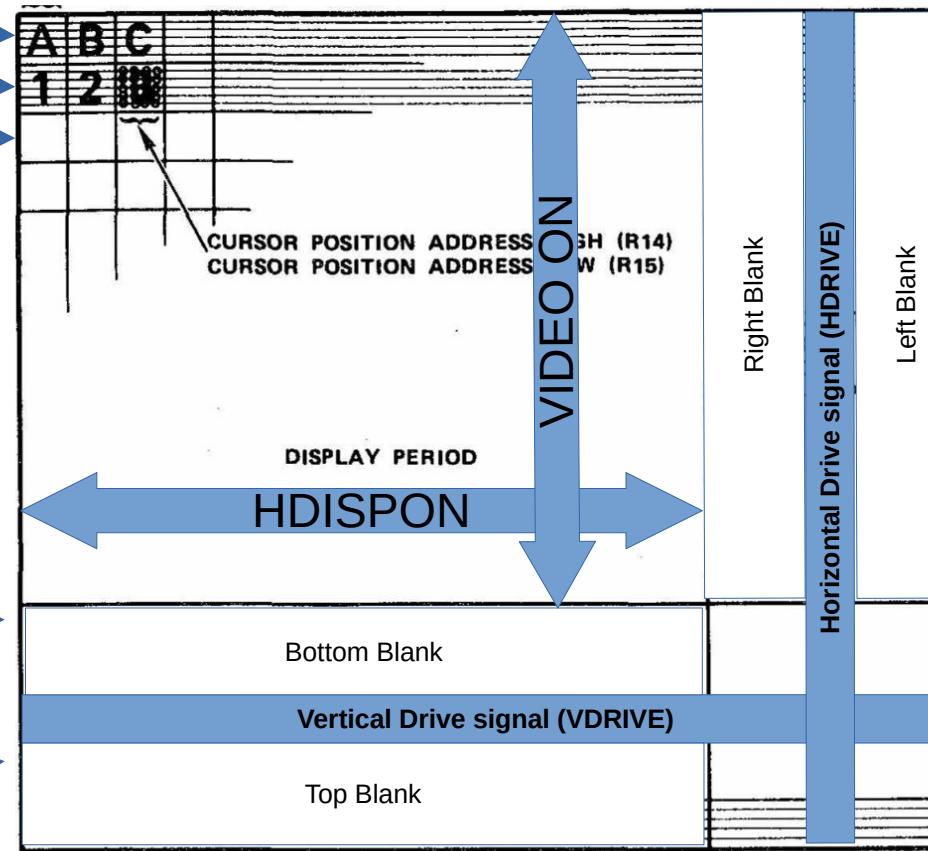
Addr → hold register

0 → \$00
40 → \$0A
80 → \$14
...

Address counter
Restarts per mode:

\$00
\$00
\$00
...

Counter value



NEXT Mode



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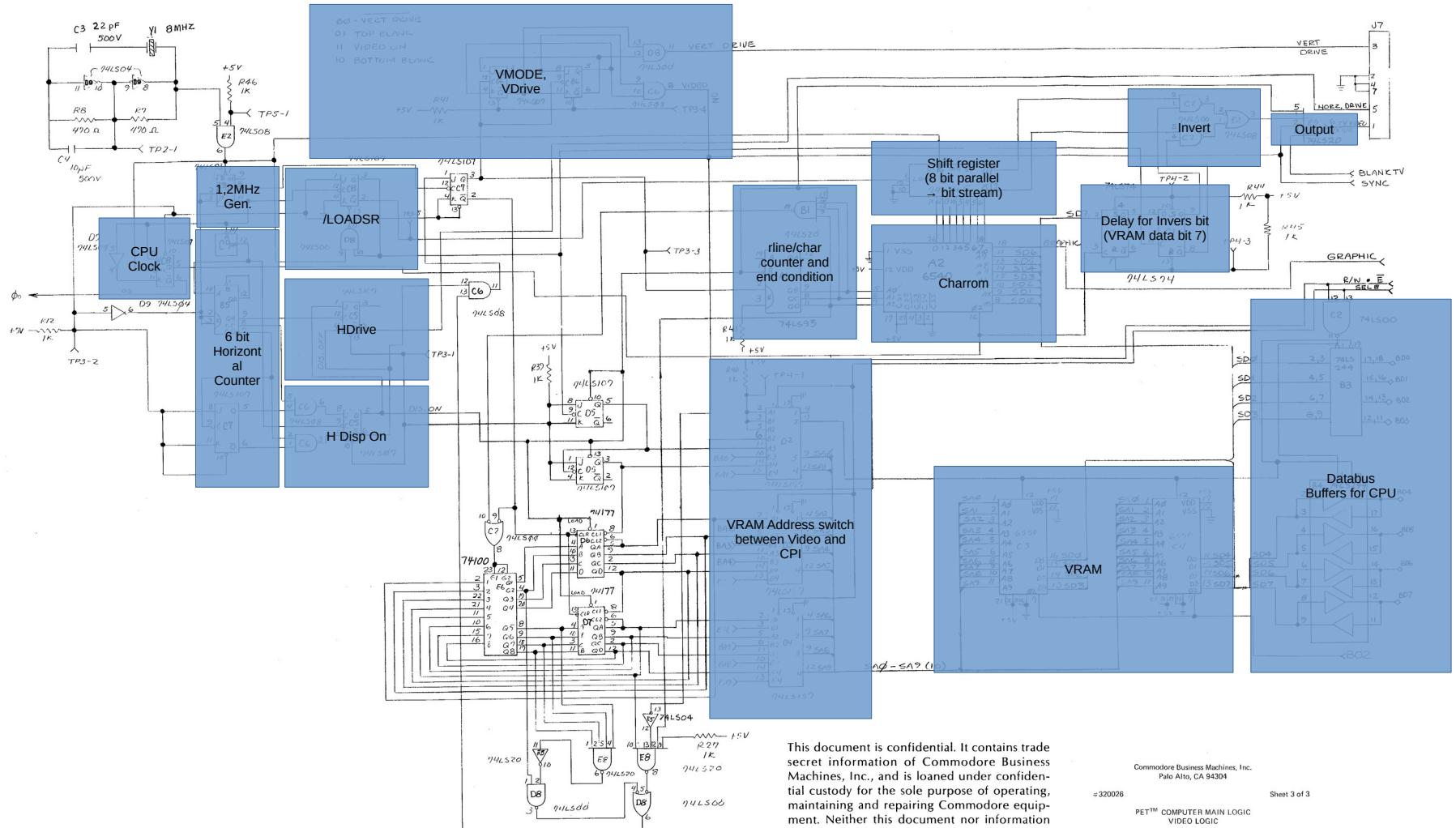
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PET™ COMPUTER MAIN LOGIC

pertaining to board assembly #320008

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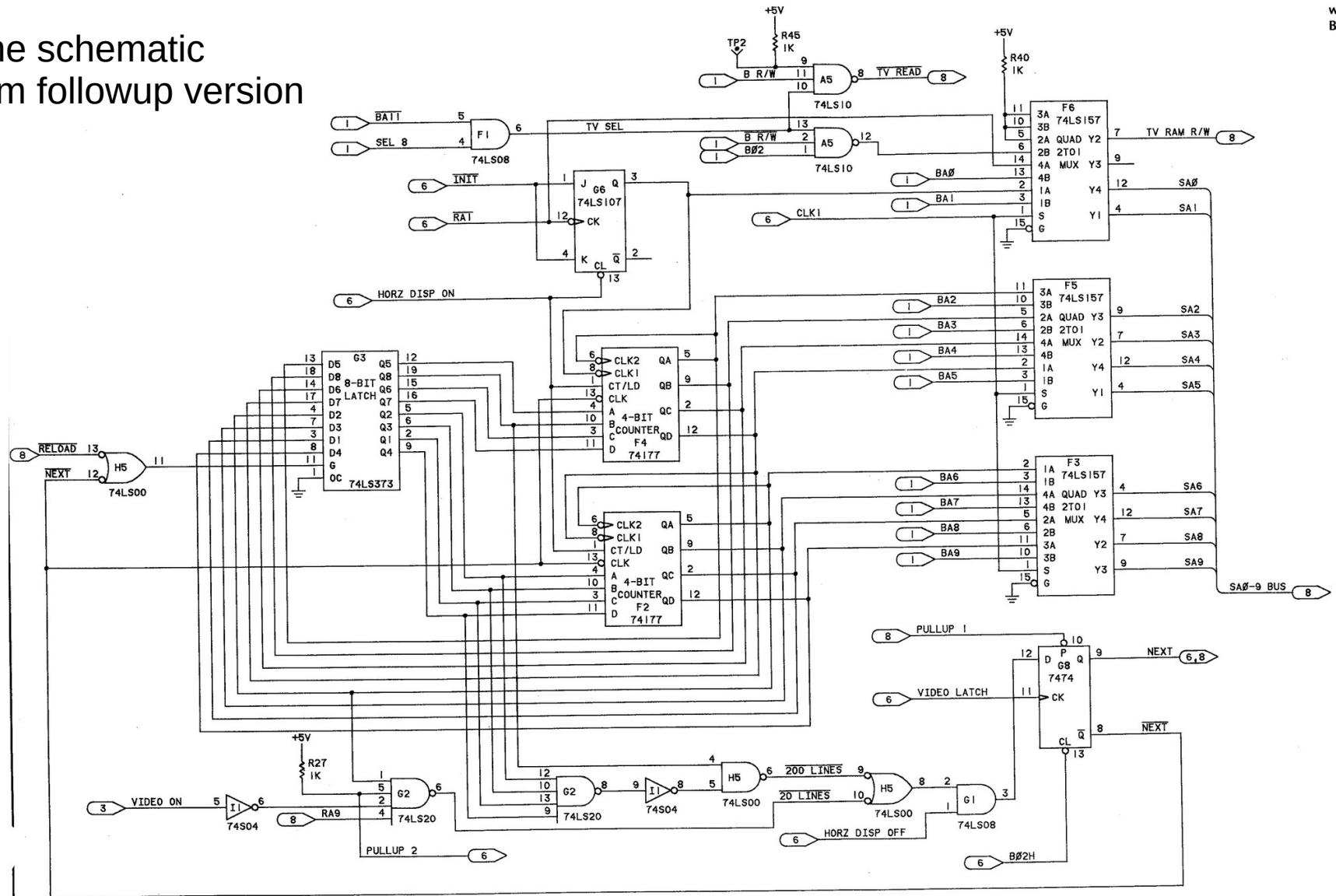
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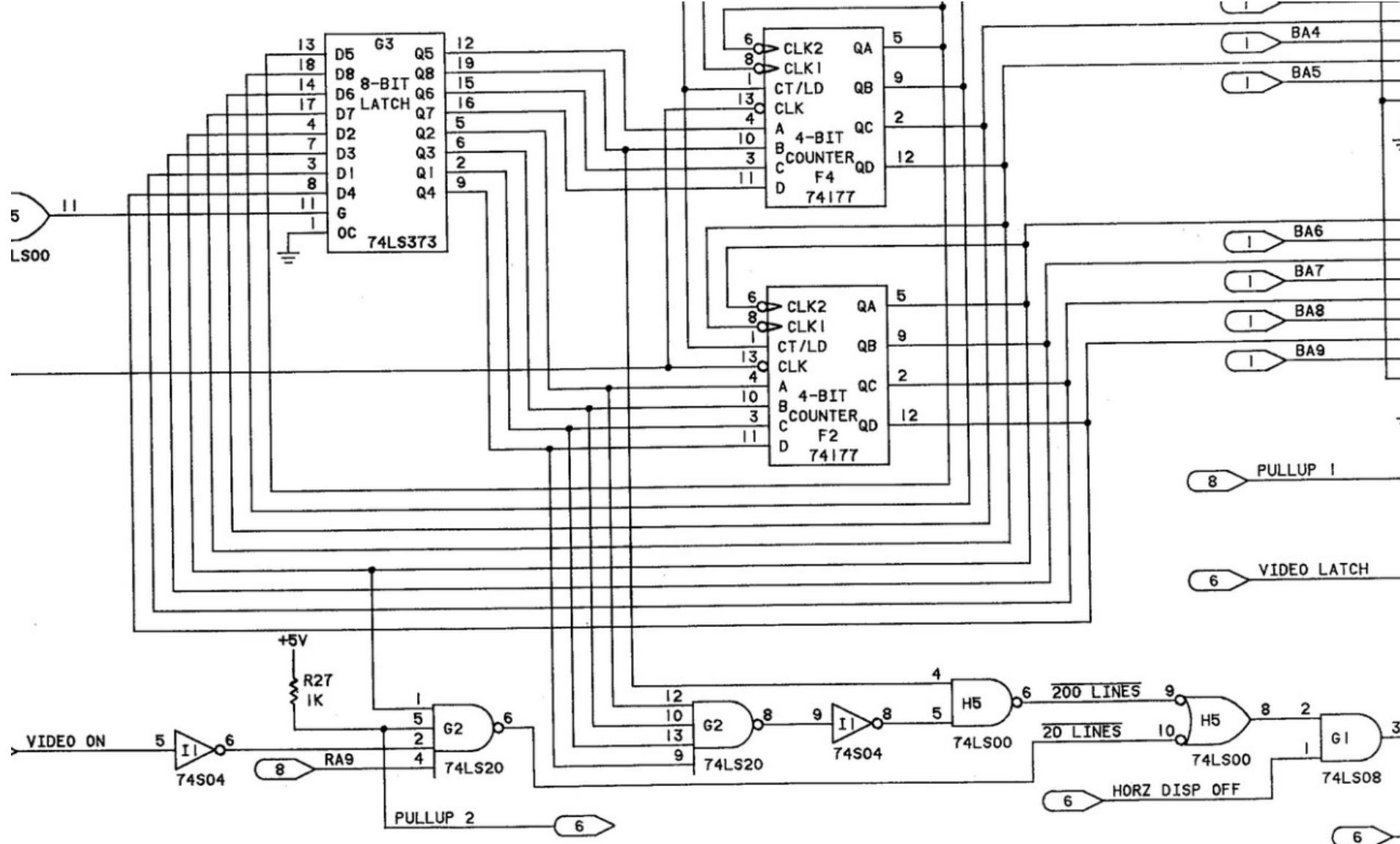
PET™ COMPUTER MAIN LOGIC

pertaining to board assembly #320008

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Same schematic - from followup version

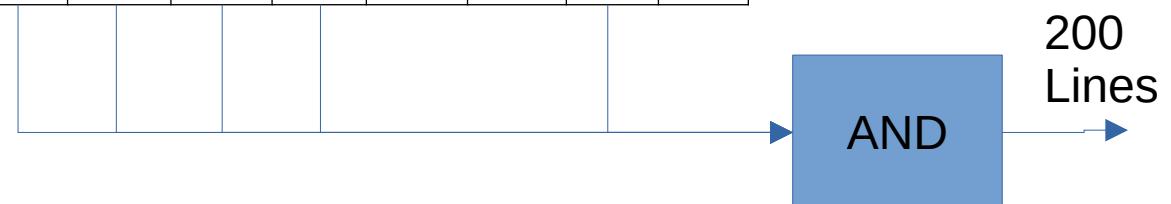




200 rlines: Hold register comparison

200 lines = 25 character lines x 8 rasterlines / character

Video address	Hold register	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	0	0	0	0
40	10	0	0	0	0	1	0	1	0
80	20	0	0	0	1	0	1	0	0
...	...								
920	230	1	1	1	0	0	1	1	0
960	240	1	1	1	1	0	0	0	0
1000	250	1	1	1	1	1	0	1	0



20 rlines:

20 lines = 2.5 character lines x 8 rasterlines / character

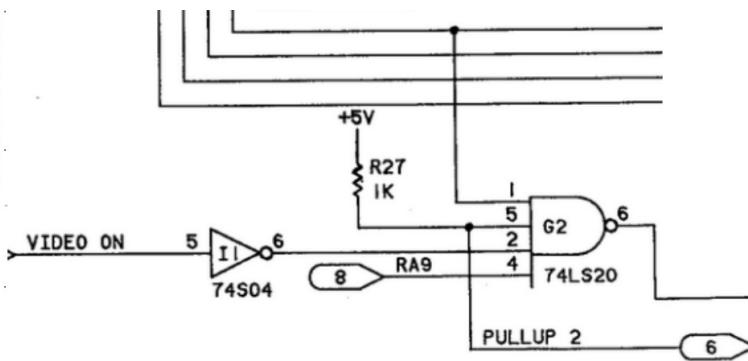
Why counter and not hold register?

Because in the middle of a char, the hold register still holds the old start address

But then why counter b4? It gets high already in the second character line (rlines 8...15)

It is evaluated at HDISPOFF, where counter is loaded with register value (async load) ...

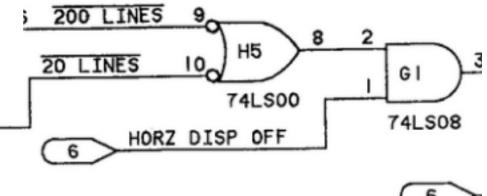
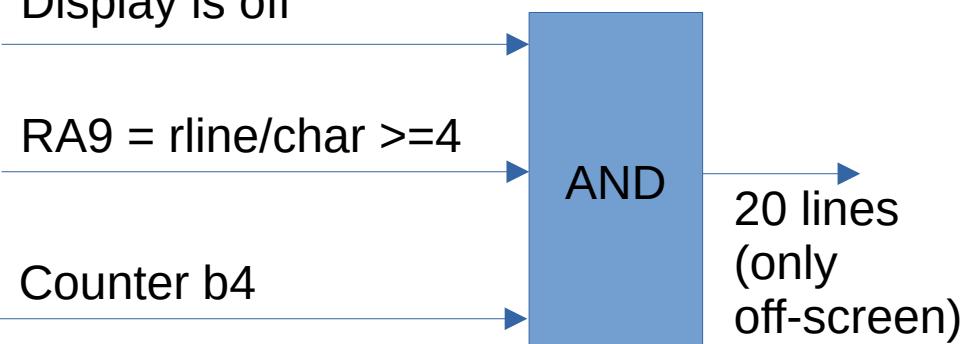
=> they could have used the hold register b4 instead...



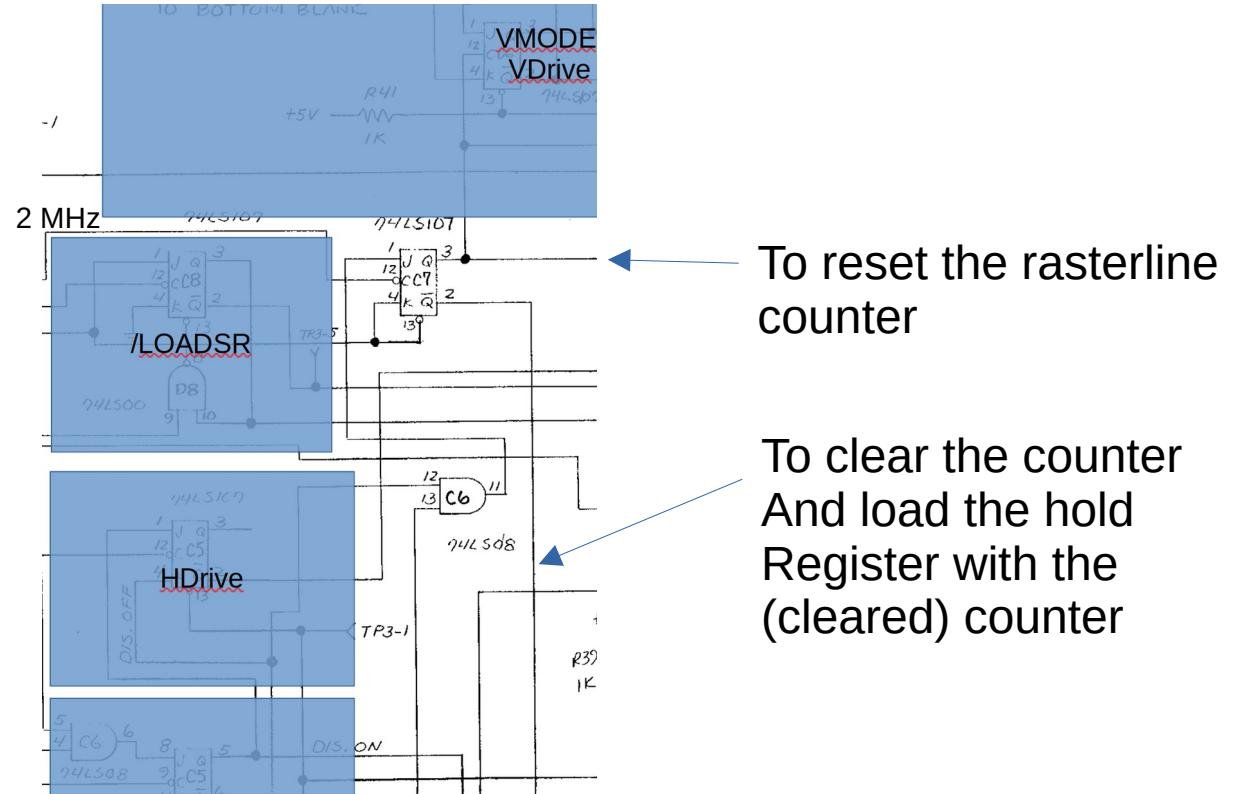
Display is off

RA9 = rline/char >= 4

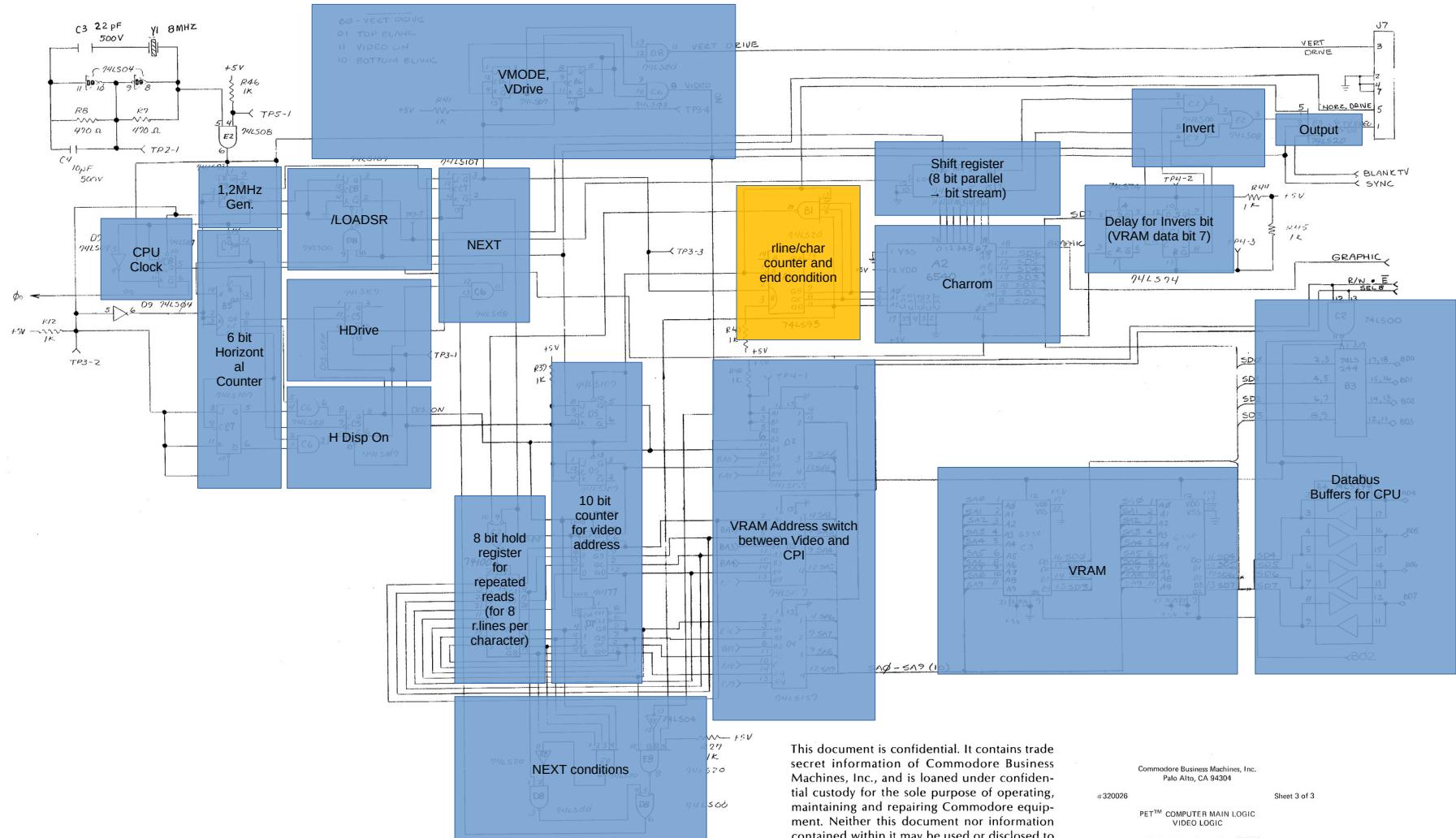
Counter b4

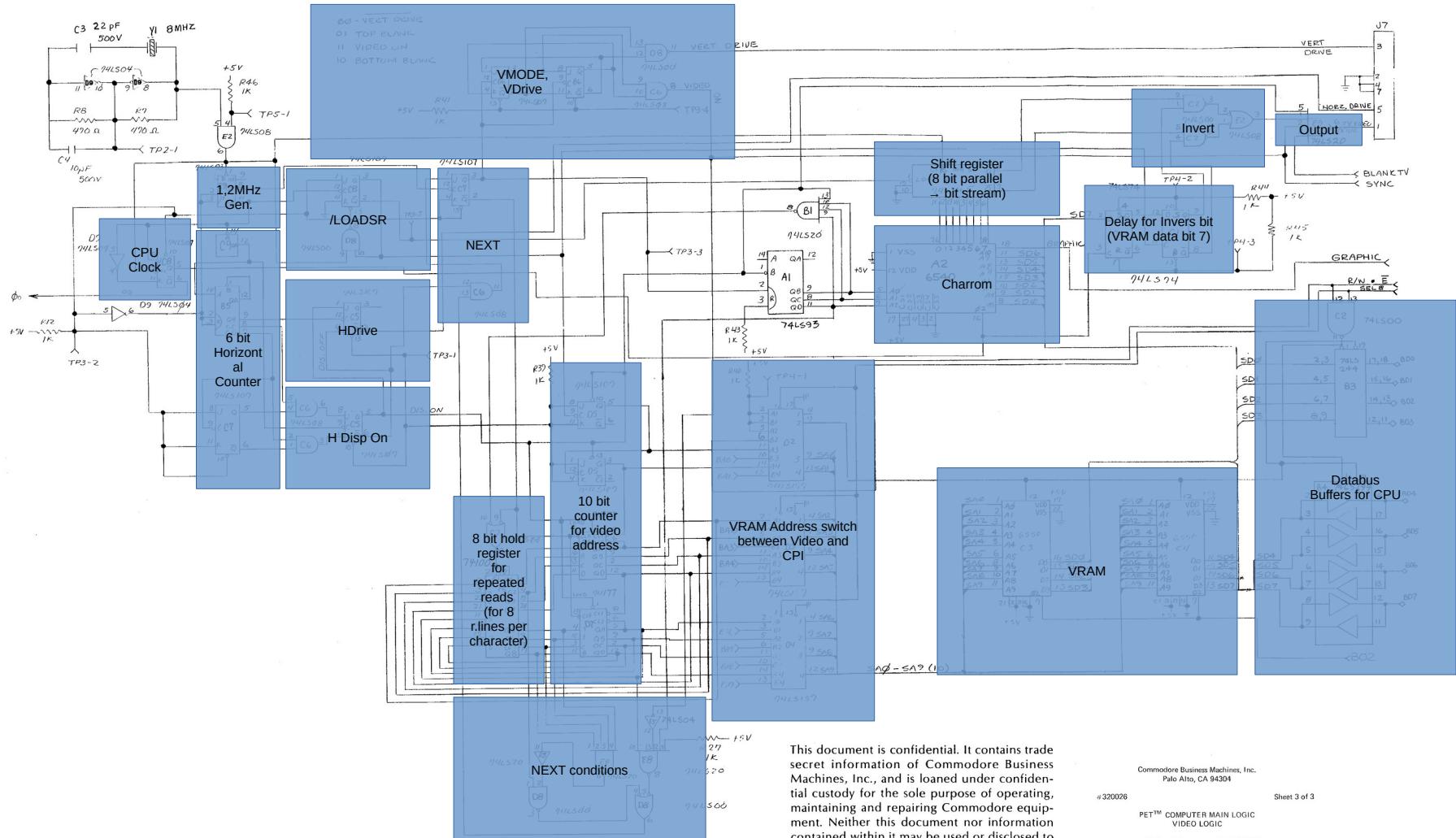


NEXT Mode



Rasterline counter

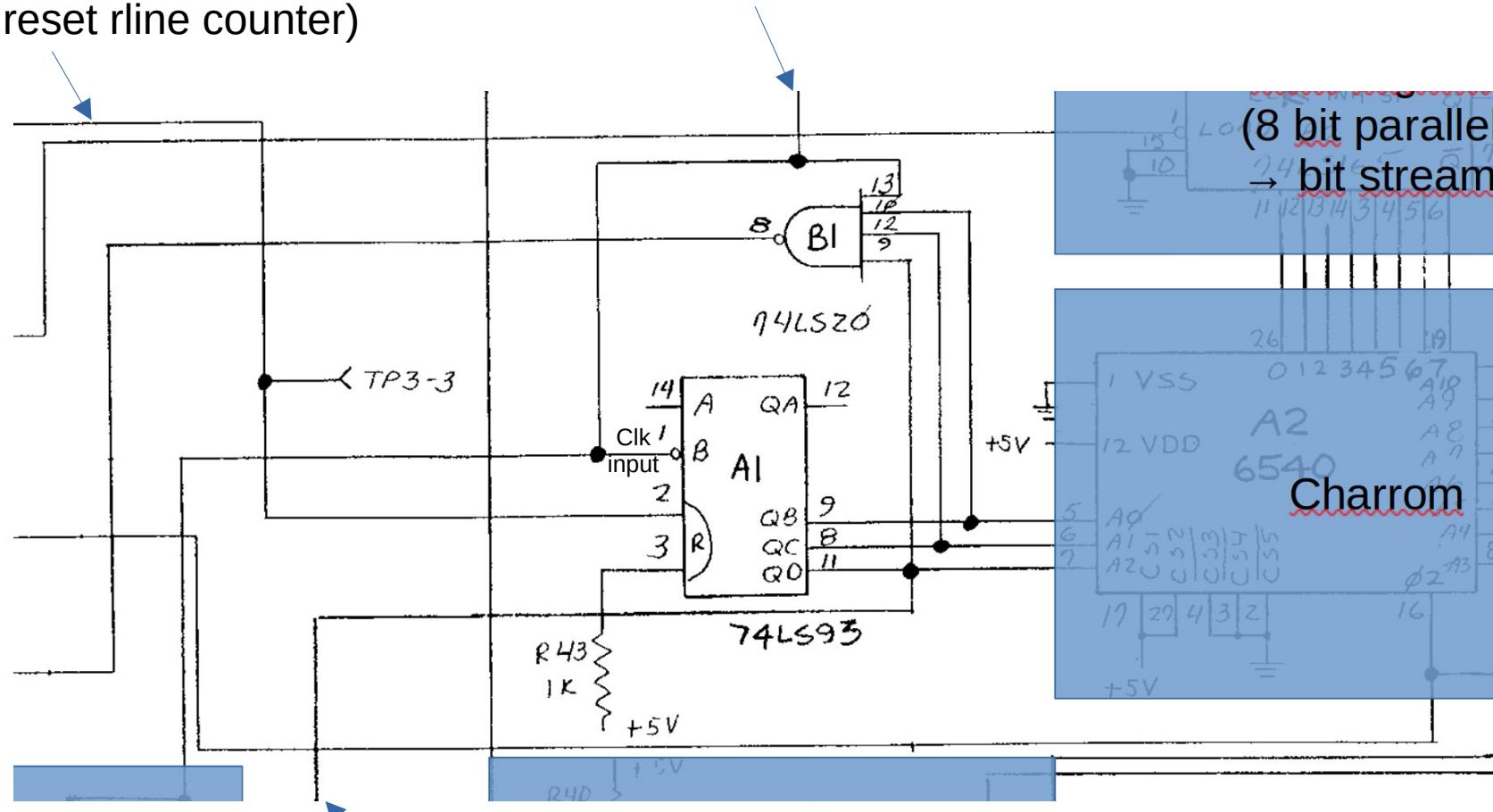




NEXT

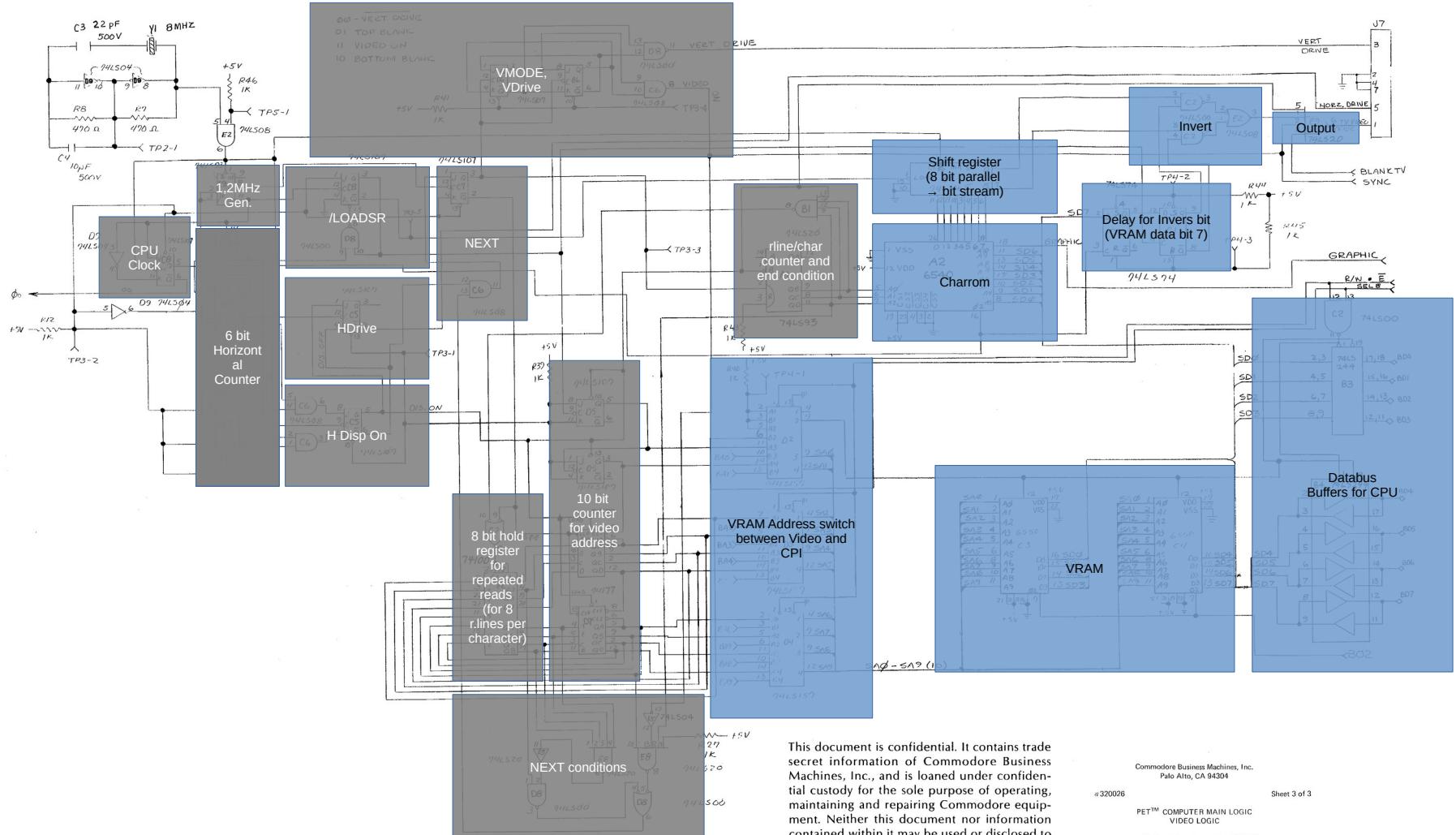
(to reset rline counter)

HDISPON



To „20 lines detection“

Recap



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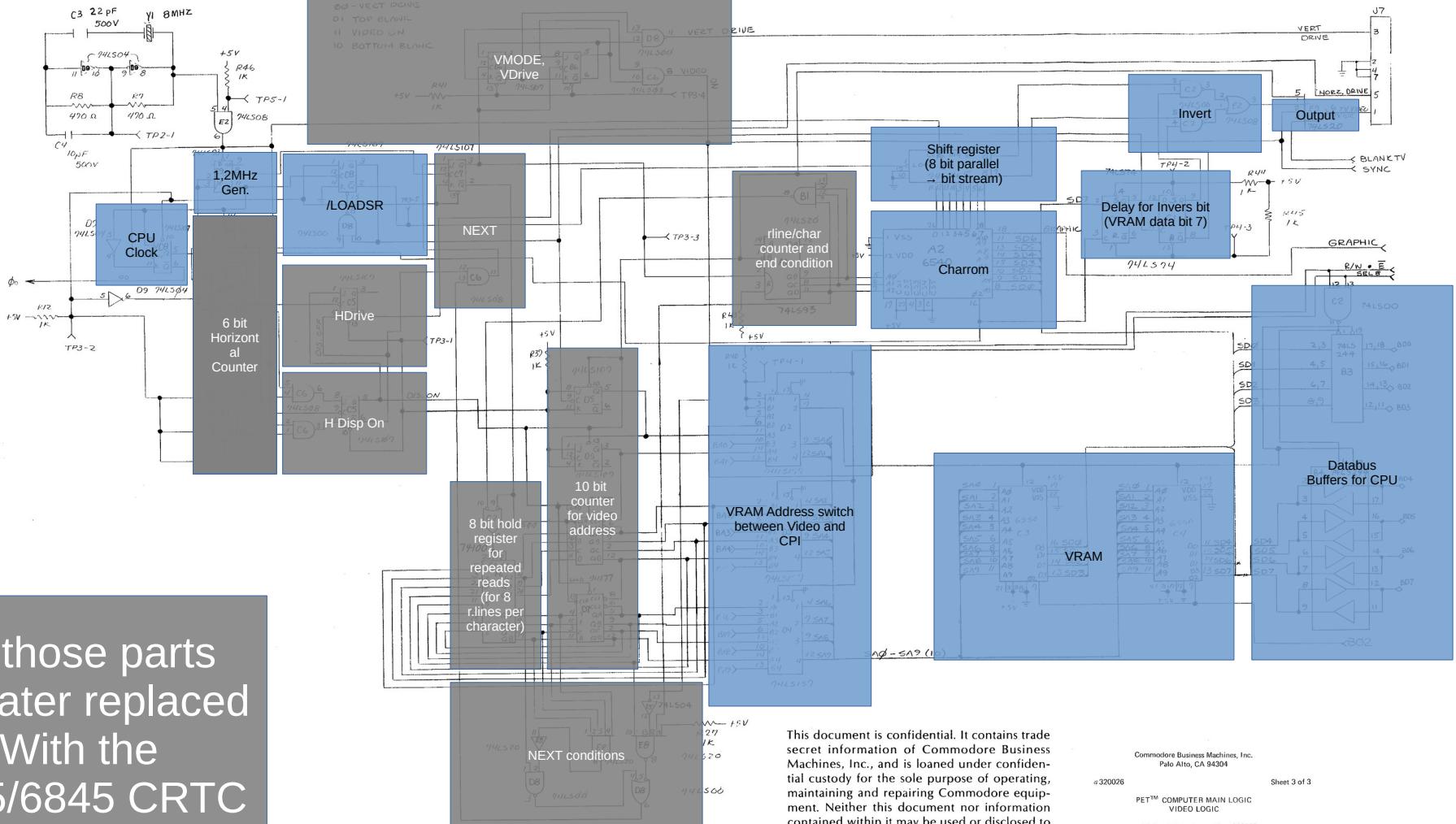
Commodore Business Machines, Inc.
Palo Alto, CA 94304

• 8 •

PET™ COMPUTER MAIN LOGIC

pertaining to board assembly #320008

NOTE: All locations are same on all boards; only the specific components will differ on boards numbered 320132, 320081, 320137, 320008.



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#320026

Sheet 3 of 3

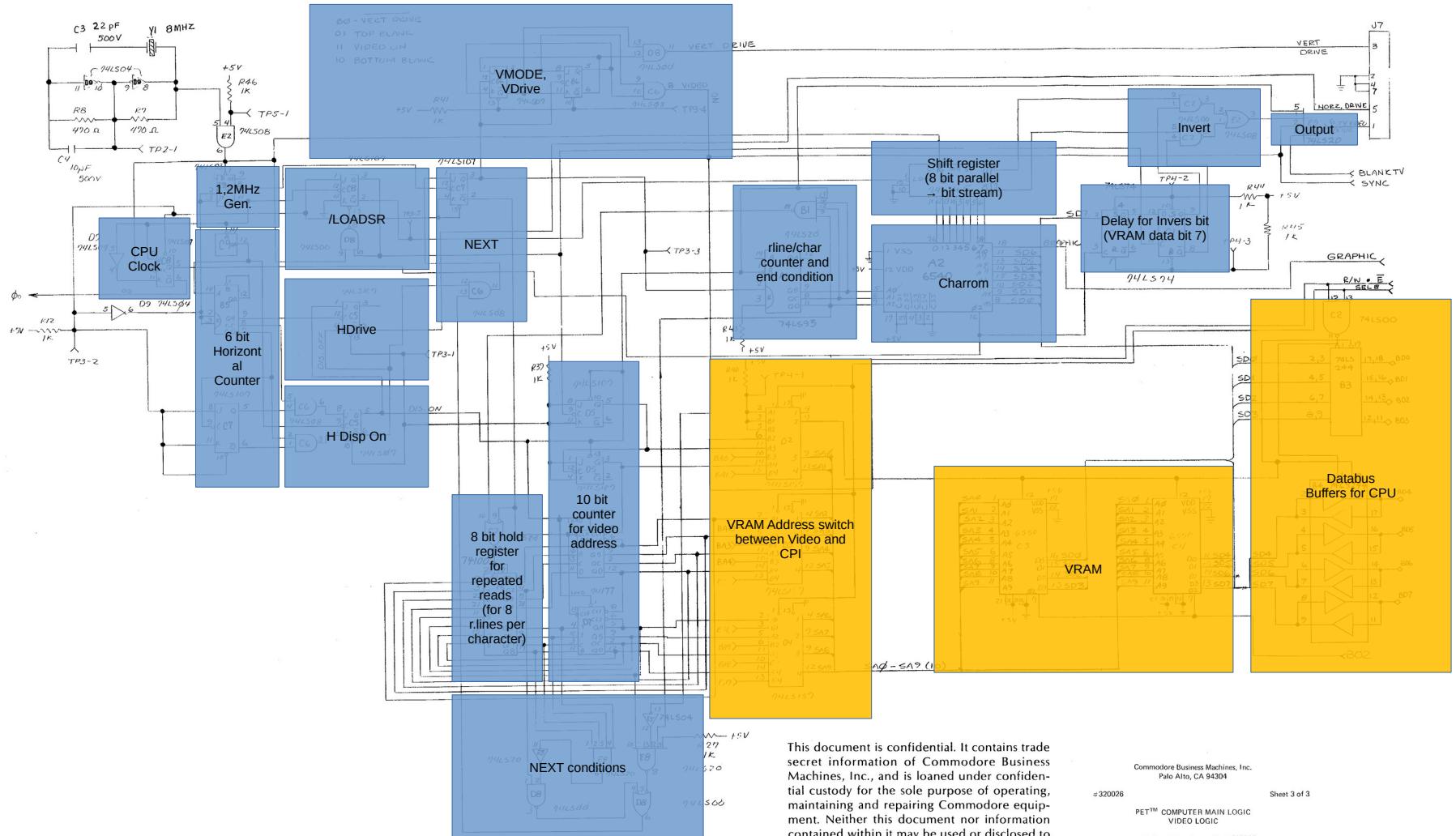
PET™ COMPUTER MAIN LOGIC
VIDEO LOGIC

pertaining to board assembly #320008

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The identifying board number is in upper left corner.

RAM access



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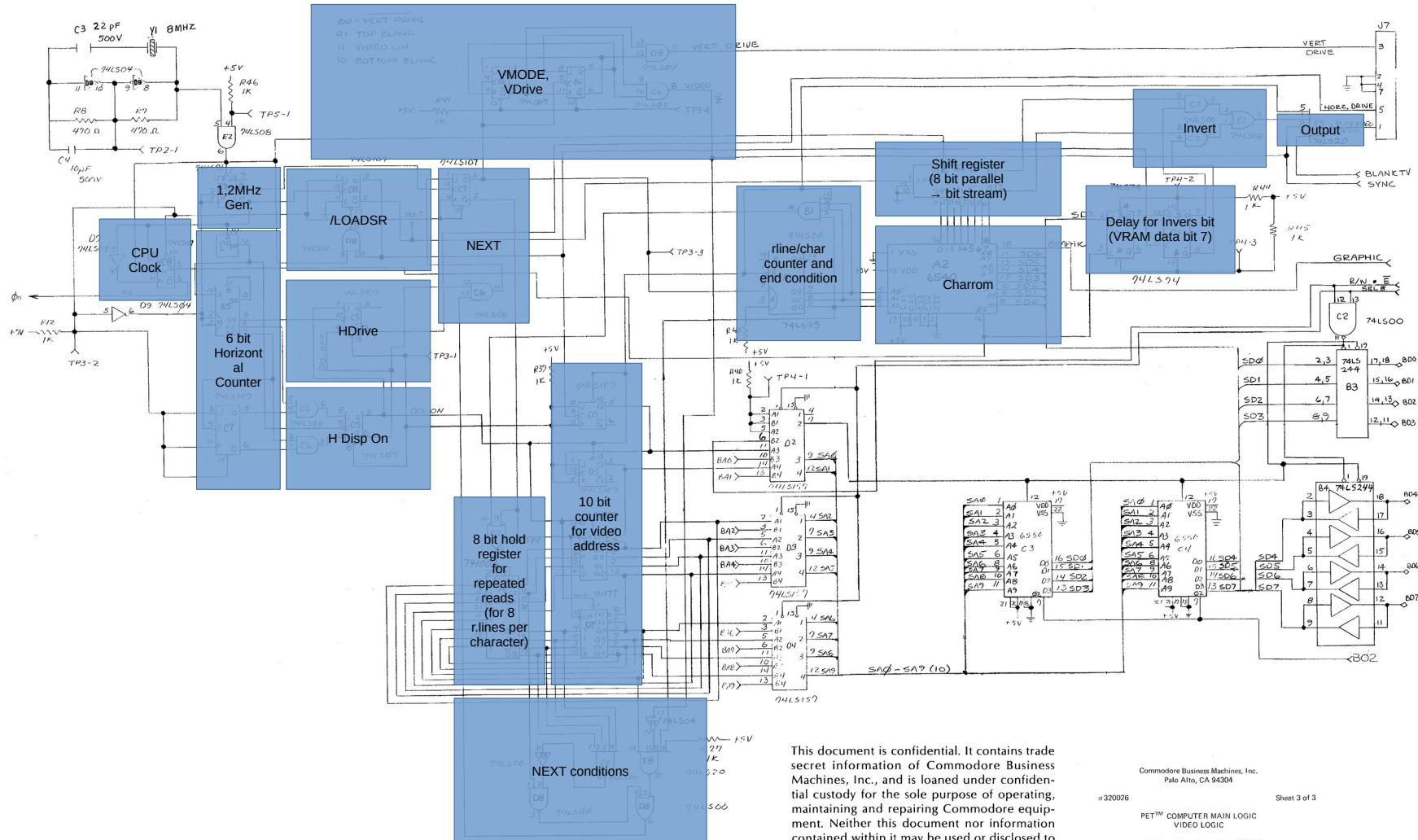
• 8 •

Sheet 3 of 3

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pertaining to board assembly #320008

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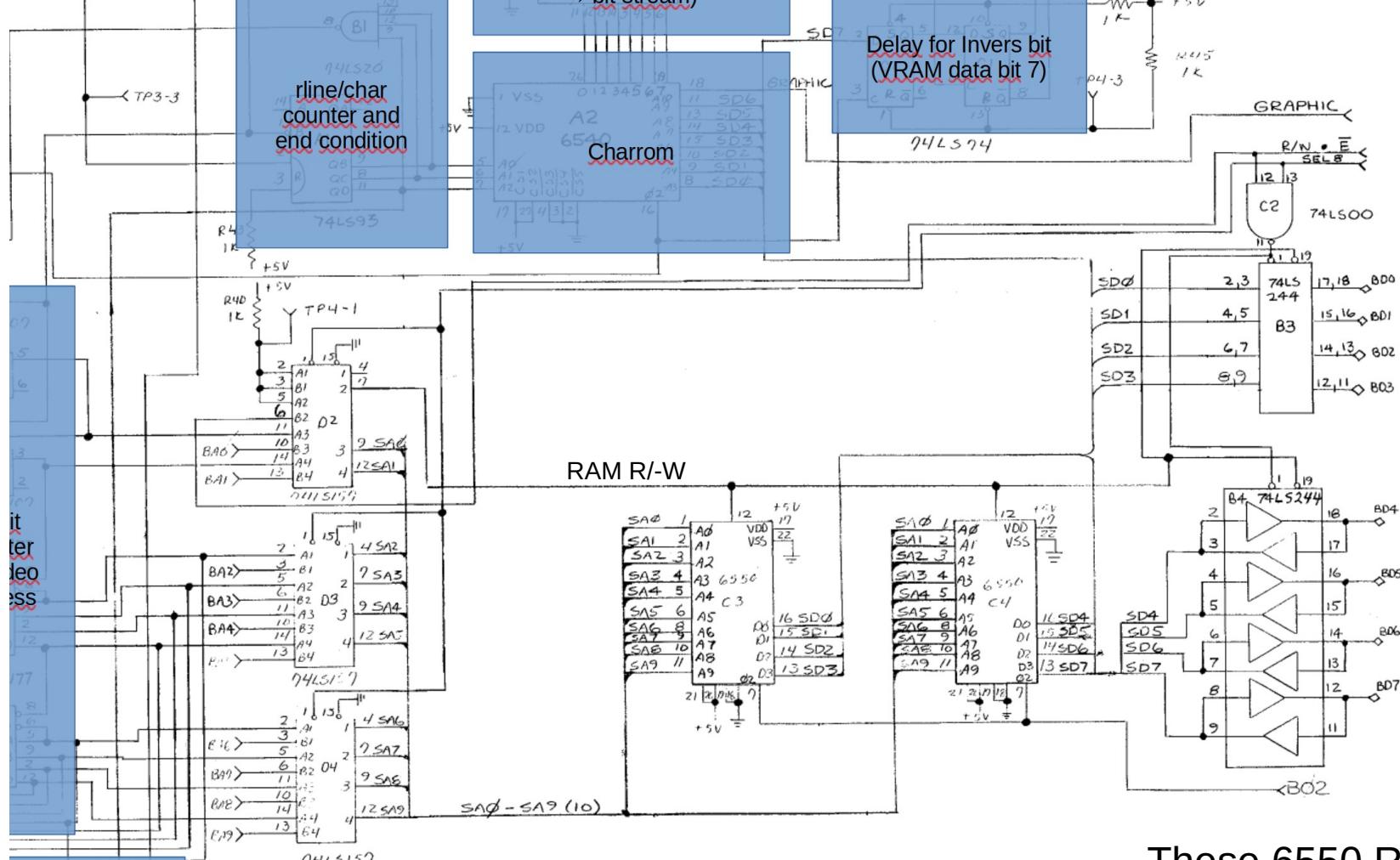
• 8 •

Sheet 3 of 3

PET™ COMPUTER MAIN LOGIC
VIDEO LOGIC

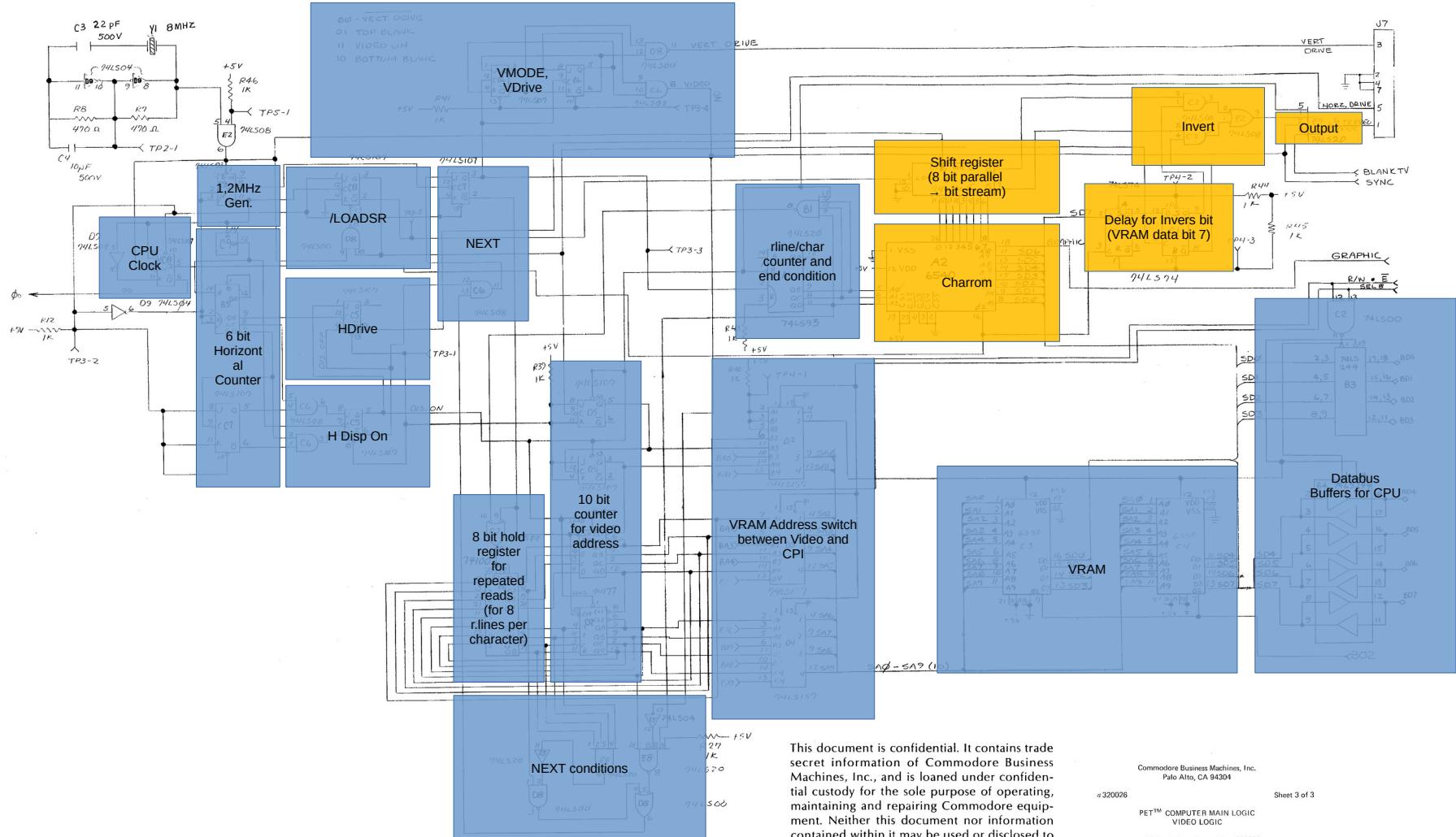
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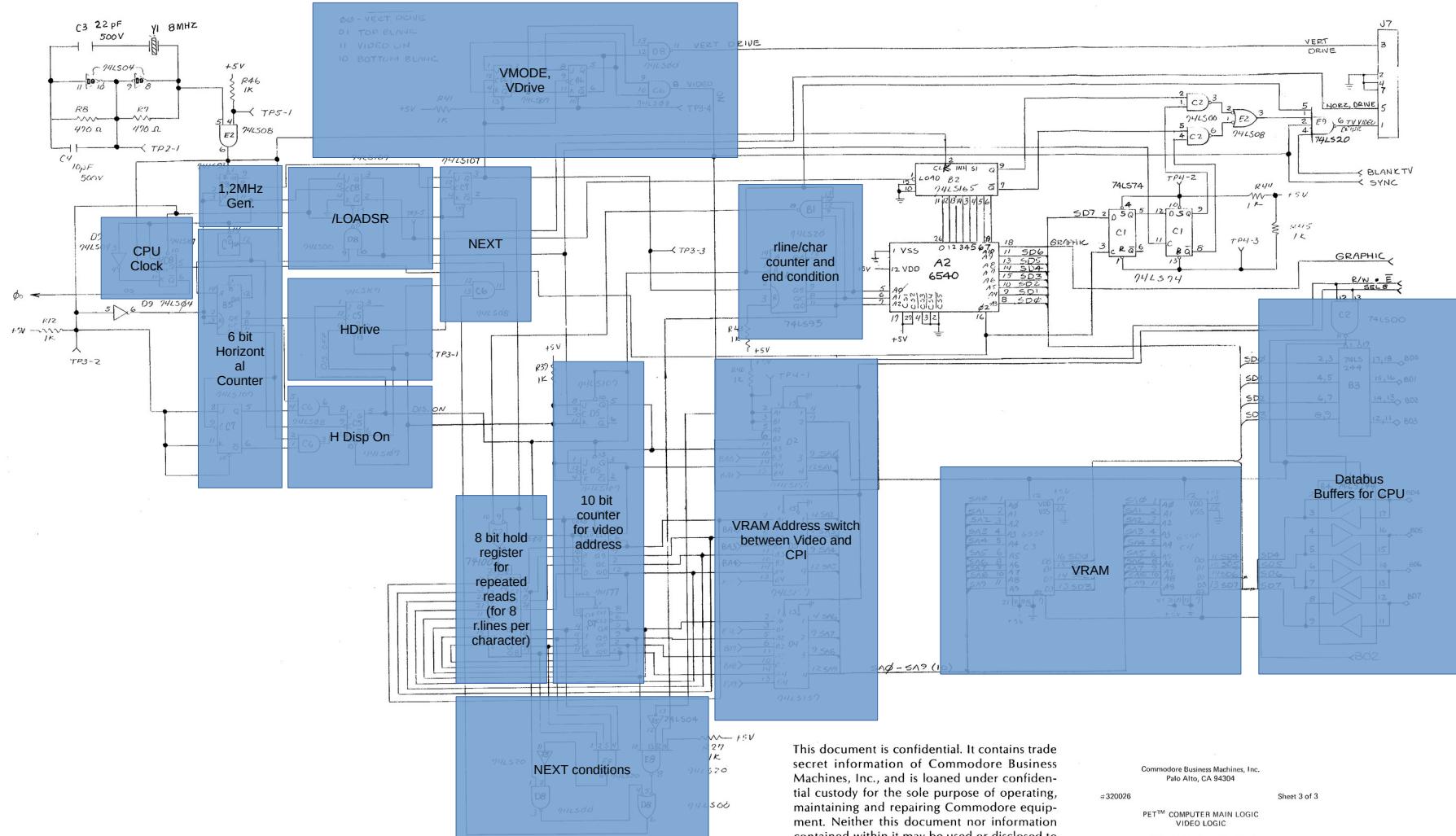
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Charrom and Pixel out





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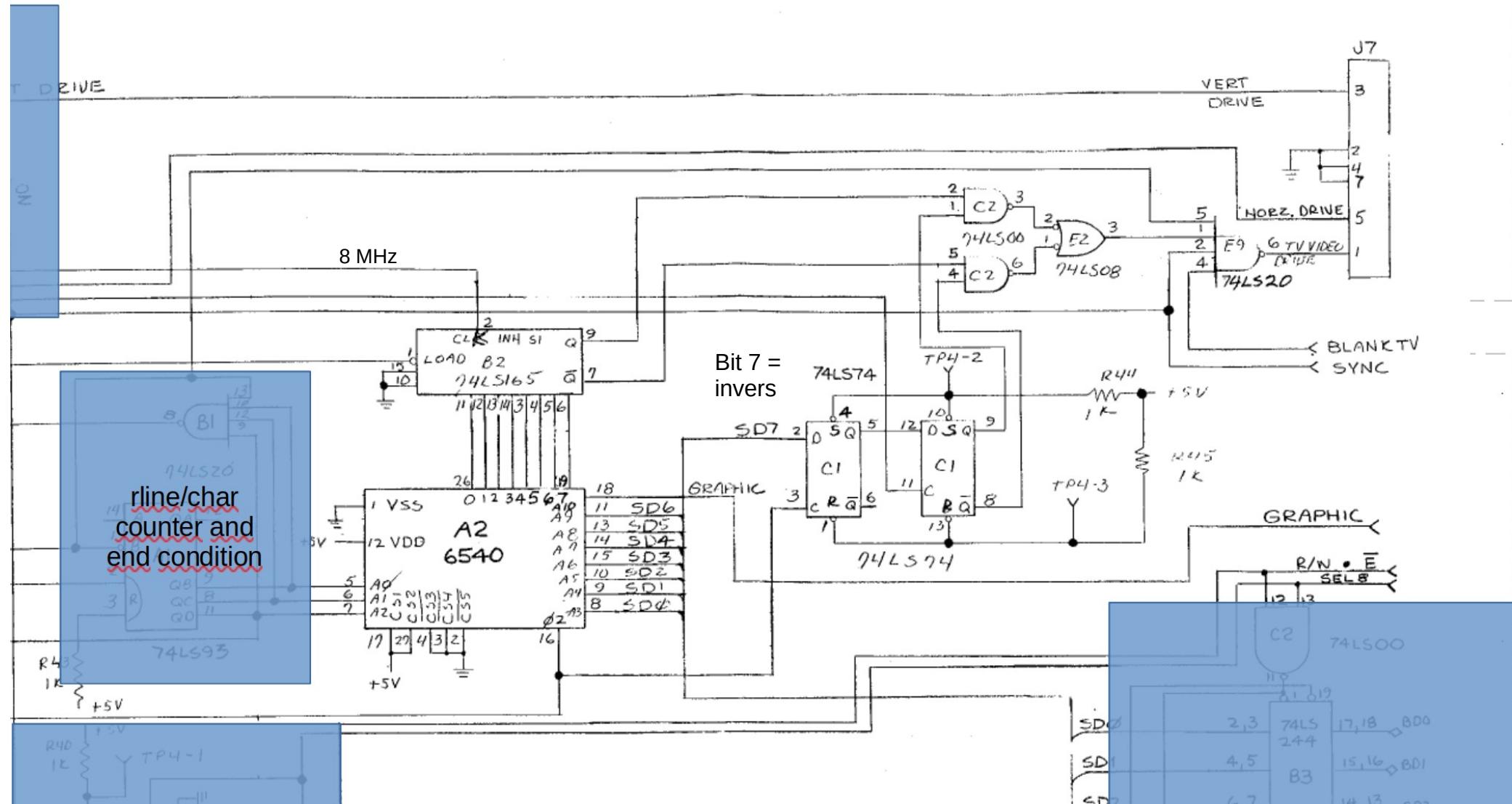
Sheet 3 of 3

PET™ COMPUTER MAIN LOGIC
VIDEO LOGIC

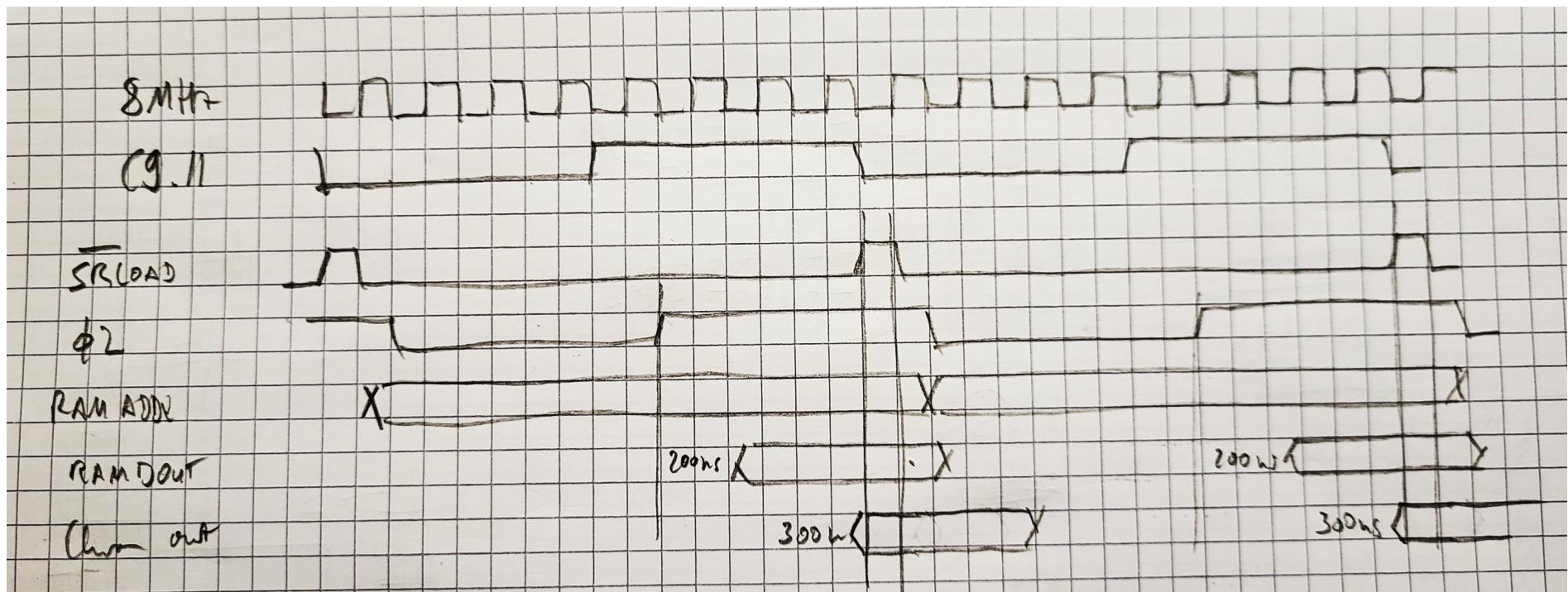
pertaining to board assembly #320008

NOTE: All locations are same on all boards; only the specific component will differ on boards numbered 320132, 320081, 320137, 320008.

The identifying board number is in upper left corner.



Timing?



Summary original PET video

- Fixed video timing
- All TTL-logic video output (except for RAM/ROM)
- Optimizations to reduce chip count:
 - Hold register only 8 bits
 - NEXT condition logic reduced to simple logic
 - Re-use address counter for off-screen timing
- 1 MHz RAM does not allow time-sharing video RAM between video and CPU
 - If video accesses the video RAM, video output is disturbed → „snow“

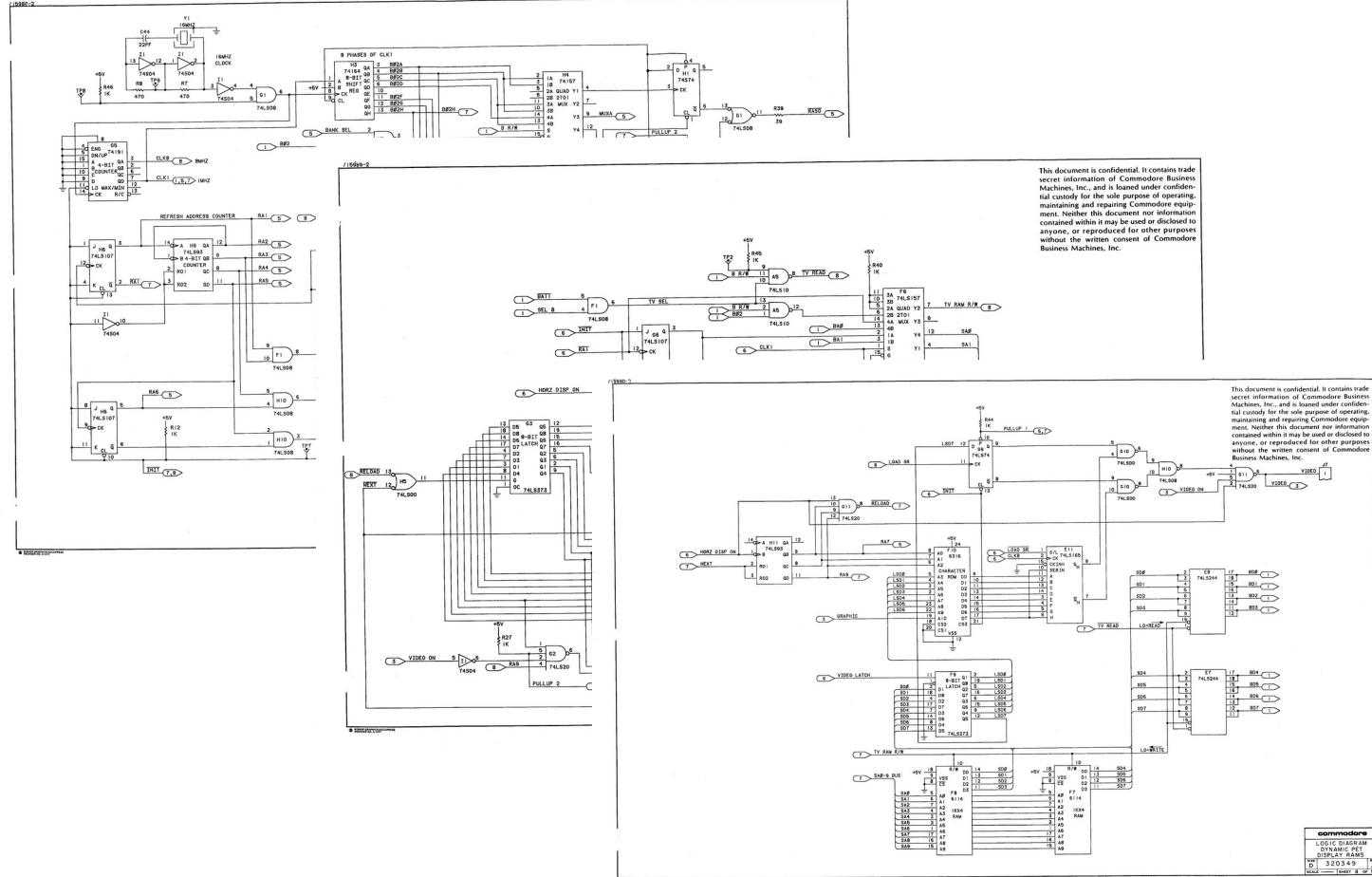
„Dynamic“ PET

- Main memory is dRAM
 - → video circuit creates refresh address
- 1k video RAM is SRAM
- 2 MHz access time for video RAM
- Video created by logic circuits, no „video chip“
- 40x25 character
- B/W
- Fixed character set
- No „snow“ due to 2 MHz video RAM timing!

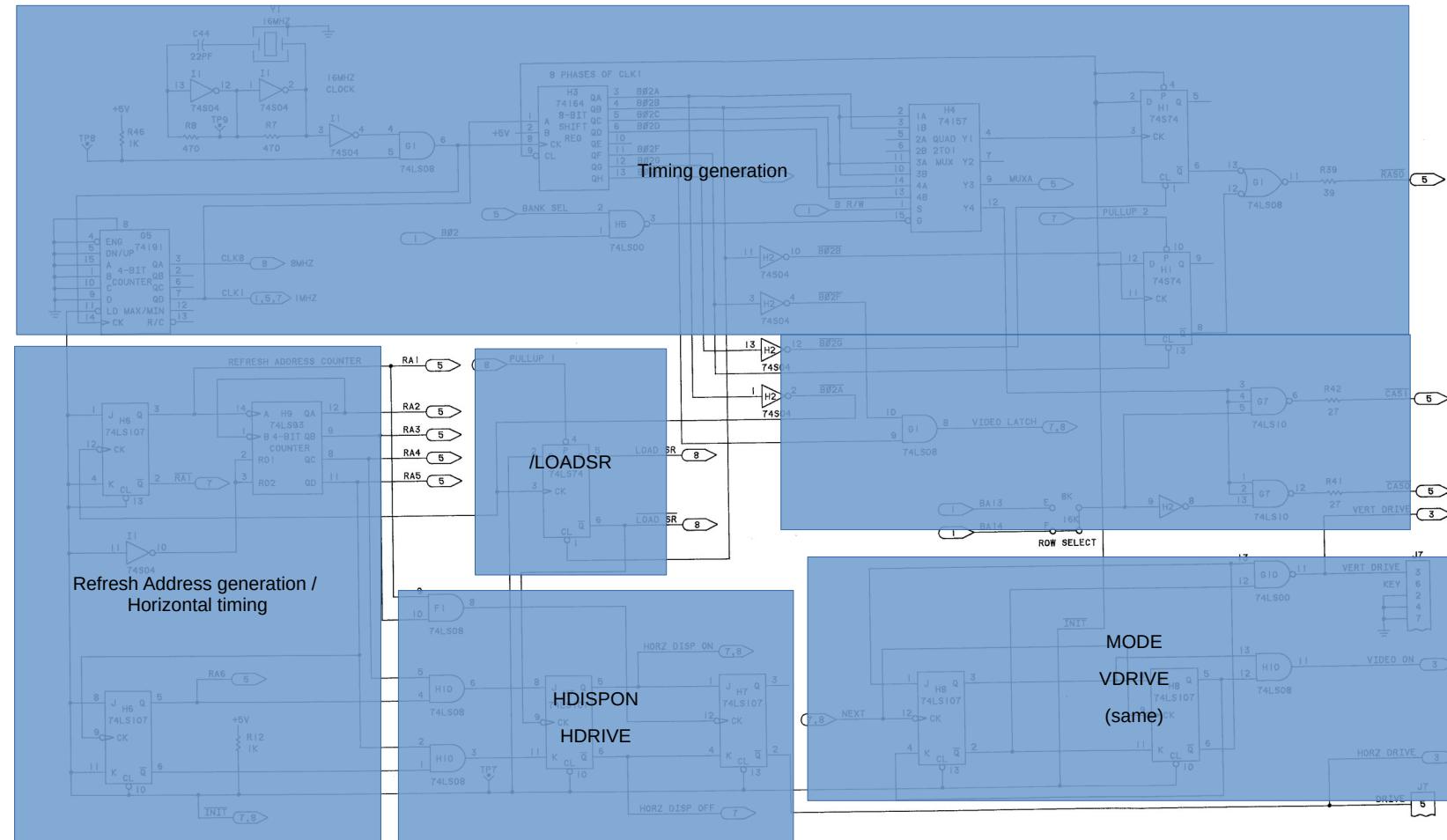


Schematics overview

- Same principles of operation
- 3 instead of 1 sheet
- Will look at differences only

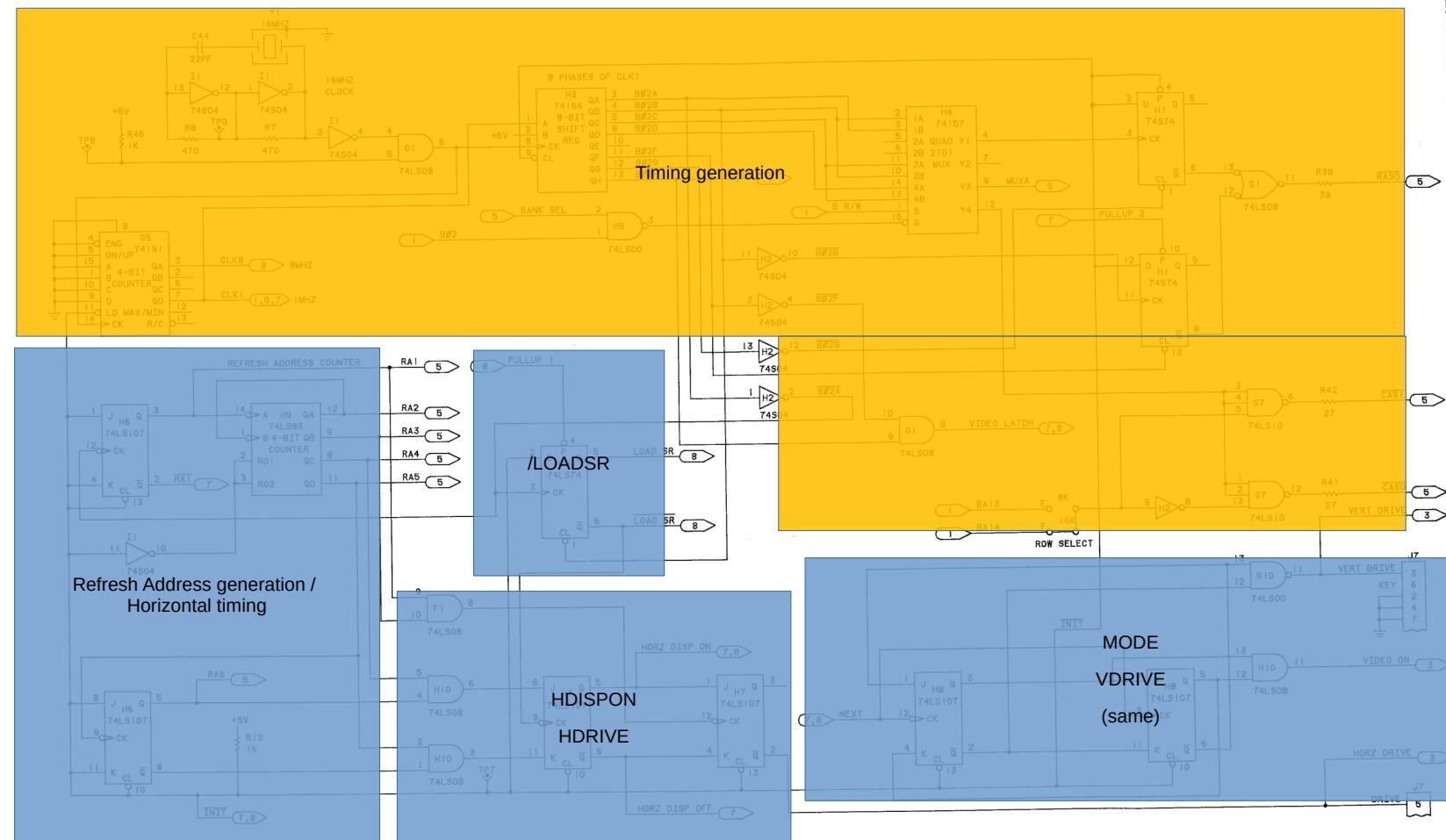


Dynamic PET – general timing



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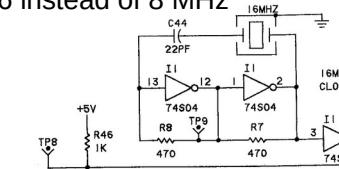
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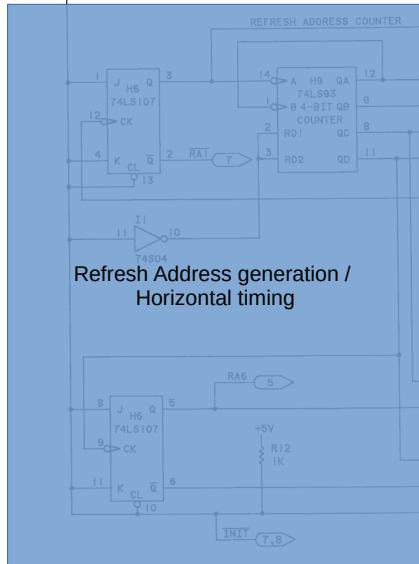
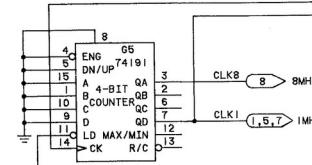
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16 instead of 8 MHz

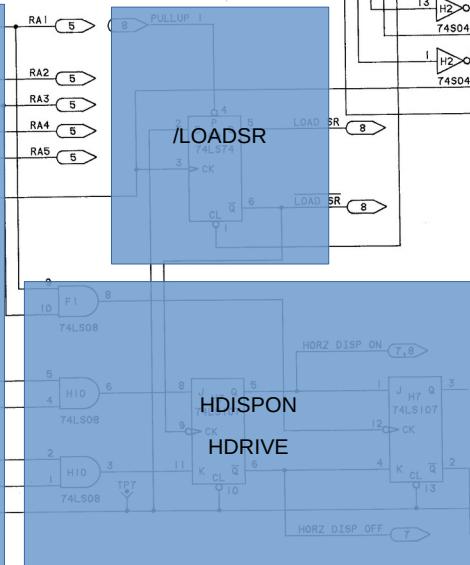


Creates 8 versions of Phi clock
Shifted by 1/16 (62.5ns)

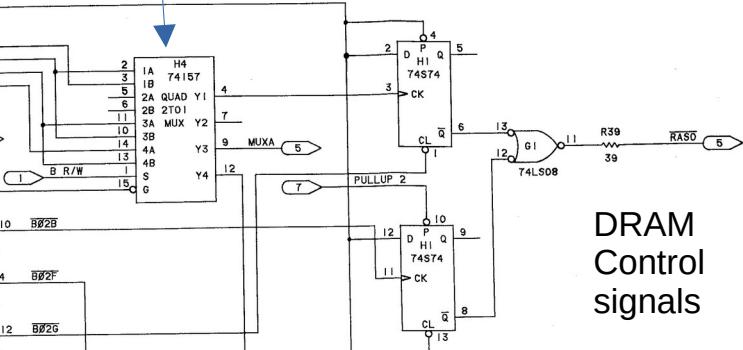
Select dRAM timing depending
On read vs. write



Refresh Address generation /
Horizontal timing

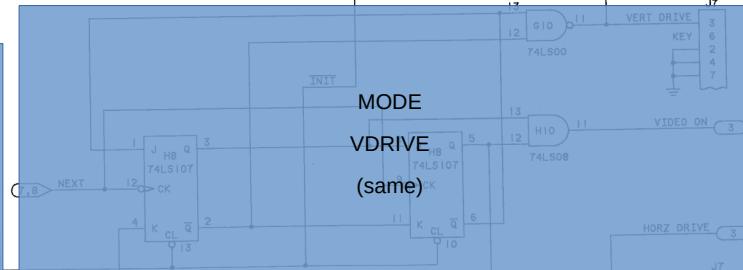


HDISPON
HDRIVE



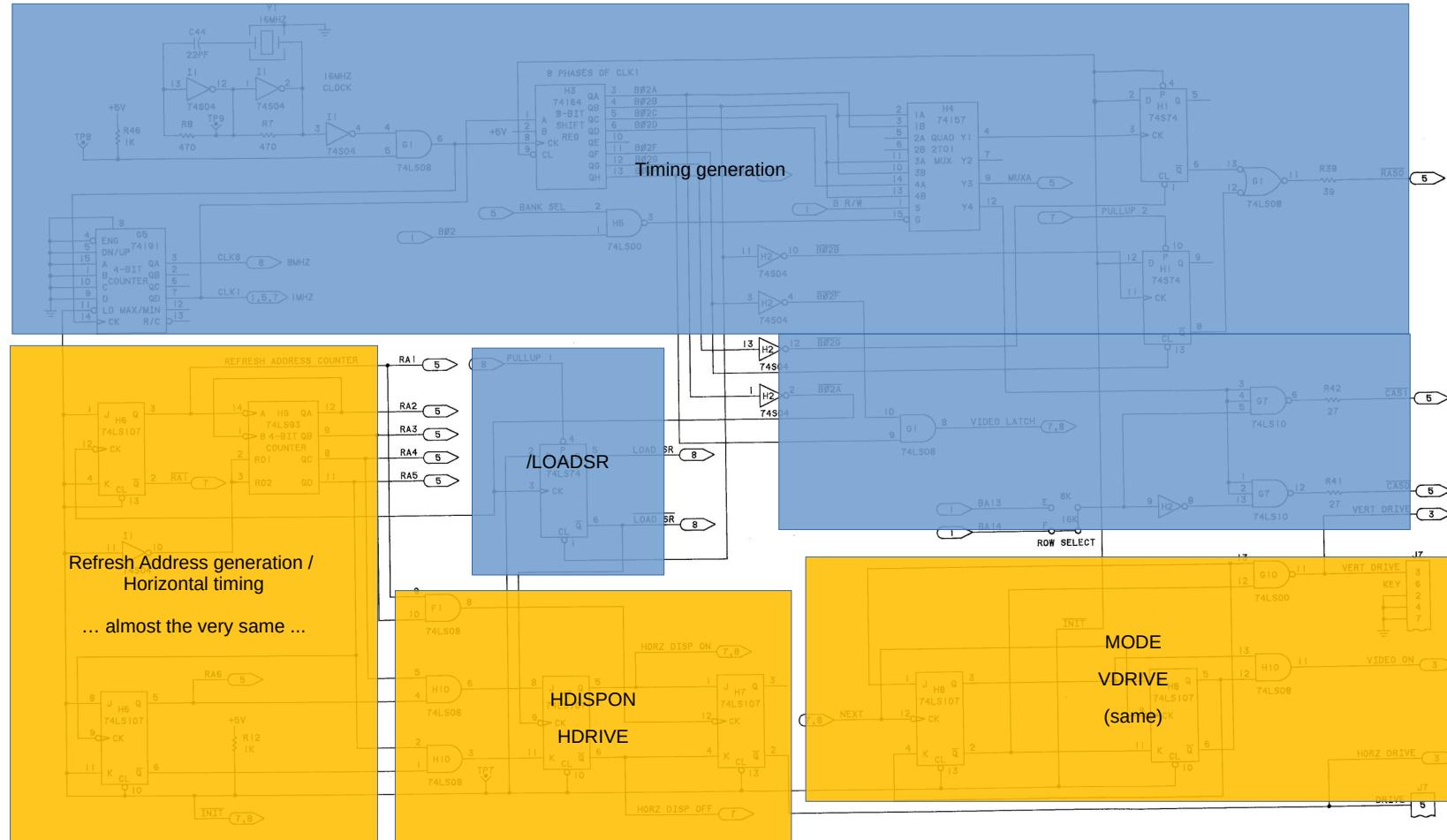
DRAM
Control
signals

New video
Latch control



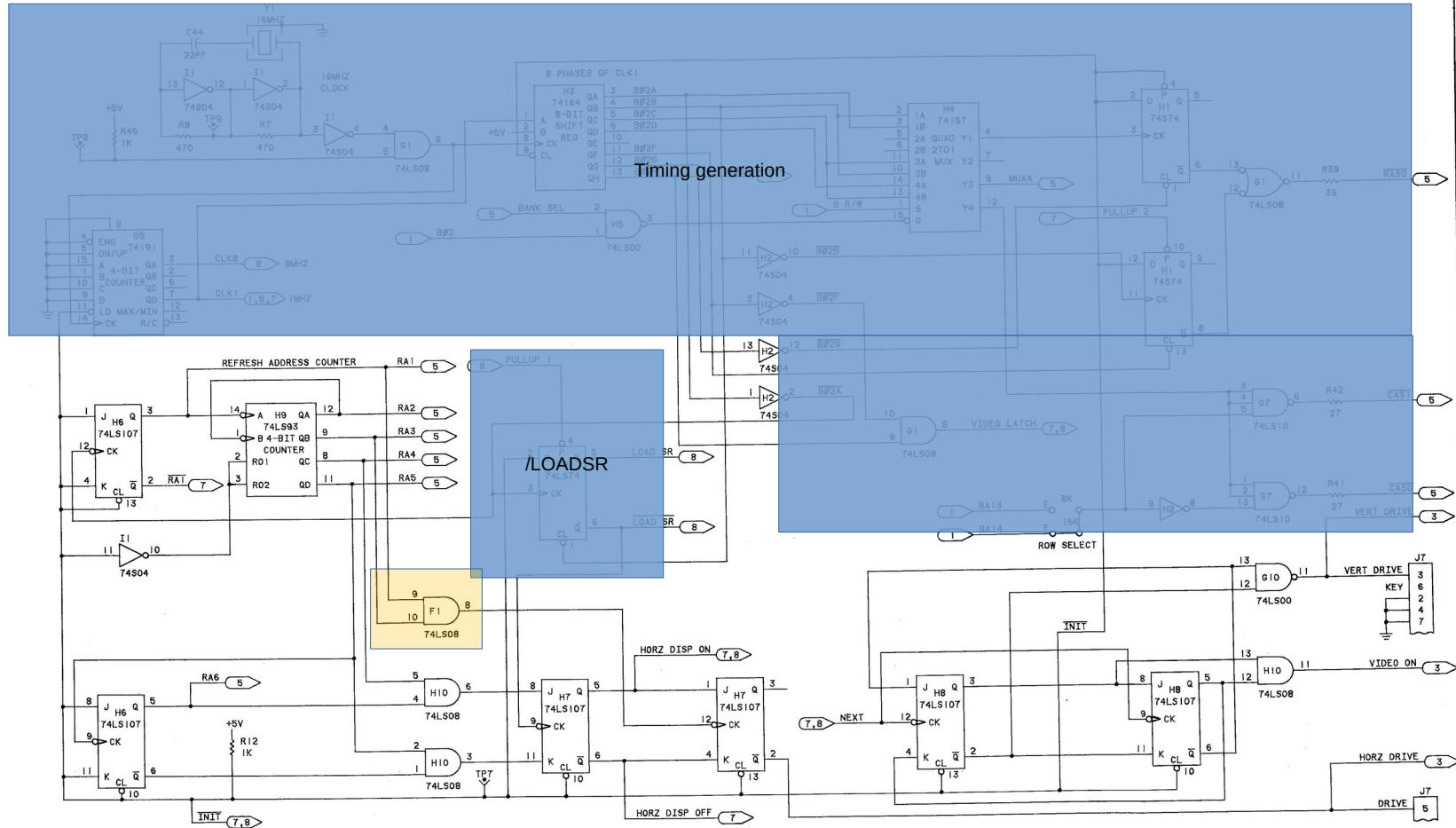
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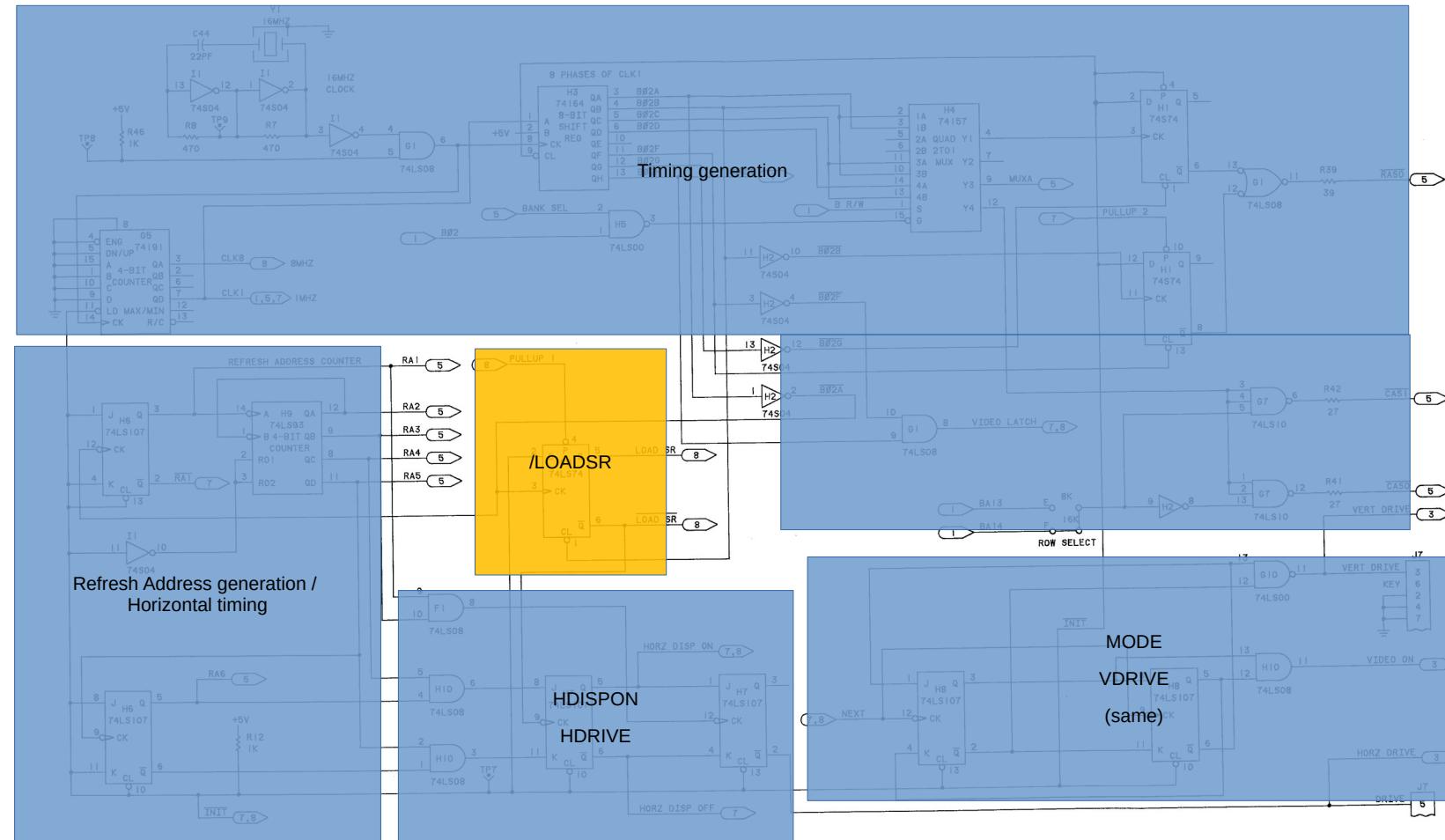
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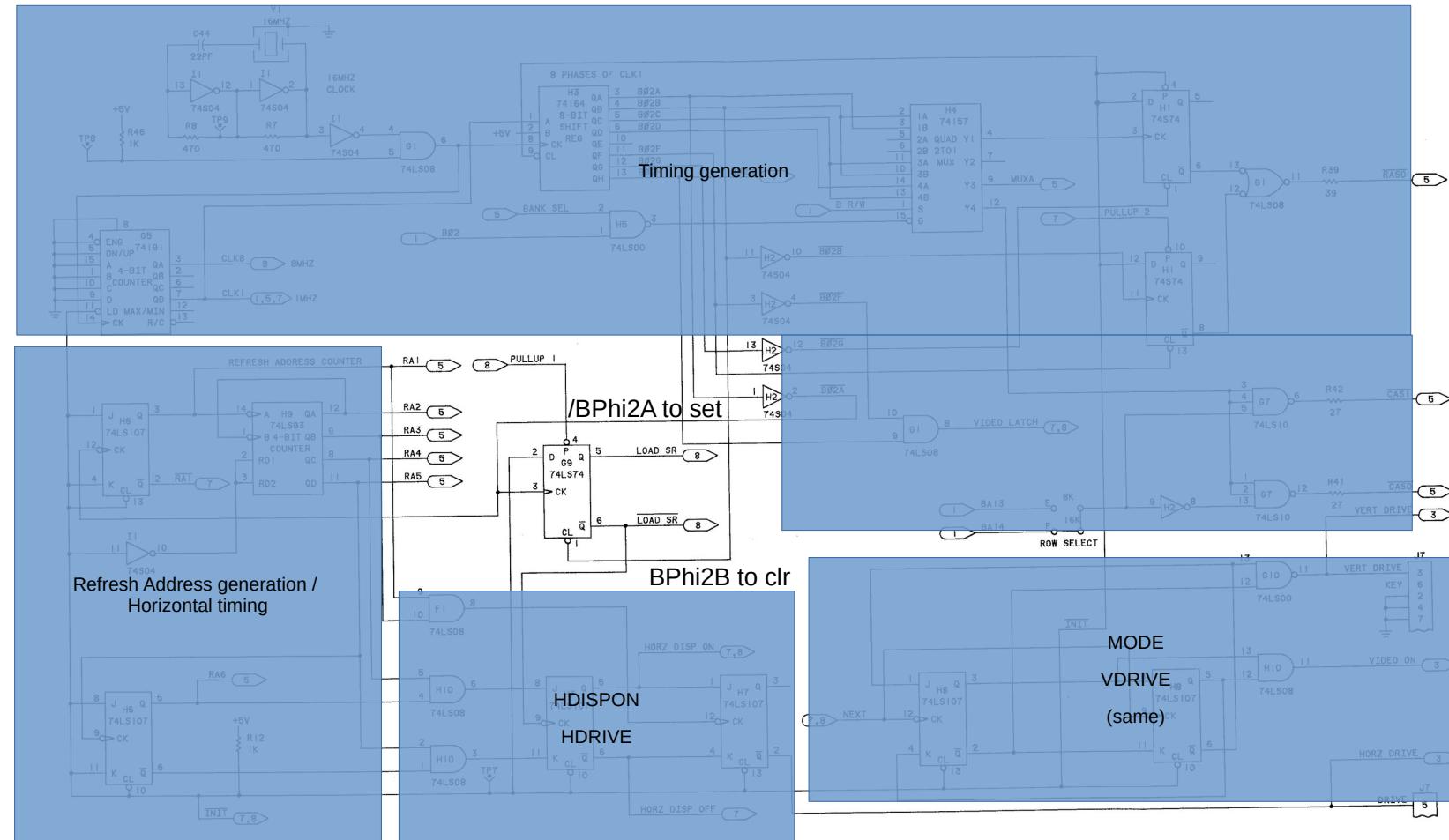
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1B02A

B02B

LOADSR

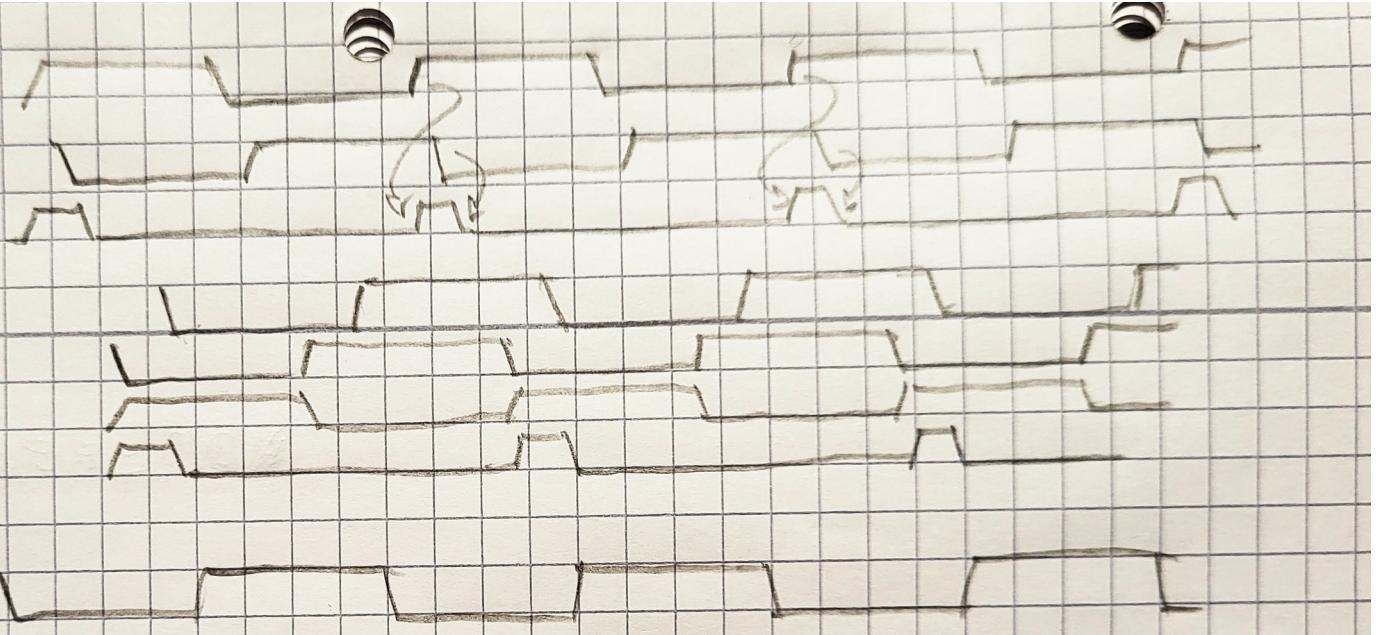
B02H

B02F

~~B02F~~

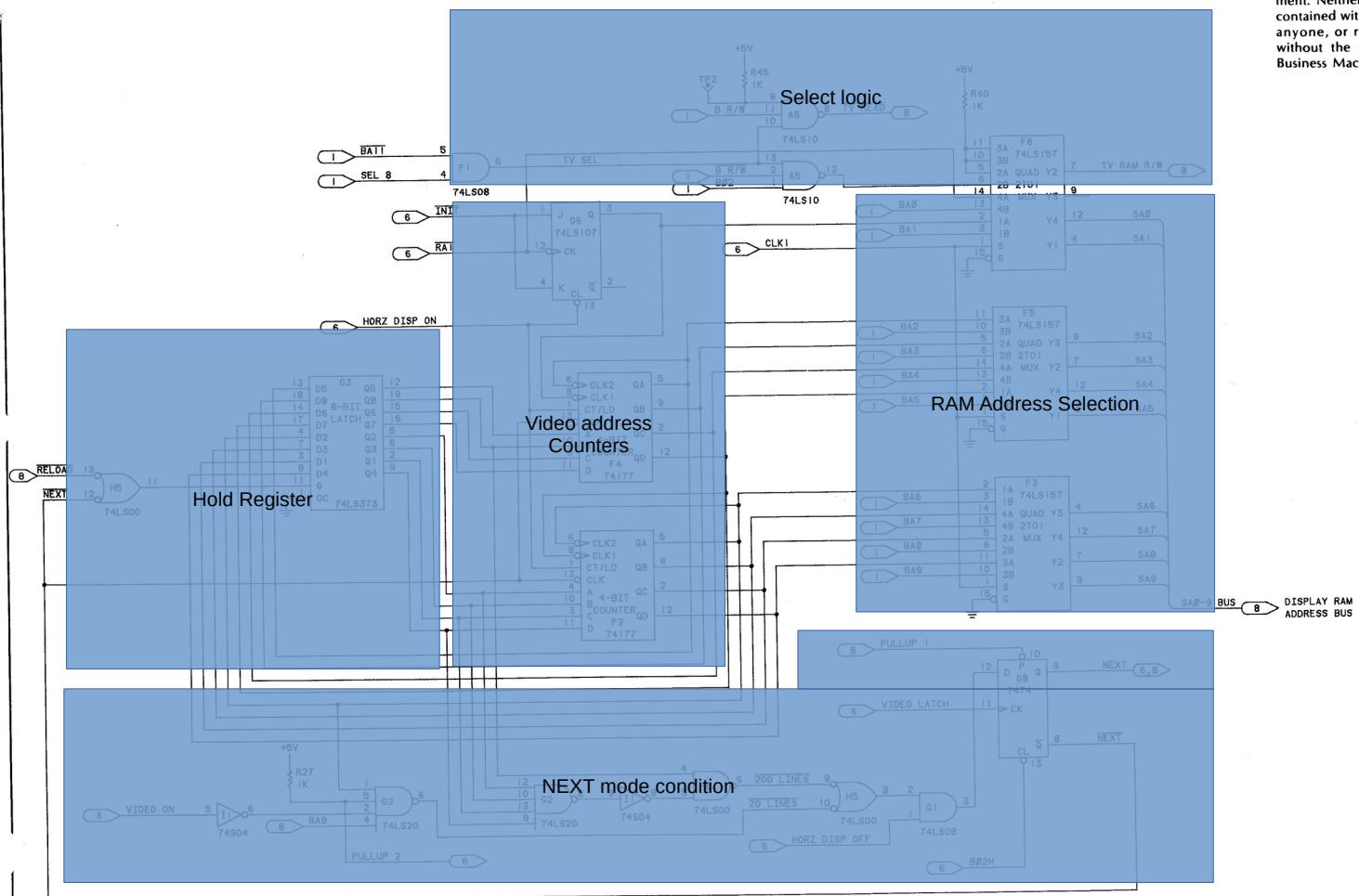
VIDEO latch

02



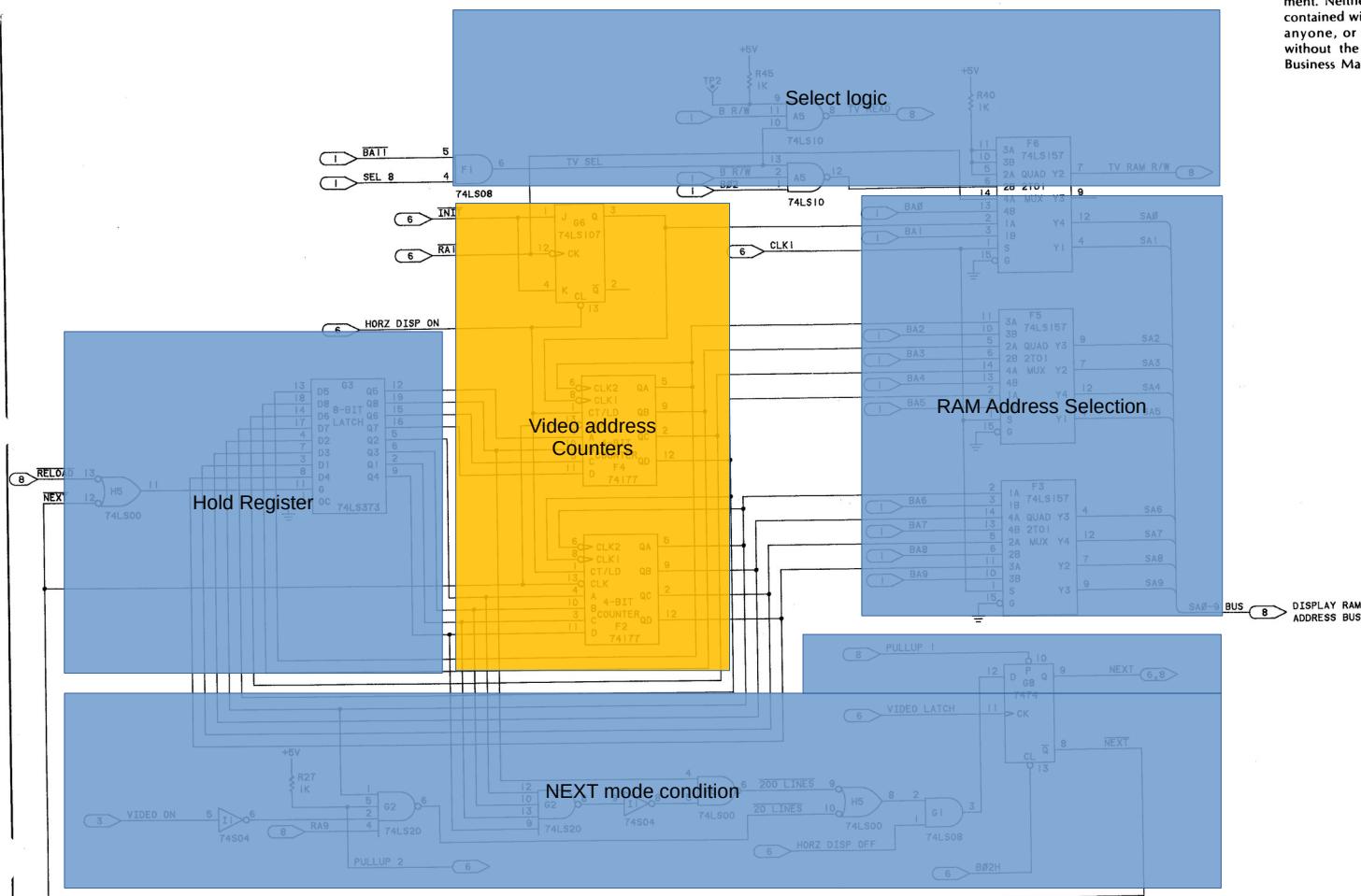
Dynamic PET – video counters

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commodore
LOGIC DIAGRAM
DYNAMIC PET
DISPLAY LOGIC
SIZE D 320349 RE A
SCALE — SHEET 7 OF 9

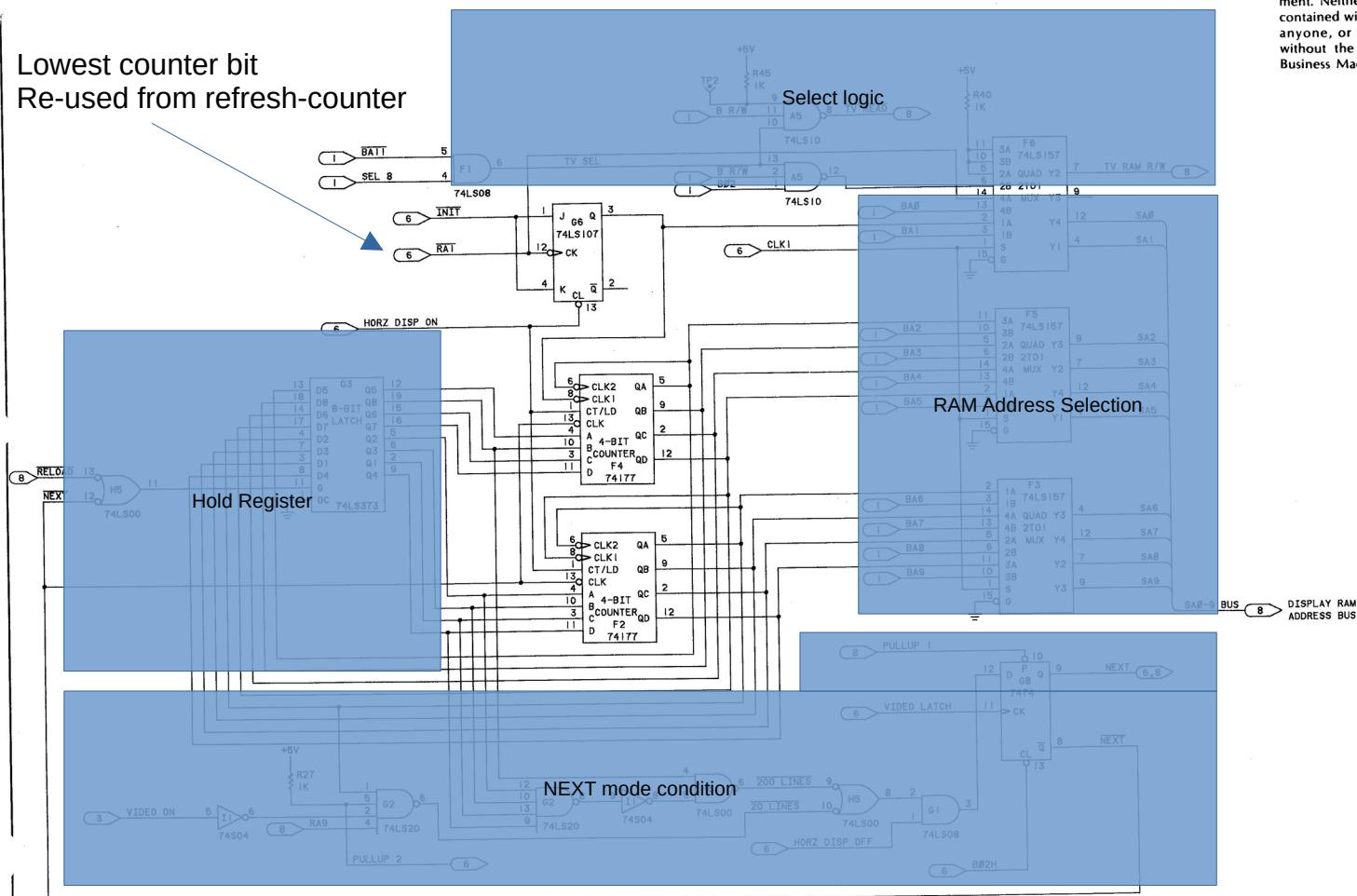
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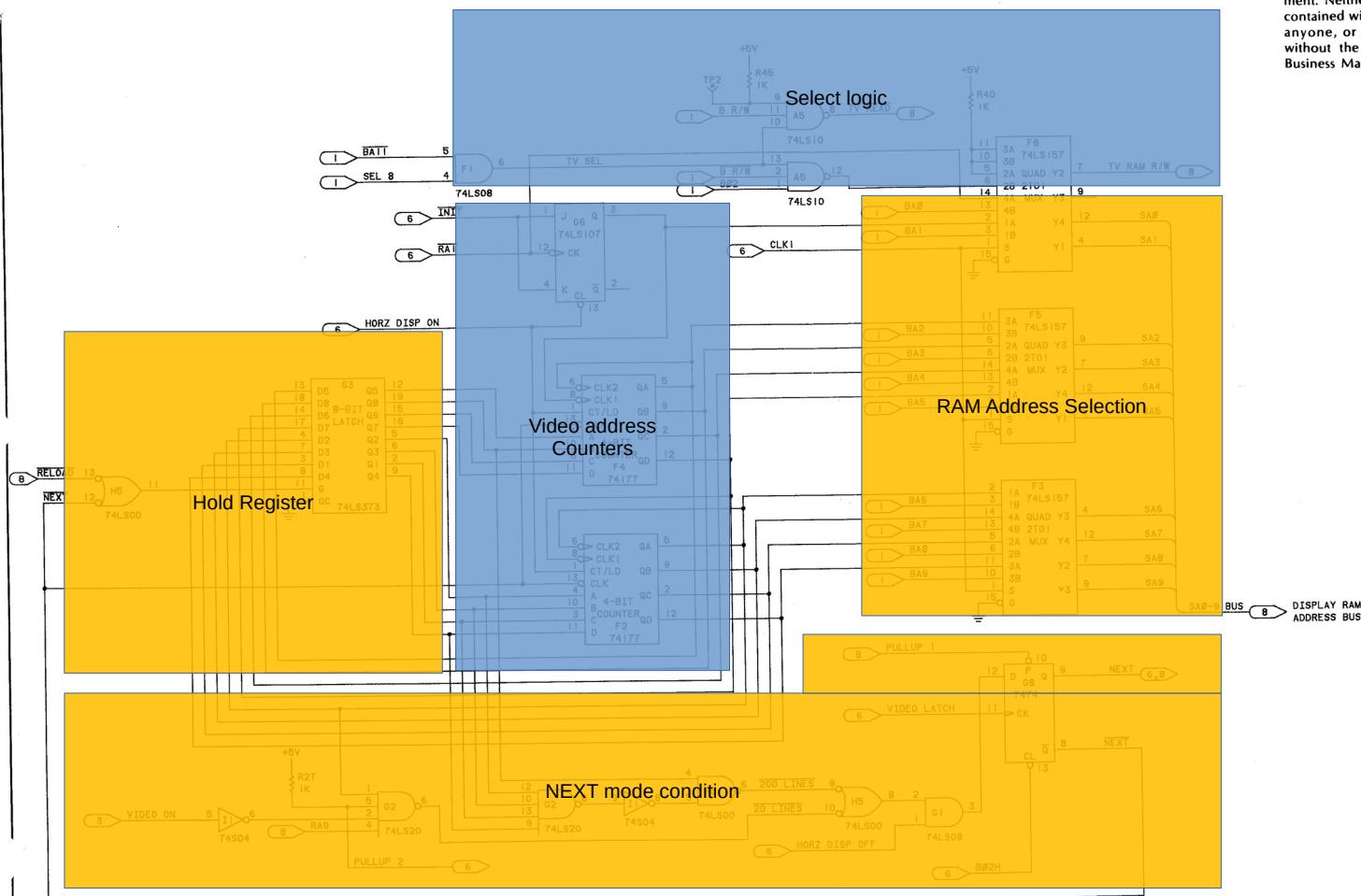
commodore
LOGIC DIAGRAM
DYNAMIC PET
DISPLAY LOGIC
SIZE D 320349
SCALE _____ SHEET 7 OF

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Lowest counter bit Re-used from refresh-counter



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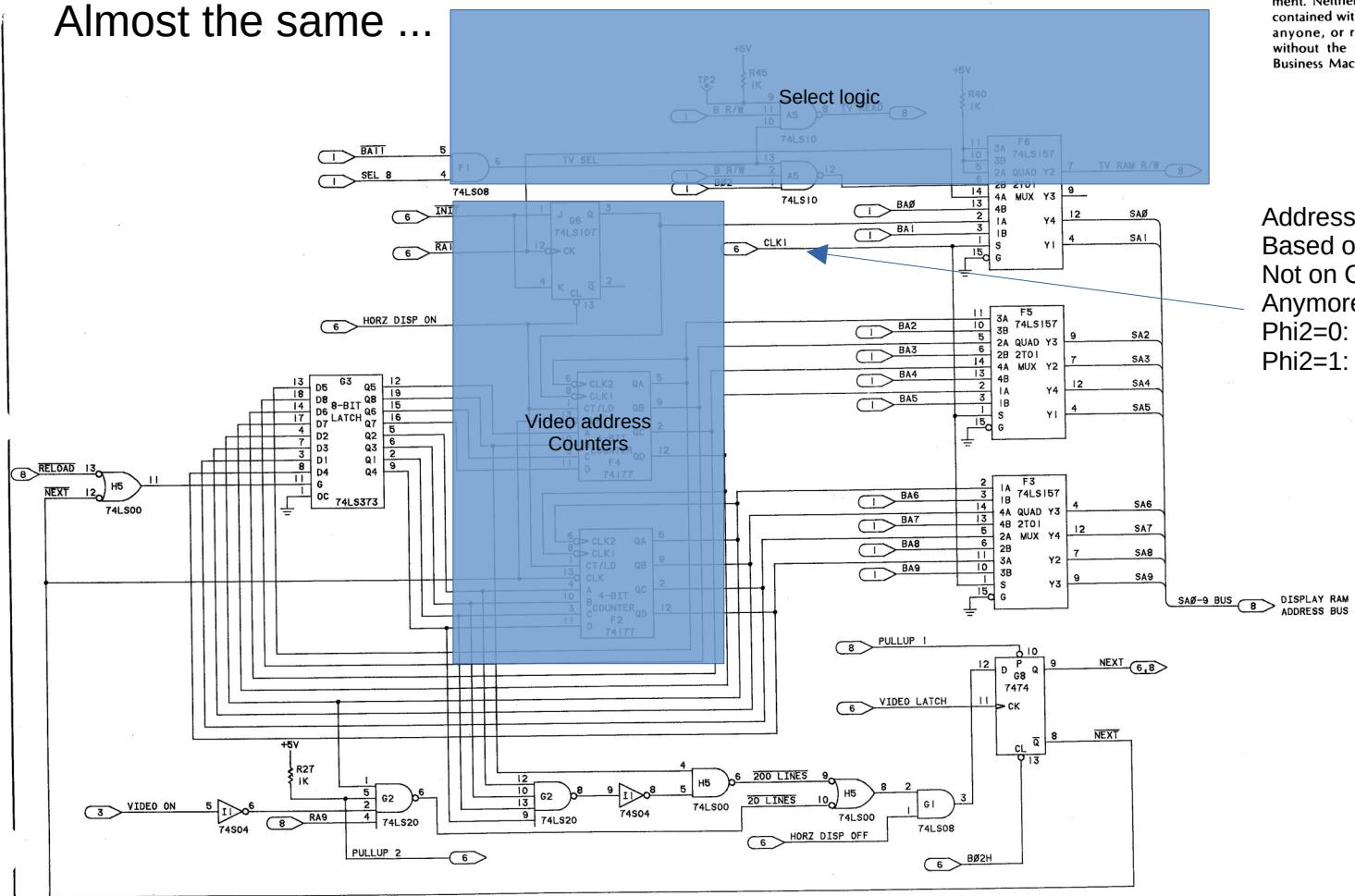
[www.silene.com](#)

LOGIC DIAGRAM
DYNAMIC PET

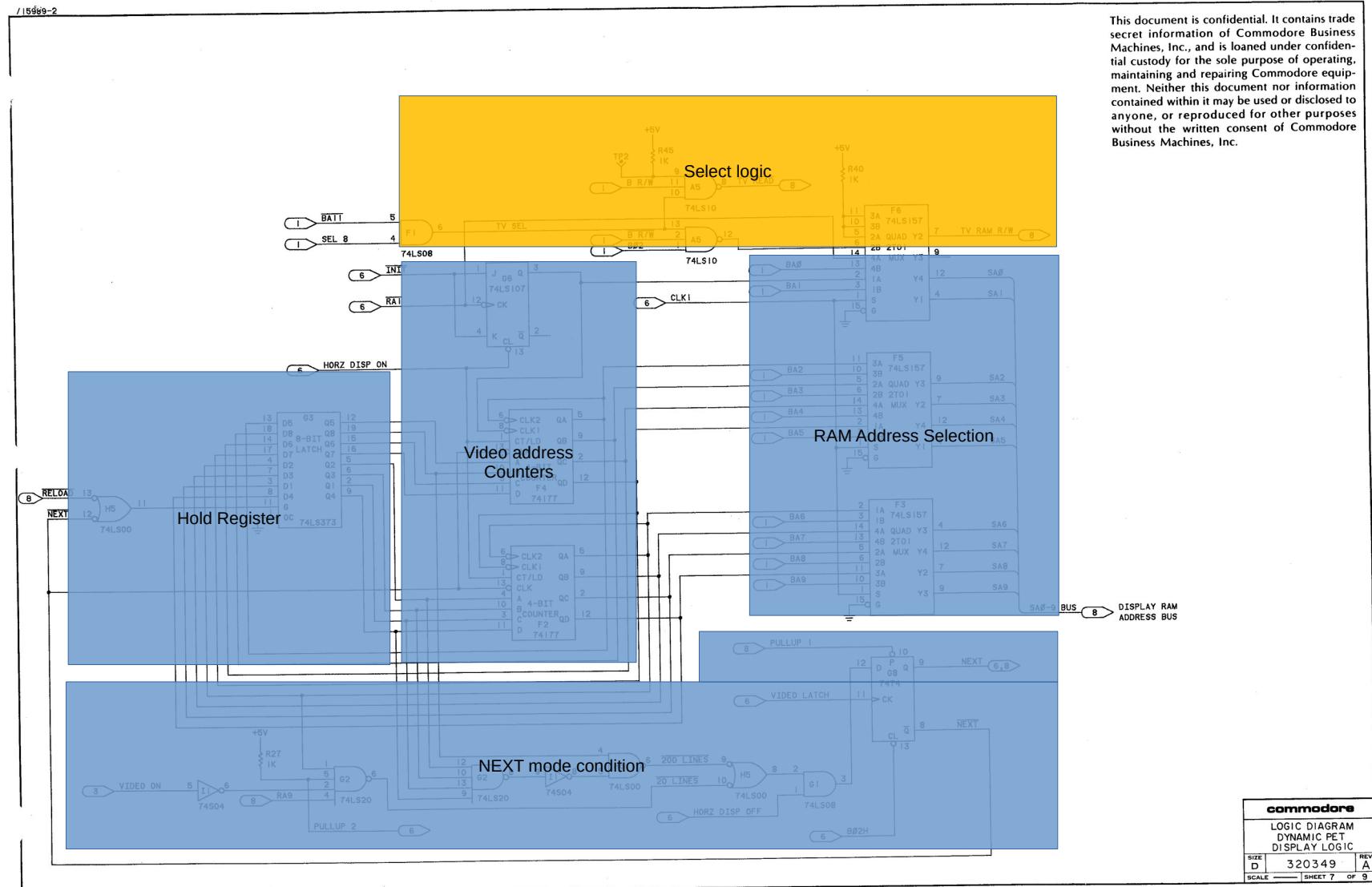
DISPLAY LOGIC
SIZE D 320349

SCALE ————— SHEET 7 OF

Almost the same ...



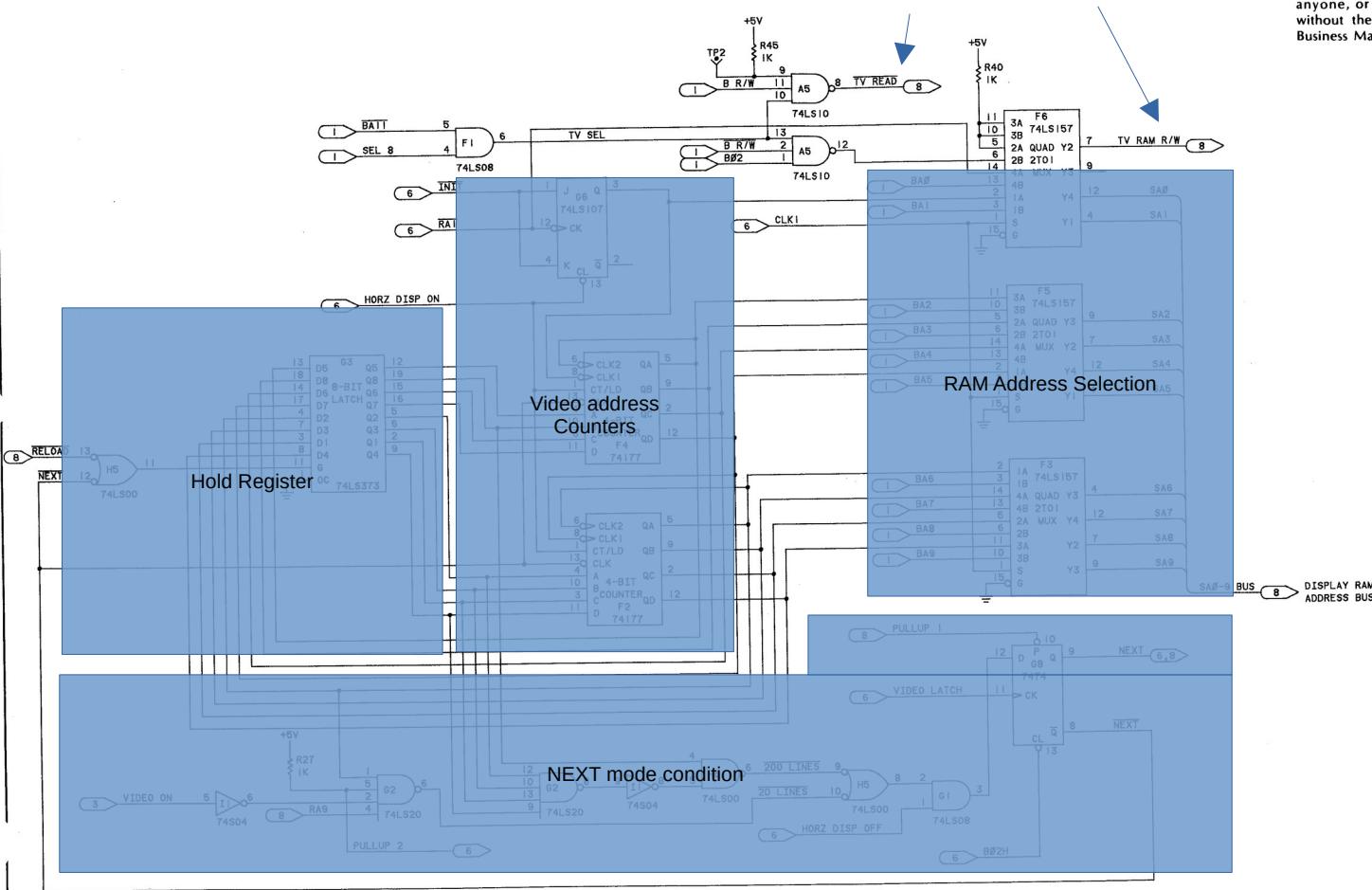
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LOGIC DIAGRAM
DYNAMIC PET
DISPLAY LOGIC
SHEET D 320349 REV A
SCALE SHEET 7 OF 9

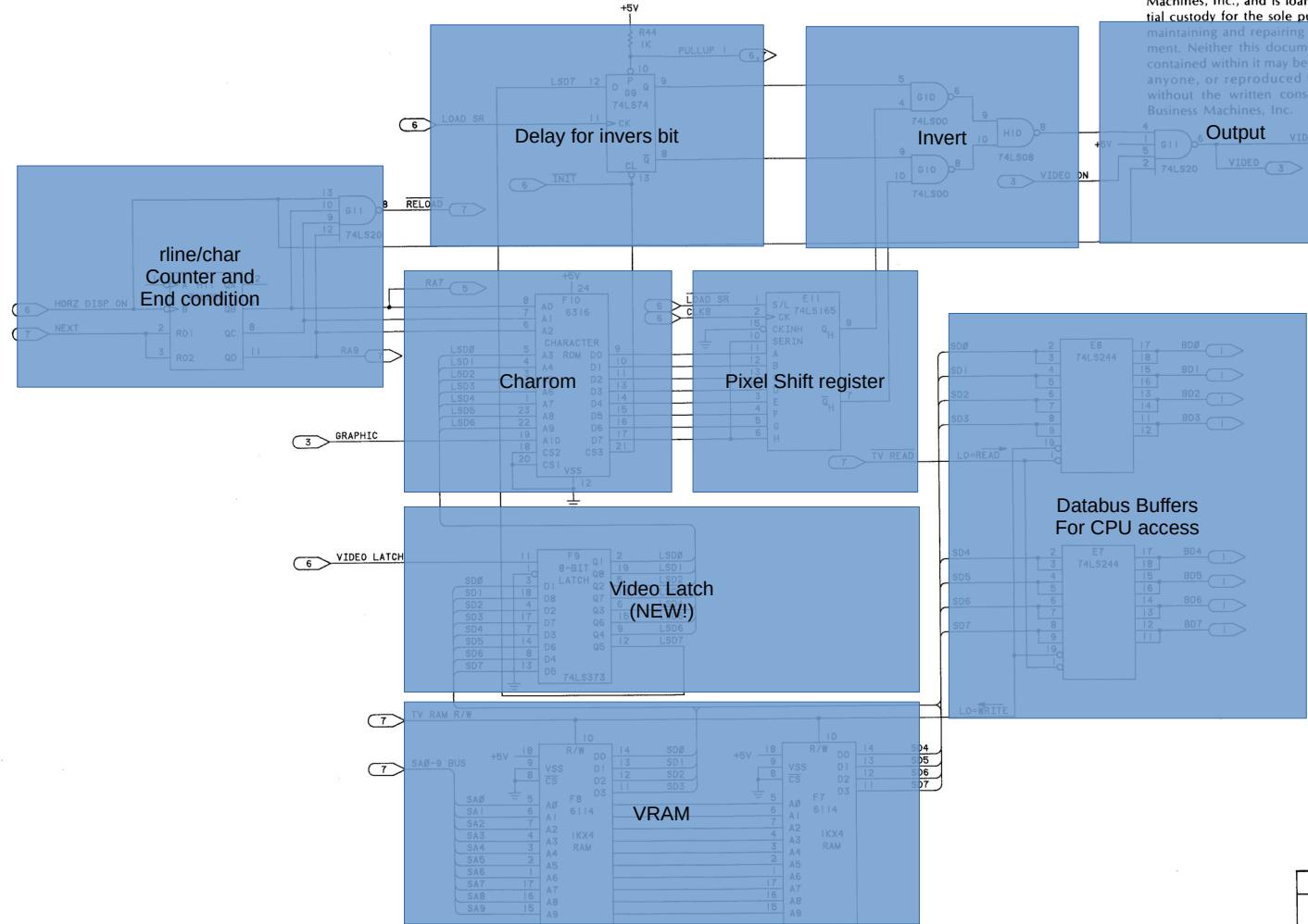
Creates signals for
CPU read and write
Access to video RAM
- wr only when Phi2 is high!

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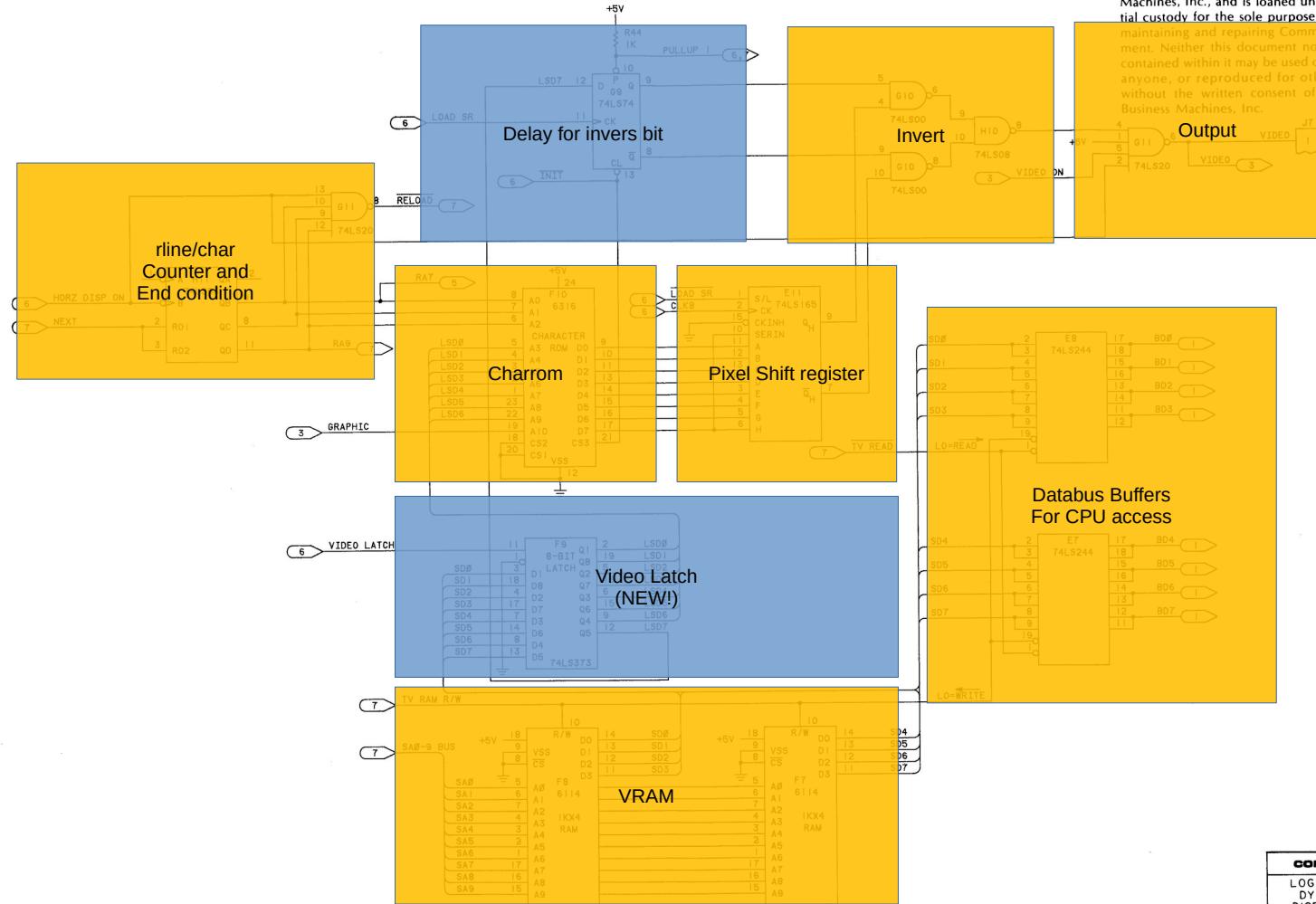


Dynamic PET – video RAM and pixel out

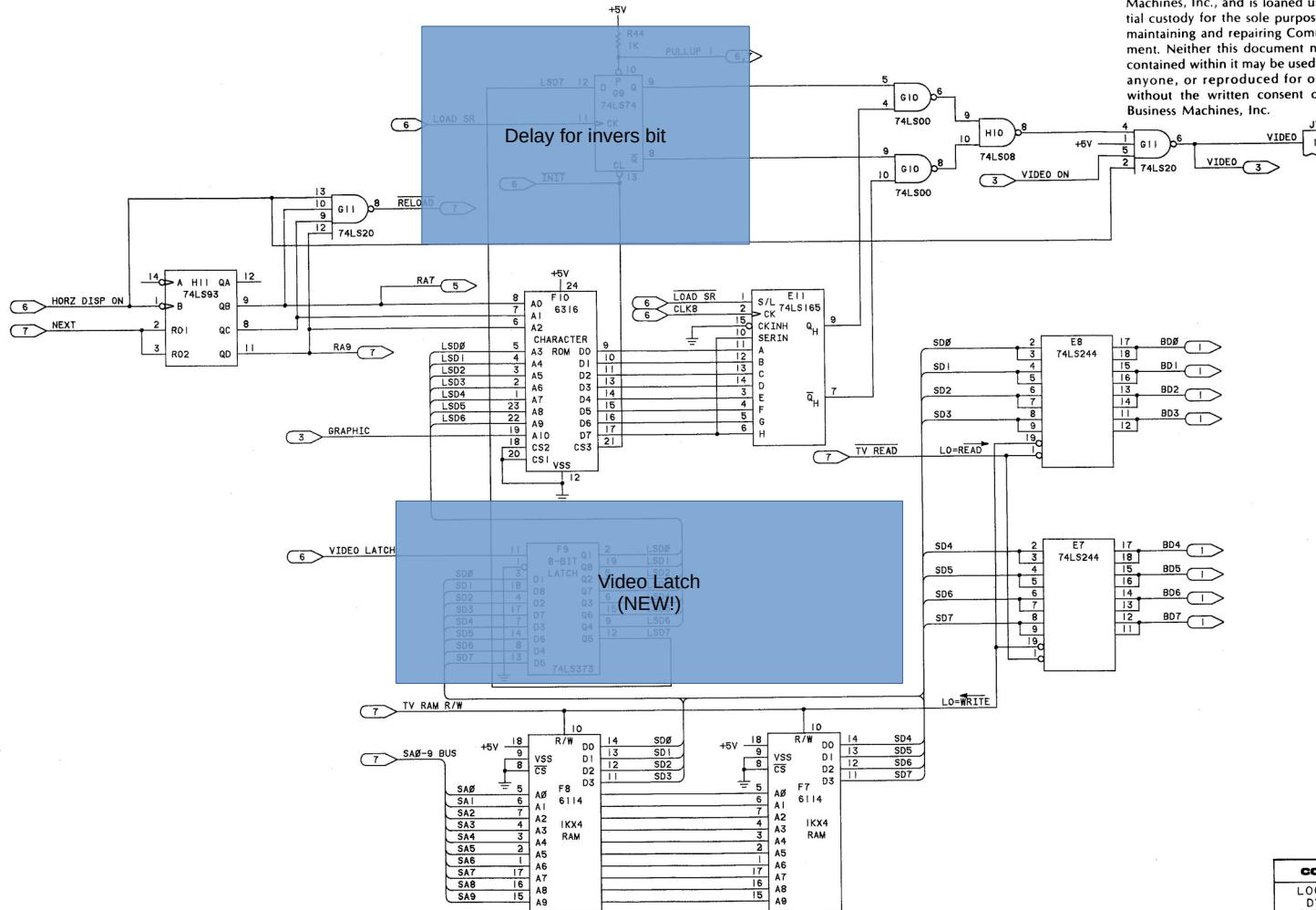
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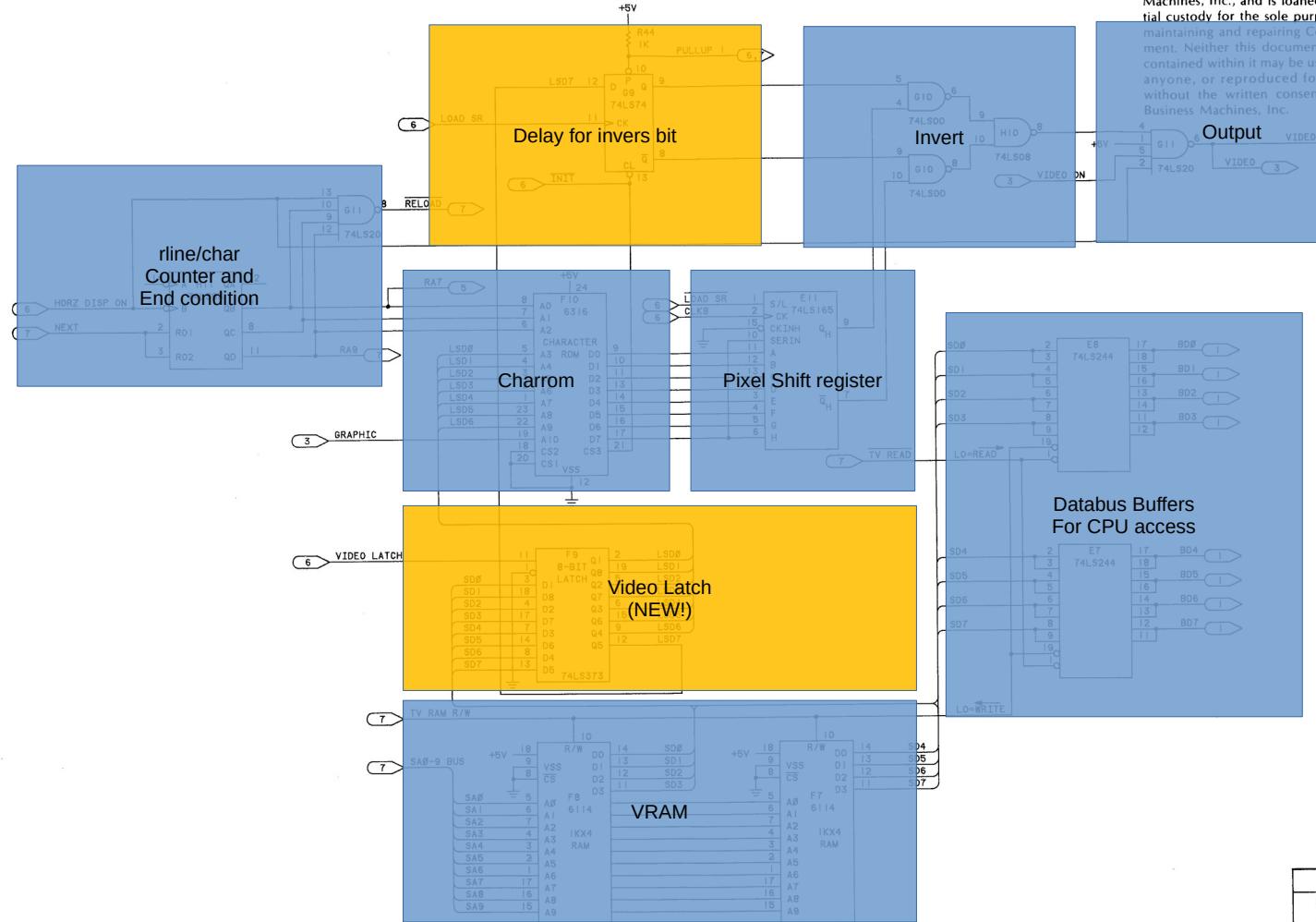
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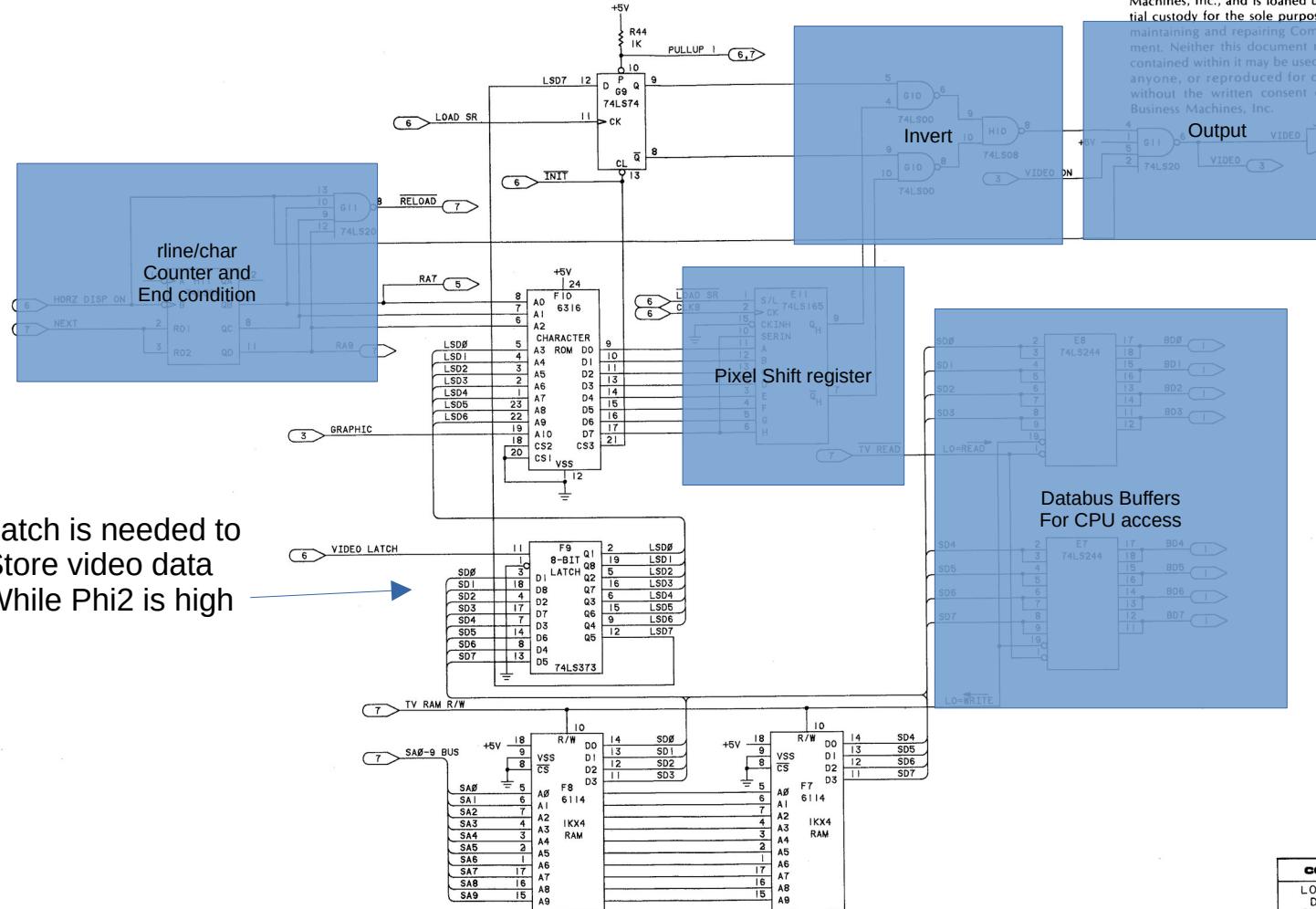
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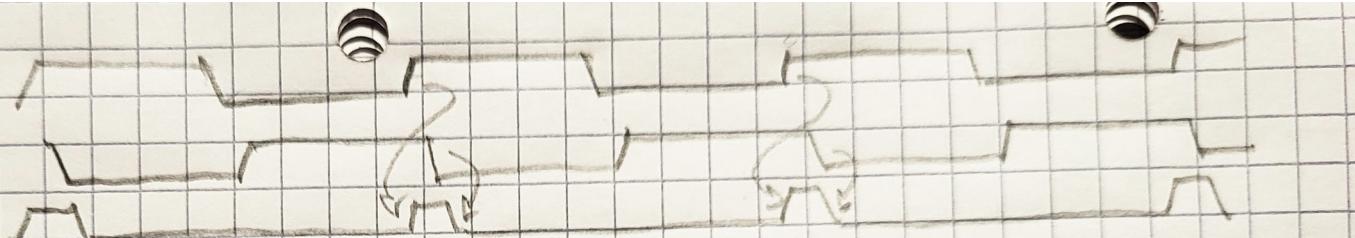
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B₀RA

B₀RB

LOADSR

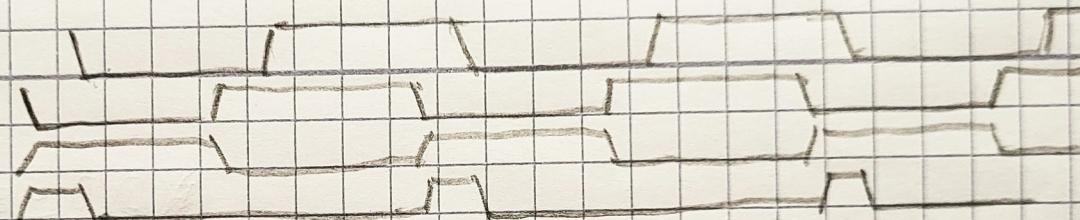


B₀RH

B₀RF

/B₀RF

Video latch



φ2

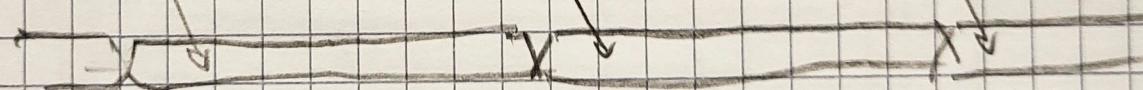
VRAM Addr

X VADDR X CPU A. X V.A. X CBAK X X X

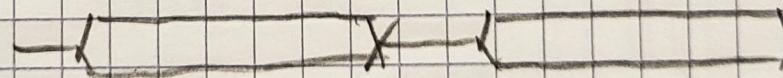
VRAM D



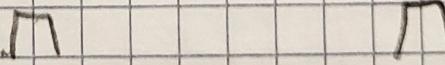
latch / charon A



charon Dout



SR load



Summary

Commodore PET Video

Five different types of Video output



2001:

- 40x25 chars
- fixed timing
- 1k VRAM
- „snow“

2001N / 3032:

- 40x25 chars
- fixed timing
- 1k VRAM

4032

- 40x25 chars
- CRTC timing
- 1k VRAM

8032

- 80x25 chars
- CRTC timing
- 2k VRAM

8296

- 80x25 chars
- CRTC timing
- 4k(+) VRAM