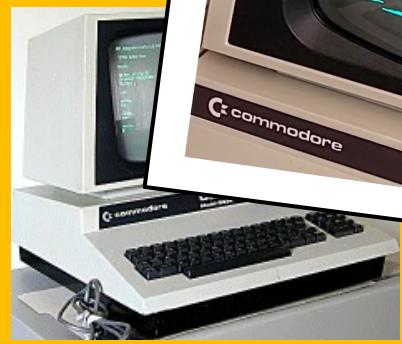


# 8-bit • times

## Commodore PET Video – Part 2

The CRTC Models

How do they work?  
what can they do?  
**Demos!**



# Commodore PET Video

Five different types of Video output



2001:

- 40x25 chars
- fixed timing
- 1k VRAM
- „snow“

2001N / 3032:

- 40x25 chars
- fixed timing
- 1k VRAM

4032

- 40x25 chars
- **CRTC timing**
- 1k VRAM

8032

- 80x25 chars
- **CRTC timing**
- 2k VRAM

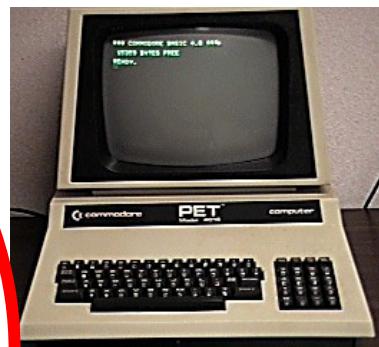
8296

- 80x25 chars
- **CRTC timing**
- 8k VRAM

# Commodore PET Video Part 1

*Recap*

Five different types of Video output



2001:

- 40x25 chars
- fixed timing
- 1k VRAM
- „SNOW“

2001N / 3032:

- 40x25 chars
- fixed timing
- 1k VRAM

4032

- 40x25 chars
- CRTC timing
- 1k VRAM

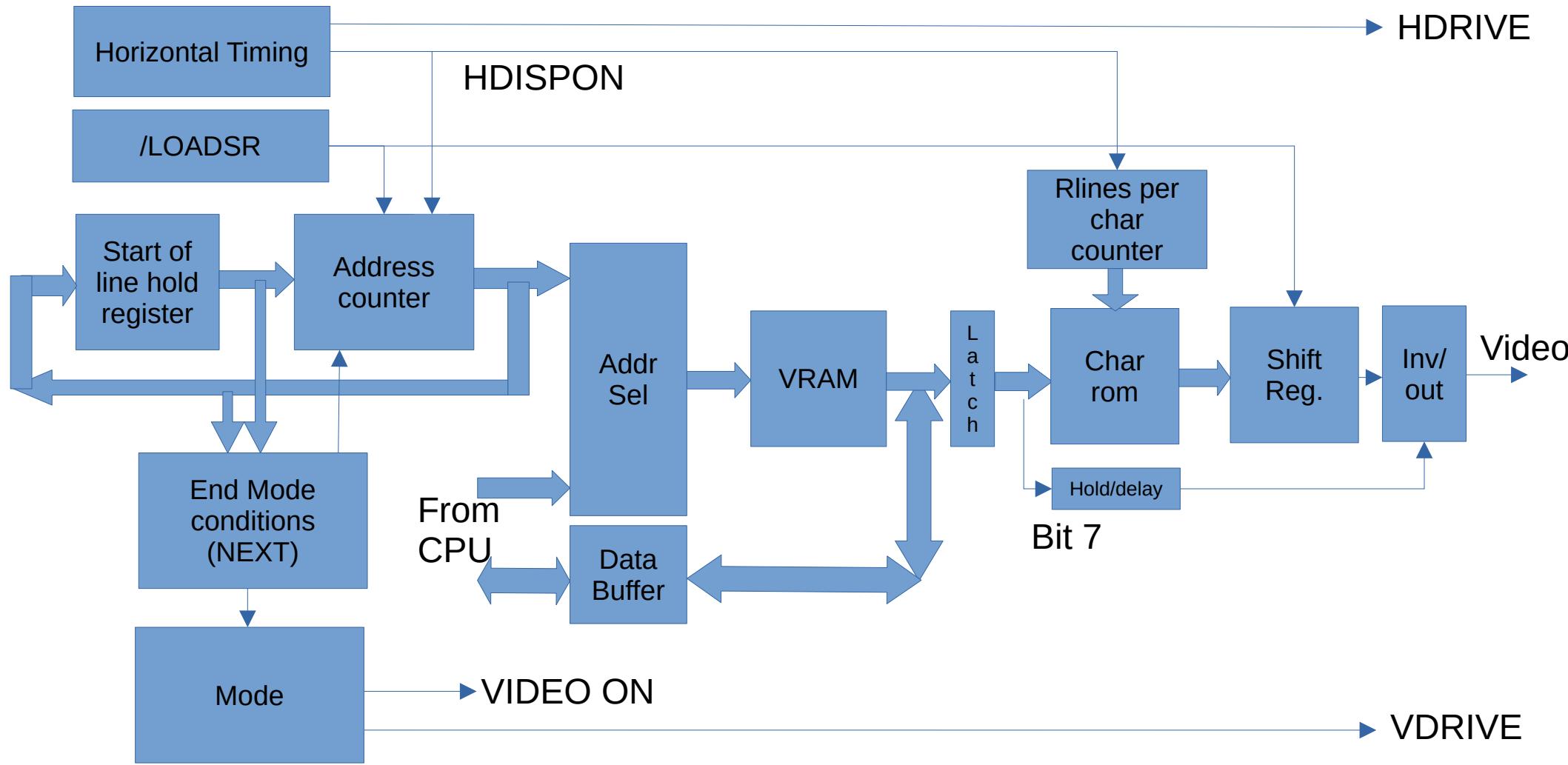
8032

- 80x25 chars
- CRTC timing
- 2k VRAM

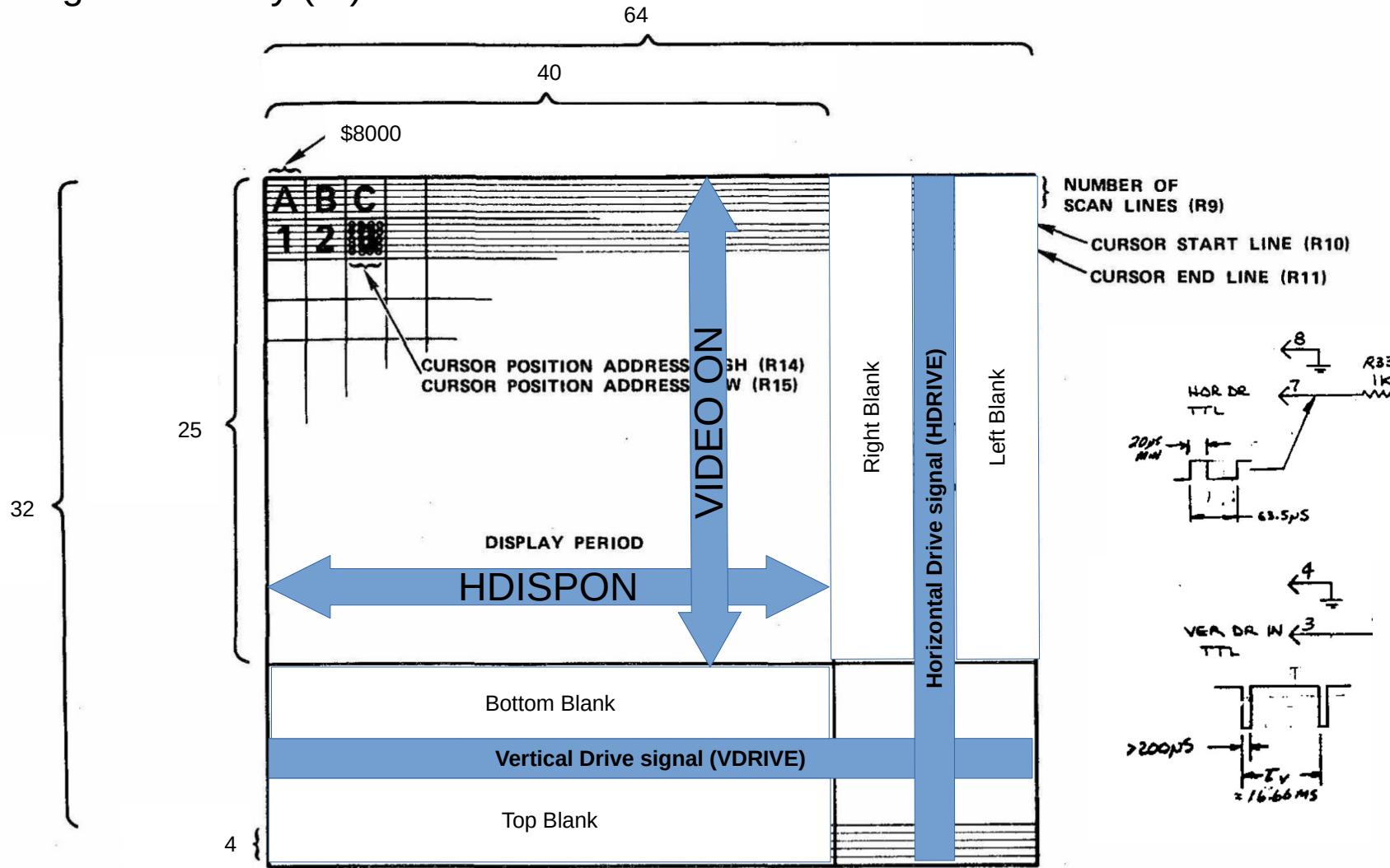
8296

- 80x25 chars
- CRTC timing
- 8k VRAM

# Dynamic PET models w/ fixed timing



# Fixed video timing on an early (9") PET



# vSYNC interrupt & Charset

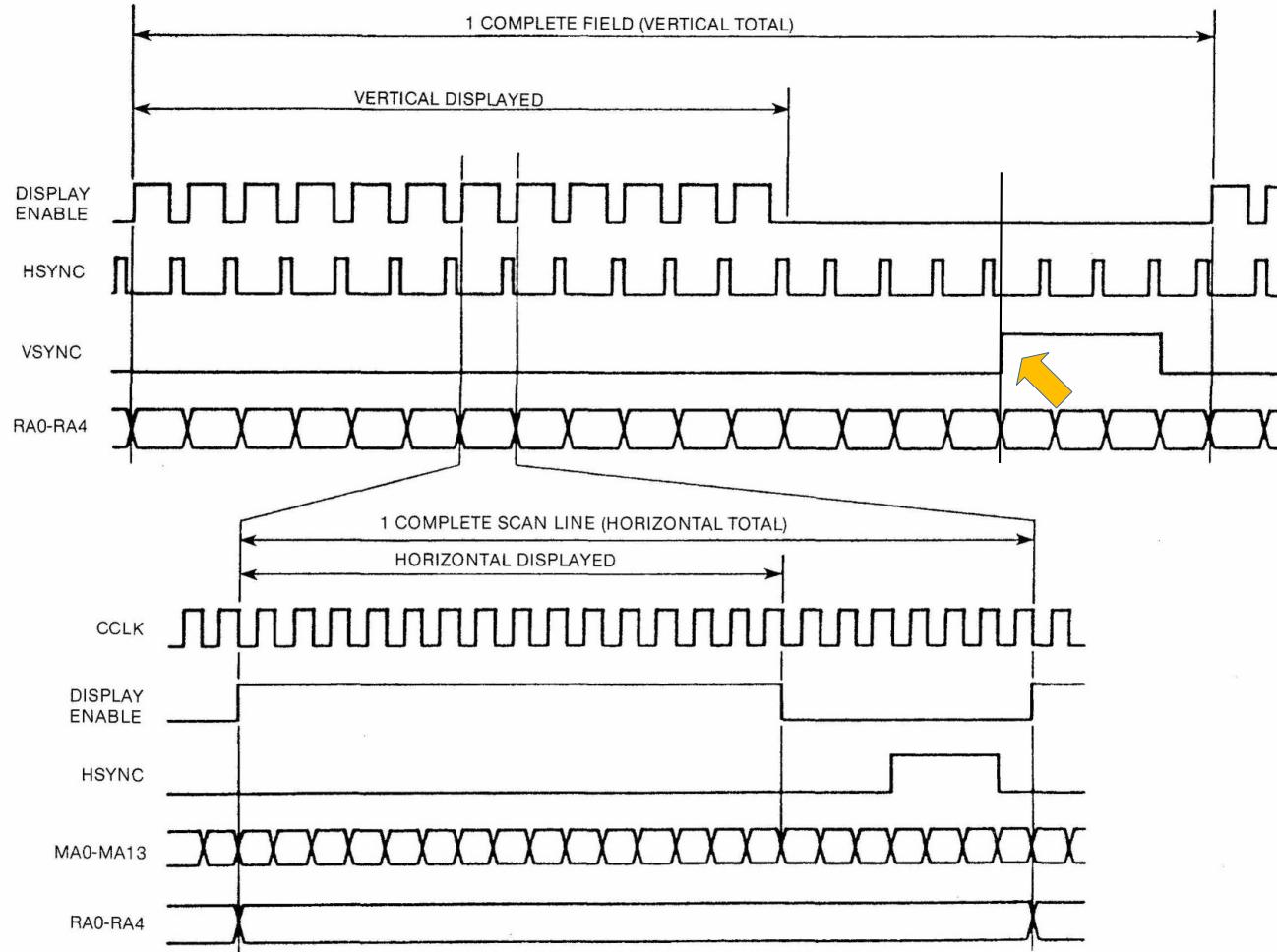
- From the schematics follows
  - Only a fixed character set
  - A single interrupt per frame (60 Hz)

# Demo charset / racing the beam

- crtcl6

# Explaining Racing the Beam

**Figure 2. Vertical and Horizontal Timing**



# Commodore PET Video Part 2

Five different types of Video output



2001:

- 40x25 chars
- fixed timing
- 1k VRAM
- „snow“

2001N / 3032:

- 40x25 chars
- fixed timing
- 1k VRAM

4032

- 40x25 chars
- CRTC timing
- 1k VRAM

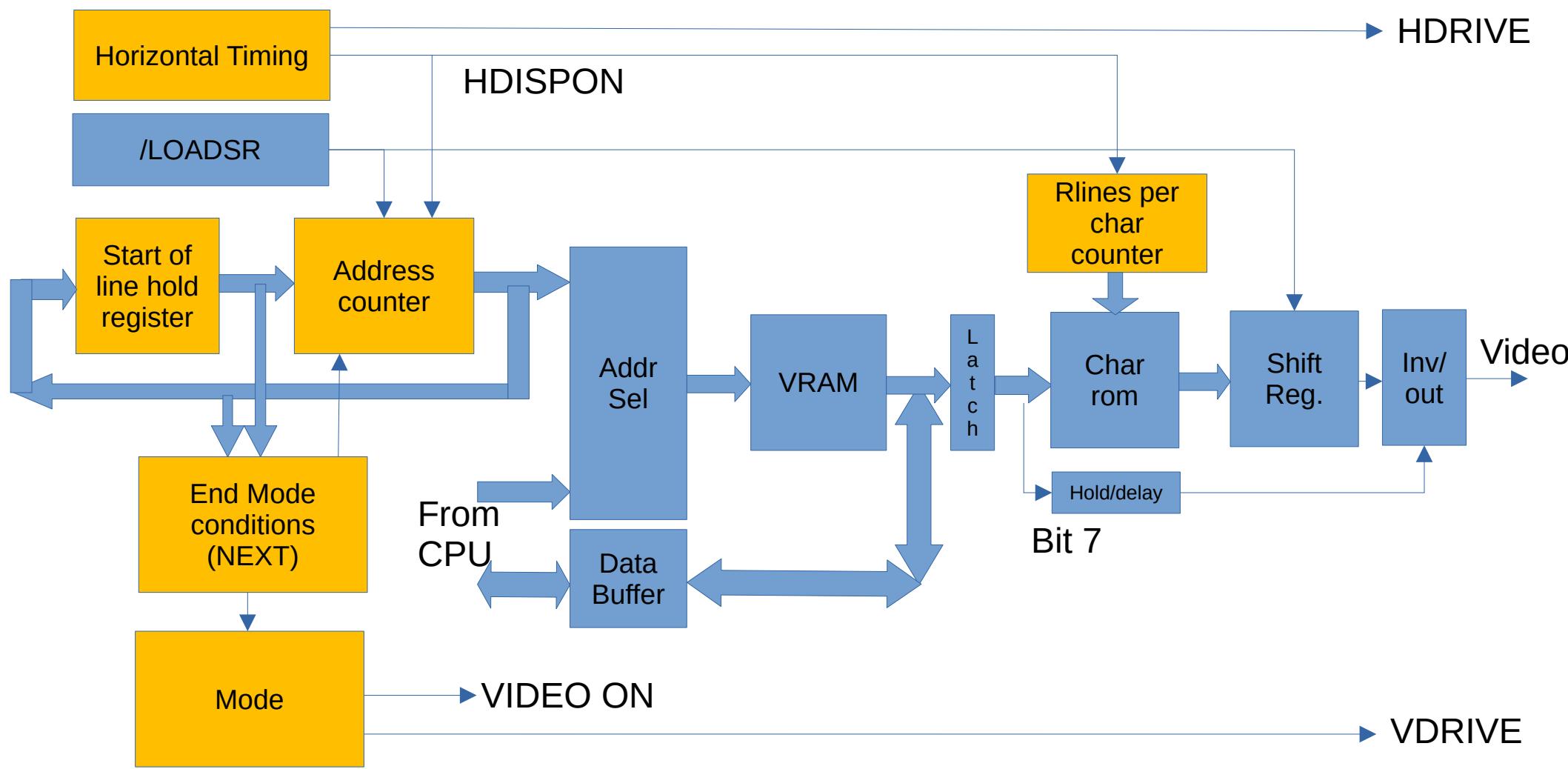
8032

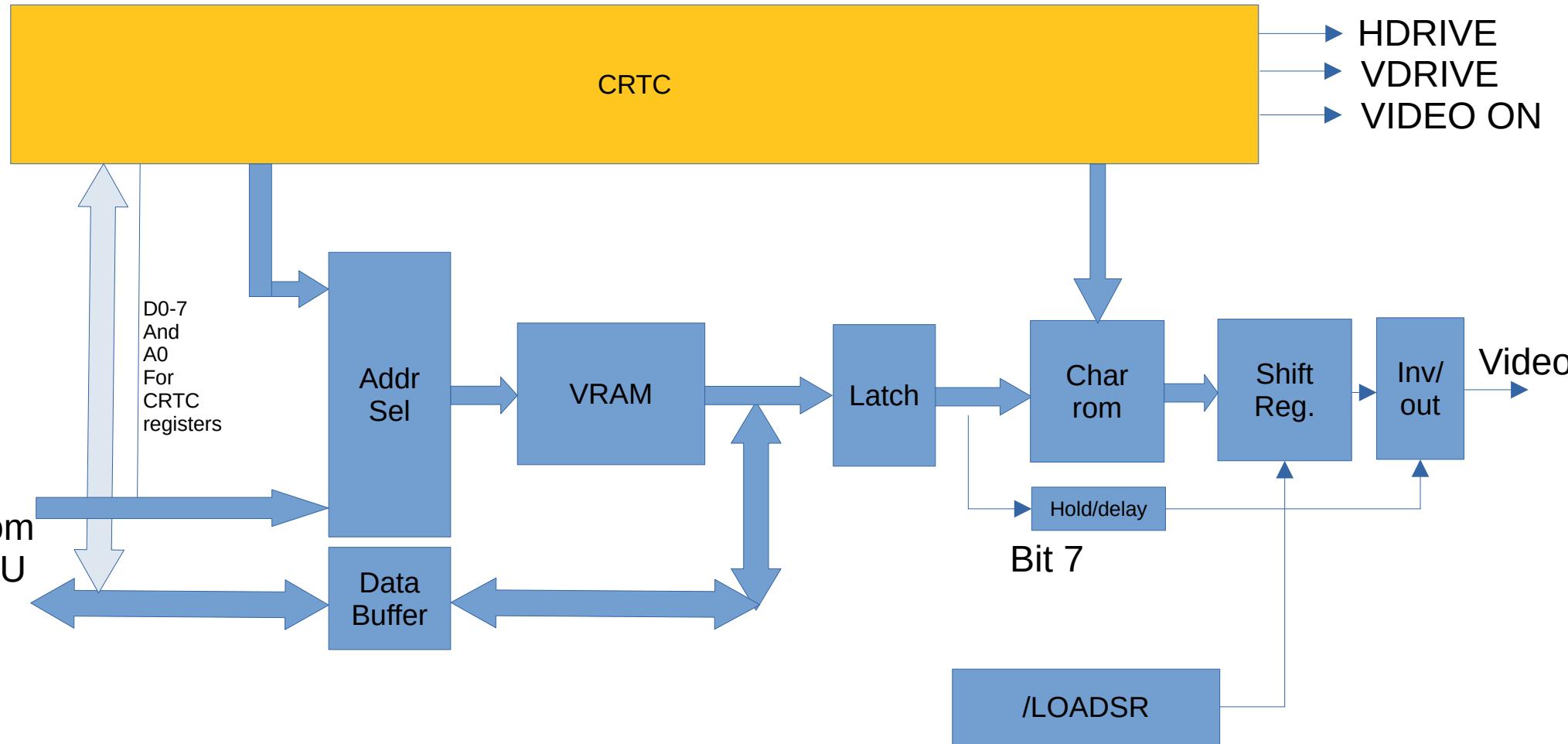
- 80x25 chars
- CRTC timing
- 2k VRAM

8296

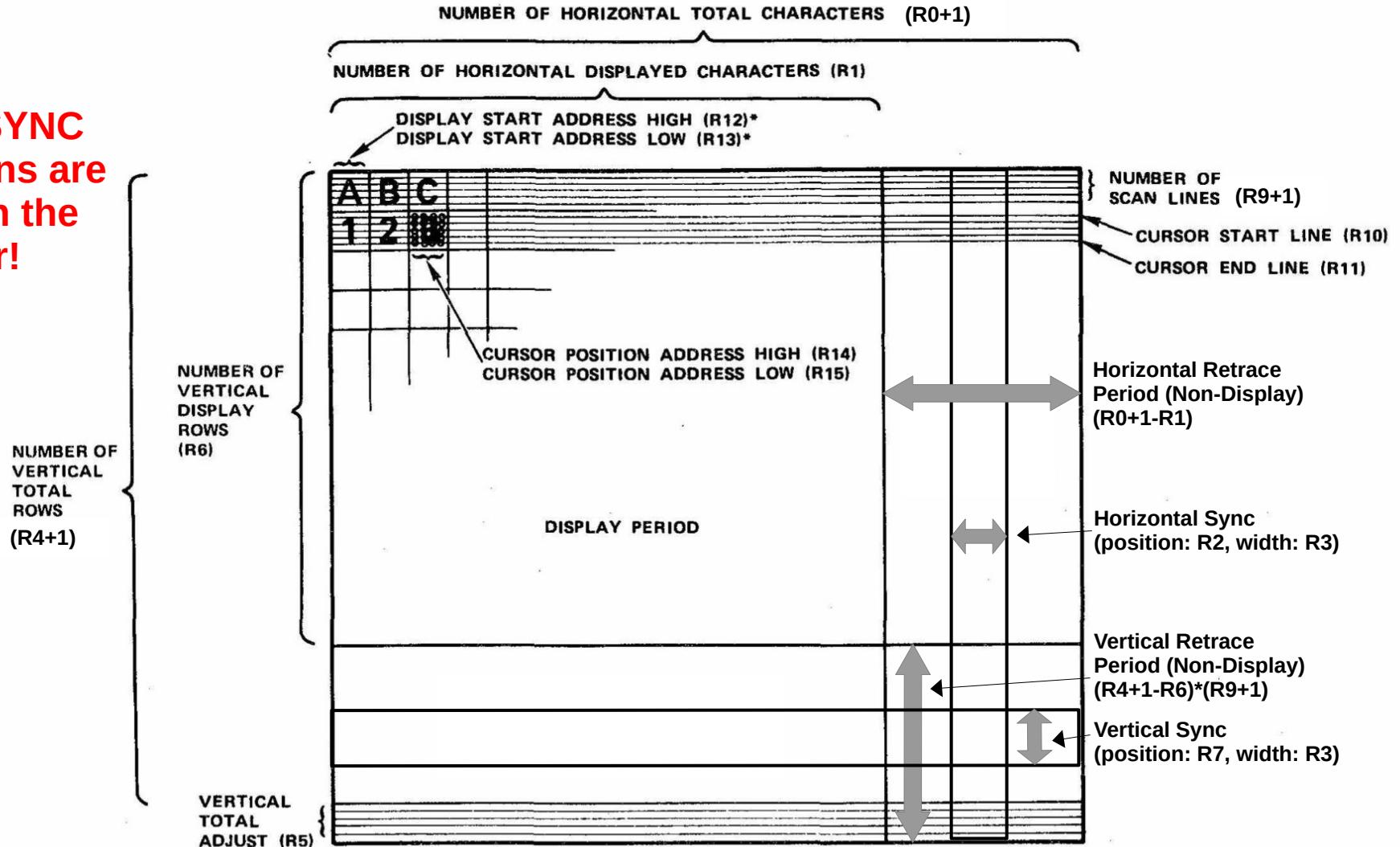
- 80x25 chars
- CRTC timing
- 8k VRAM

# Dynamic PET models w/ fixed timing

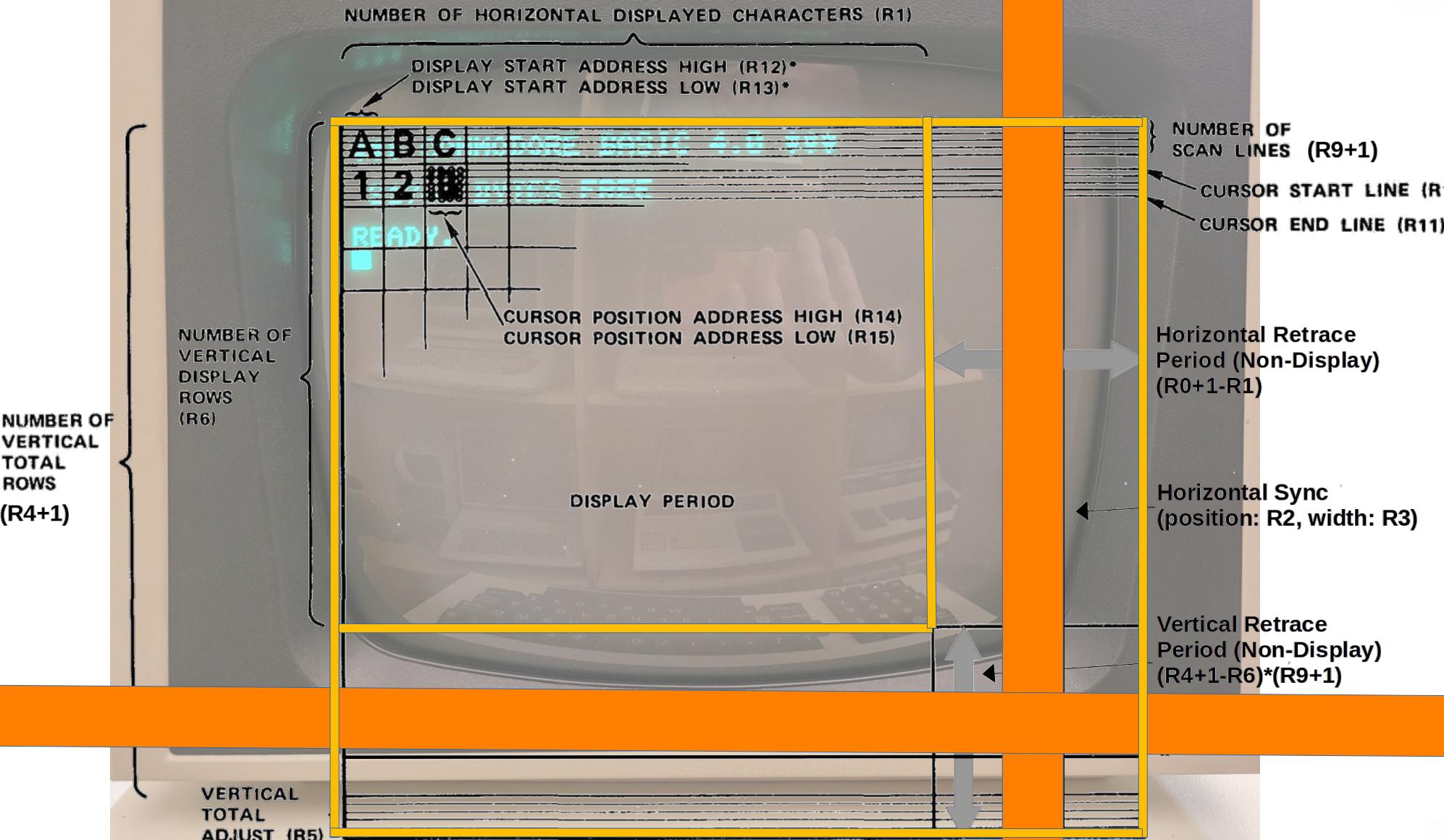


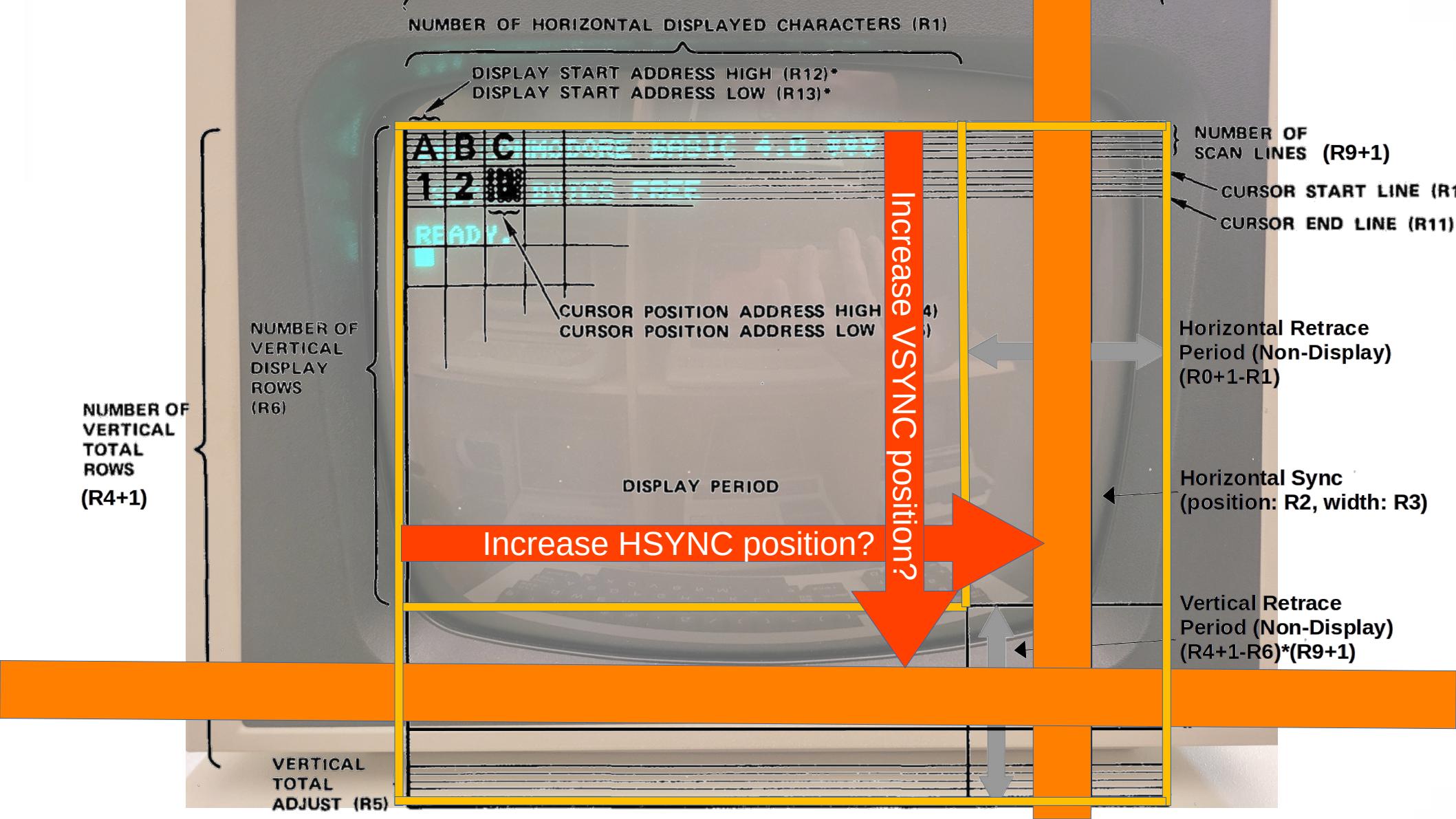


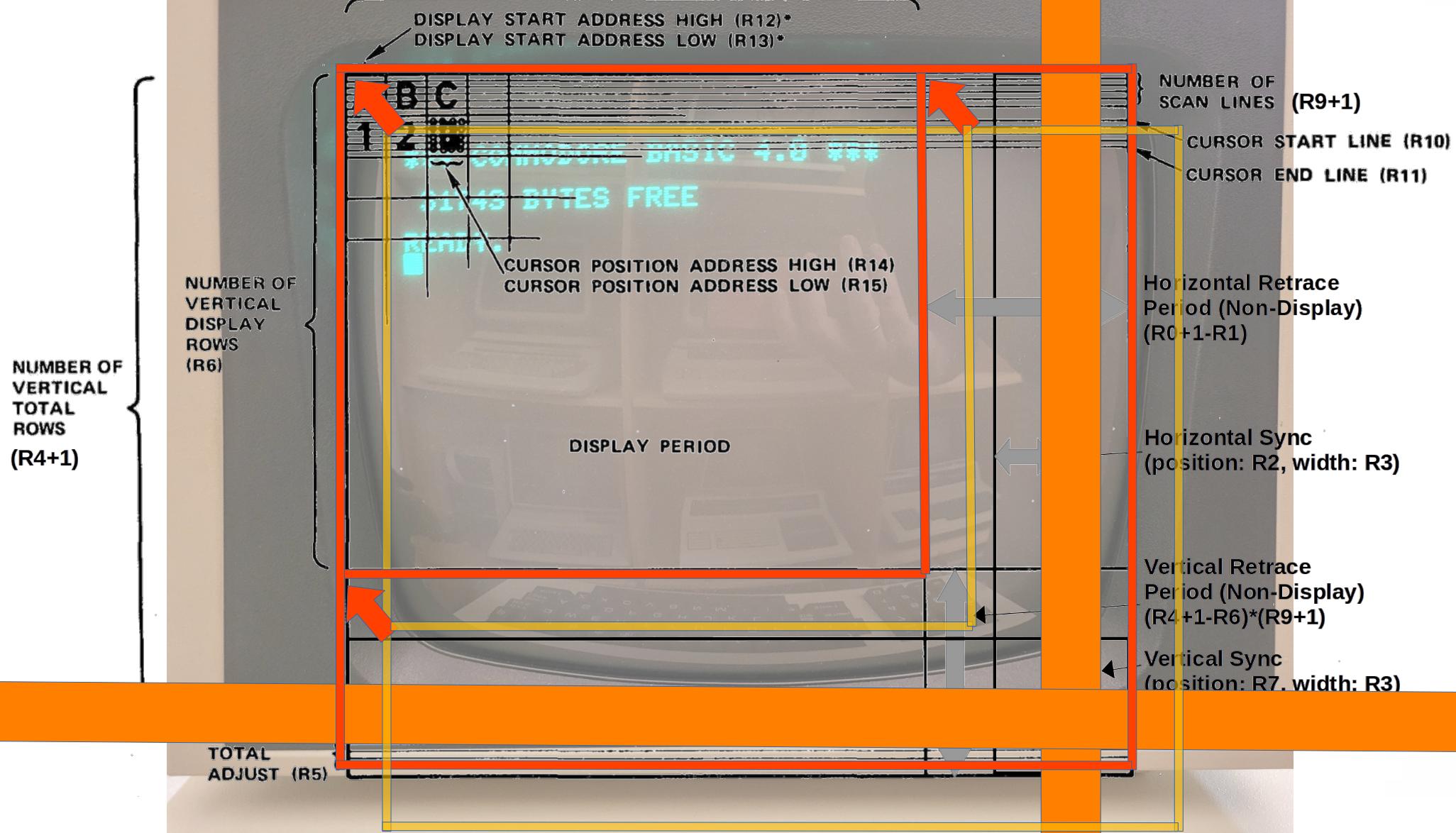
**Note:  
(H+V) SYNC  
Positions are  
Fixed in the  
monitor!**



Source: Rockwell 6545-1 datasheet







# Demos

# How to access CRTC registers?

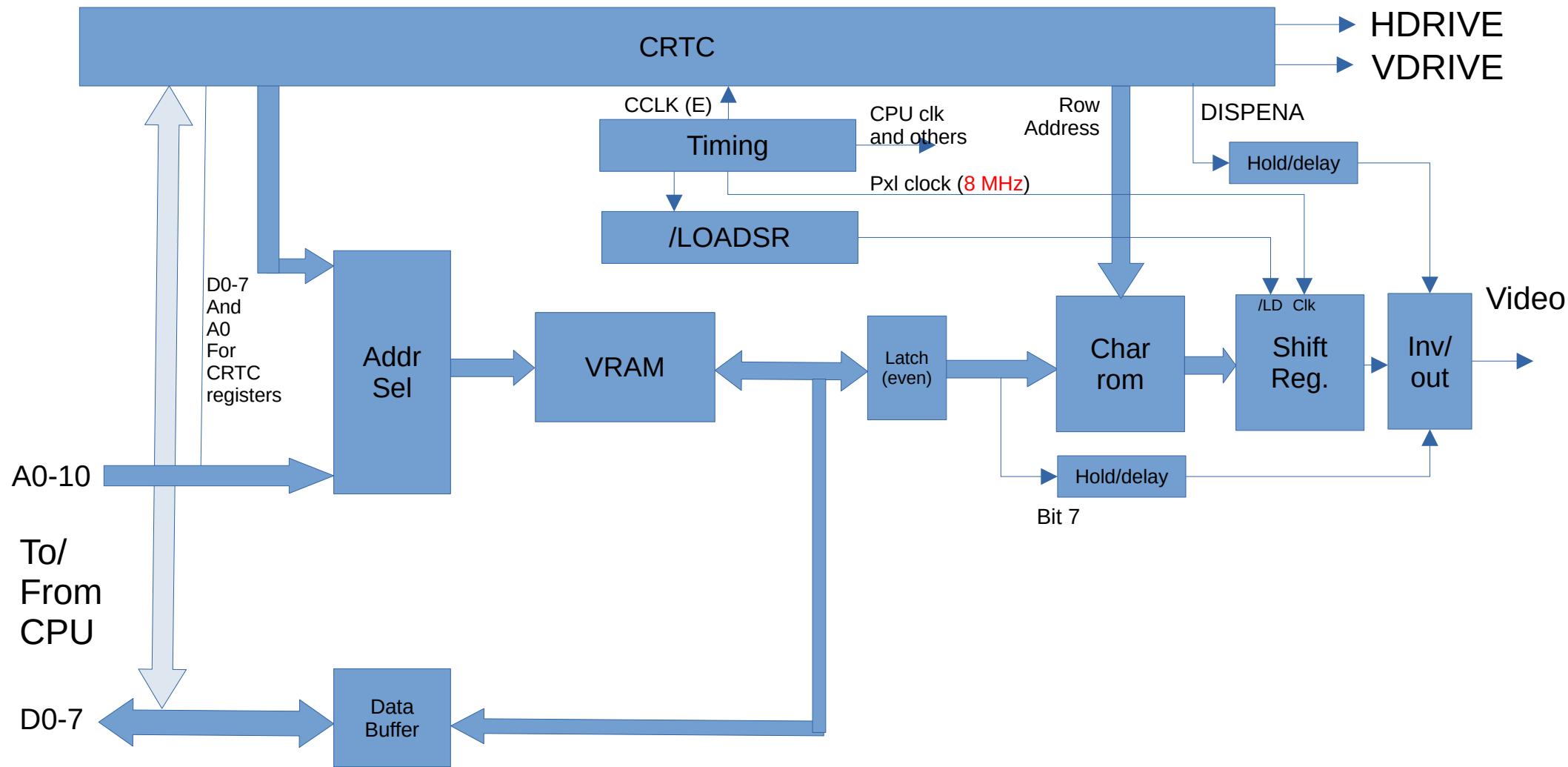
- The CRTC has only two registers:
  - Status (read) / register index (write)
  - Register content (read/write depending on register)
- In the PET these are at:
  - \$E880 = 59520
  - \$E881 = 59521
- To change a register:
  - POKE 59520, <register number>
  - POKE 59521, <new value>
- For example:
  - POKE 59520,1: POKE 59521, 38

# Static tests

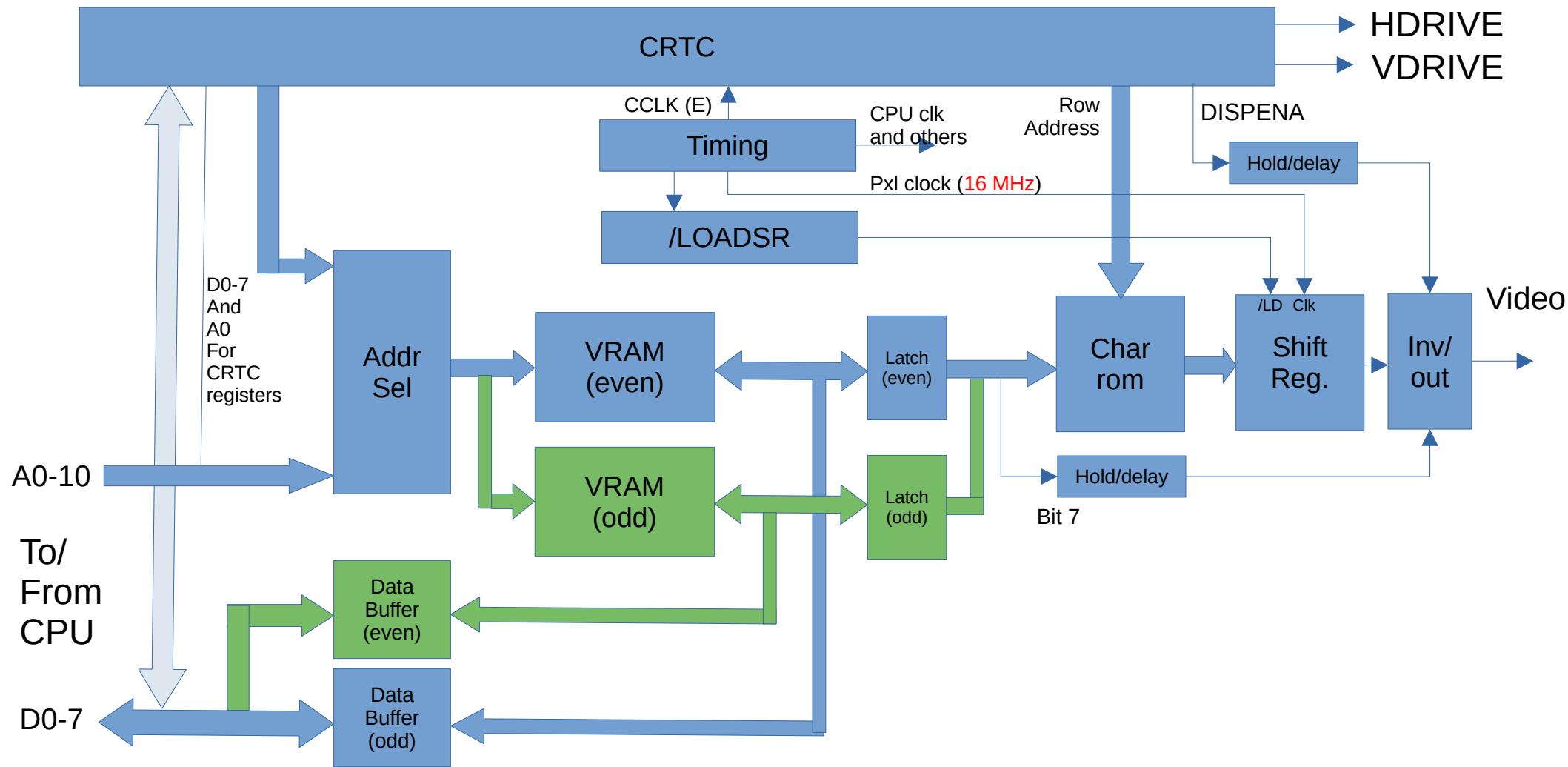
- Hsync / vsync position
  - HSYNC: R2 – default is 41
  - VSYNC: R7 – default is 37
    - 11 is where cursor can be top+bottom
  - Crtc3, crtc4
- Horizontal displayed
  - R1 – default is 40
  - Into retrace, to create „mode 2“
- Character height
  - Small prog to adjust timing (crtc14)
  - 2x8 graphics mode (crtc15)

# Theory of operation

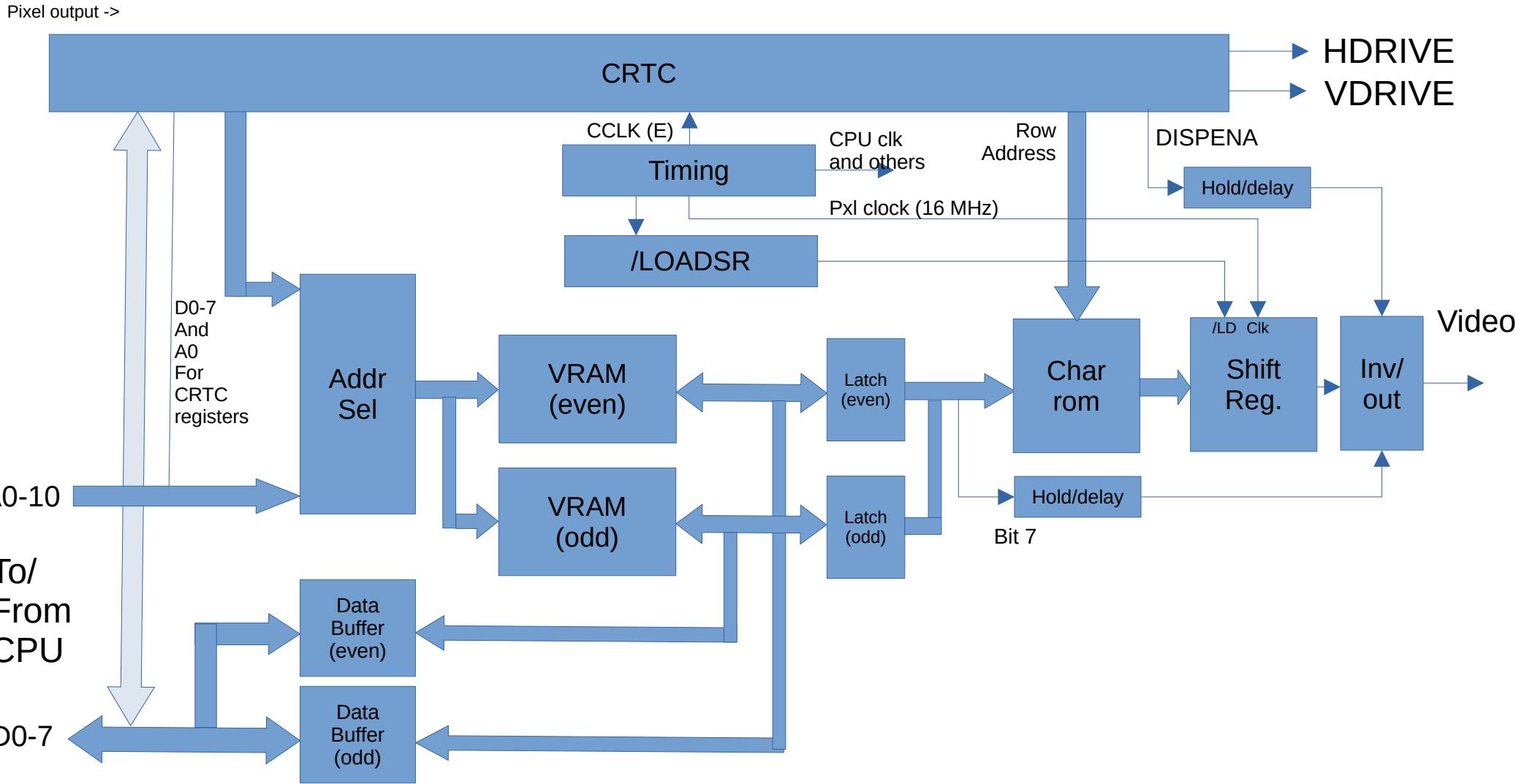
# 40-Column-PET (4032)



# 80-Column-PET (8032)

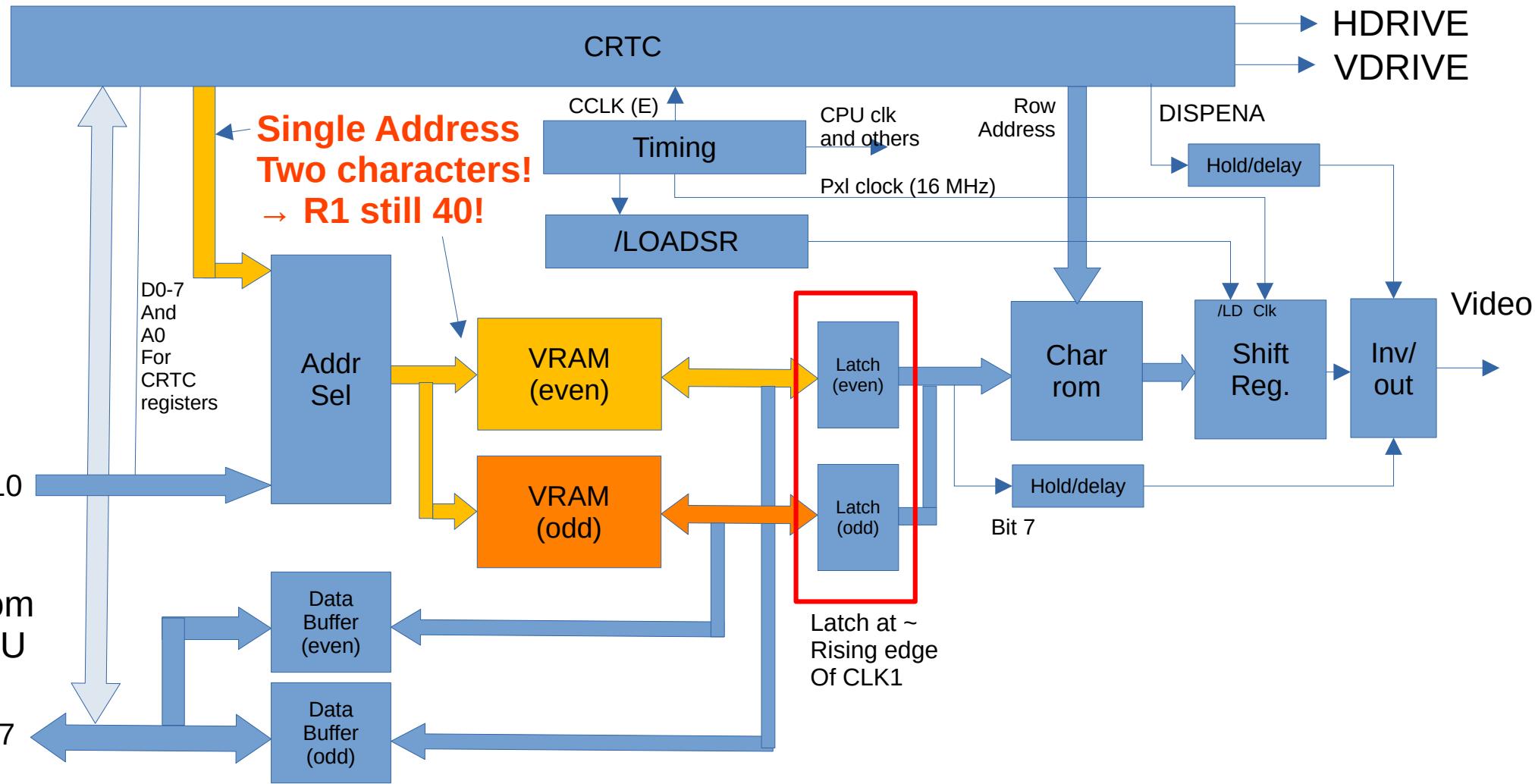


# Timing Overview



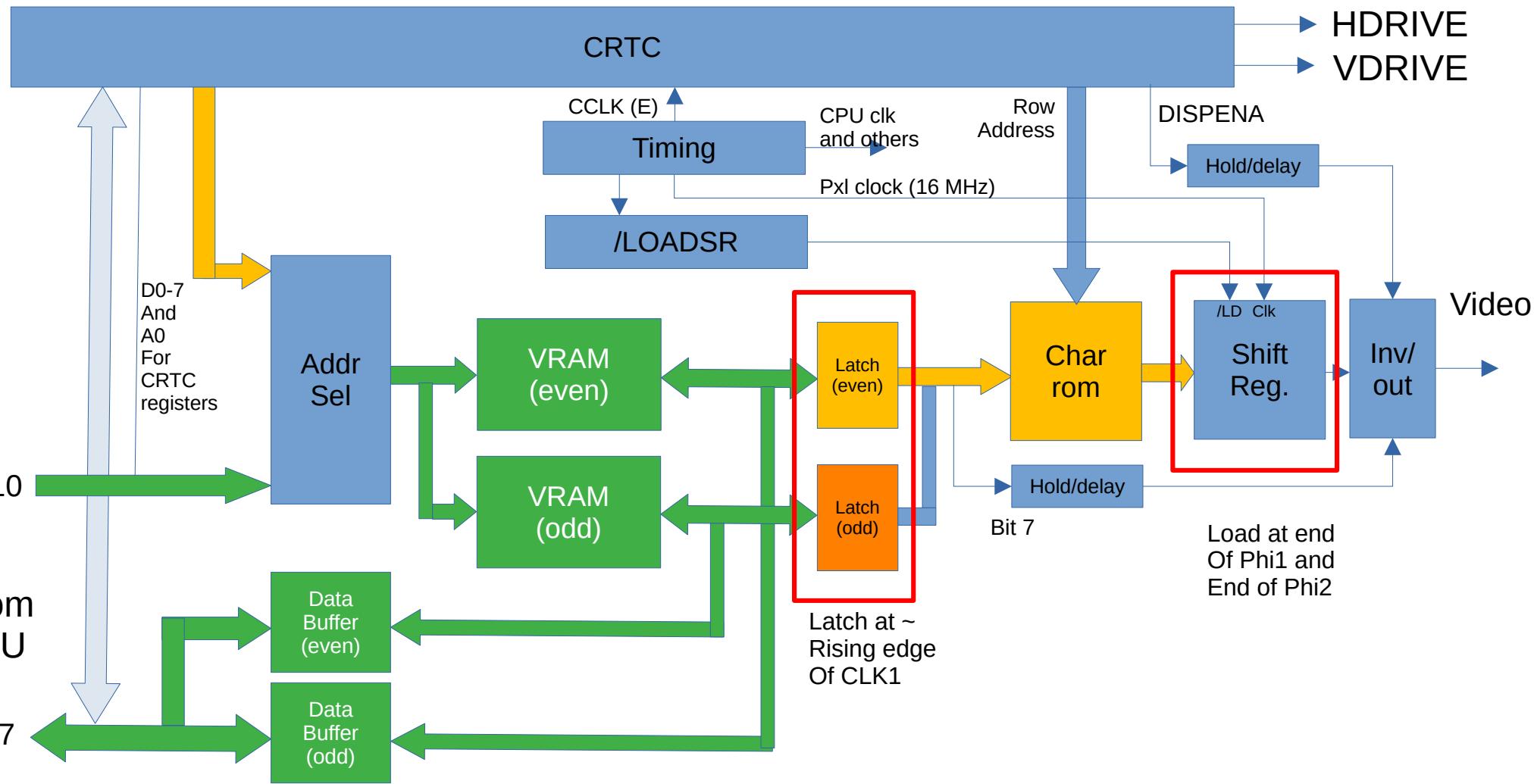


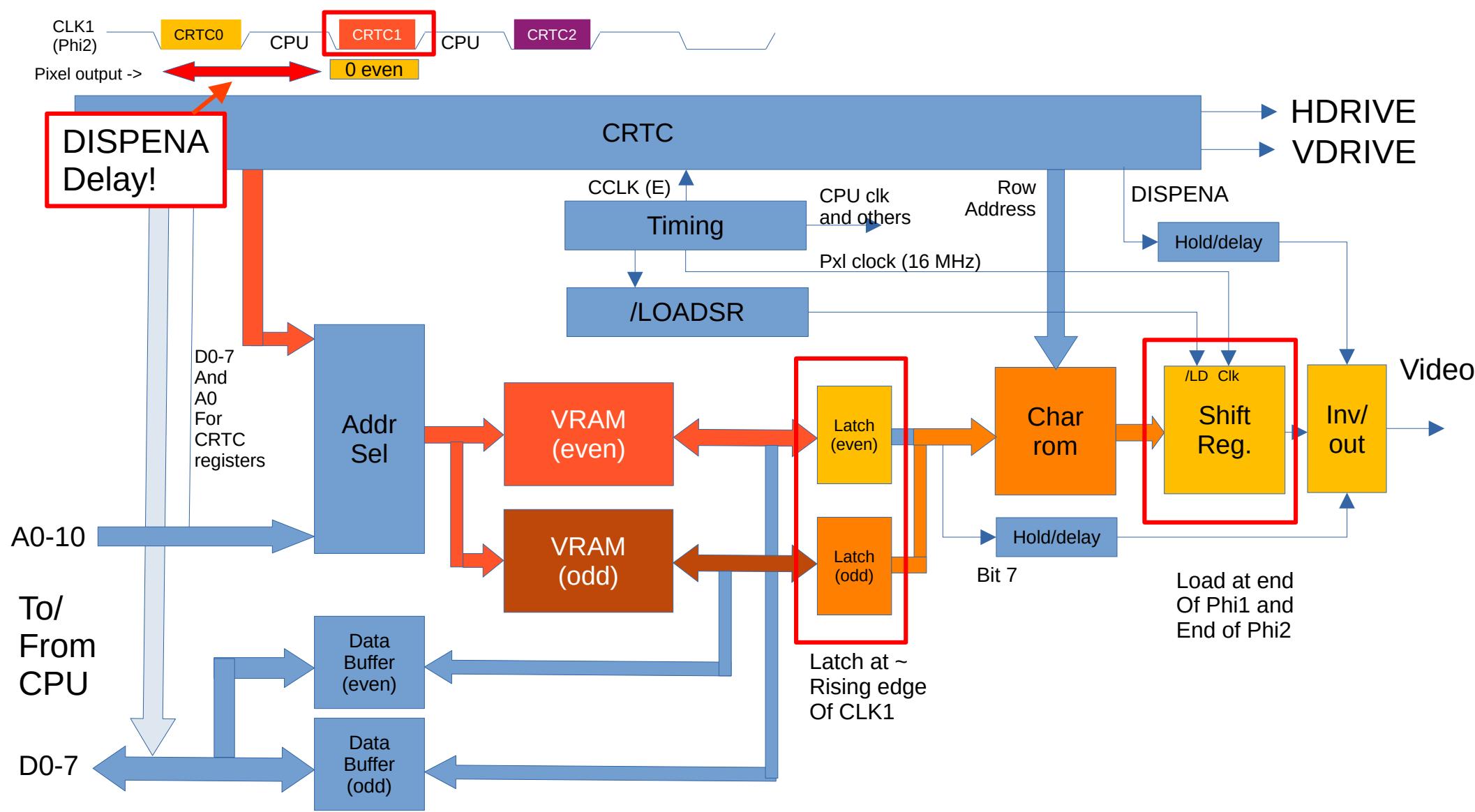
Pixel output ->

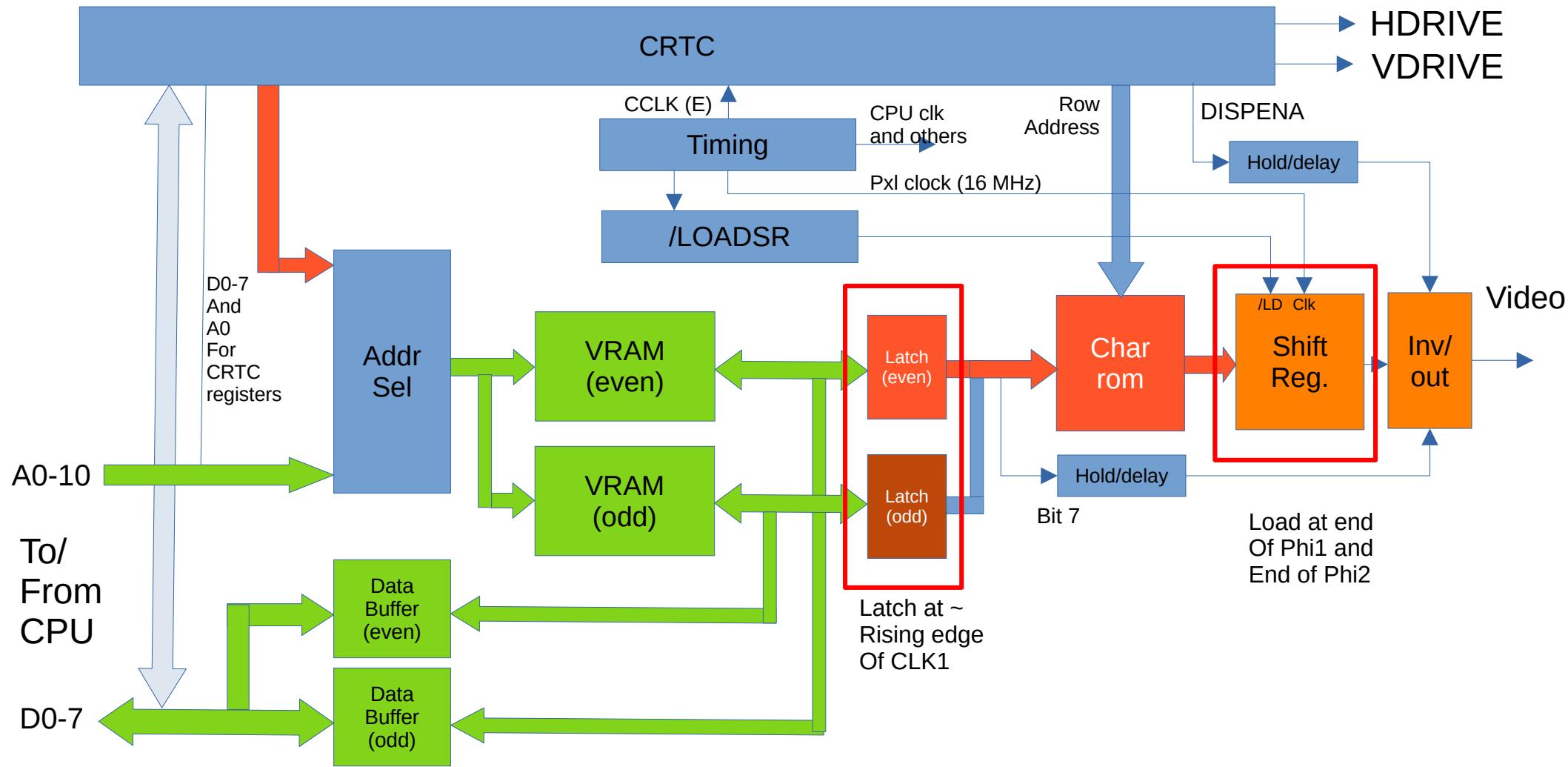
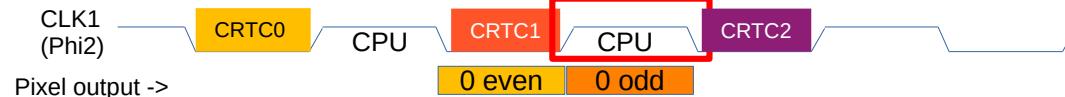


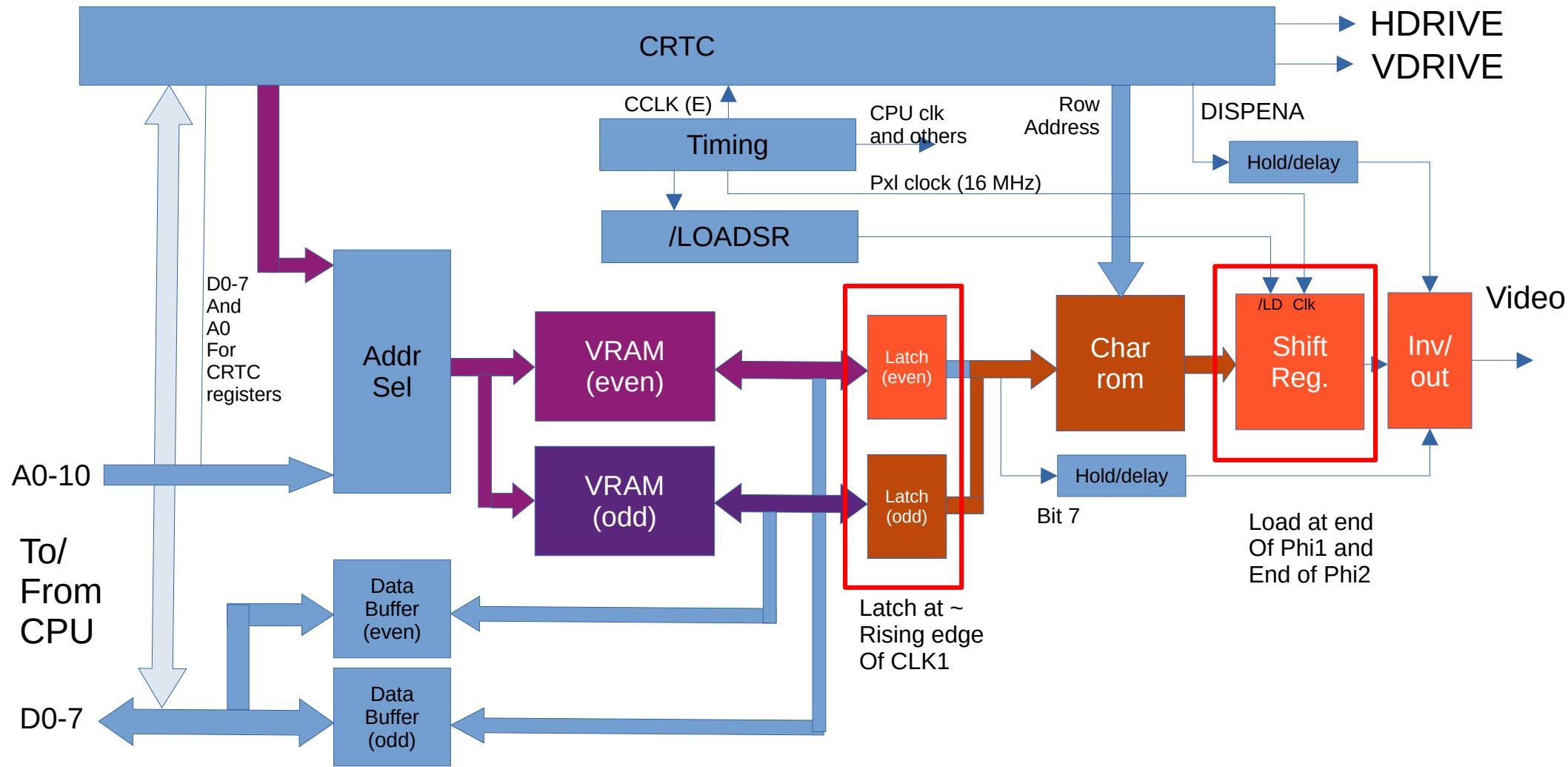
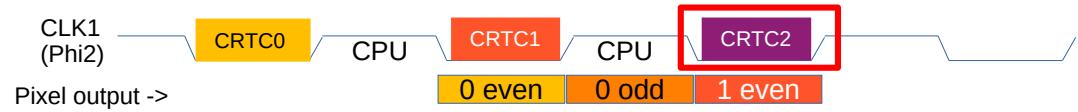


Pixel output ->



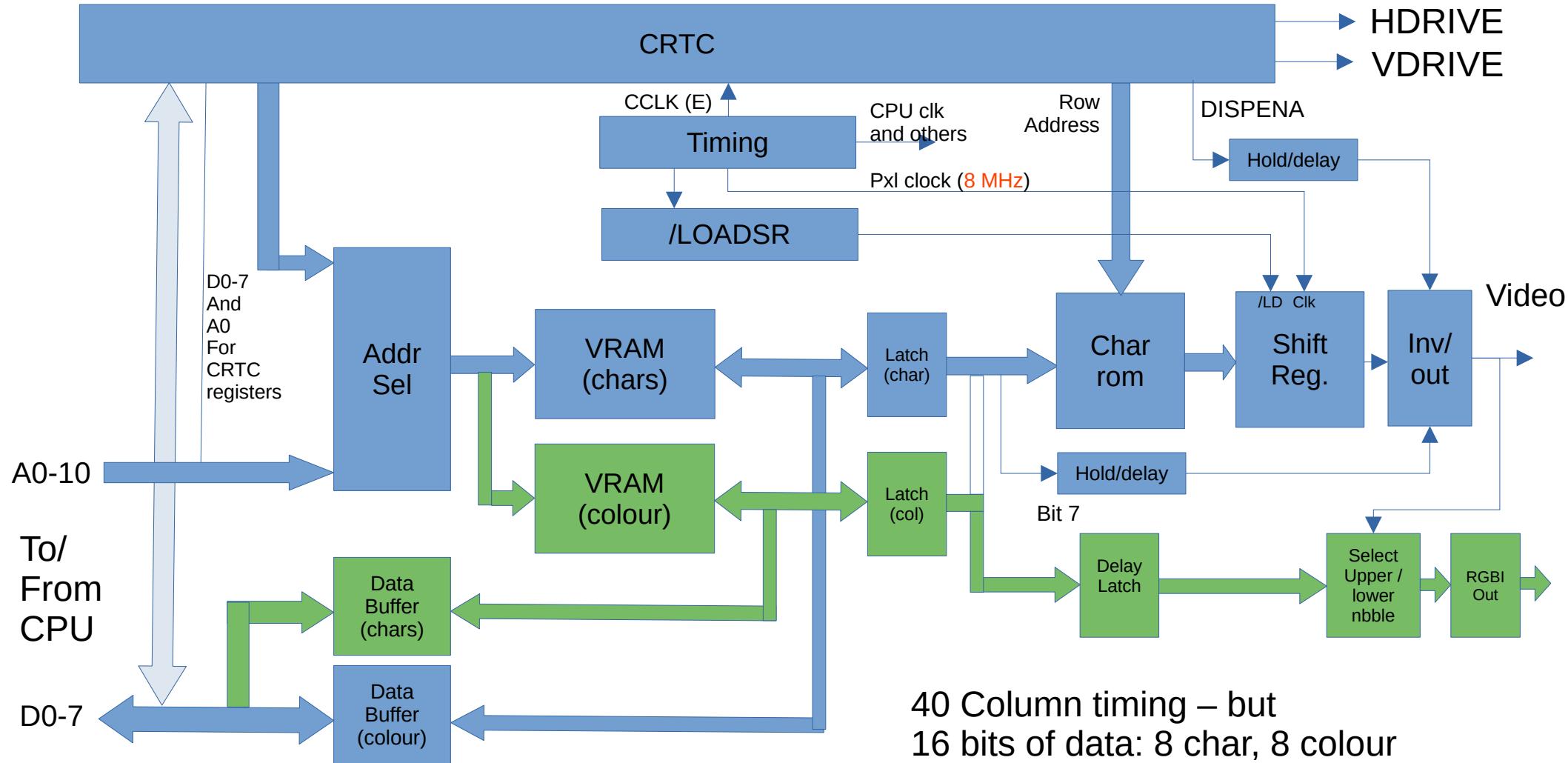






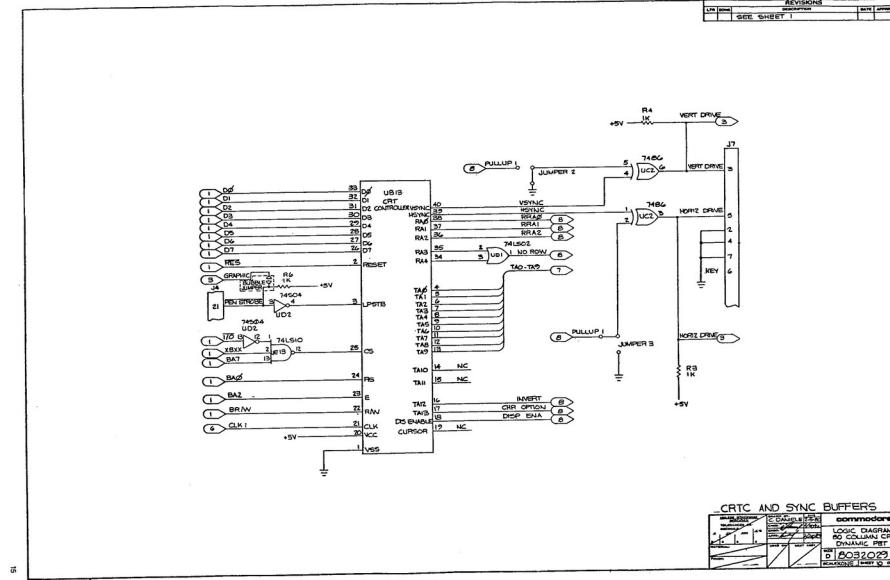
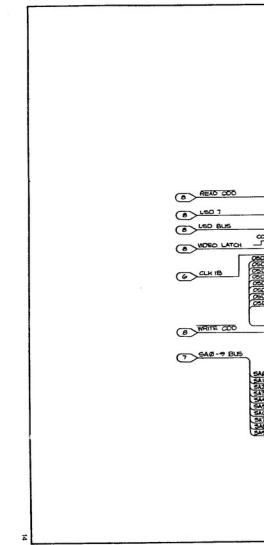
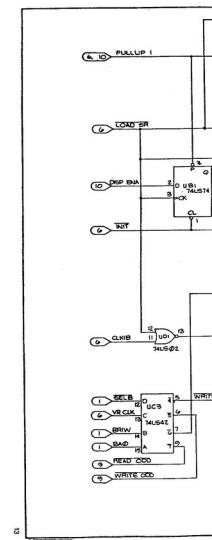
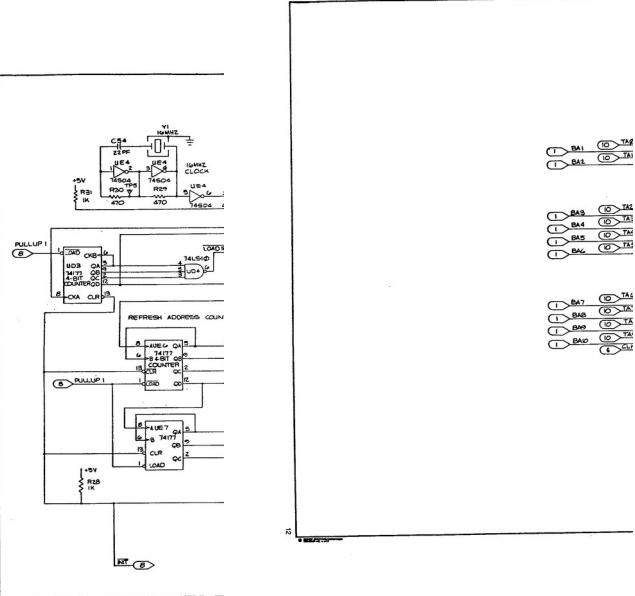
# Colour-PET

# Colour-PET by Steve Gray with improvements by Nils Eilers and Christian Dirks



# Schematics deep dive

# Schematics Deep Dive



## Clock Generation

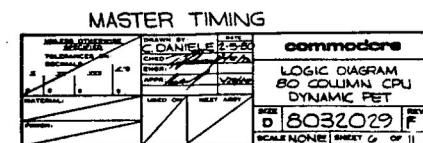
PULLI  
8

# Refresh Address counter

# DRAM Control

一

8



## Clock Generation

PULL  
8

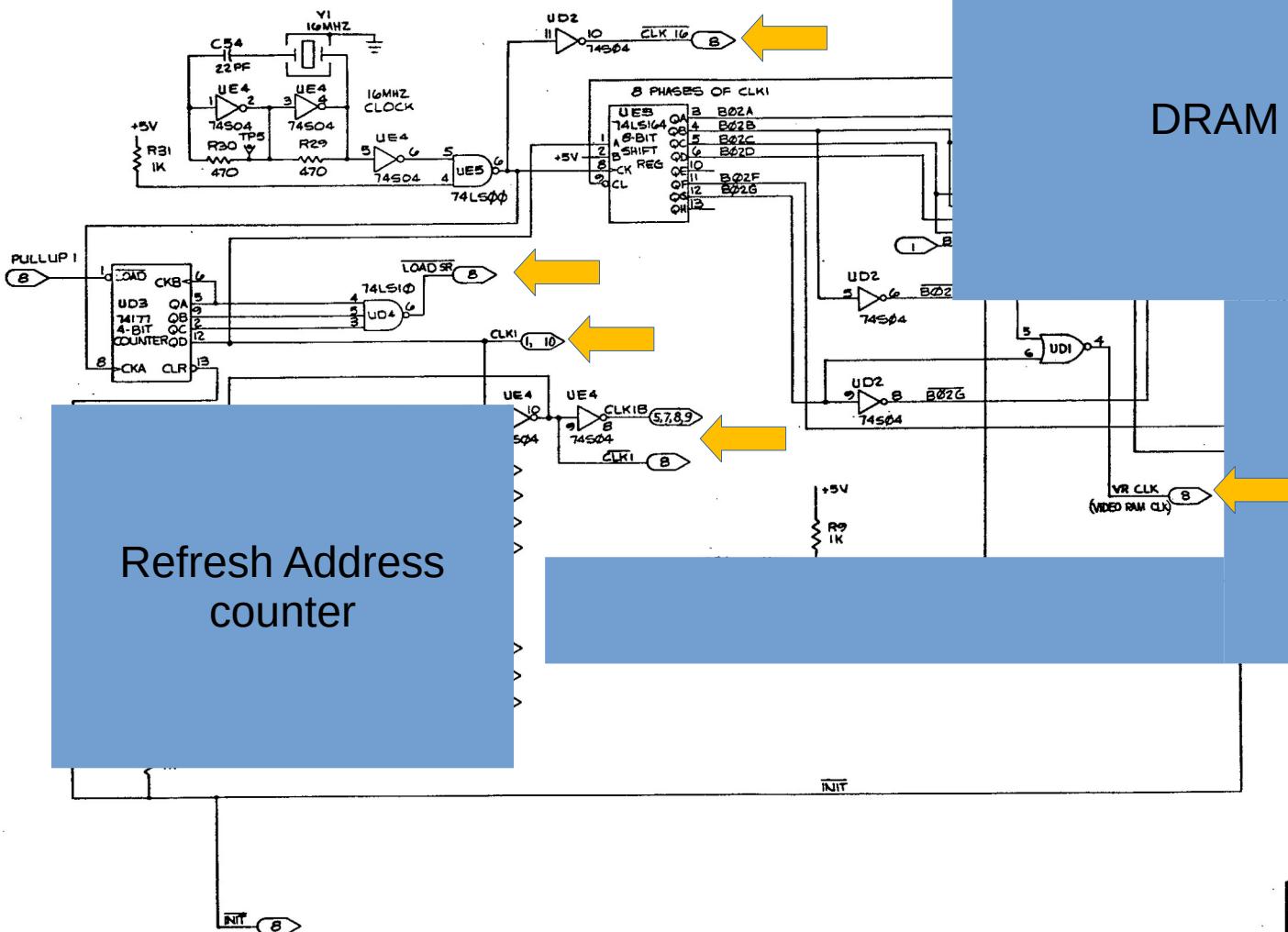
# Refresh Address counter

# DRAM Control

INIT

8

MASTER TIMING			
MASTER ADDRESS REGISTER		DRAWN BY C. DANIELLE	DATE 2-2-80
TELETYPE TELEMECHANIC		commodore	
DATA BUS		LOGIC DIAGRAM 80 COLUMN CPU DYNAMIC PET	
INTERNAL		USED ON	NEXT APPT.
POWER:		SIZE 2029	
		D 80329 F	
		SCALE NONE SHEET G OF 11	



## DRAM Control

Refresh Address  
counter

### MASTER TIMING

MASTER CONTROL	DESIGNED BY	DATE
	C. DANIELLE	2-2-80
TELEGRAMS	CHIPS	PCB
	1000	1000
WATERMARK	VERIFIED	VERIFIED
INITIAL	1	1
FINAL	1	1
REVISION	1	1
MANUFACTURED	1	1
TESTED	1	1
PACKAGED	1	1
SHIPPED	1	1

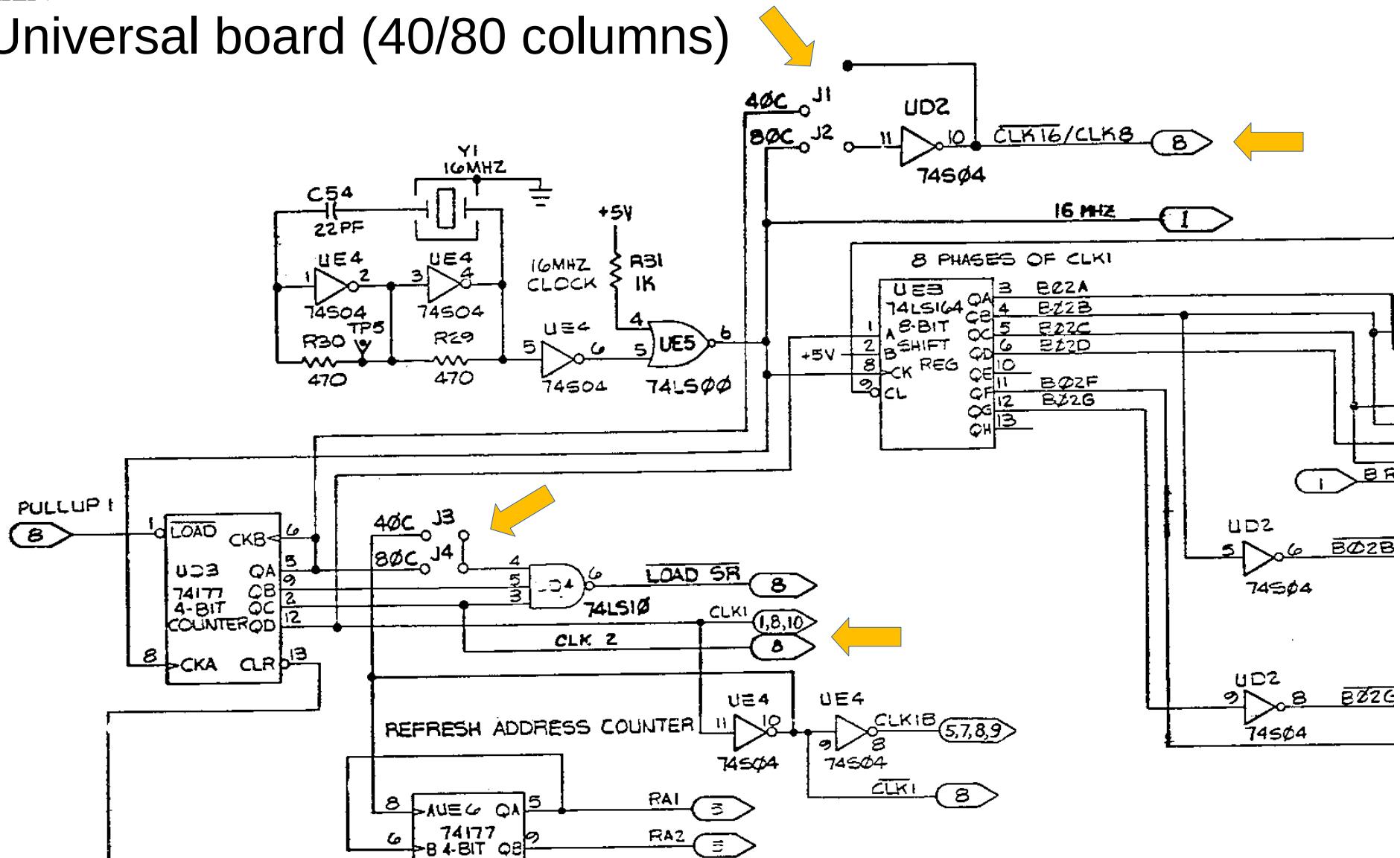
commodore

LOGIC DIAGRAM  
80 COLUMN CPU  
DYNAMIC PET

REV. D 8032029

SCALE NONE SHEET 6 OF 11

# Universal board (40/80 columns)



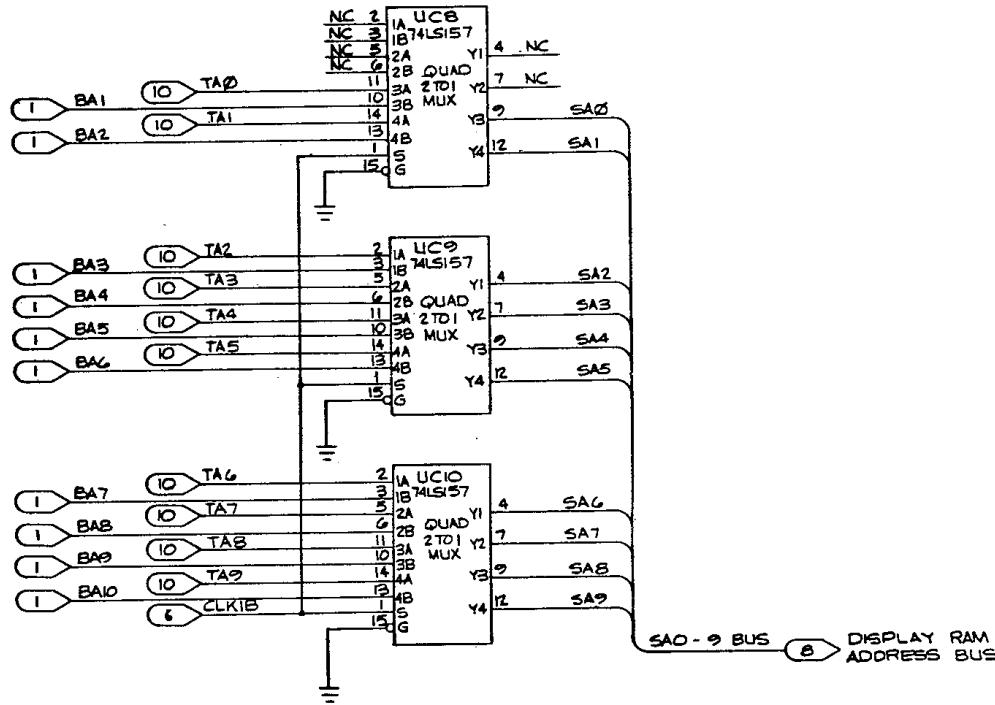
# Video RAM Address Selector

		REVISIONS	DATE	APPROVED
LTR	ZONE	DESCRIPTION		
		SEE SHEET 1		

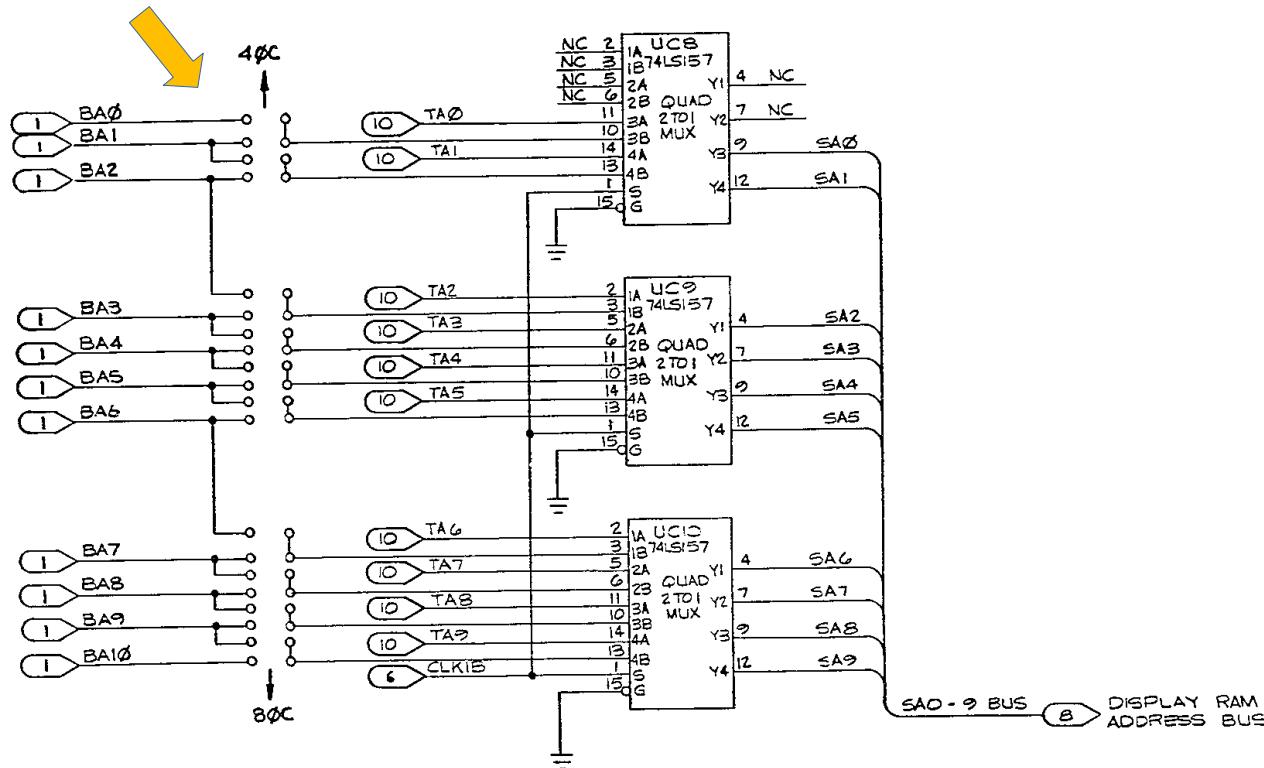
DISPLAY ADDRESS MUX			
MAILING ADDRESS COMMODORE INC. 1050 NORTH BROADWAY SCHAUMBURG, IL 60193		DRAWN BY: C. DANIELLE E. 2/26 REV. DATE: 3/26 DESIGNED BY: C. DANIELLE APPROVED BY: C. DANIELLE CHECKED BY: C. DANIELLE DATE: 3/26/83	
		<b>commodore</b> LOGIC DIAGRAM 80 COLUMN CPU DYNAMIC PET	
MATERIALS 		USED ON 	
		SHEET SIZE: 8032029 10V SCALE: NONE SHEET 7 OF 11	

## Video RAM Address Selector

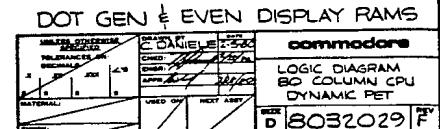
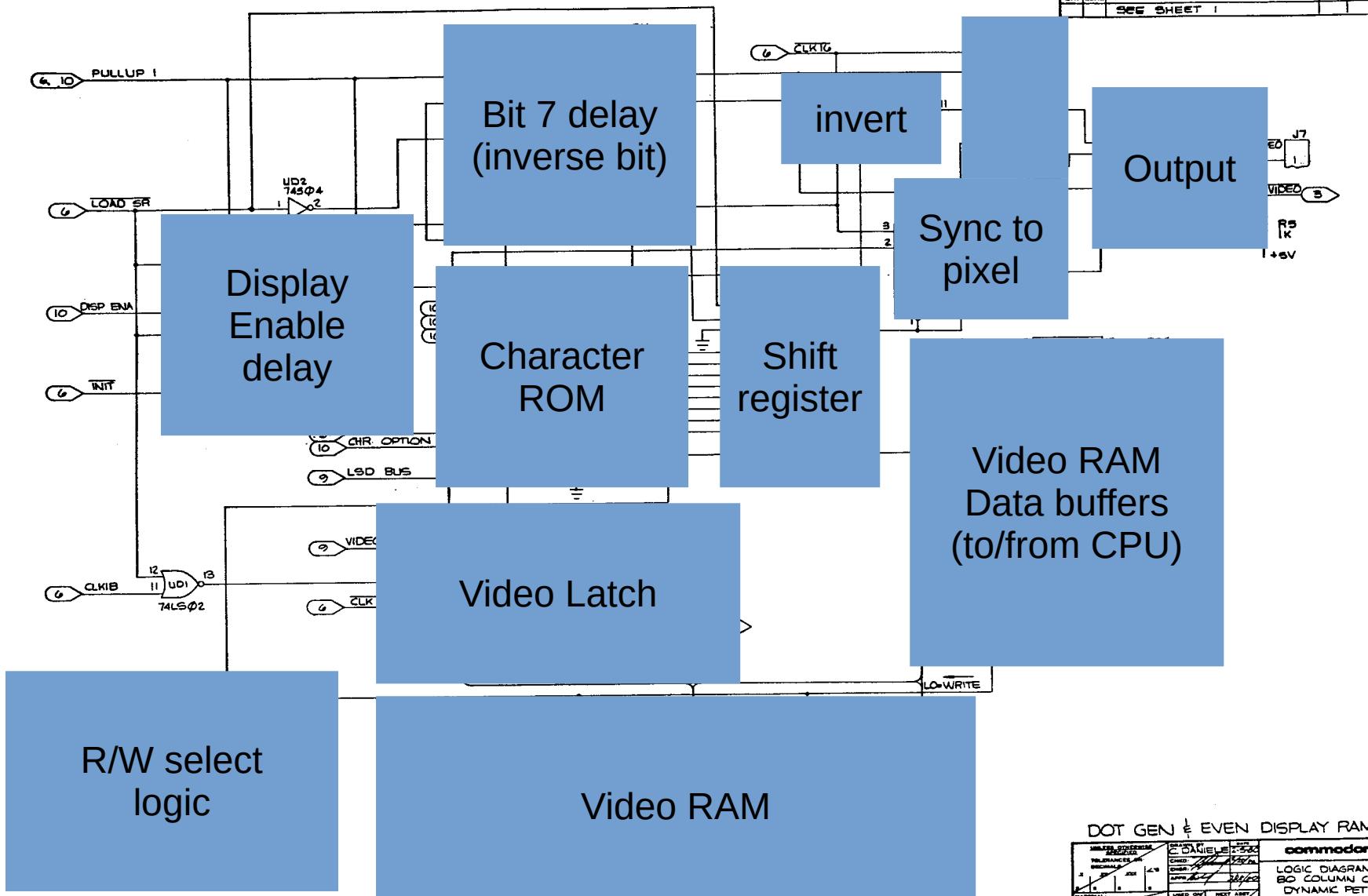
REVISIONS			
LTR	ZONE	DESCRIPTION	DATE
		SEE SHEET 1	

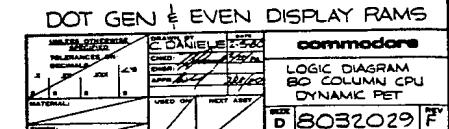
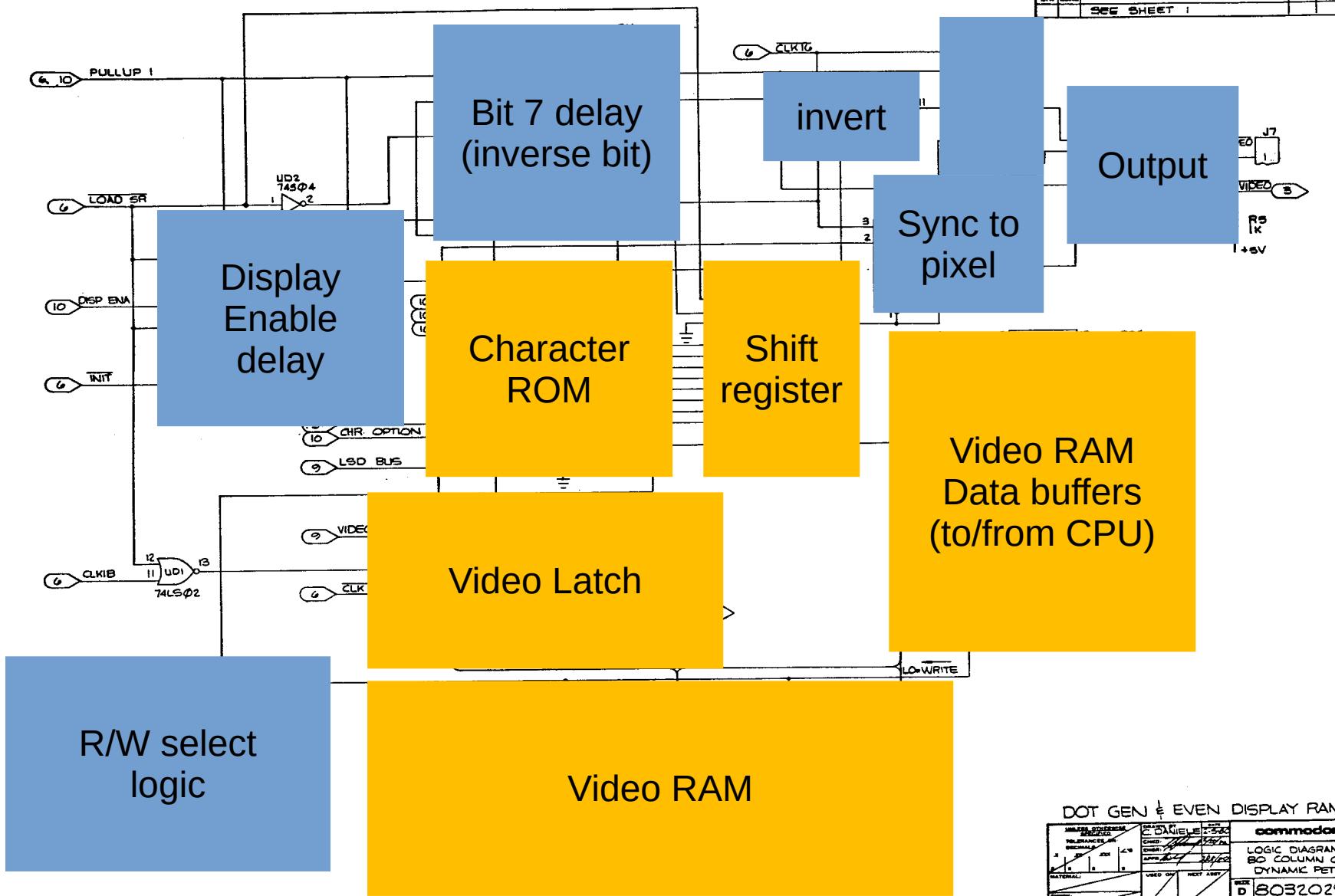


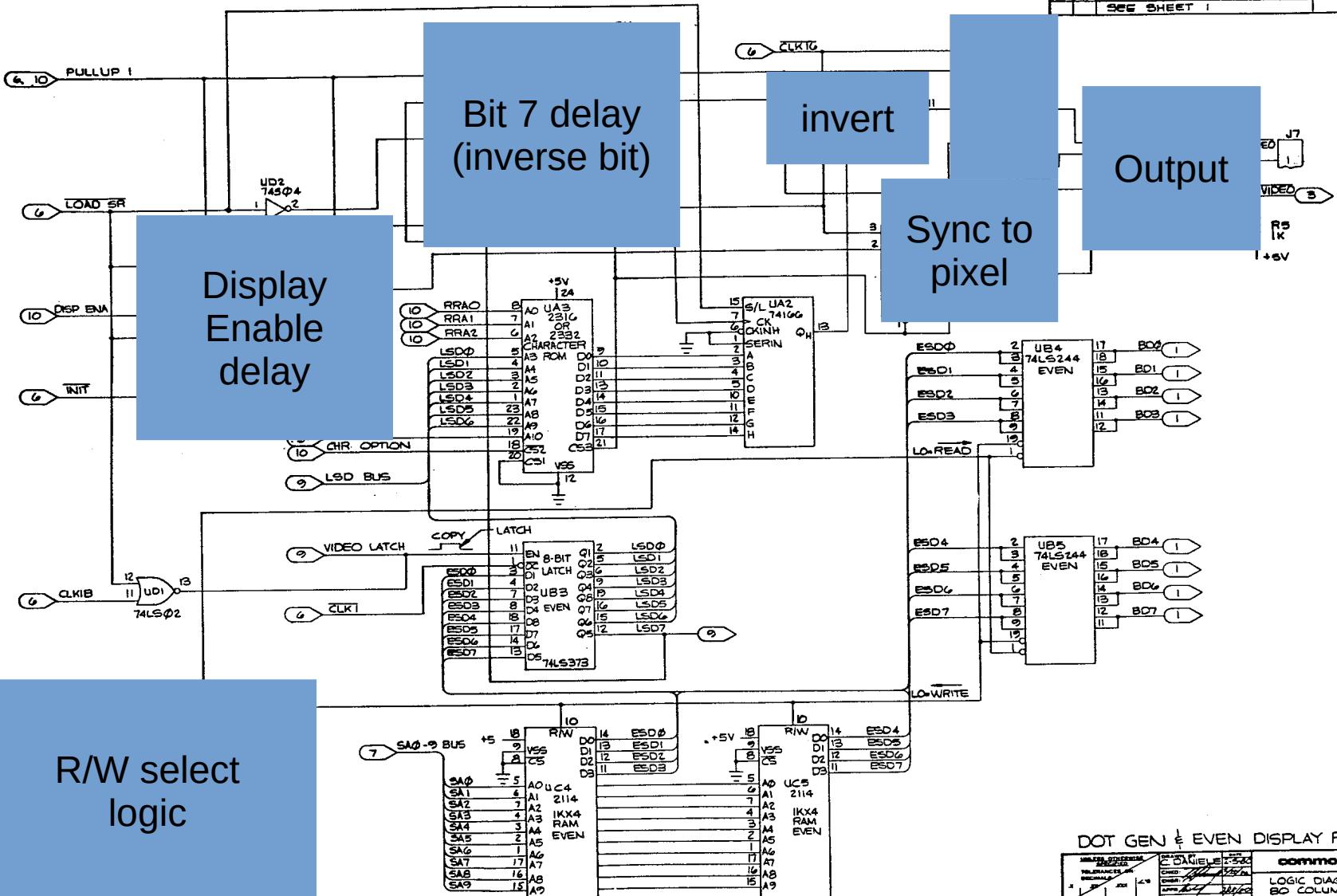
# Universal board (40/80 columns)

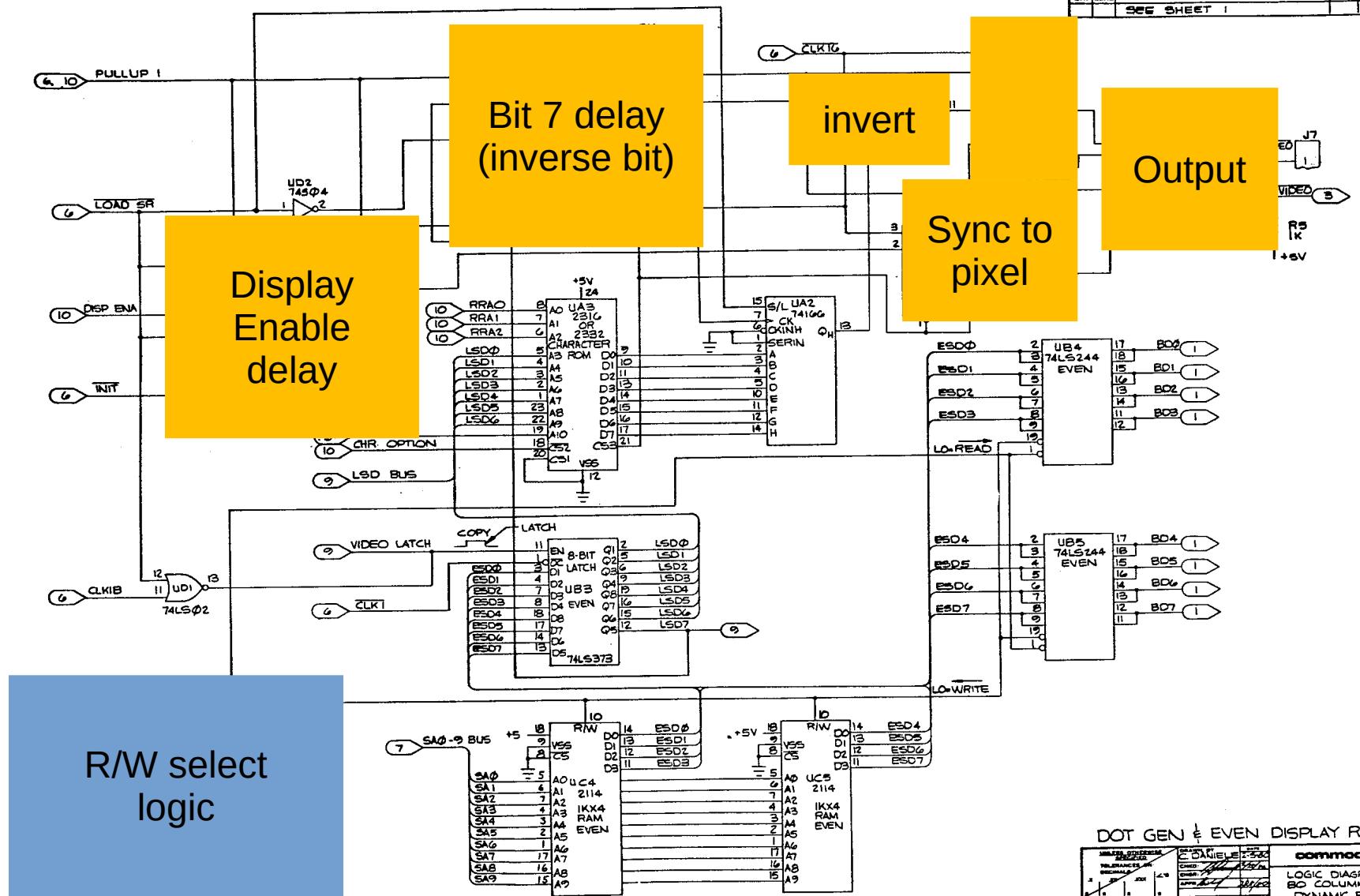


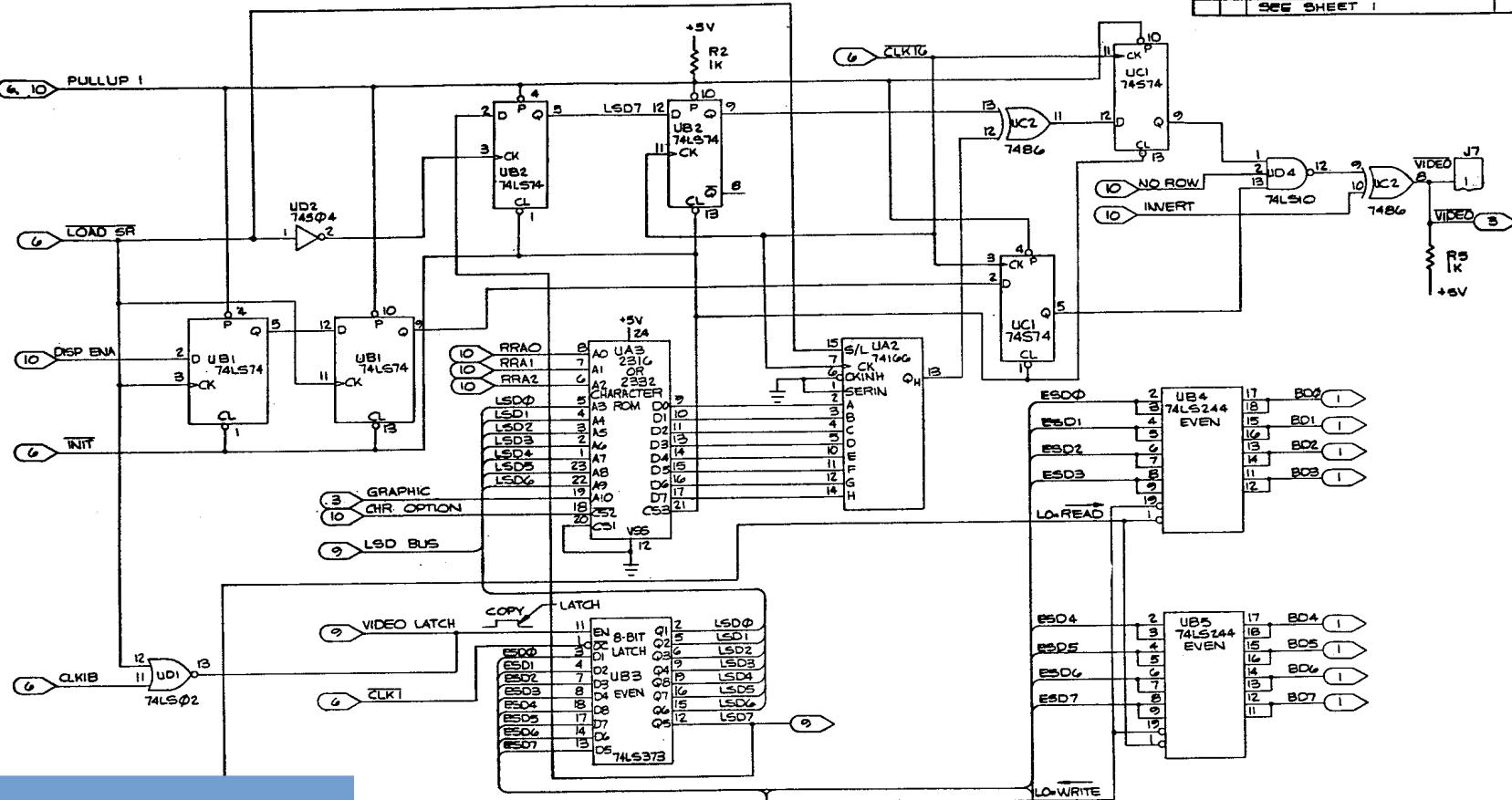
DISPLAY ADDRESS



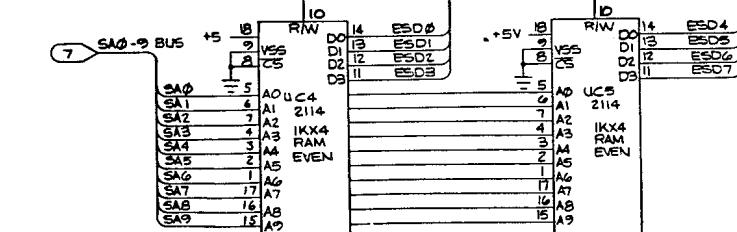


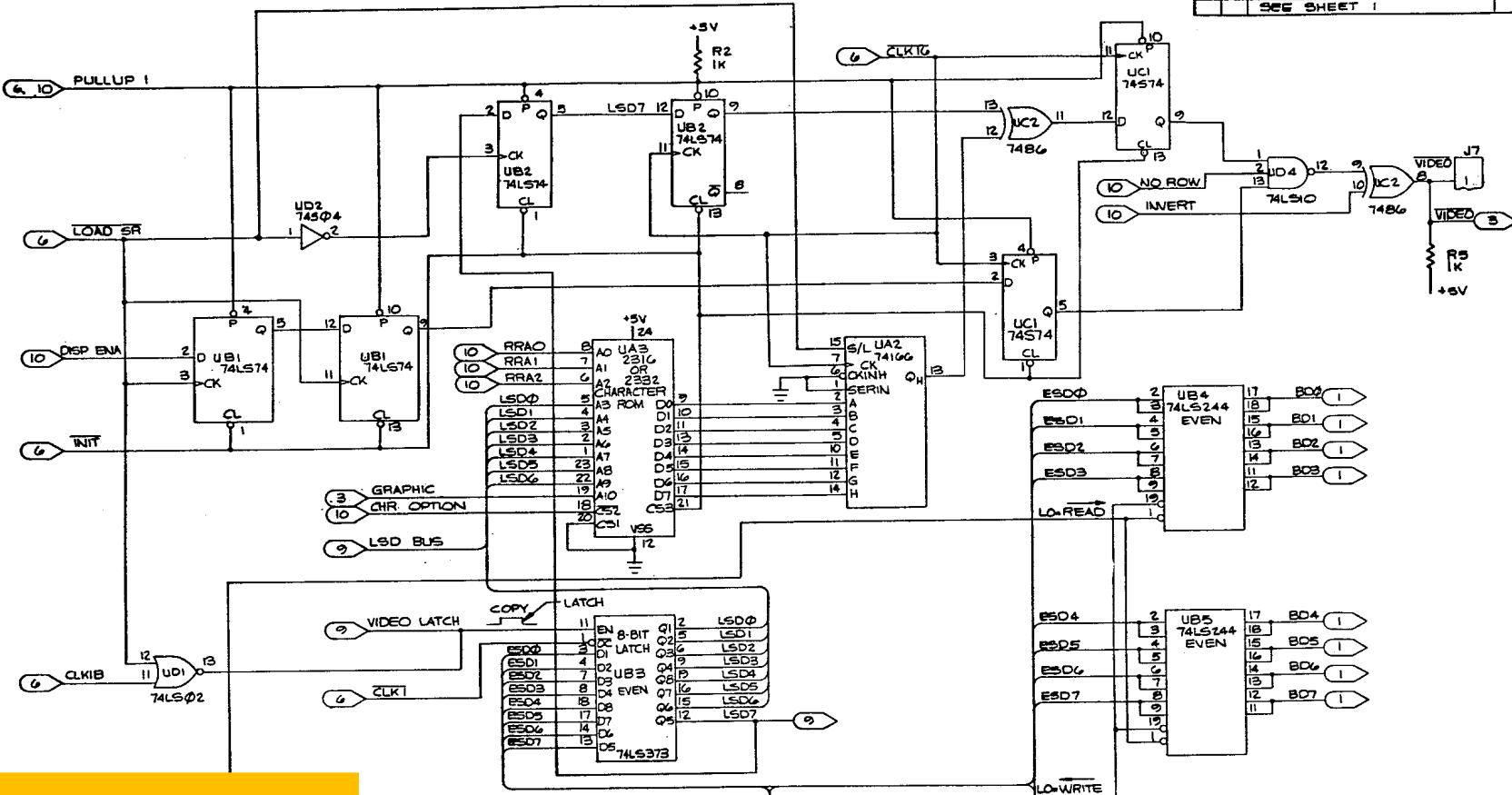




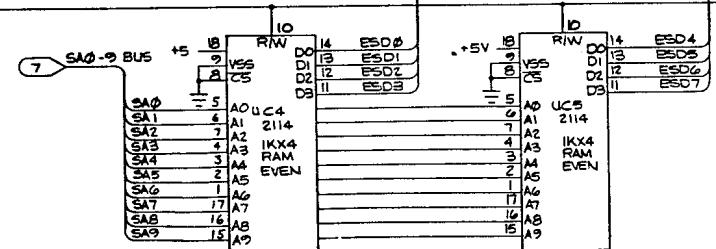


R/W select logic

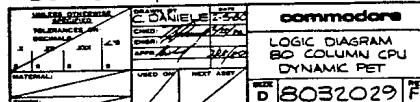


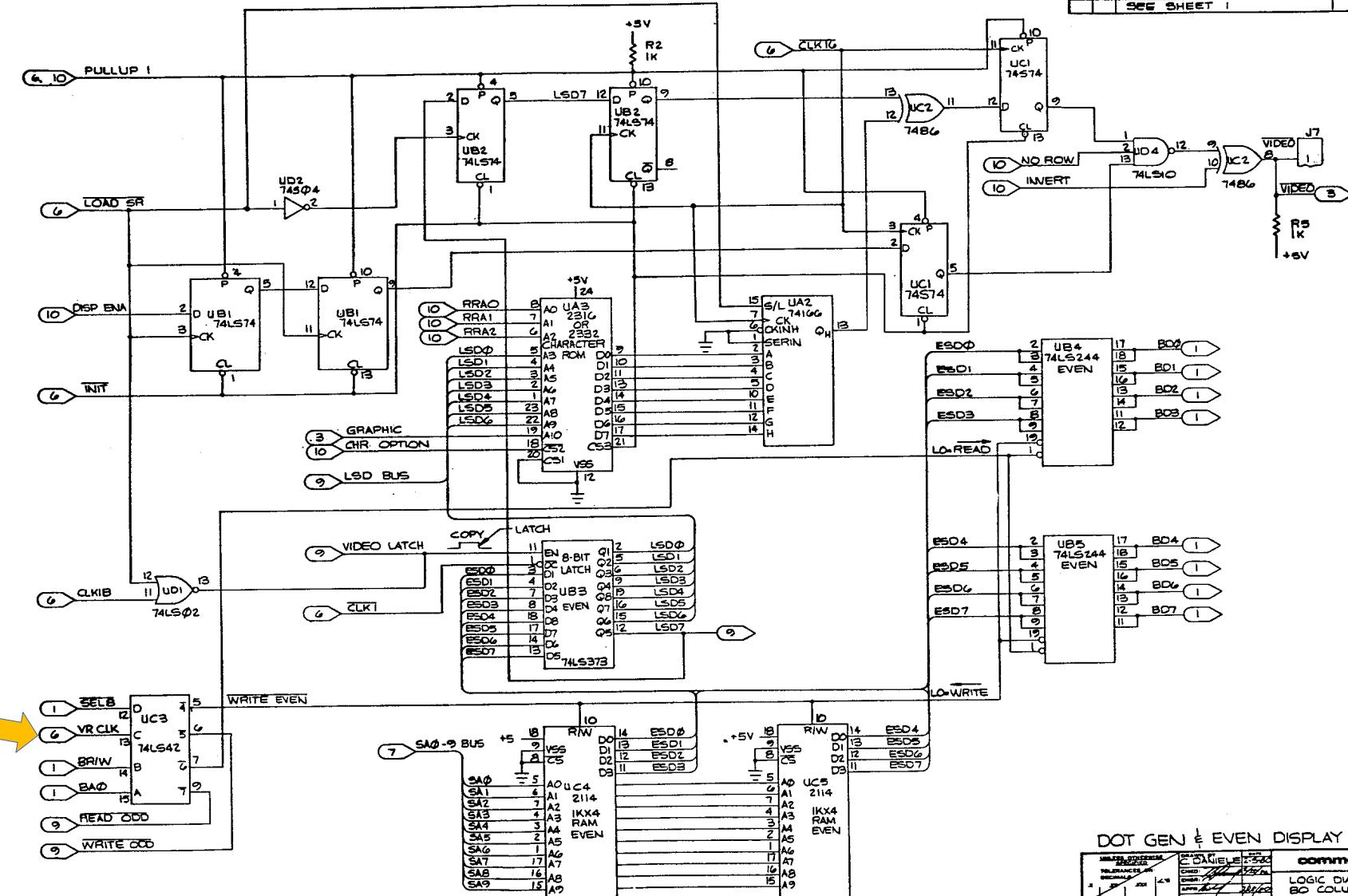


# R/W select logic

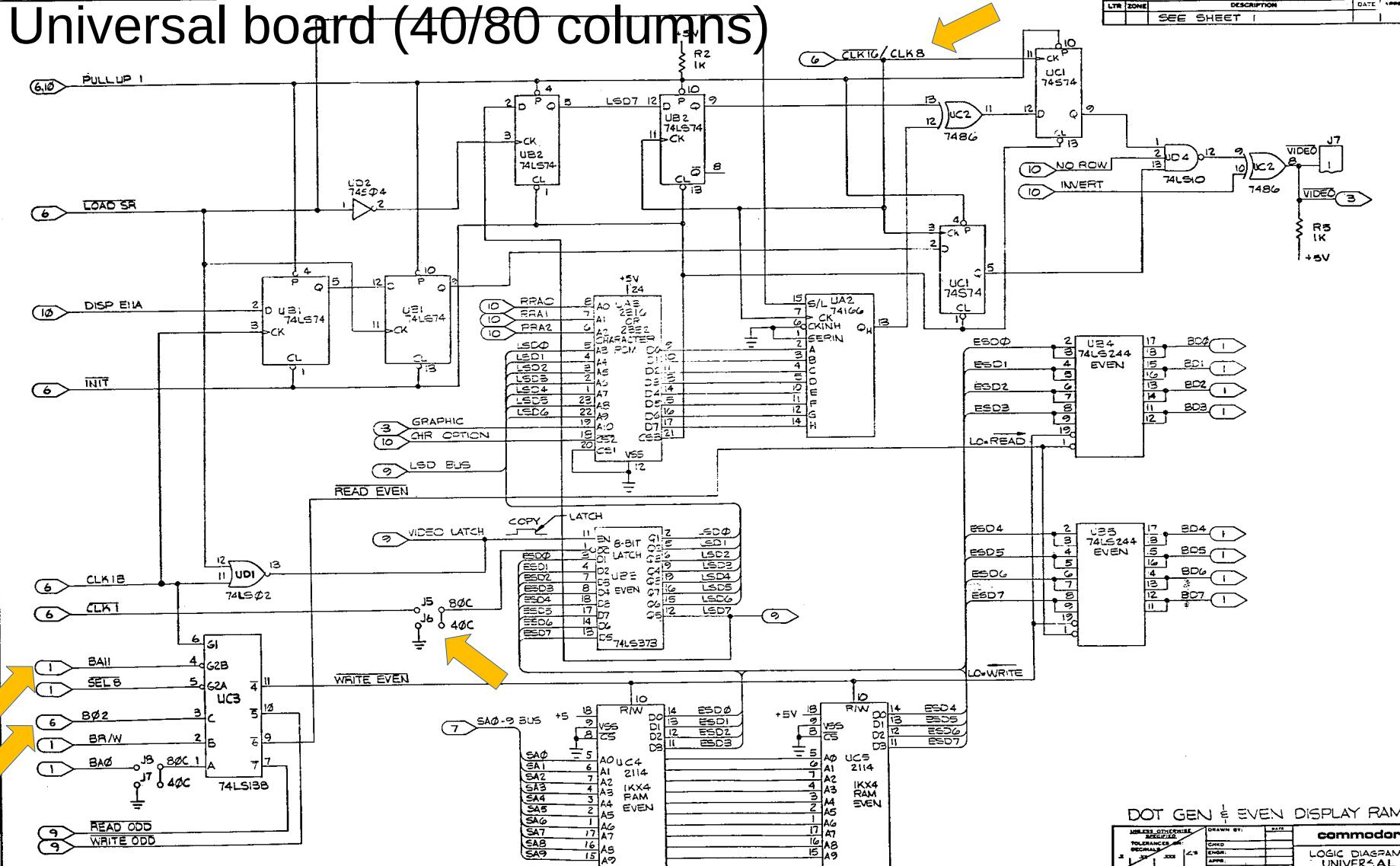


## DOT GEN & EVEN DISPLAY RAMS

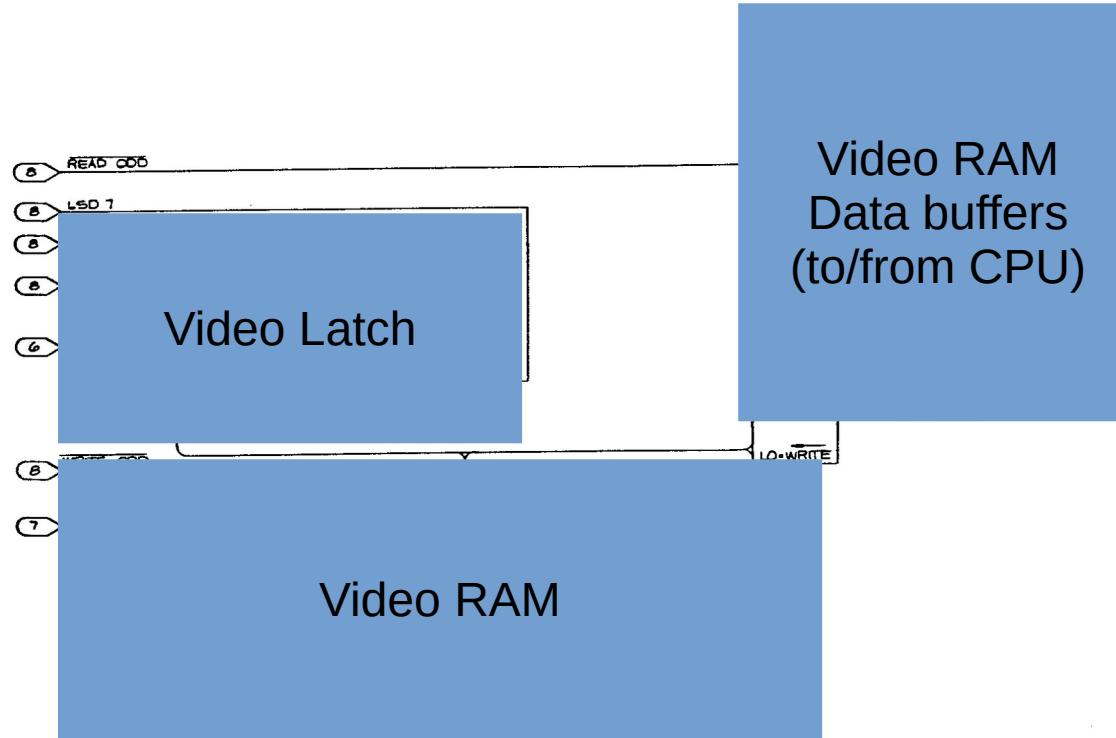




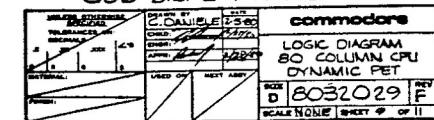
# Universal board (40/80 columns)



## 80 Column board & Universal board (80 columns only)

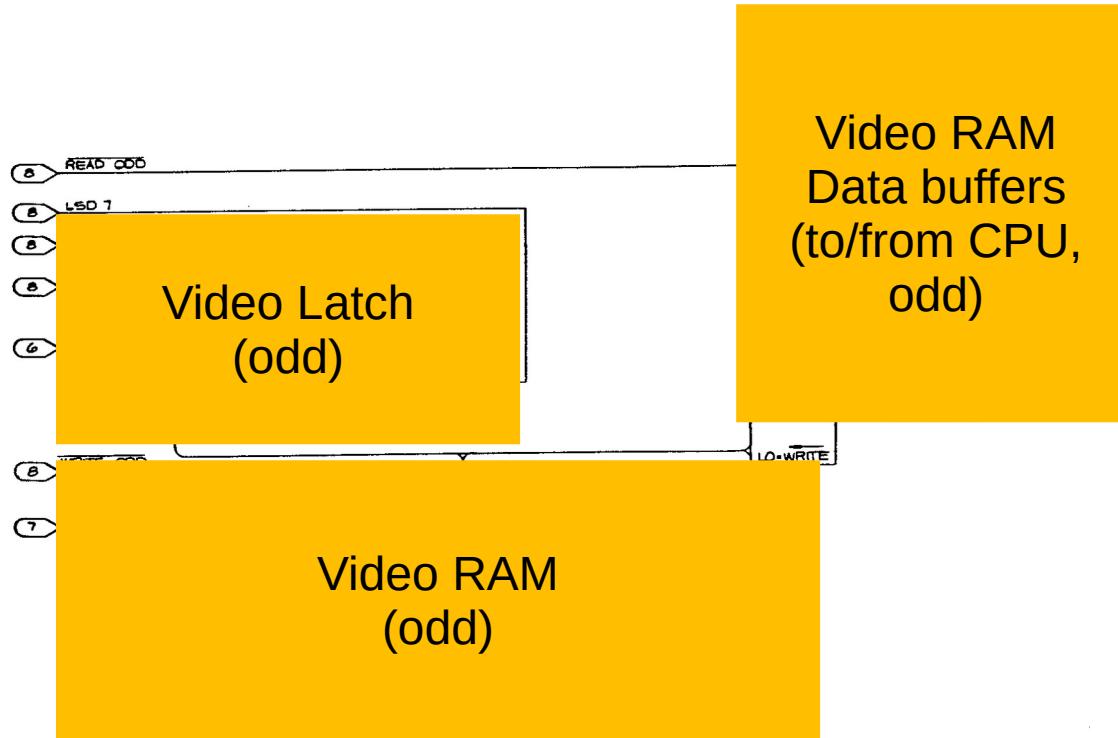


## ODD DISPLAY RAMS

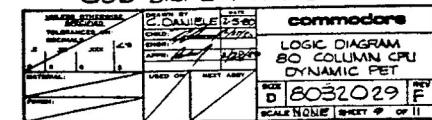


# 80 Column board & Universal board (80 columns only)

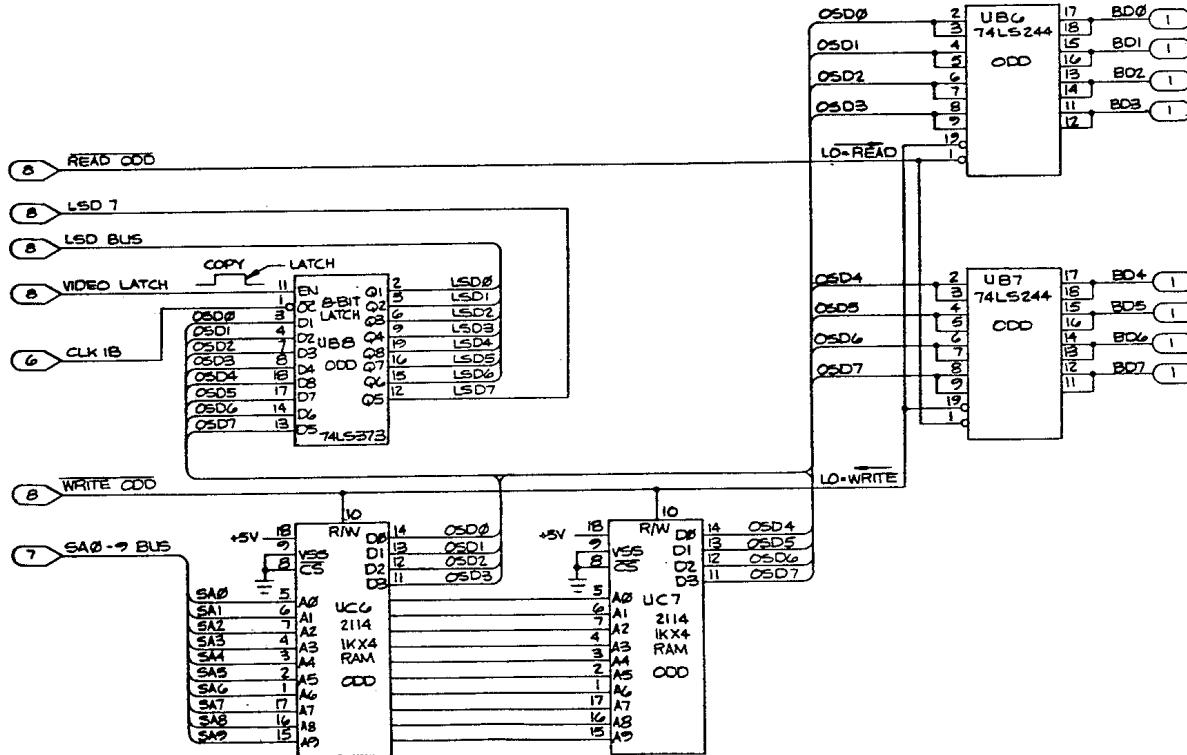
LTH	DOMC	DESCRIPTION	DATE	APPROVED
SEE SHEET 1				



ODD DISPLAY RAMS

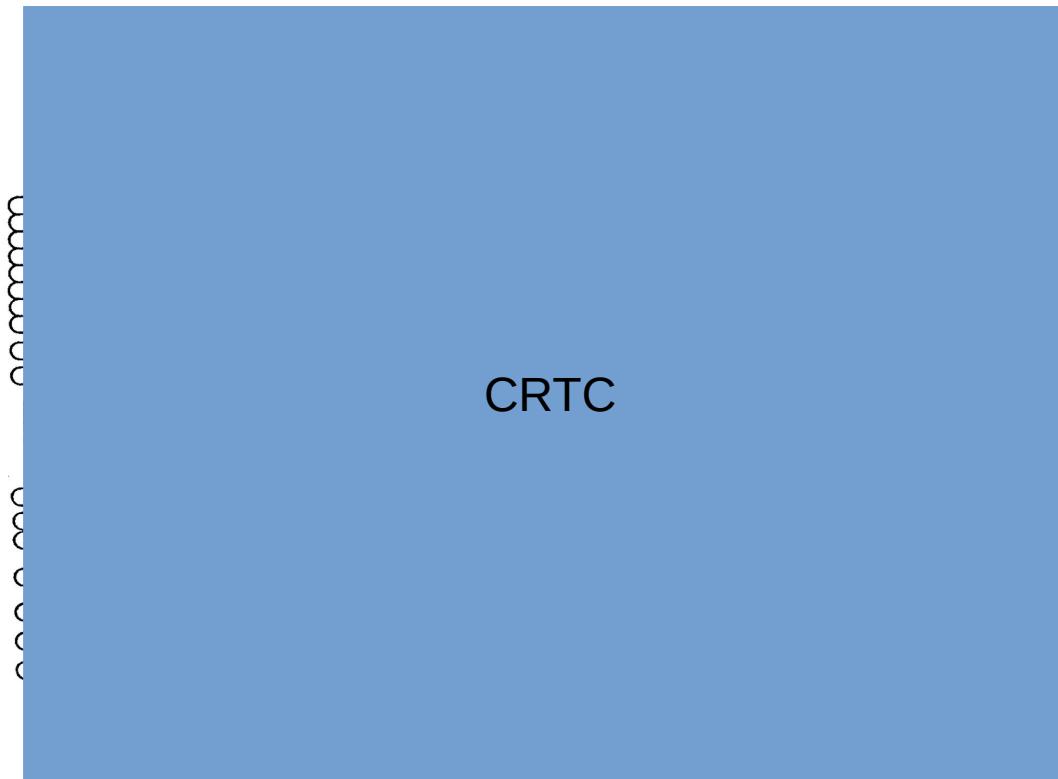


# 80 Column board & Universal board (80 columns only)



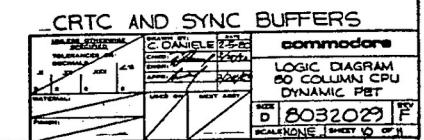
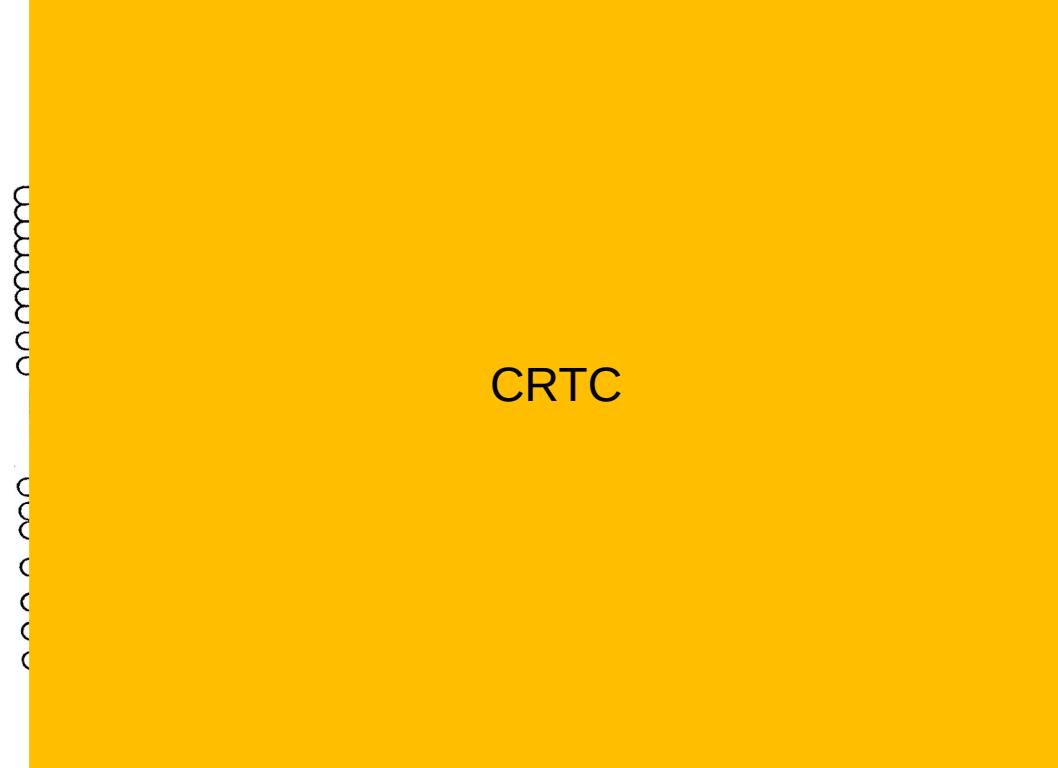
DRAWN BY		DATE
C. DANIELLE		2-5-80
TITLE		UNBALANCED
DESCRIPTION		LOGIC DIAGRAM
APPROVED		2-5-80
SIGNED		COMMODORE
INITIALS		LOGIC DIAGRAM
		80 COLUMN CPU
		DYNAMIC PET
VIA FAX	NEXT AMT	

## 80 Column board & Universal board (40/80 columns)

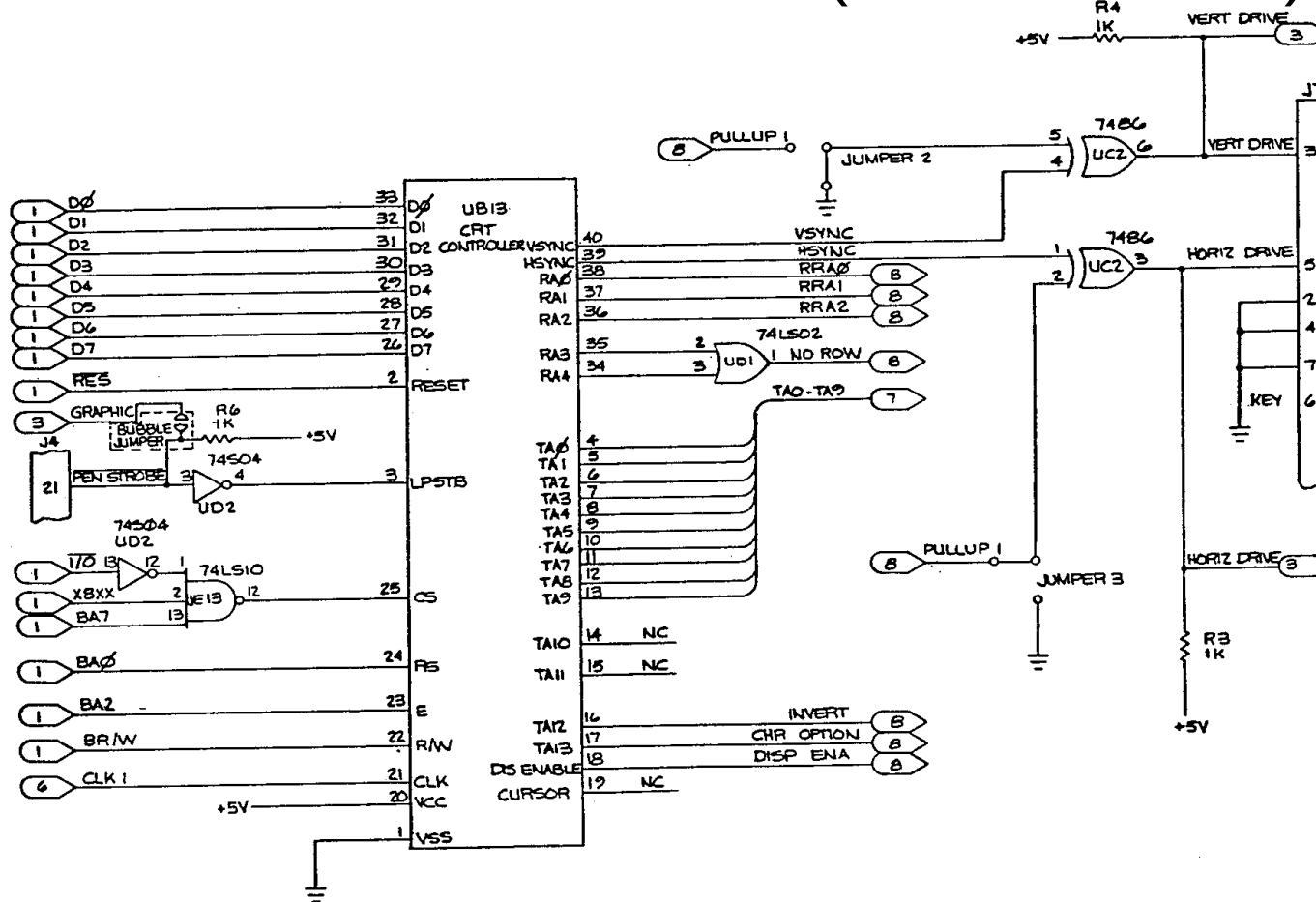


## CRTC AND SYNC BUFFERS

# 80 Column board & Universal board (40/80 columns)

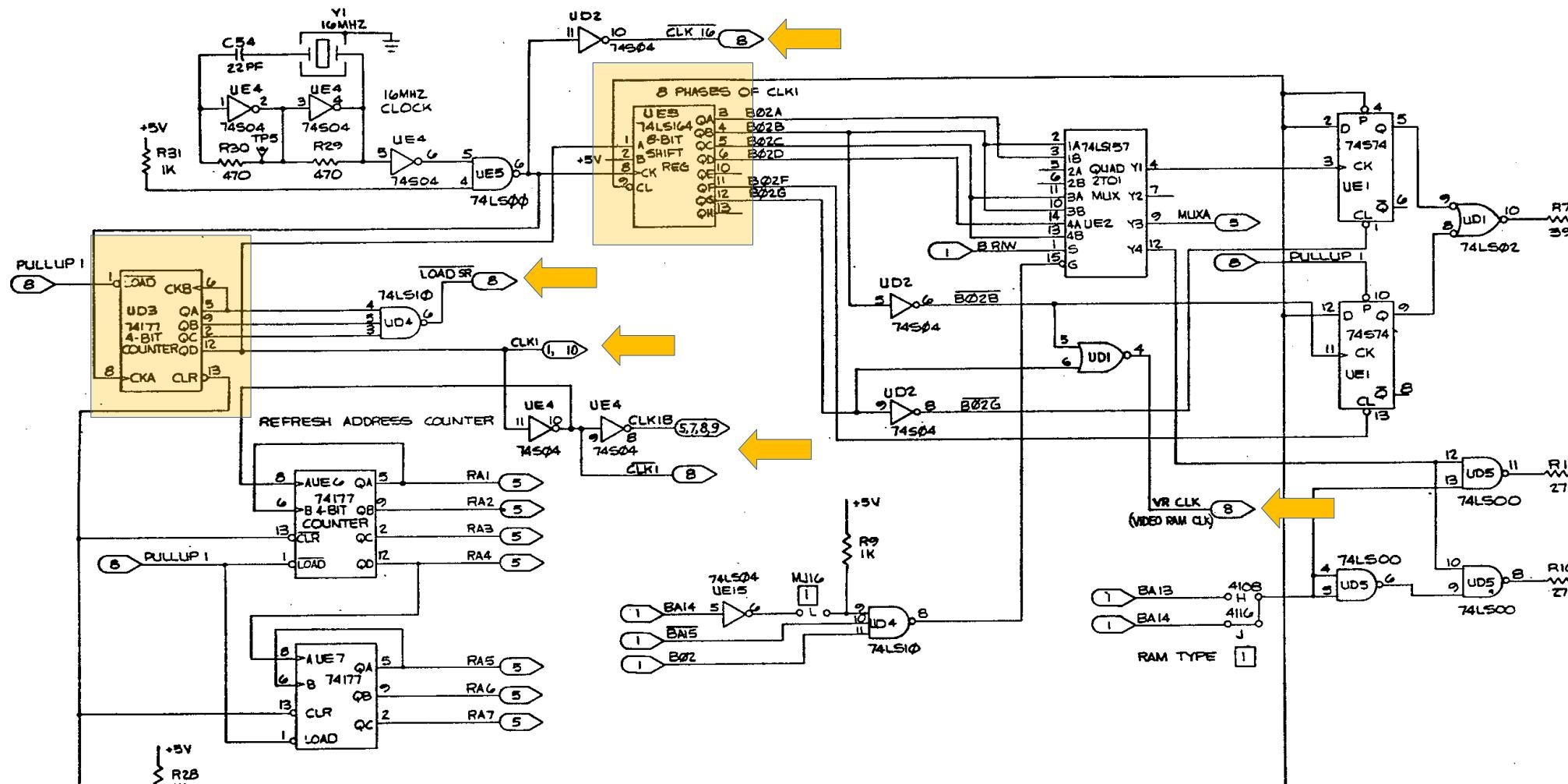


# 80 Column board & Universal board (40/80 columns)

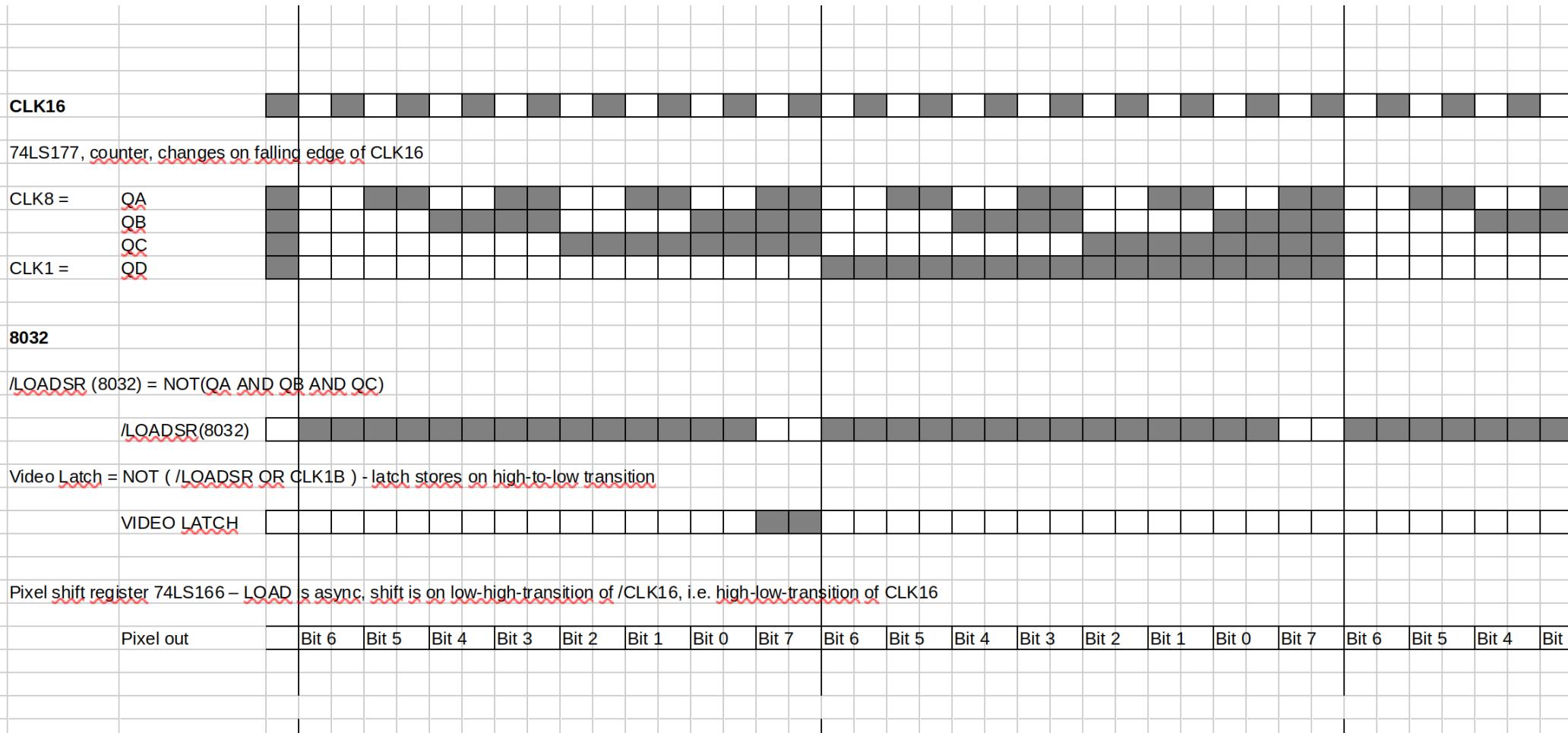


# Detailed Timing

SEE SHEET 1
-------------



# 8032



# 4032 & 8032

74LS164 Shift register, input is Clk1, changes on rising edge of Phi2

BPhi2A = QA  
BPhi2B = OB  
BPhi2C = QC  
BPhi2D = QD  
BPhi2E = QE  
BPhi2F = QF  
BPhi2G = QG  
BPhi2H = OH

VRCLK (8032) = NOT ( /BPhi2B OR B02G )

VRCLK (8032)

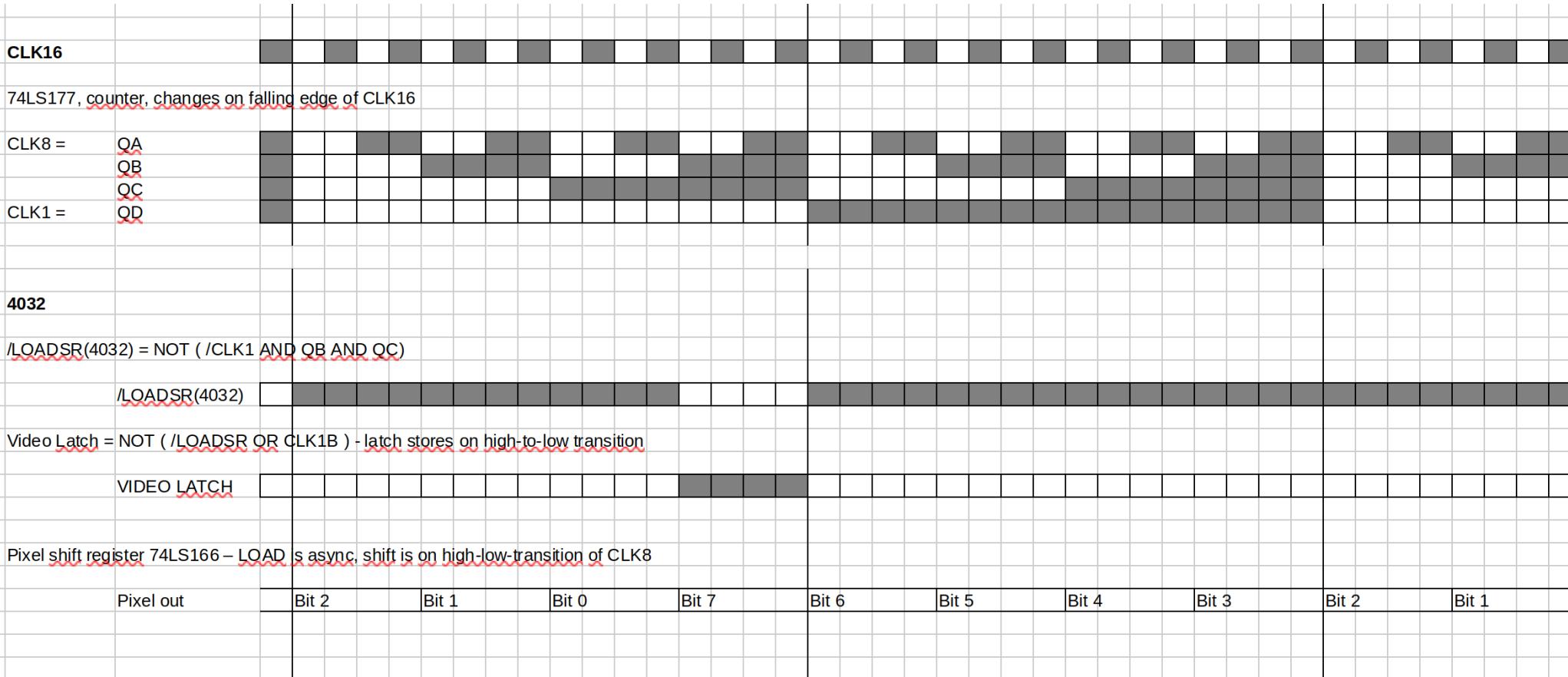
VRCLK (universal) = BPhi2

VRCLK (universal)



Cycle in Rasterline #	0	1	2		
CLK1					
DISPENA					
8032					
Delayed display enable					
CLK1B up	U31A Q				
/LOADSR up	U31B Q (8032)				
Video RAM	V	C	V	C	V
Video latch odd		VO		VO	
Video latch even		VE		VE	
Charrom in		VE	VO	VE	VO
Charrom out		PE	PO	PE	PO
SR out		PE	PO	PE	PO

# 4032



Cycle in Rasterline #	0	1	2
CLK1			
DISPENA			
4032			
Delayed display enable			
CLK1B up	U31A Q		
/LOADSR up	U31B Q (4032)		
Video RAM	V	C	V
Video latch even		VE	VE
Charrom in		VE	VE
Charrom out		PE	PE
SR out (8px per cycle)			PE
			PE

# Summary

# Commodore PET Video

Five different types of Video output



2001:

- 40x25 chars
- fixed timing
- 1k VRAM
- „snow”

2001N / 3032:

- 40x25 chars
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4032

- 40x25 chars
- CRTC timing
- 1k VRAM

8032

- 80x25 chars
- CRTC timing
- 2k VRAM

8296

- 80x25 chars
- CRTC timing
- 8k VRAM