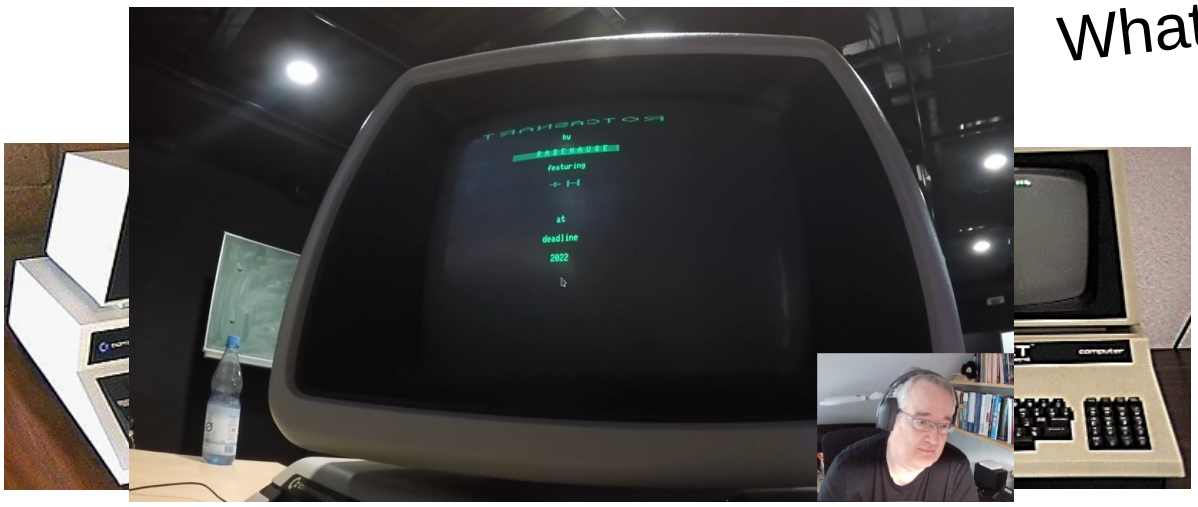
8-bit times

Commodore PET Video – Part 3

The 8296 Model!

How does it work?
What's so special about it?
Demo Reaction!



Commodore PET Video

Five different types of Video output

2001:
- 40x25 chars
- fixed timing
- 1k VRAM
- „snow“

2001N / 3032:
- 40x25 chars
- fixed timing
- 1k VRAM

4032
- 40x25 chars
- CRTC timing
- 1k VRAM

8032
- 80x25 chars
- CRTC timing
- 2k VRAM

8296
- 80x25 chars
- CRTC timing
- 8k VRAM

Commodore PET Video Part 3

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8296
- 80x25 chars
- CRTC timing
- 8k VRAM
- 128k RAM
- 8096 ext.

Commodore PET Video Part 3

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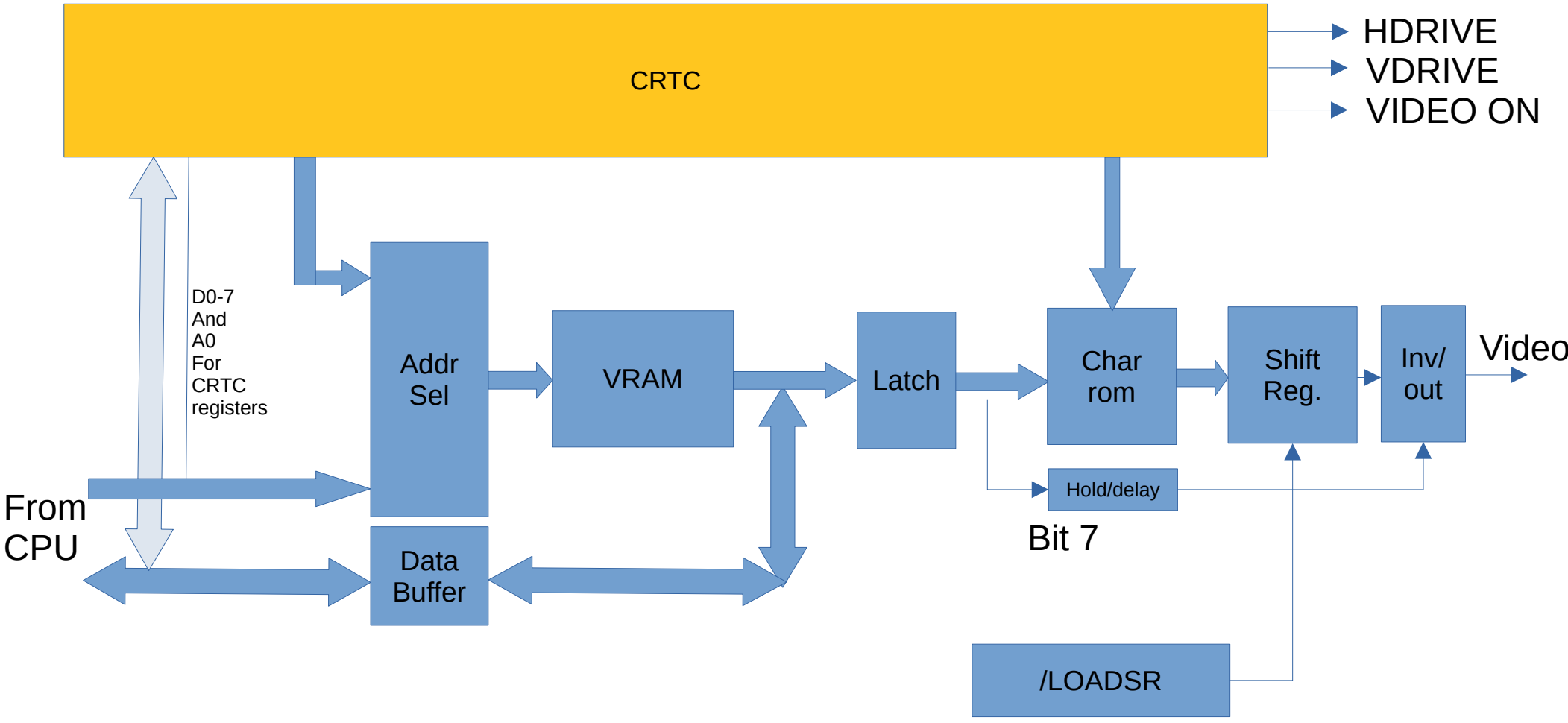
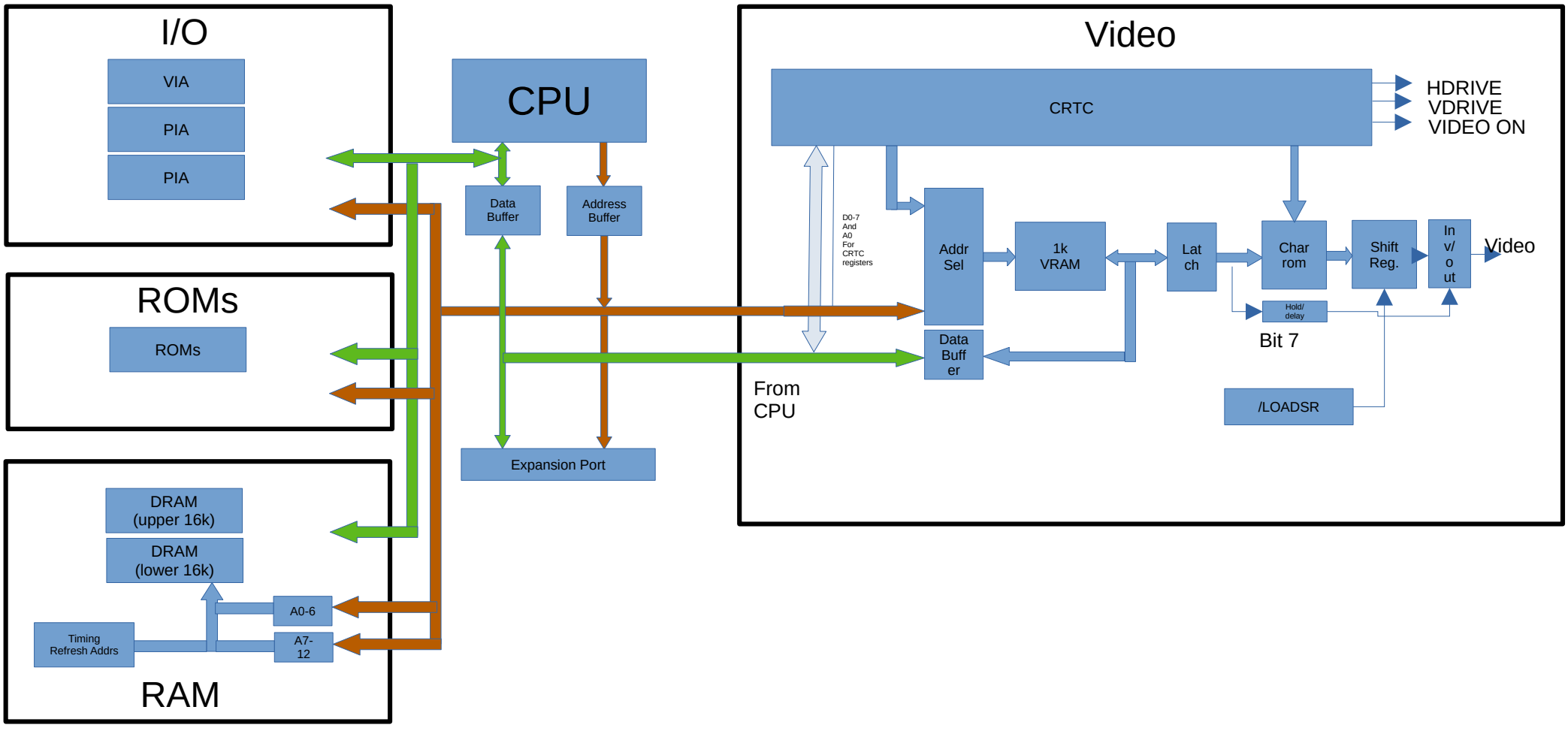
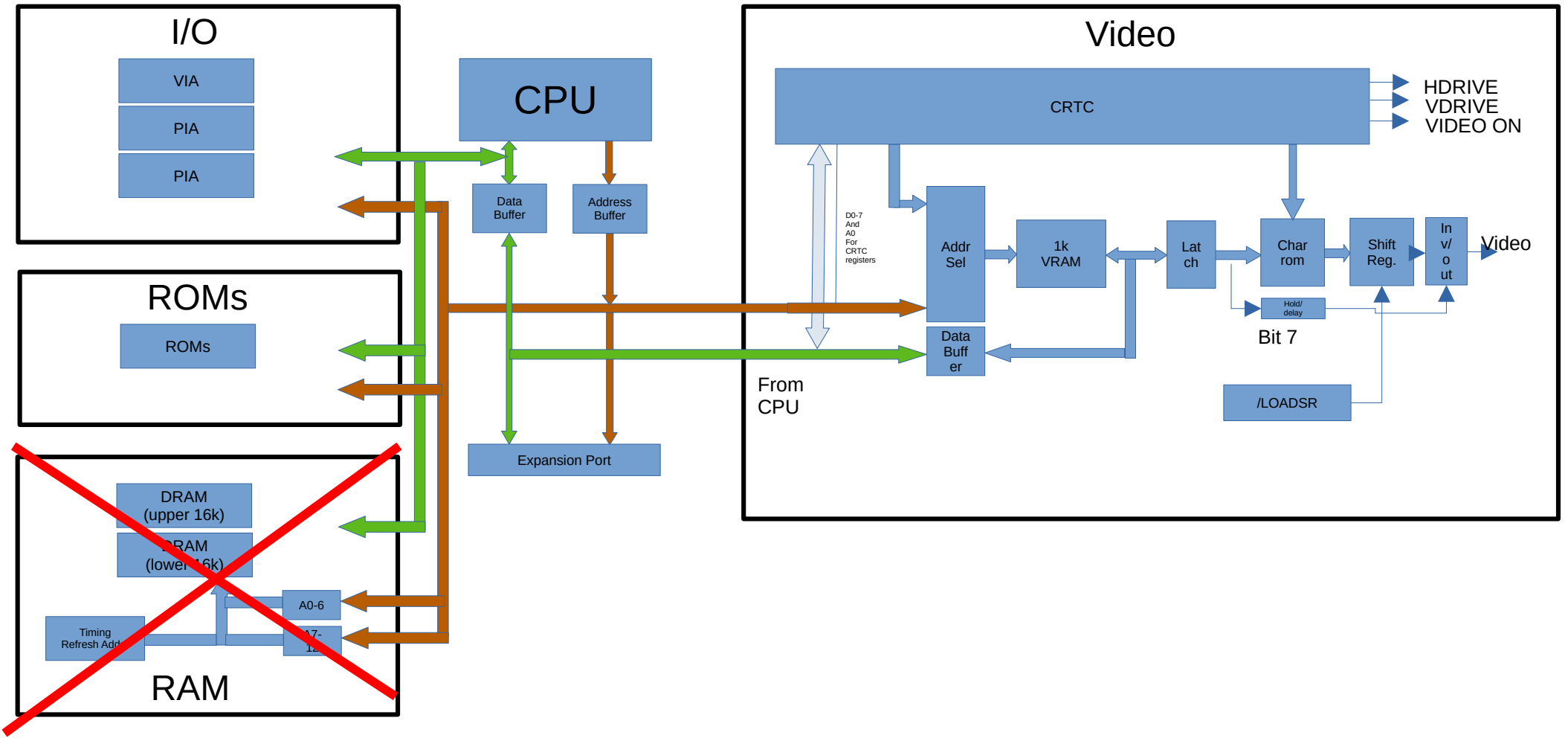
- 128k RAM


CRTC
HDRIVE
VDRIVE
VIDEO ON
D0-7
And
A0
For
CRTC
registers
Addr
Sel
VRAM
Latch
Char
rom
Shift
Reg.
Inv/
out
Video
From
CPU
Data
Buffer
Hold/delay
Bit 7
/LOADSR

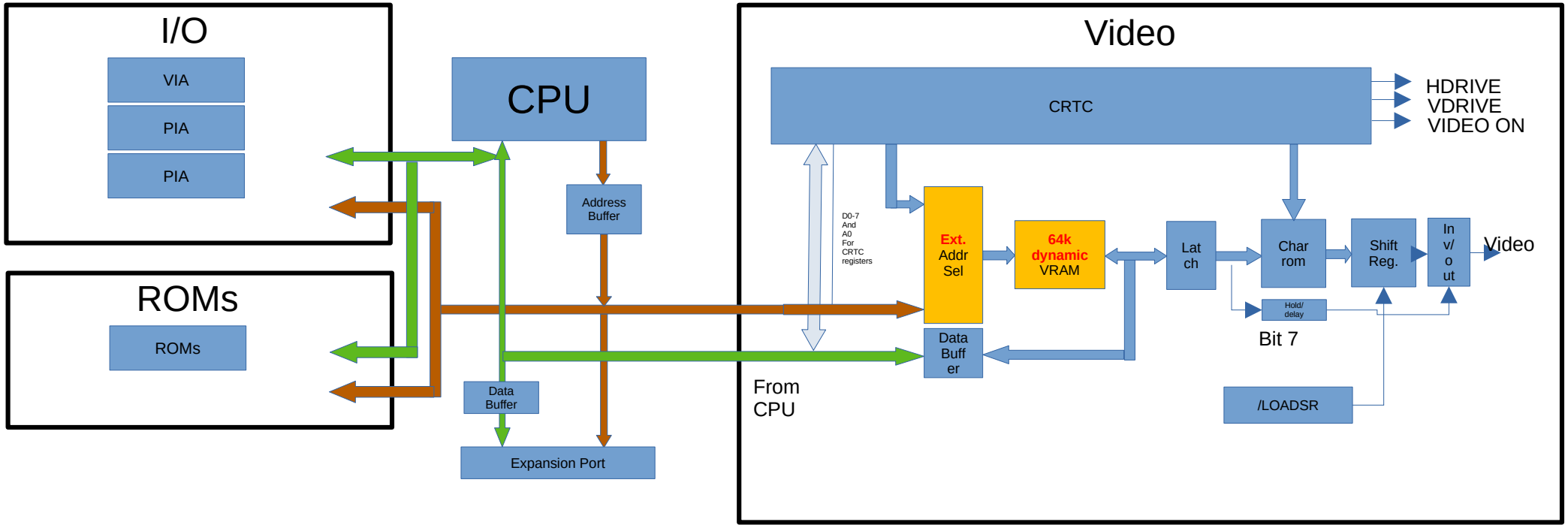
PET - 2001-4032



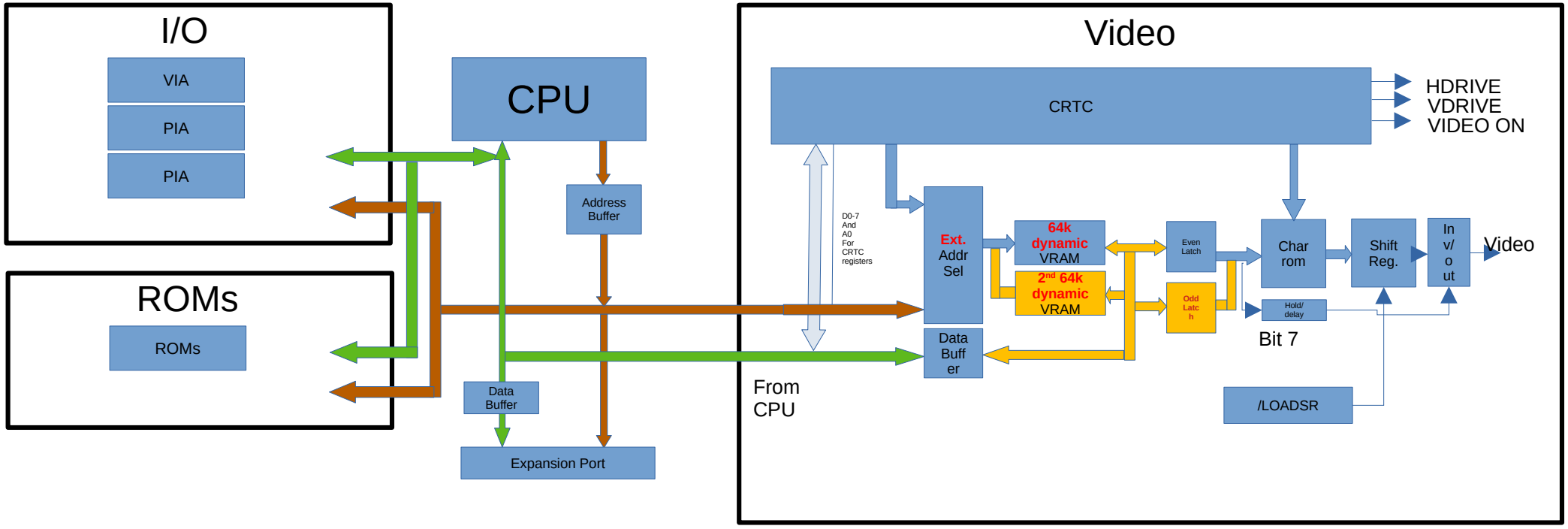
What if?


I/O
VIA
PIA
PIA
ROMs
ROMs
RAM
DRAM
(upper 16k)
DRAM
(lower 16k)
A0-6
Timing
Refresh Addr
A7-
12
CPU
Data
Buffer
Address
Buffer
Expansion Port
Video
CRTC
HDRIVE
VDRIVE
VIDEO ON
D0-7
And
A0
For
CRTC
registers
From
CPU
Addr
Sel
1k
VRAM
Lat
ch
Char
rom
Shift
Reg.
In
v/
o
ut
Video
Hold/
delay
Bit 7
Data
Buff
er
/LOADSR

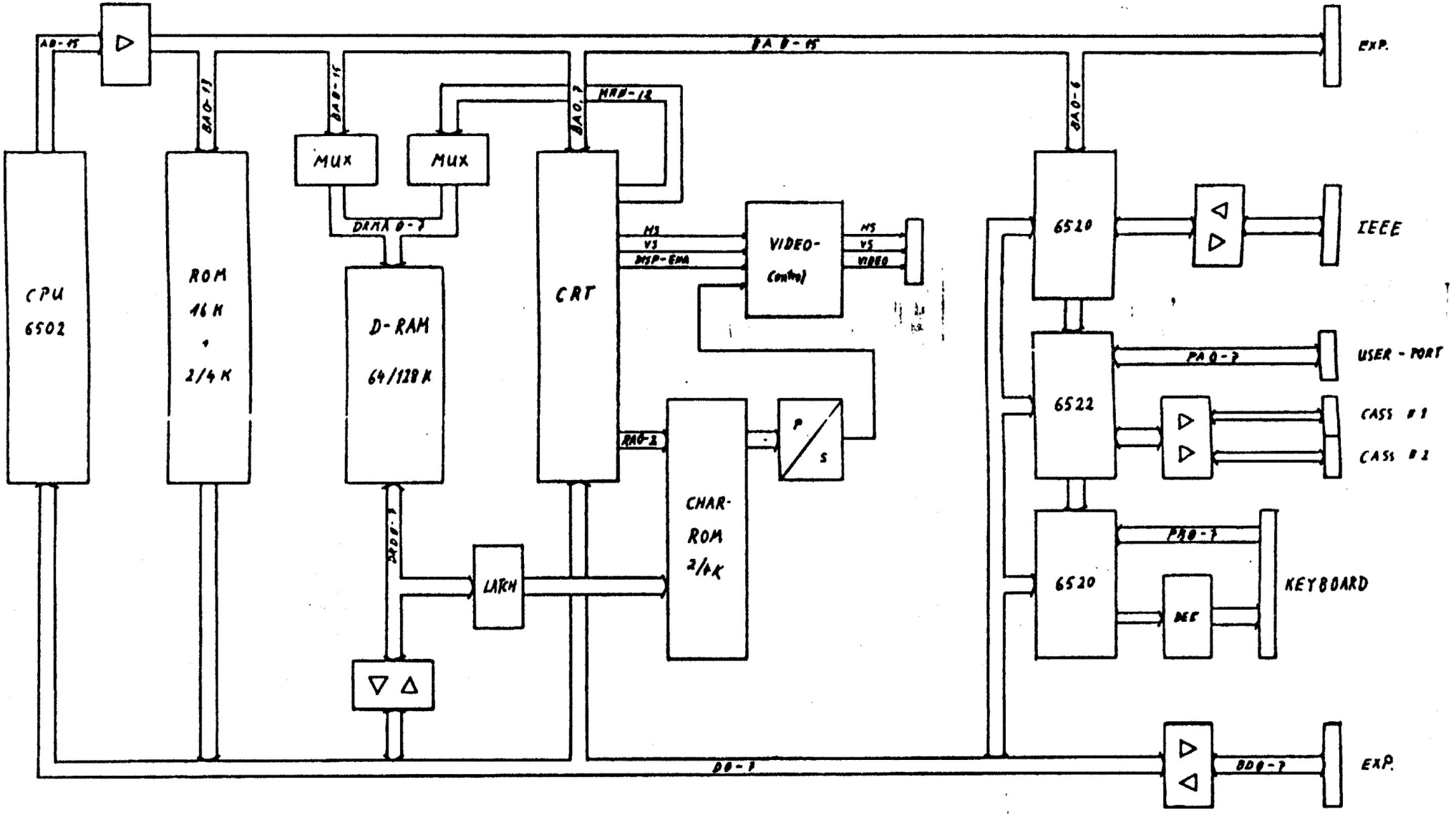
Replace RAM by extended Video RAM!

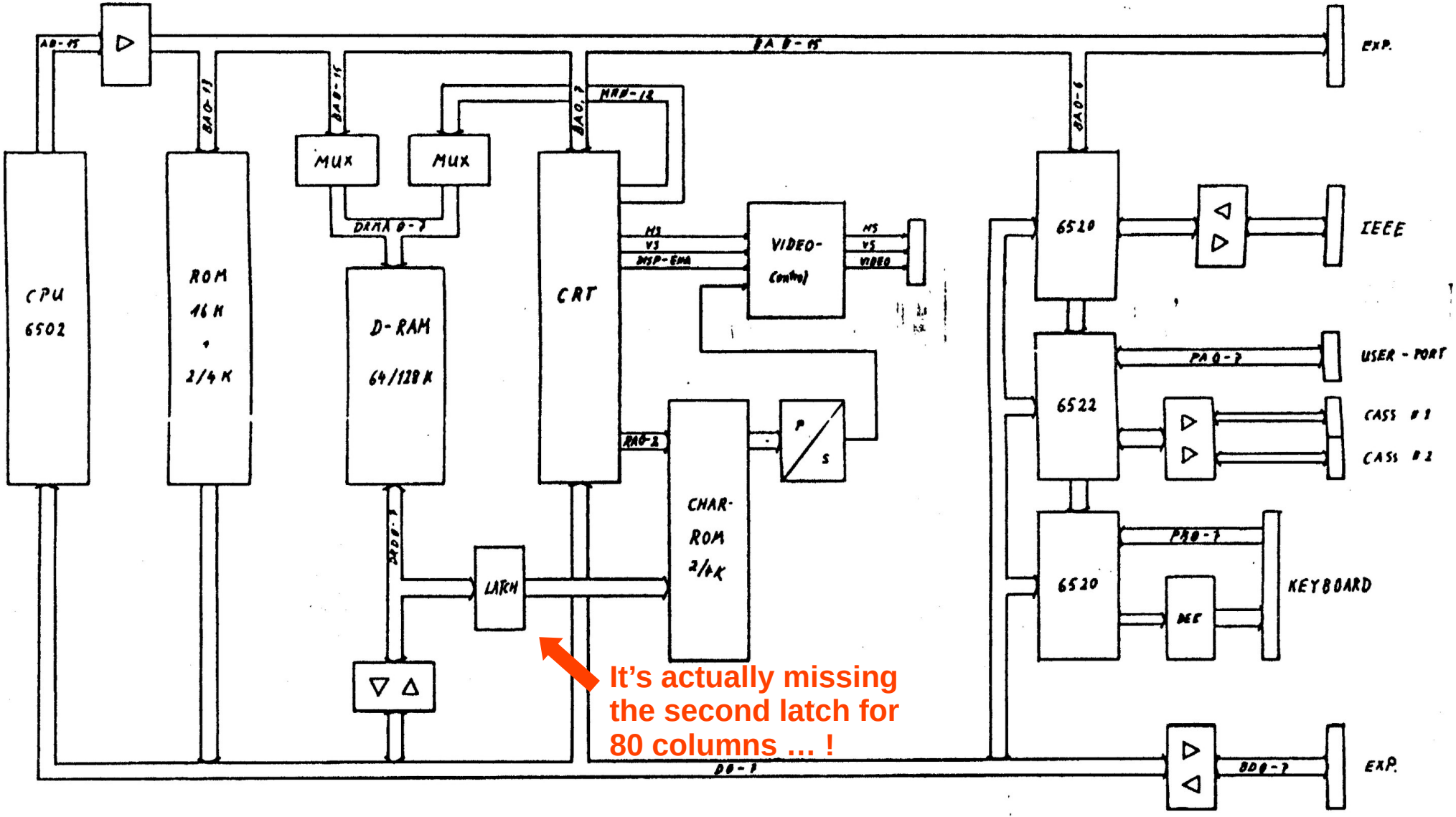


Then add 80 cols & 8096 extension ...

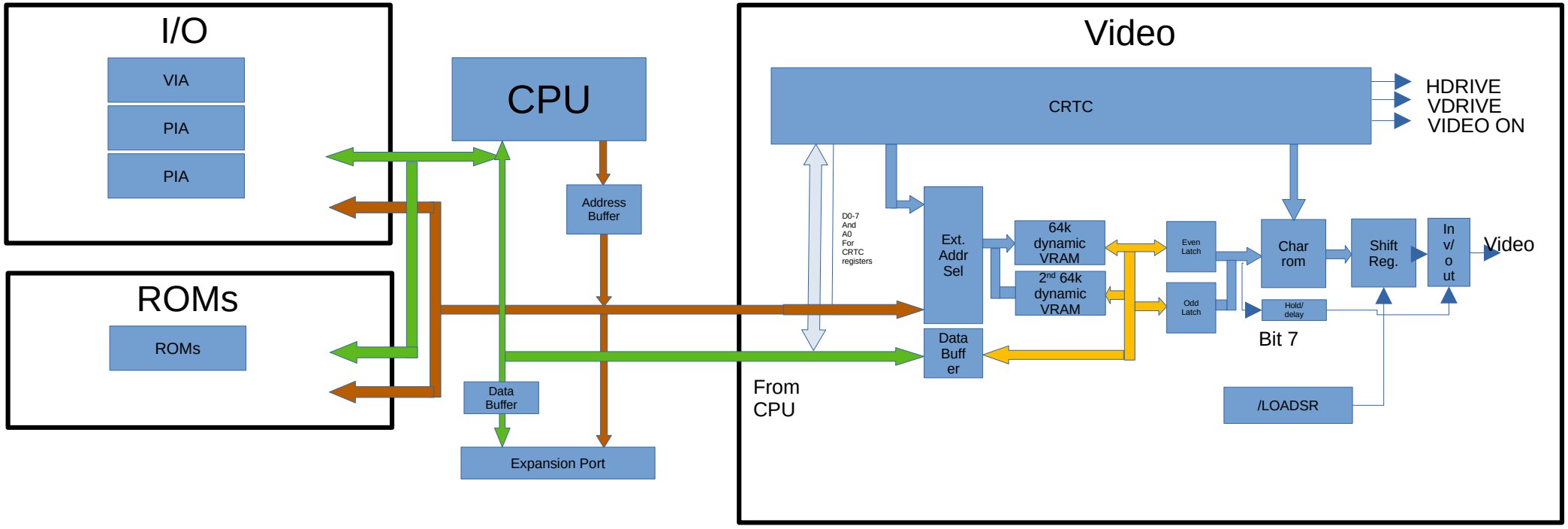


… and we get the 8296!


AD-15
BAD-11
BAD-15
MUX
MUX
DRAM 0-7
CPU
6502
ROM
16K
+
2/4K
D-RAM
64/128K
BAD 7
MRD-12
CRT
HS
VS
DISP-ENA
VIDEO-
Control
HS
VS
VIDEO
PA0-2
CHAR-
ROM
2/4K
P
S
LATCH
DBD-7
BA 8-15
BAD-6
6520
6522
6520
PA0-7
PA0-7
REC
EXP.
IEEE
USER - PORT
CASS # 1
CASS # 2
KEYBOARD
DD-7
BDD-7
EXP.


CPU
6502
ROM
16 K
+
2/4 K
MUX
MUX
D-RAM
64/128 K
CRT
VIDEO-
Control
CHAR-
ROM
2/4K
LATCH
P
S
6520
6522
6520
IEEE
USER - PORT
CASS # 1
CASS # 2
KEYBOARD
EXP.
EXP.
It's actually missing
the second latch for
80 columns ... !

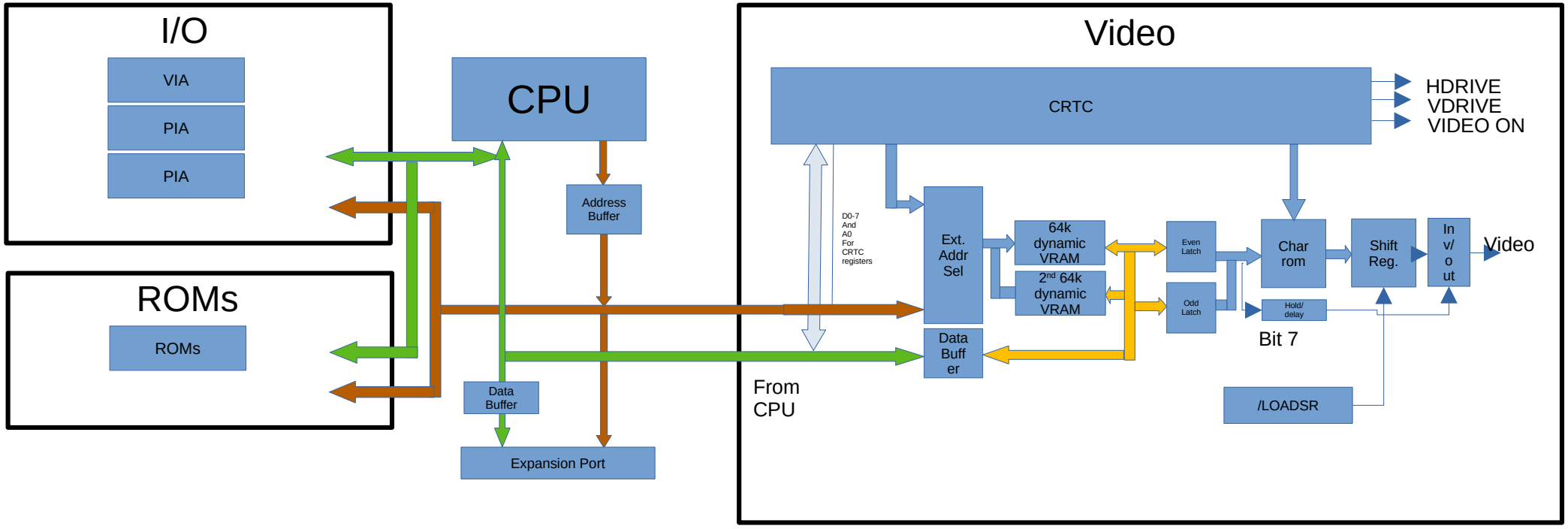
But what's strange for 1 MHz 80 col machine:



Single video RAM data bus?

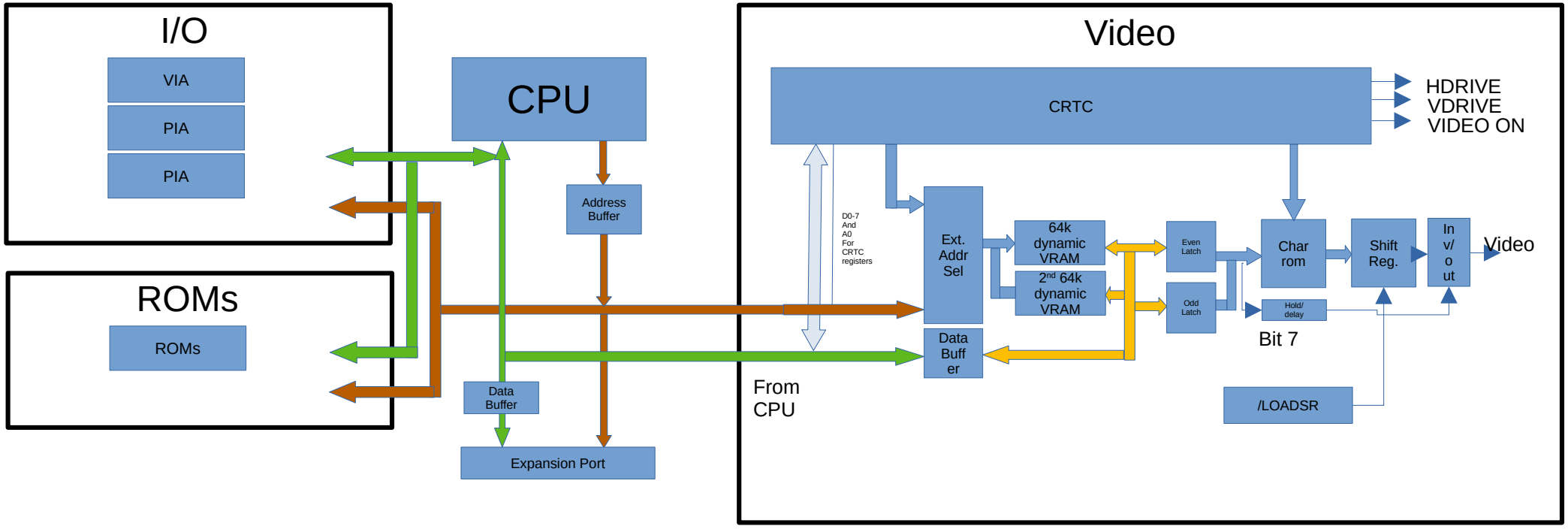
RAM access timing

But what's strange for 1 MHz 80 col machine:



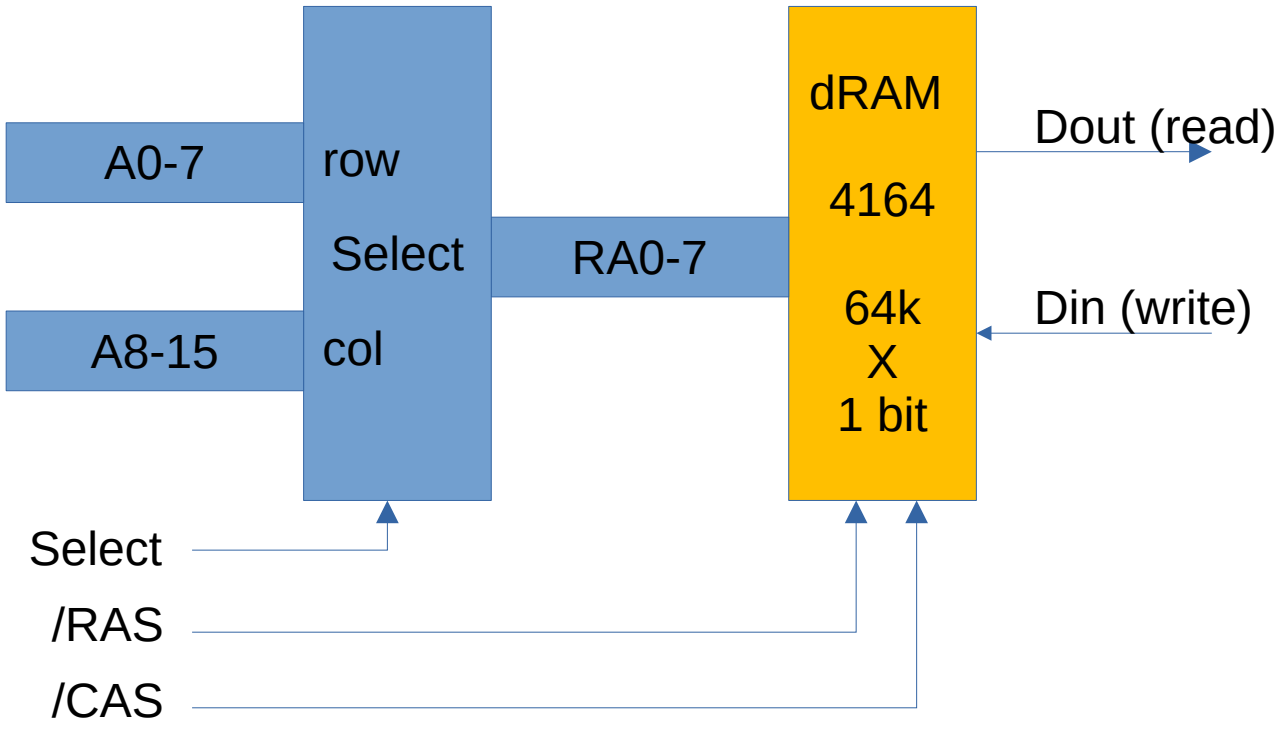
Single video RAM data bus?

It’s the timing!



faster RAM, 2 page mode read cycles per Phi1

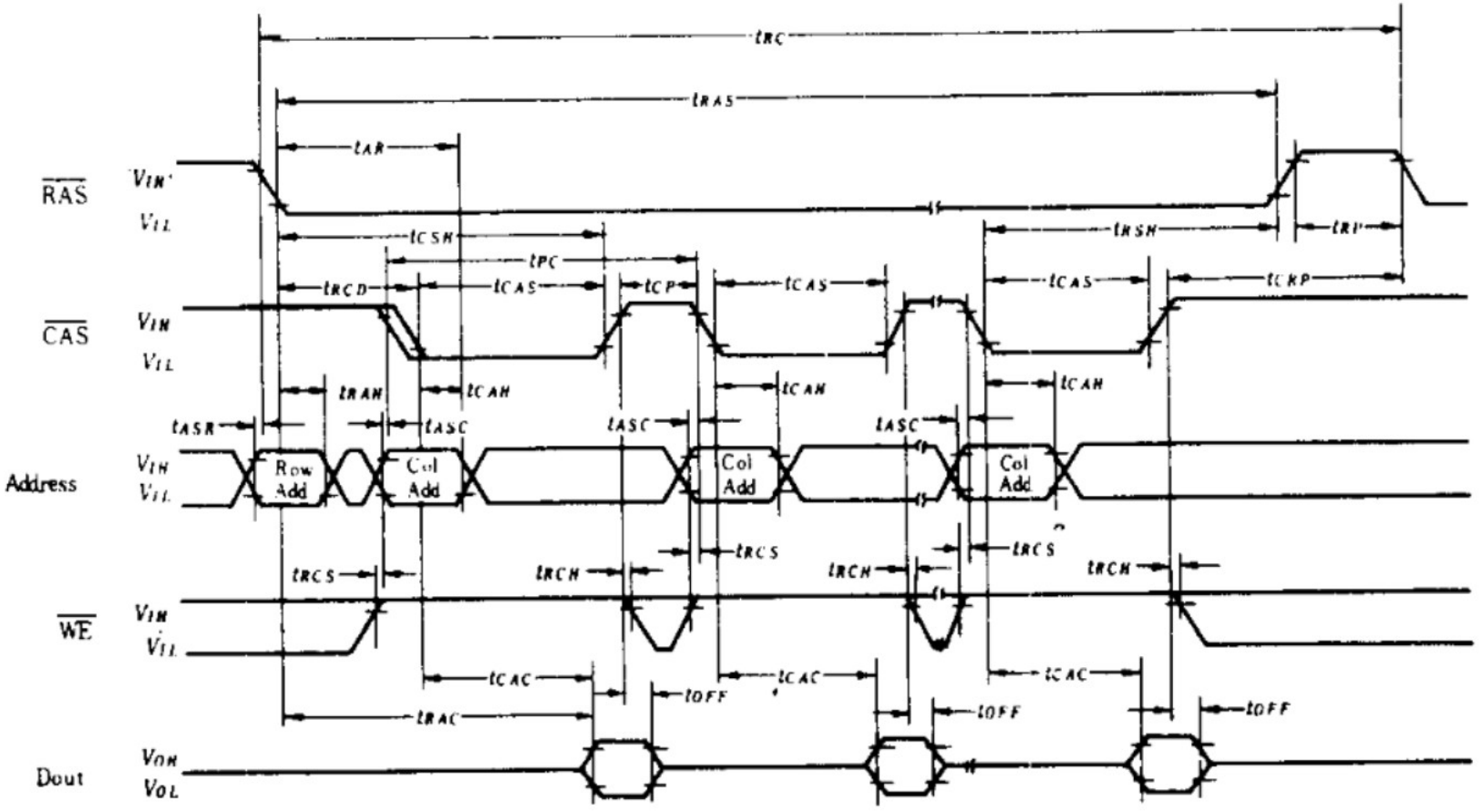
How does dRAM work?



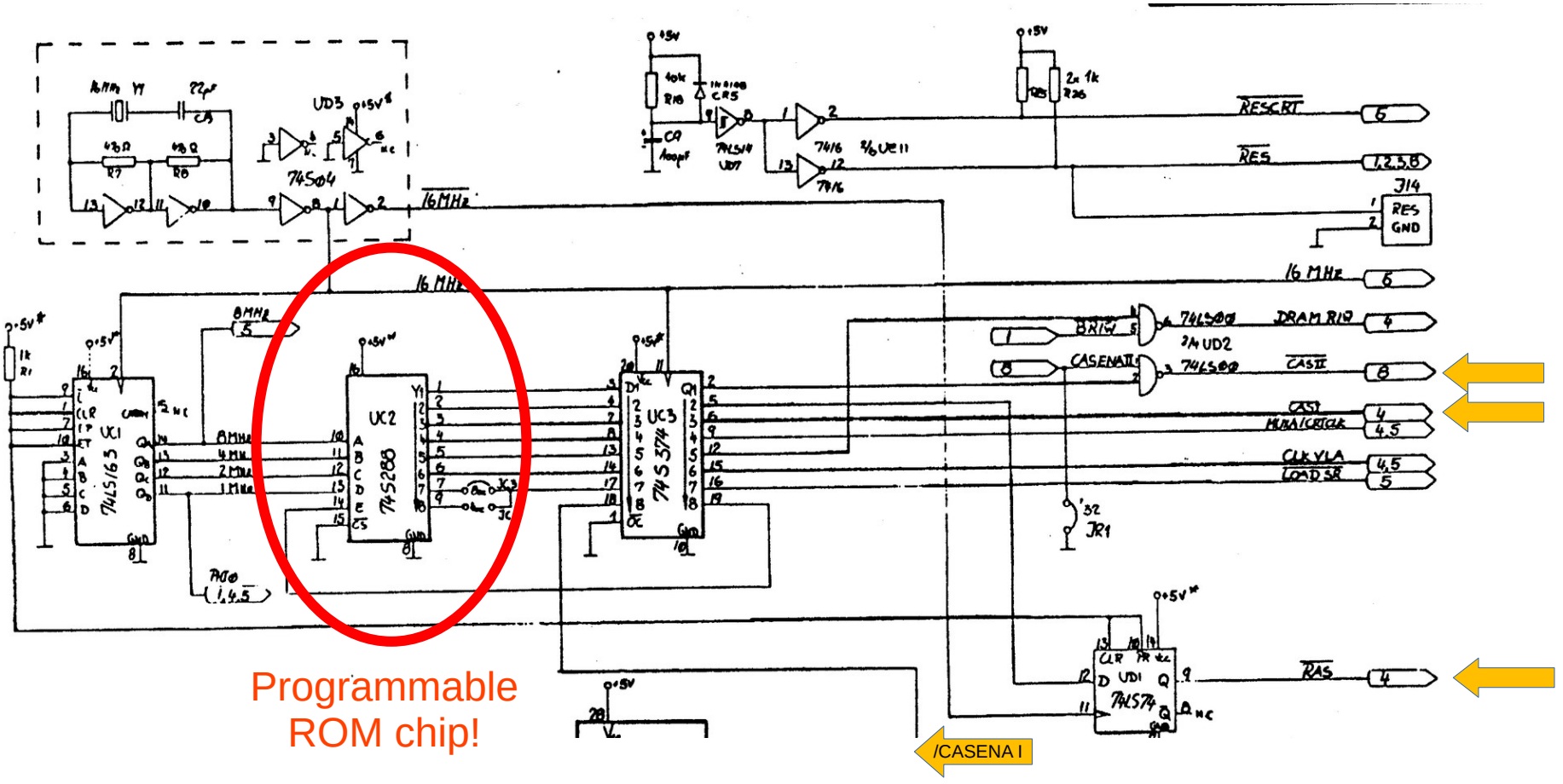
- Only half the address lines as one expects – split into row and column addresses
- 1st Row address is sent, using /RAS going low
- Then Column address is send, using /CAS going low
- When transfer is done, /CAS and /RAS go high

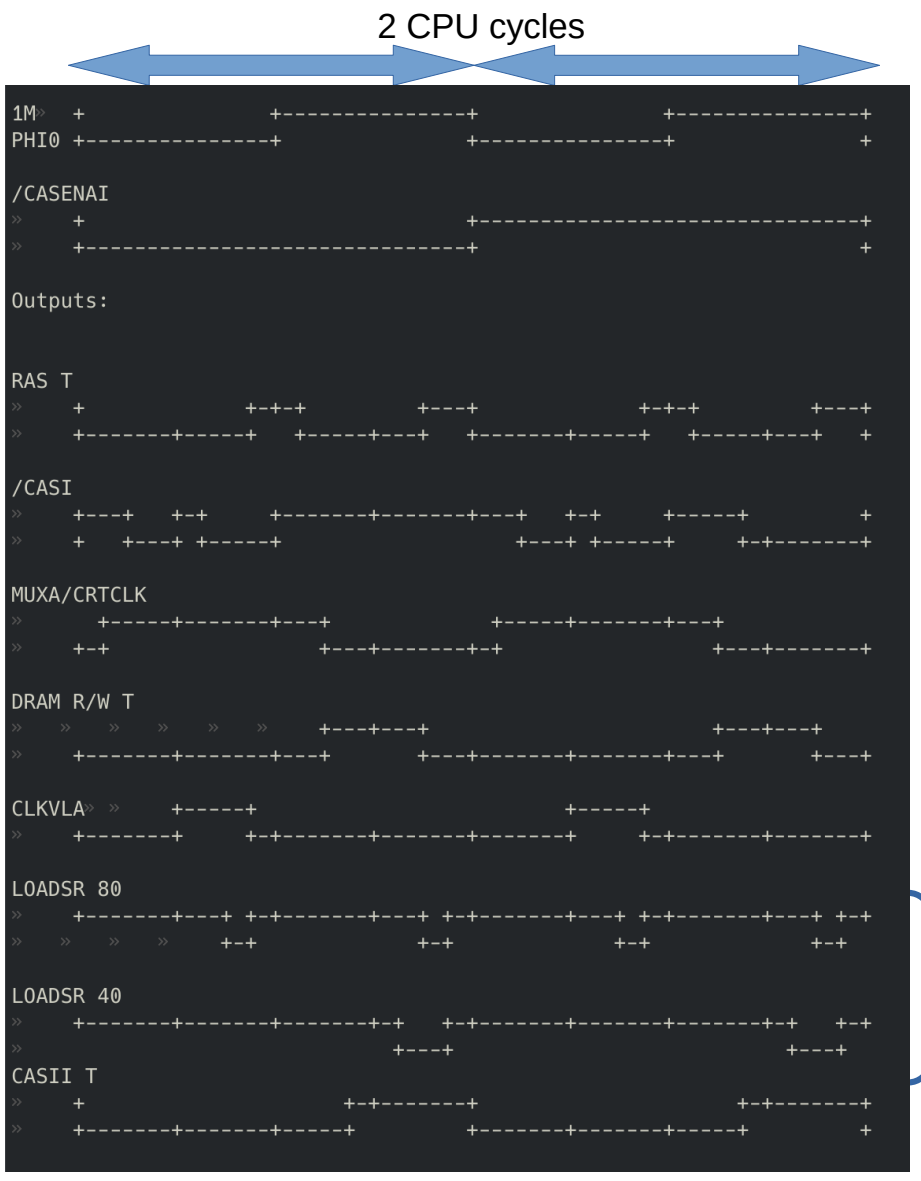
How does dRAM work?

● PAGE MODE READ CYCLE



Master timing





Inputs

1 MHz CPU clock (input)

Bank 0 select

Outputs

DRAM /RAS signal for both banks – 2 cycles per CPU clock
Externally delayed one half 16MHz clock tick

DRAM bank 1 /CAS signal
2 (video) page mode read accesses in 1st /RAS cycle
1 access for 2nd /RAS cycle

Switch between upper/lower dRAM address bits;
Also, CRTC clock!

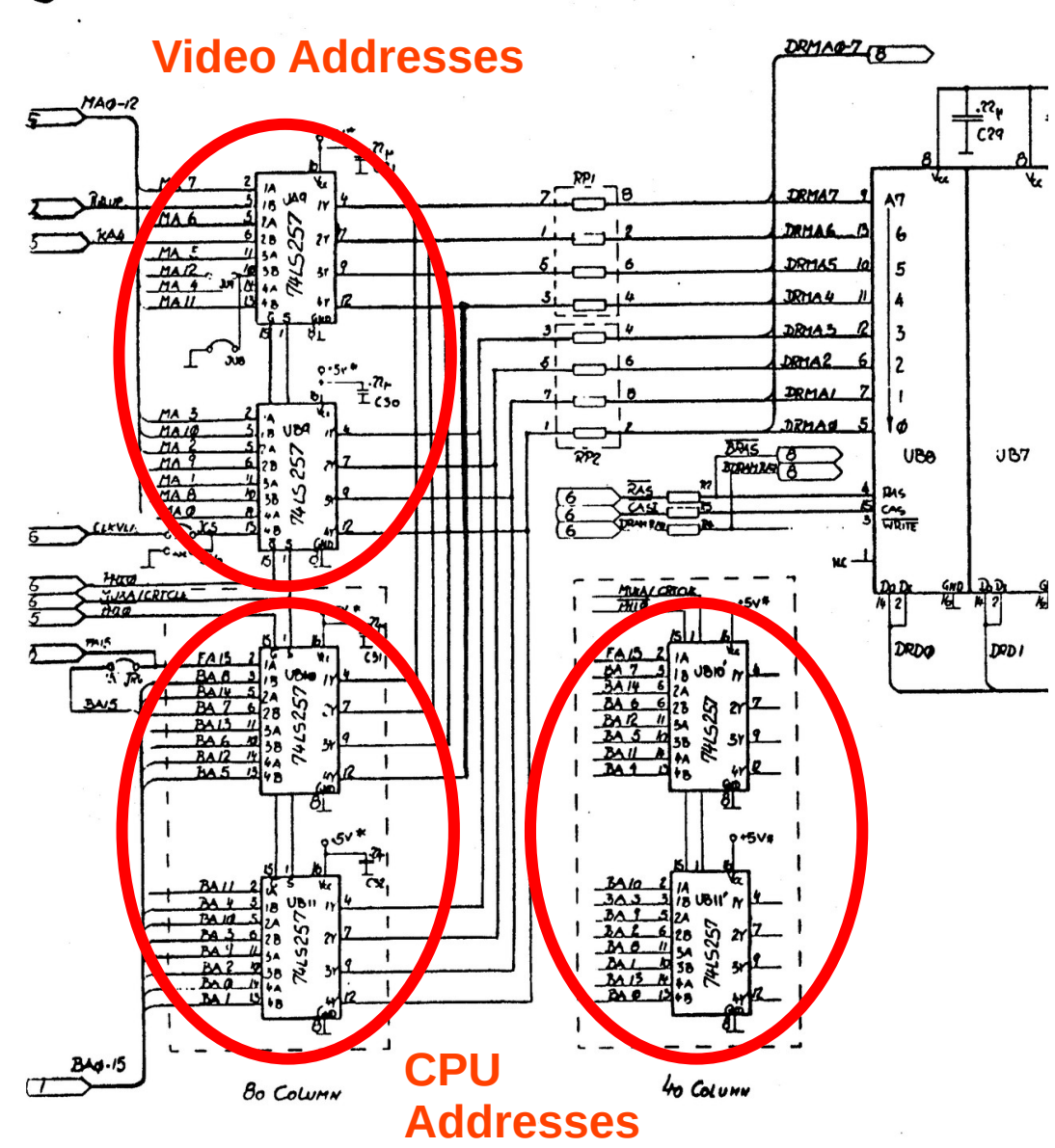
Writes only during Phi2, externally mixed with CPU R/-W

Even/Odd
Latch video data on rising (even)/falling (odd) edge

/LOADSR, Selectable by jumper

DRAM bank 2 CAS timing, externally combined with the address select signal, to create /CAS II

Video address mapping



- Extended Address decoders for 16 (8 row, 8 col) address bits
- Corresponding address selectors enabled via Phi1:
  - 0 is video
  - 1 is CPU
- Two different setups for 40 and 80 column machines – for the CPU addresses!
  - Same chips – just different locations on the board

Address mapping 40/80 columns

Video

Select: LOW is Row → A inputs; HIGH is Column → B inputs

Row	Col
7	pullup
6	RA4
5	low via JU8
4	11
3	10
2	9
1	8
0	GND / CLKVLA

CPU

Select: HIGH is Row → B inputs; LOW is Column → A inputs

40 cols		80 cols	
Row	**Col**	**Row**	**Col**
7	FA15	8	BA15/FA15
6	14	7	14
5	12	6	13
4	11	5	12
3	10	4	11
2	9	3	10
1	8	2	9
0	13	1	0

- MUXA/CRTCLK is used to select – and is different polarity for CPU vs. Video accesses!
- Video Row being MA0-7 is important, to have dRAM refresh cycles
- Video mapping corresponds to 40 column – 80 column CPU addresses are shifted one bit
- Video has 12 valid address bits (MA0-11) + CLKLVA for dual fetch during single cycle
  - So, the CRTC can read 8k VRAM. The CPU can read/write $8xxx, but write only to $9xxx (RAM under ROM)

Video Timing

Video Timing

- Different monitor hardware
  - „new“ swivel monitor with new schematics
  - Shared with 700 series (CBM-II)
- Do they need different timing?

ROM Video Timing

	4032				8032				8296					
ROM #	901499-01		901498-01		901474-03.bin		901474-04-3681		324243-01.bin “E-901474-04” in ROM		324243-03.bin “E-324243-03” in ROM		324243-04.bin “E-324243-04” in ROM	
	60 Hz		50 Hz		60 Hz		60 Hz		50 Hz		50 Hz		50 Hz	
	text	graphics	text	graphics	text	graphics	text	graphics	text	graphics	text	graph	text	graph
System clock [MHz]	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R0 – horizontal total	49	49	49	49	49	49	49	49	49	49	58	58	58	58
R1 – horizontal display	40	40	40	40	40	40	40	40	40	40	40	40	40	40
R2 – horizontal sync	41	41	41	41	41	41	41	41	41	41	44	44	44	44
R3 – sync width	15	15	15	15	15	15	15	15	15	15	8	8	8	8
R4 – vertical total	32	40	39	49	32	40	39	49	39	49	32	41	32	41
R5 – vertical adjust	3	5	0	0	3	5	0	0	0	0	9	3	9	3
R6 – vertical display	25	25	25	25	25	25	25	25	25	25	25	25	25	25
R7 – vertical sync	29	33	32	37	29	33	32	37	32	37	29	34	29	34
R9 – scanlines/char	9	7	9	7	9	7	9	7	9	7	9	7	9	7
Time / scanline [us]	50	50	50	50	50	50	50	50	50	50	59	59	59	59
horizontal Freq. [kHz]	20,00	20,00	20,00	20,00	20,00	20,00	20,00	20,00	20,00	20,00	16,95	16,95	16,95	16,95
Scanlines / char	10	8	10	8	10	8	10	8	10	8	10	8	10	8
scanlines total	333	333	400	400	333	333	400	400	400	400	339	339	339	339
Framerate / vert. Freq (Hz)	60,06	60,06	50,00	50,00	60,06	60,06	50,00	50,00	50,00	50,00	50,00	50,00	50,00	50,00

This is like the 8032, unlike the other 8296 timings

Other ROM timings seem to exist

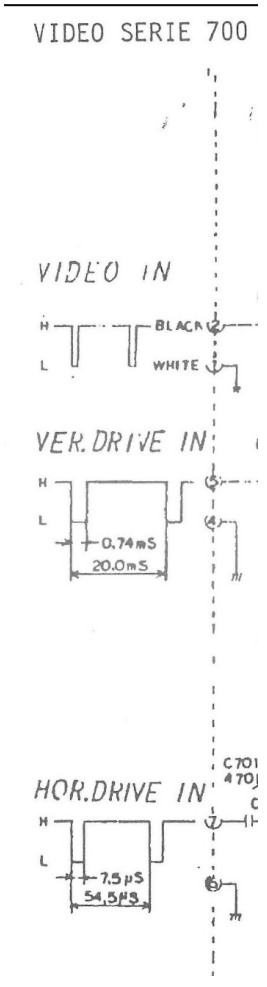
	4032						8032				8296					
ROM #	901499-01		901498-01		901474-03.bin		901474-04-0283.bin PAL Standard		901474-04-3681		324243-01.bin “E-901474-04” in ROM		324243-03.bin “E-324243-03” in ROM		324243-04.bin “E-324243-04” in ROM	
	60 Hz		50 Hz		60 Hz		50 Hz		60 Hz		50 Hz		50 Hz		50 Hz	
	text	graphics	text	graphics	text	graphics	text	graphics	text	graphics	text	graphics	text	graph	text	graph
System clock [MHz]	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R0 – horizontal total	49	49	49	49	49	49	63	63	49	49	49	49	58	58	58	58
R1 – horizontal display	40	40	40	40	40	40	40	40	40	40	40	40	40	40	40	40
R2 – horizontal sync	41	41	41	41	41	41	50	50	41	41	41	41	44	44	44	44
R3 – sync width	15	15	15	15	15	15	8	8	15	15	15	15	8	8	8	8
R4 – vertical total	32	40	39	49	32	40	32	36	39	49	39	49	32	41	32	41
R5 – vertical adjust	3	5	0	0	3	5	16	17	0	0	0	0	9	3	9	3
R6 – vertical display	25	25	25	25	25	25	25	25	25	25	25	25	25	25	25	25
R7 – vertical sync	29	33	32	37	29	33	29	32	32	37	32	37	29	34	29	34
R9 – scanlines/char	9	7	9	7	9	7	8	7	9	7	9	7	9	7	9	7
Time / scanline [us]	50	50	50	50	50	50	64	64	50	50	50	50	59	59	59	59
horizontal Freq. [kHz]	20,00	20,00	20,00	20,00	20,00	20,00	15,63	15,63	20,00	20,00	20,00	20,00	16,95	16,95	16,95	16,95
Scanlines / char	10	8	10	8	10	8	9	8	10	8	10	8	10	8	10	8
scanlines total	333	333	400	400	333	333	313	313	400	400	400	400	339	339	339	339
Framerate / vert. Freq (Hz)	60,06	60,06	50,00	50,00	60,06	60,06	49,92	49,92	50,00	50,00	50,00	50,00	50,00	50,00	50,00	50,00

This PAL timing ROM seems to exist as official ROM,
But it is a true outlier

What timing is „correct“?

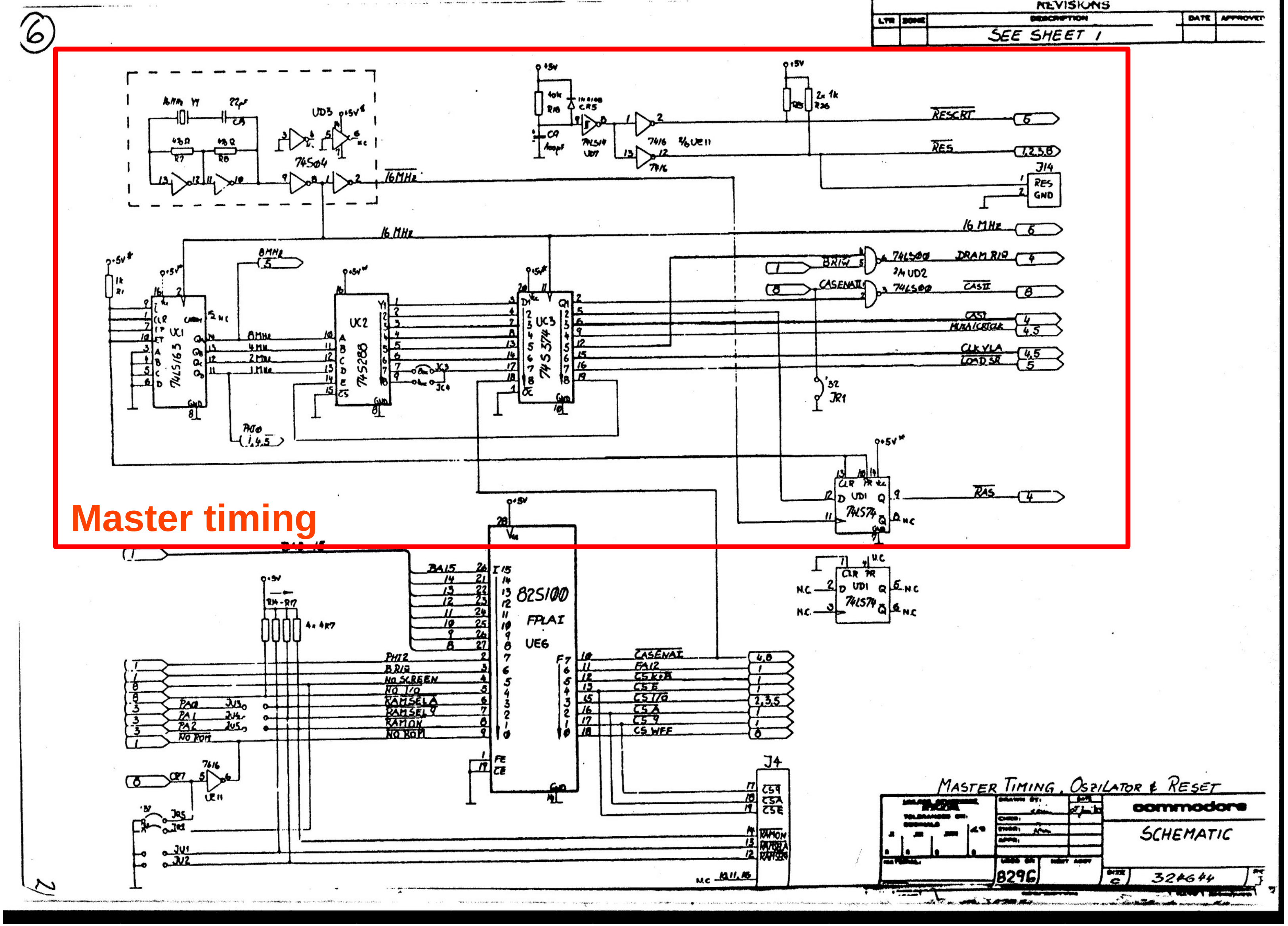
8296					
324243-01.bin “E-901474-04” in ROM 50 Hz		324243-03.bin “E-324243-03” in ROM 50 Hz		324243-04.bin “E-324243-04” in ROM 50 Hz	
text	graphics	text	graph	text	graph
1	1	1	1	1	1
49	49	58	58	58	58
40	40	40	40	40	40
41	41	44	44	44	44
15	15	8	8	8	8
39	49	32	41	32	41
0	0	9	3	9	3
25	25	25	25	25	25
32	37	29	34	29	34
9	7	9	7	9	7
50	50	59	59	59	59
20,00	20,00	16,95	16,95	16,95	16,95
10	8	10	8	10	8
400	400	339	339	339	339
50,00	50,00	50,00	50,00	50,00	50,00

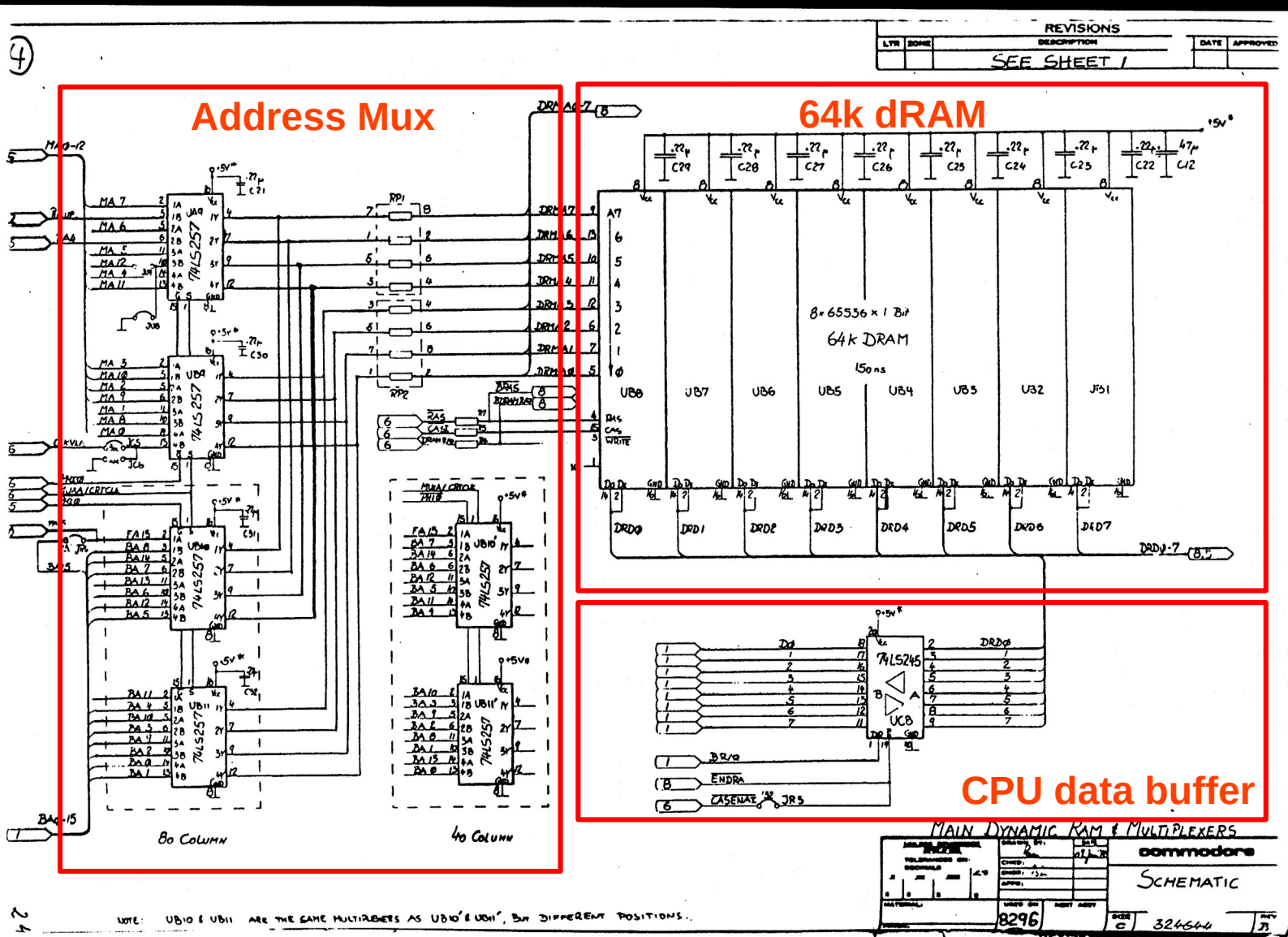
- Neither timing conforms to the monitor’s specs…

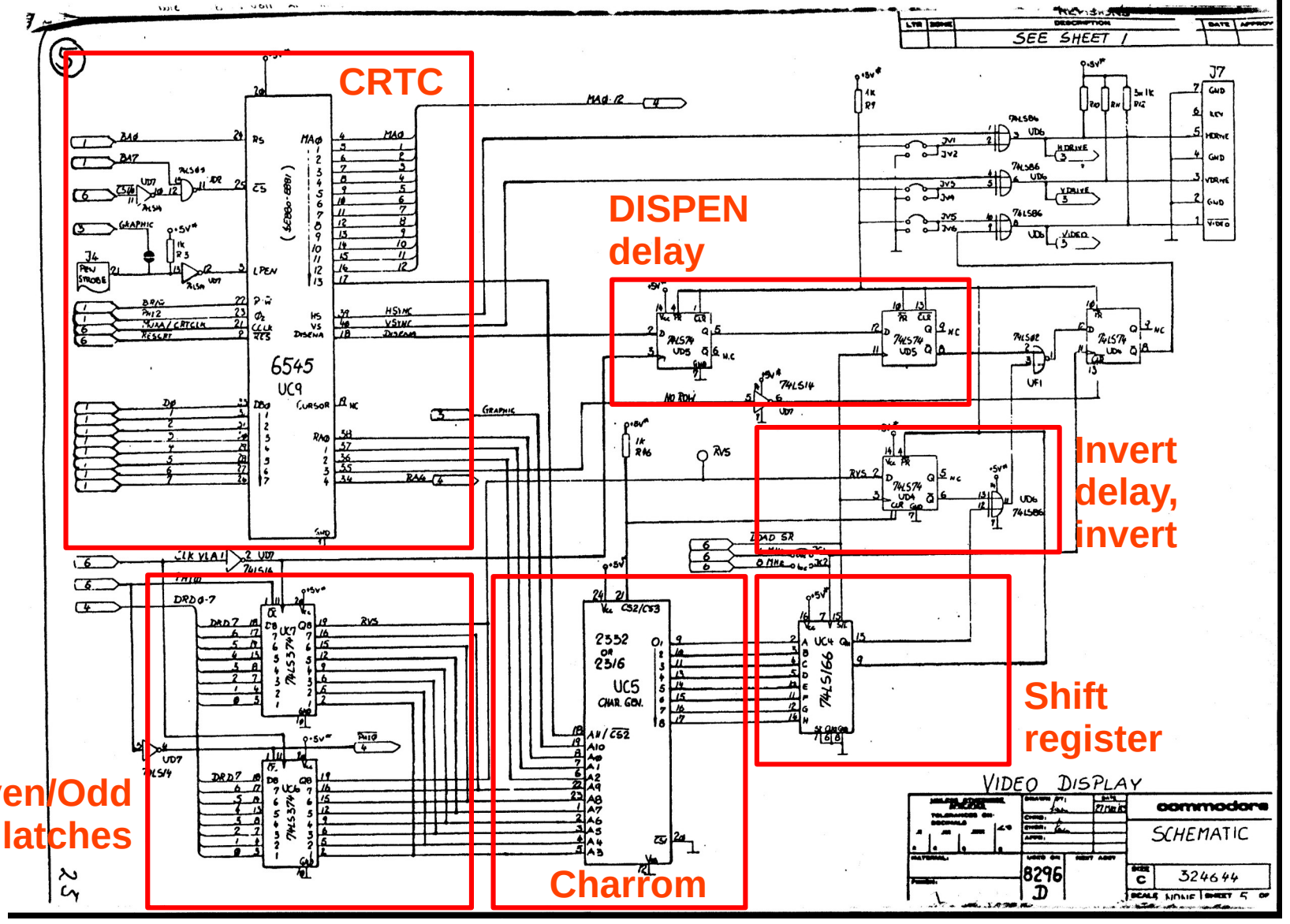


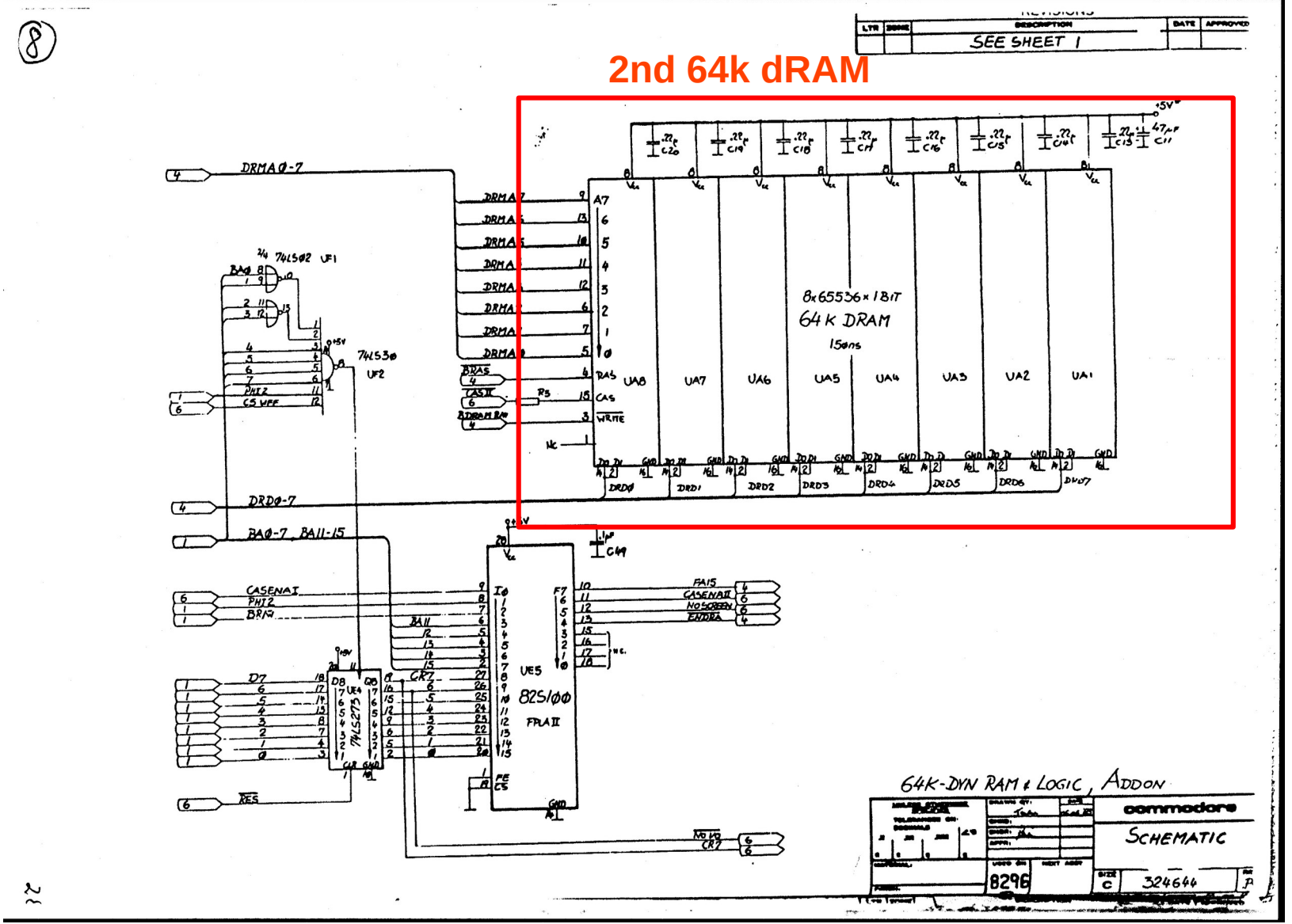
Demo reaction

Schematics deep dive


6
REVISIONS
SEE SHEET 1
Master timing
16MHz
RESCRT
RES
J14
RES
GND
16 MHz
DRAM R/W
CASENAI
74LS00
CAS
CLK VLA
LOAD SR
74LS163
UC1
74S288
UC2
74S374
UC3
74S74
UD1
RAS
82S100
FPLAI
UE6
CASENAI
FA12
CS E
CS I/O
CS 9
CS WFF
J4
RAMON
PHI2
BR/W
NO SCREEN
NO I/O
RAMSEL A
RAMSEL 9
NO ROM
4x 4K7
MASTER TIMING, OSZILATOR & RESET
commodore
SCHEMATIC
8296
324644


Address Mux
64k dRAM
CPU data buffer
REVISIONS
SEE SHEET 1
8x65536 x 1 Bit
64k DRAM
150ns
74LS257
74LS245
80 Column
40 Column
MAIN DYNAMIC RAM & MULTIPLEXERS
commodore
SCHEMATIC
8296
324544
NOTE: UB10 & UB11 ARE THE SAME MULTIPLEXERS AS UB10' & UB11', BUT DIFFERENT POSITIONS.


CRTC
DISPEN delay
Invert delay, invert
Shift register
Even/Odd data latches
Charrom
6545 UC9
2332 OR 2316 UC5 CHAR. GEN.
74LS166 UC4
74LS374 UC7
74LS374 UC6
SEE SHEET 1
VIDEO DISPLAY
commodore
SCHEMATIC
8296 D
324644


2nd 64k dRAM
SEE SHEET 1
8x65536x1BIT
64K DRAM
150ns
74LS30
74LS273
8251ØØ
64K-DYN RAM & LOGIC, ADDON
commodore
SCHEMATIC
8296
324644

Summary

Commodore PET Video Part 3

Five different types of Video output

2001:
- 40x25 chars
- fixed timing
- 1k VRAM
- „snow“

2001N / 3032:
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- fixed timing
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