Bus

File: Bus.kicad_sch

CPU, FPGA, FRAM

File: CPU,_FPGA,_FRAM.kicad_sch

Power

File: Power.kicad_sch

A/V

File: A%2fV.kicad_sch

USB

File: USB.kicad_sch

VRAM, DAC

File: VRAM,_DAC.kicad_sch

PETIO

File: PETIO.kicad_sch

SID

File: SID.kicad_sch

SID Power

File: SID_Power.kicad_sch

Mixer

File: Mixer.kicad_sch

Keylock

File: Keylock.kicad_sch

Smallbus

File: Smallbus.kicad_sch

UART

File: UART.kicad_sch

Userport

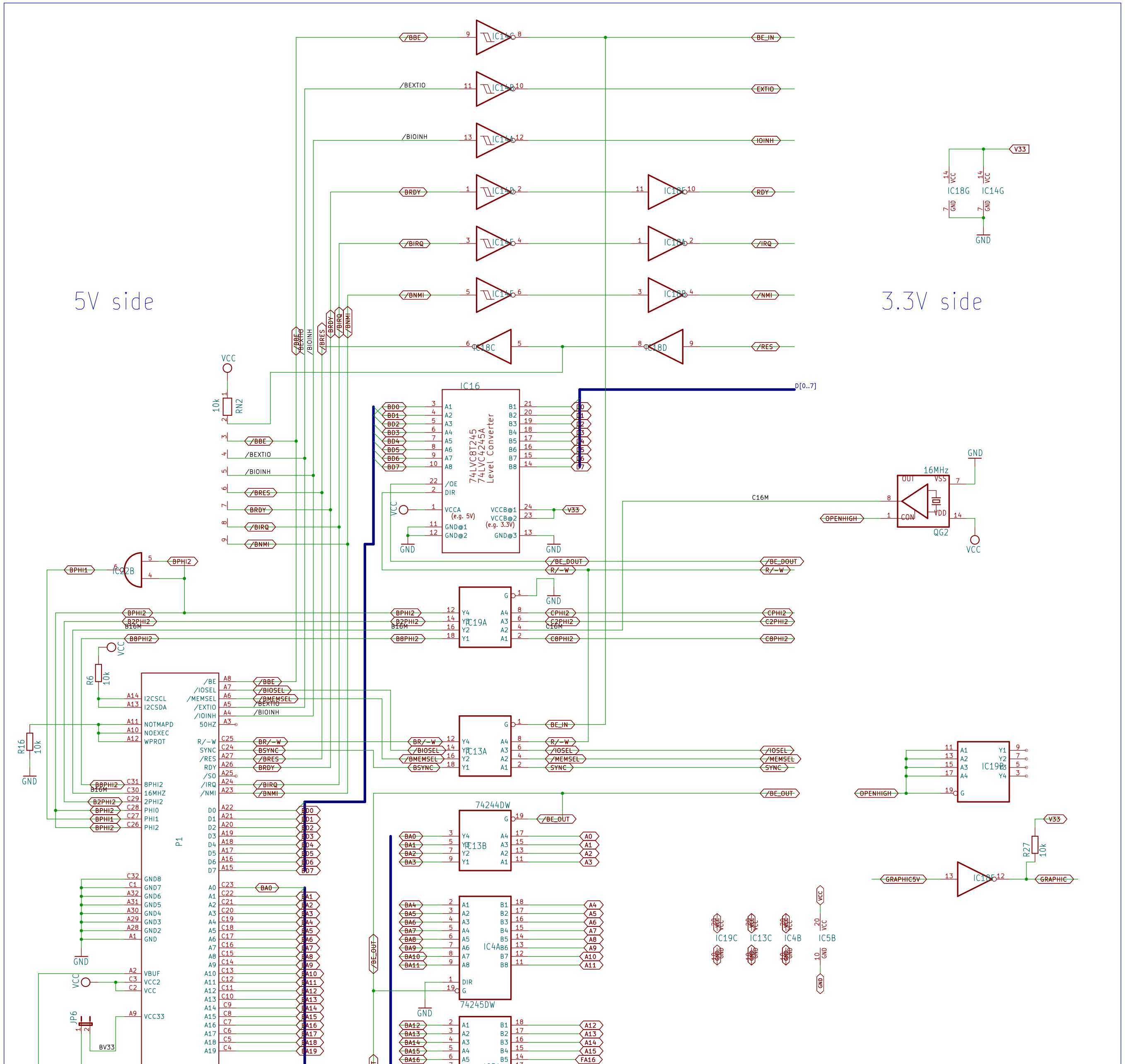
File: Userport.kicad_sch

FastIEC

File: FastIEC.kicad_sch

NANO488

File: NANO488.kicad_sch



CBM-ULTIPET-V1.0A
(C) A. Fachat

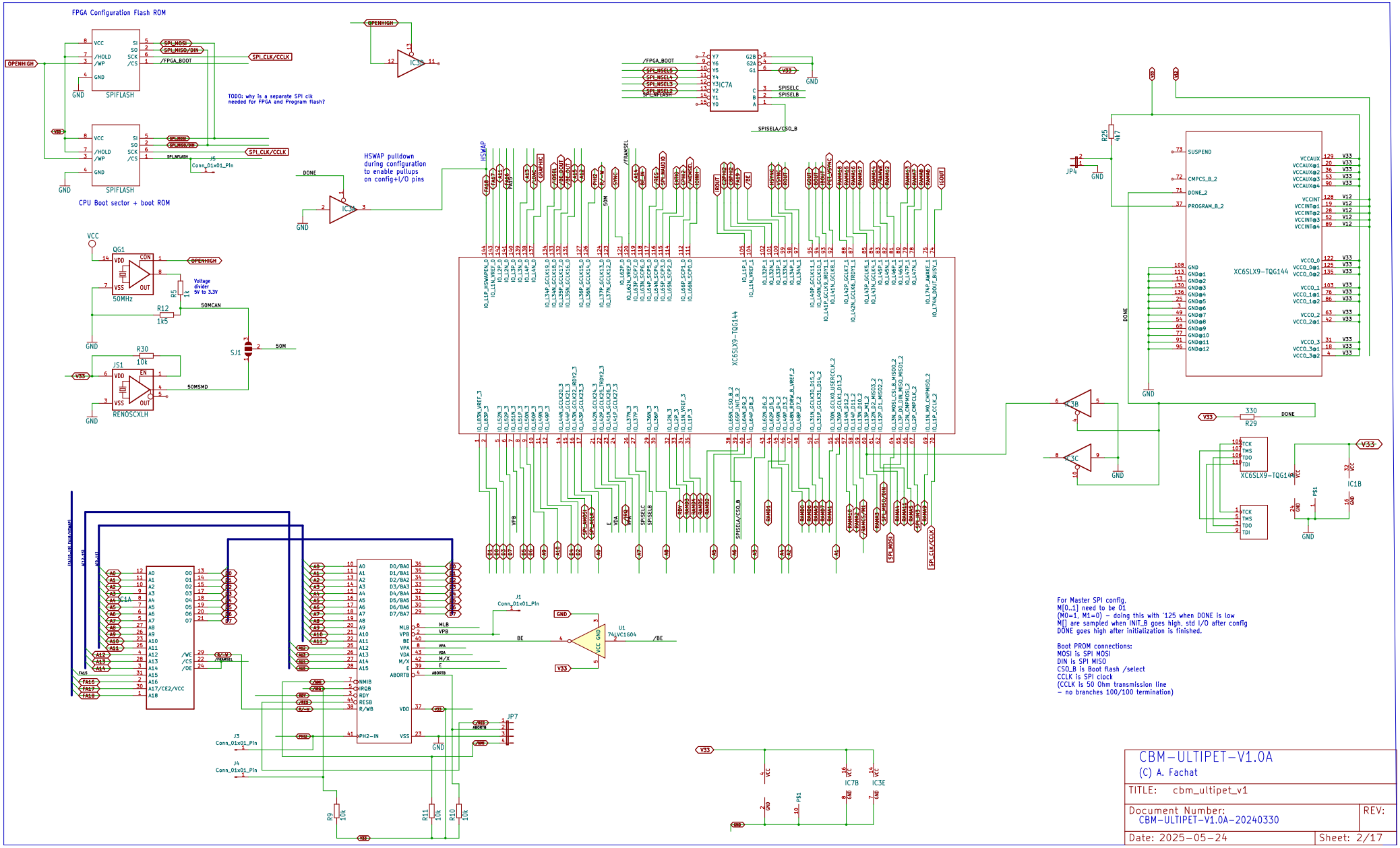
TITLE: cbm_ultipet_v1

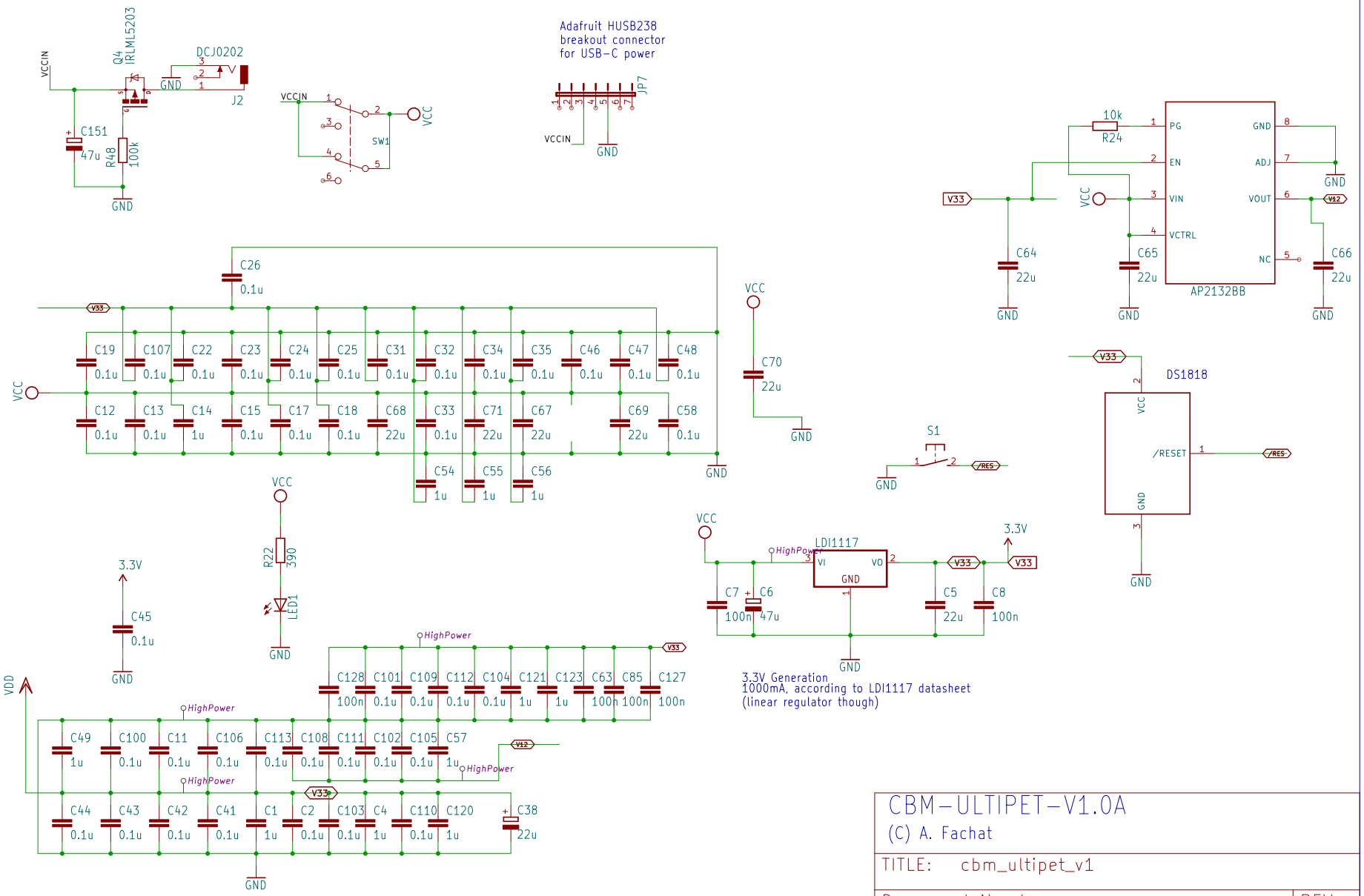
Document Number: CSA-ULTRACPU-V1.3C-20231117

REV:

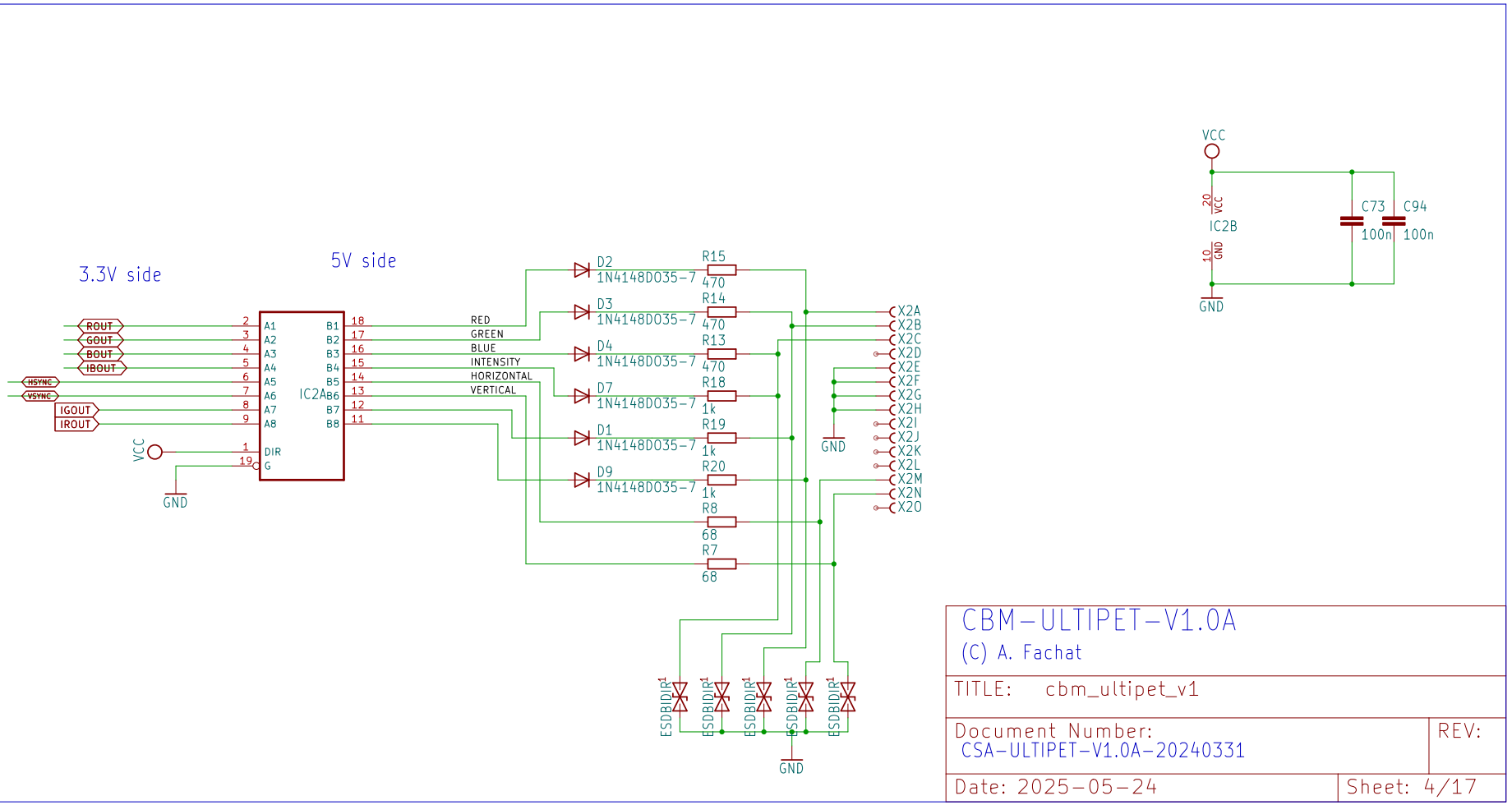
Date: 2025-05-24

Sheet: 1/17

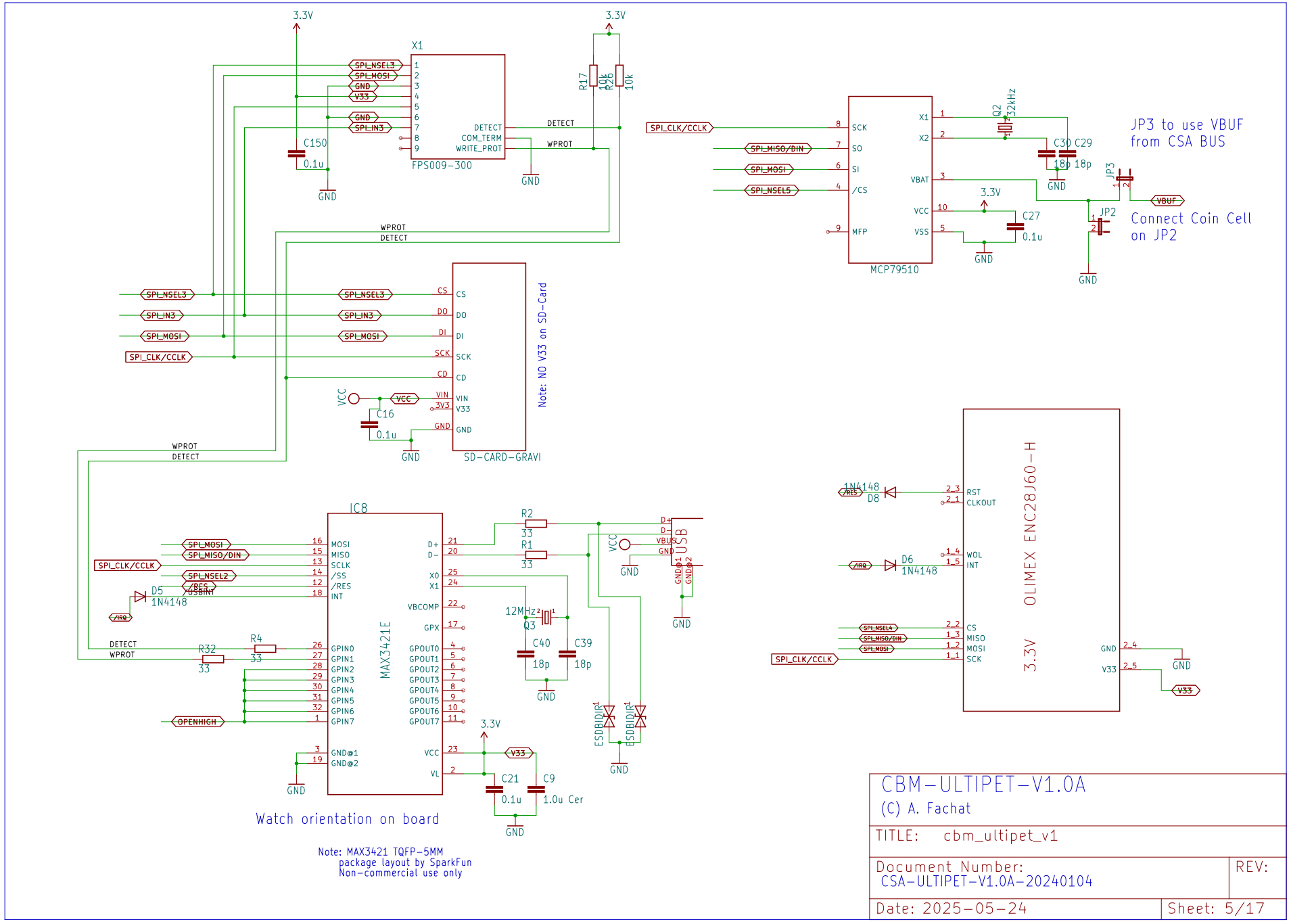

FPGA Configuration Flash ROM
SPIFLASH
SPI_MOSI
SPI_MISO/DIN
SPI_CLK/CCLK
/FPGA_BOOT
TODO: why is a separate SPI clk needed for FPGA and Program flash?
CPU Boot sector + boot ROM
HSWAP pulldown during configuration to enable pullups on config+I/O pins
50MHz
Voltage divider 5V to 3.3V
50MCAN
50MSMD
RENOSCXLH
50M
XC6SLX9-TQG144
SPISELA/CSO_B
SPISELC
SPISELB
For Master SPI config, M[0_1] need to be 01 (M0=1, M1=0) - doing this with '125 when DONE is low M[] are sampled when INIT_B goes high, std I/O after config DONE goes high after initialization is finished.
Boot PROM connections: MOSI is SPI MOSI DIN is SPI MISO CSO_B is Boot flash /select CCLK is SPI clock (CCLK is 50 Ohm transmission line - no branches 100/100 termination)
CBM-ULTIPET-V1.0A
(C) A. Fachat
TITLE: cbm_ultipet_v1
Document Number: CBM-ULTIPET-V1.0A-20240330
REV:
Date: 2025-05-24
Sheet: 2/17



CBM-ULTIPET-V1.0A (C) A. Fachat	
TITLE: cbm_ultipet_v1	
Document Number: CSA-ULTIPET-V1.0A-20240104	REV:
Date: 2025-05-24	Sheet: 3/17



CBM-ULTIPET-V1.0A (C) A. Fachat	
TITLE: cbm_ultipet_v1	
Document Number: CSA-ULTIPET-V1.0A-20240331	REV:
Date: 2025-05-24	Sheet: 4/17



CBM-ULTIPET-V1.0A

(C) A. Fachat

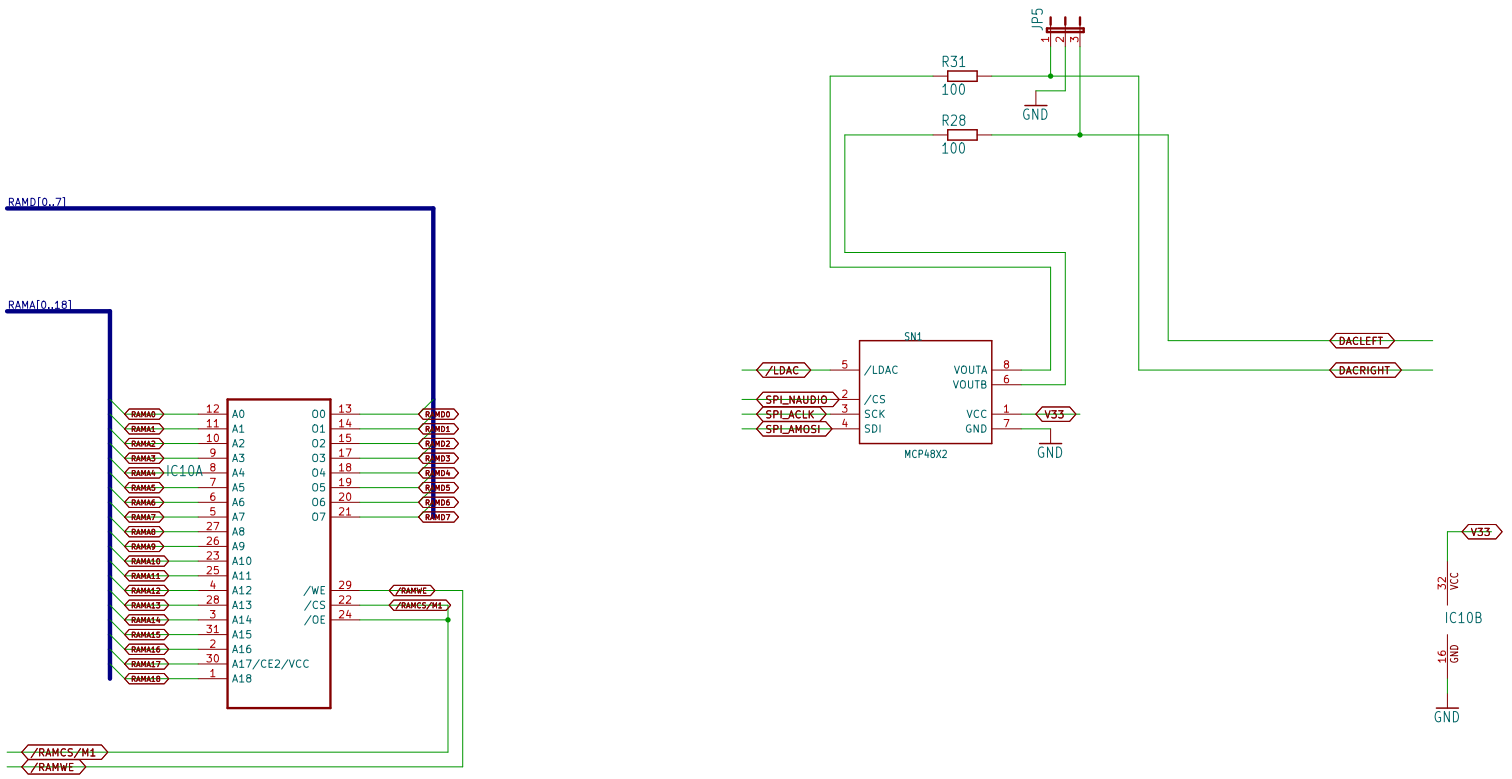
TITLE: cbm_ultipet_v1

Document Number: CSA-ULTIPET-V1.0A-20240104

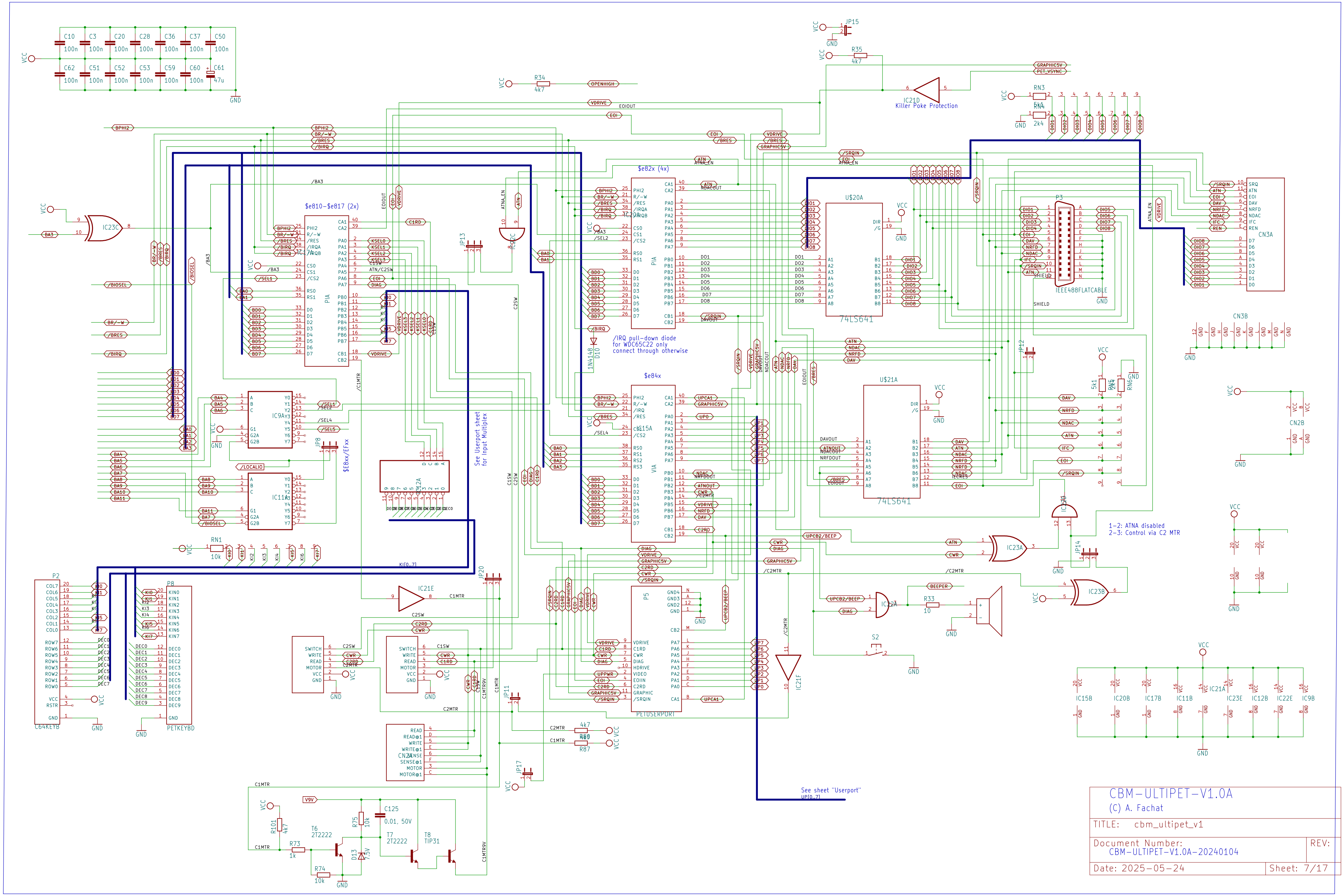
REV:

Date: 2025-05-24

Sheet: 5/17



CBM-ULTIPET-V1.0A (C) A. Fachat	
TITLE: cbm_ultipet_v1	
Document Number: CBM-ULTIPET-V1.0A-20240104	REV:
Date: 2025-05-24	Sheet: 6/17



CBM-ULTIPET-V1.0A

(C) A. Fachat

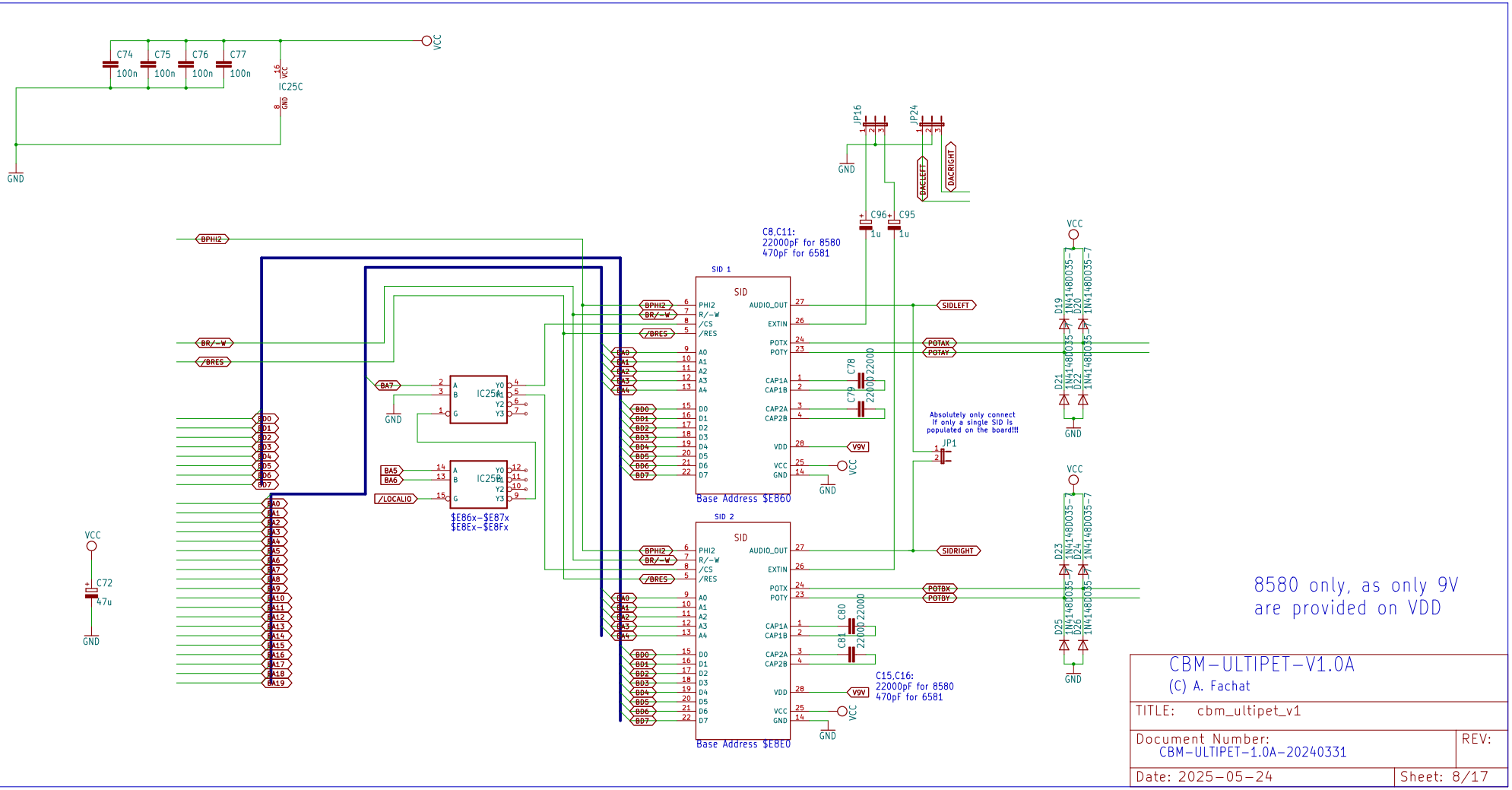
TITLE: cbm_ultipet_v1

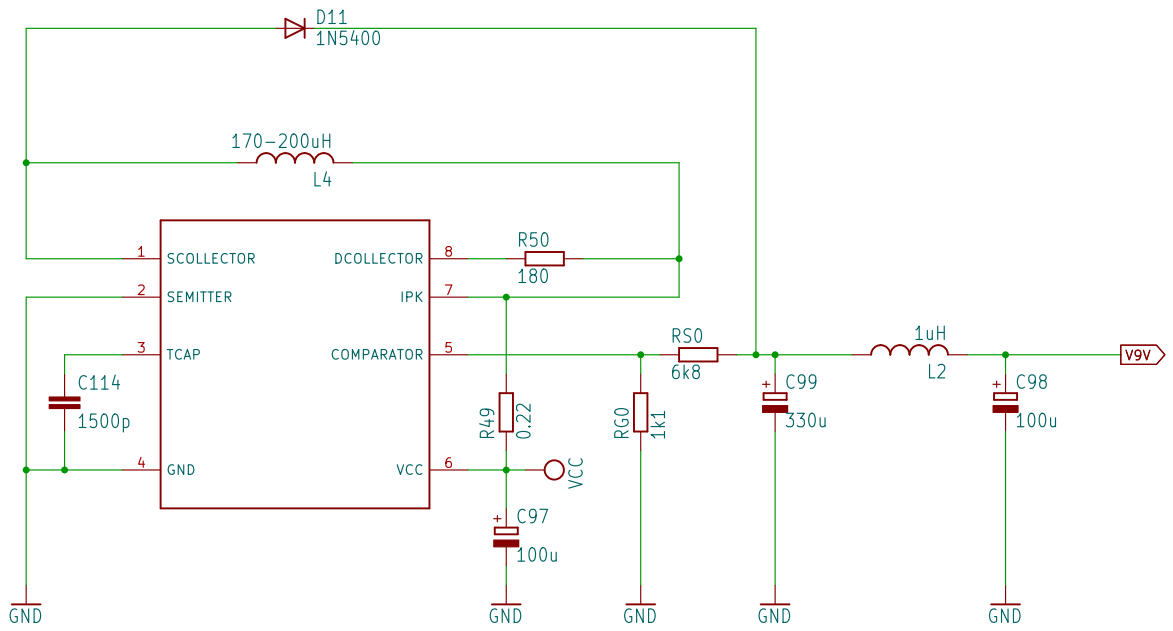
Document Number: CBM-ULTIPET-V1.0A-20240104

REV:

Date: 2025-05-24

Sheet: 7/17


C74 100n
C75 100n
C76 100n
C77 100n
IC25C
VCC
GND
JP16
JP24
DACLEFT
DACRIGHT
C96 1u
C95 1u
C8,C11:
22000pF for 8580
470pF for 6581
SID 1
SID
Base Address $E860
SID 2
Base Address $E8E0
SIDLEFT
SIDRIGHT
POTAX
POTAY
POTBX
POTBY
V9V
C78 22000
C79 22000
C80 22000
C81 22000
C15,C16:
22000pF for 8580
470pF for 6581
Absolutely only connect
if only a single SID is
populated on the board!!!
JP1
D19 1N4148D035-7
D20 1N4148D035-7
D21 1N4148D035-7
D22 1N4148D035-7
D23 1N4148D035-7
D24 1N4148D035-7
D25 1N4148D035-7
D26 1N4148D035-7
IC25A
IC25B
$E86x-$E87x
$E8Ex-$E8Fx
C72 47u
8580 only, as only 9V
are provided on VDD
CBM-ULTIPET-V1.0A
(C) A. Fachat
TITLE: cbm_ultipet_v1
Document Number:
CBM-ULTIPET-1.0A-20240331
REV:
Date: 2025-05-24
Sheet: 8/17



V1.0B:
- Fix parts footprint for L4, D2 and some caps

Vout=1.25 x (1 + RS/RG)

RS/RG = (Vout / 1.25) - 1

Vout = 9V -> RS/RG = 6.2
-> RG=1.1k, RS=6.8k

Vout = 12V -> ~~RS/RG = 8.6~~
-> ~~RG=1.2k~~, RS=10k

9V is not only used by SID
but also by Tape

CBM-ULTIPET-V1.0A

(C) A. Fachat

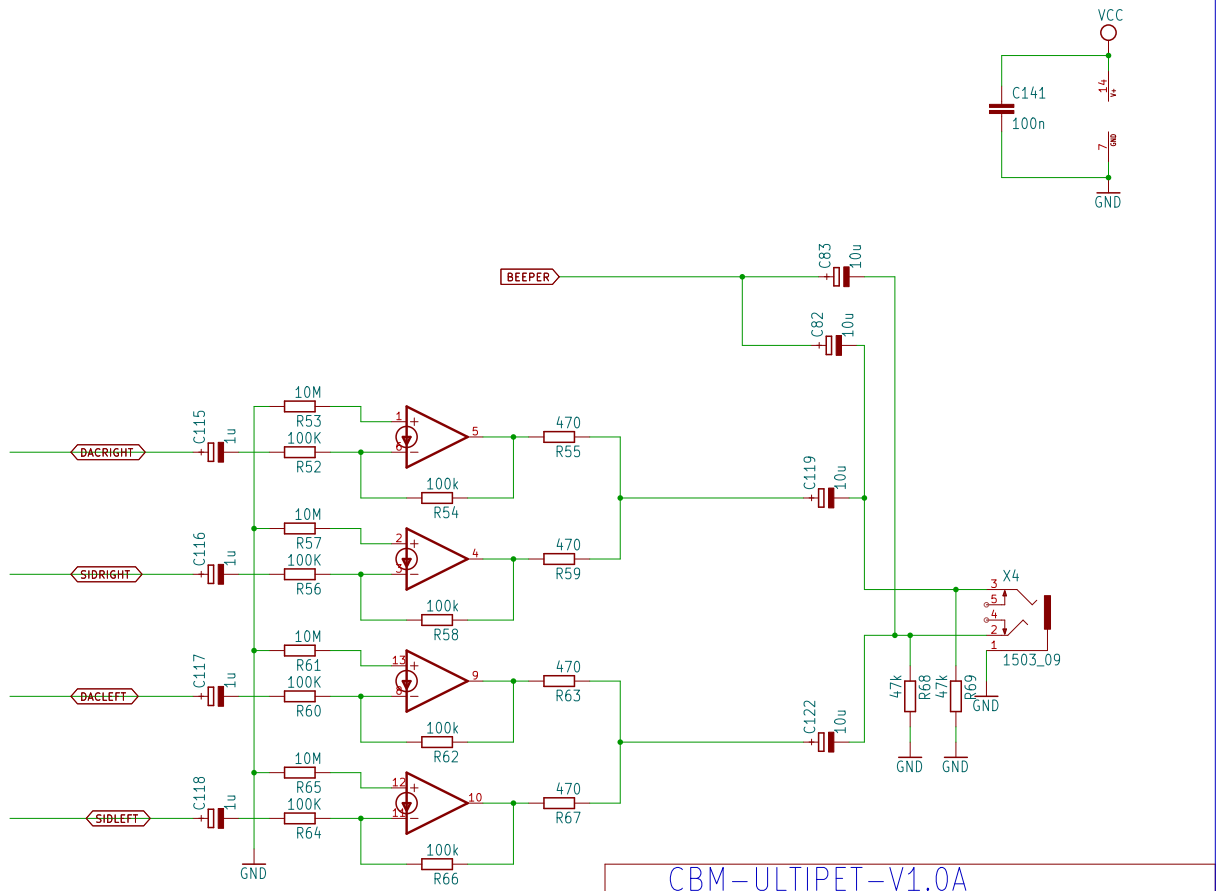
TITLE: cbm_ultipet_v1

Document Number:
CSA-DUALSID-1.0B-20231212

REV:

Date: 2025-05-24

Sheet: 9/17



CBM-ULTIPET-V1.0A

(C) A. Fachat

TITLE: cbm_ultipet_v1

Document Number: CBM-ULTIPET-1.0A-20240104

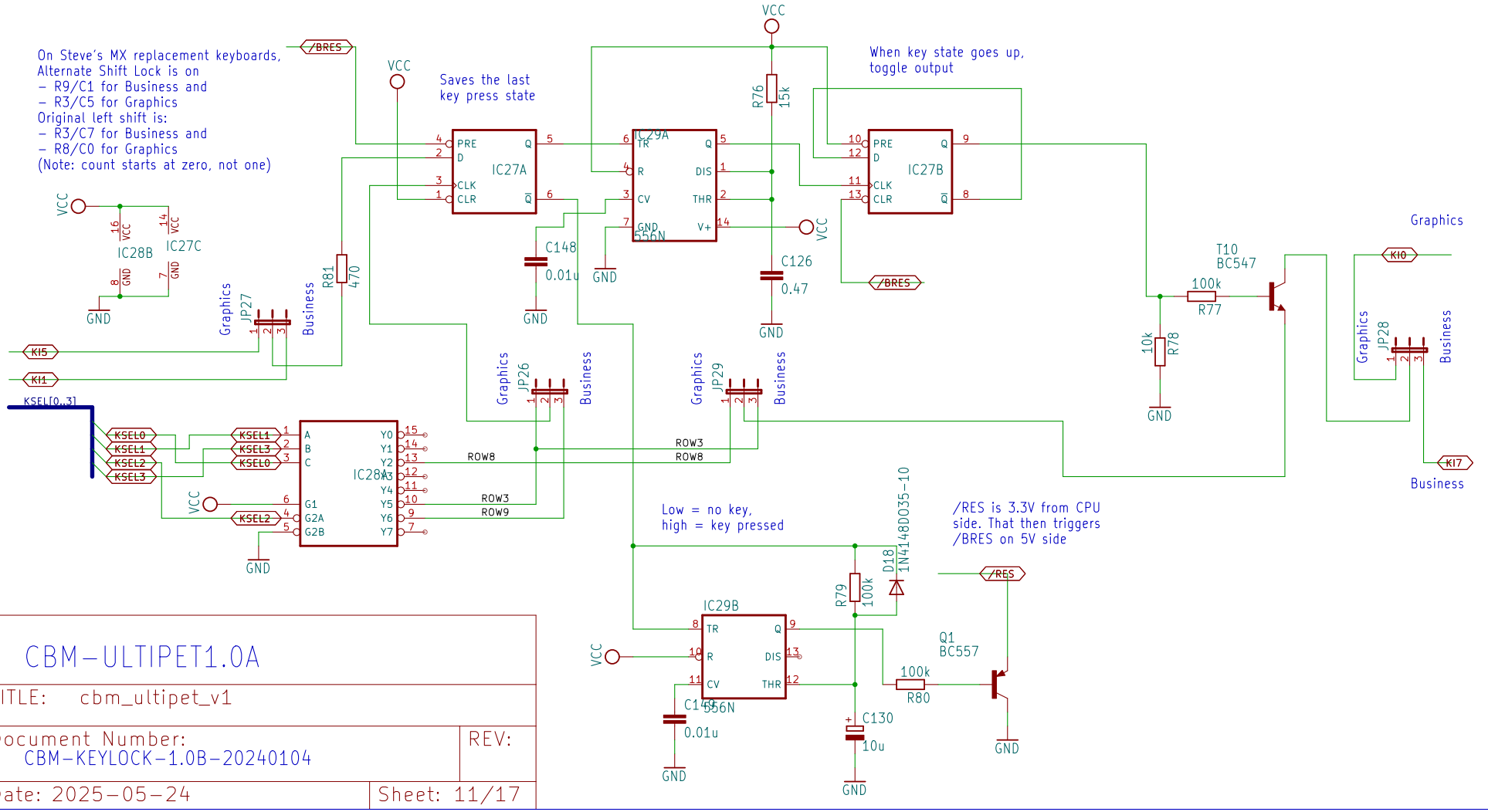
REV:

Date: 2025-05-24

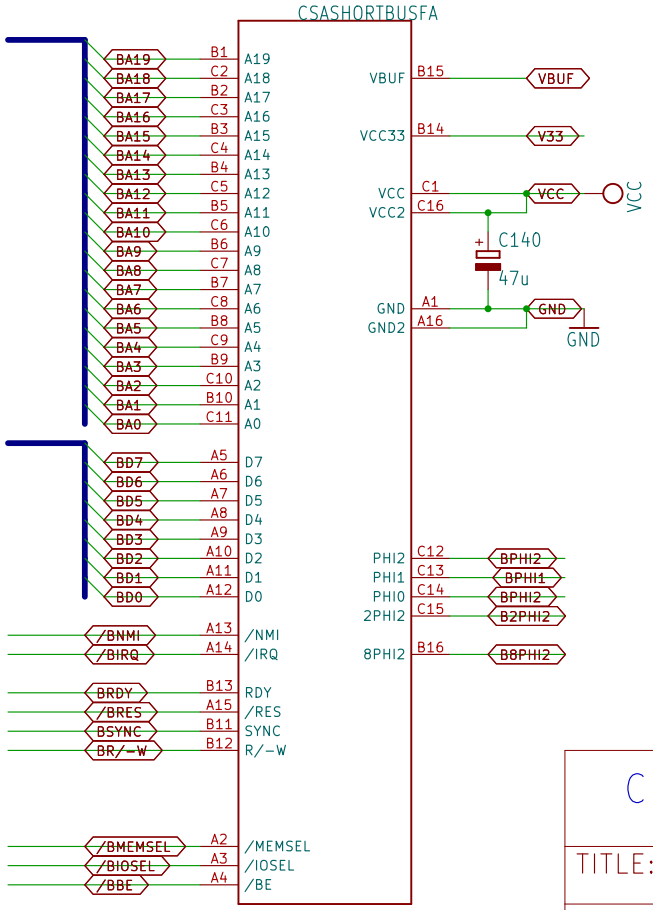
Sheet: 10/17

Commodore PET SHIFT-LOCK simulator + RESET on long push

Inspired by SX64 keyboard and discussions with Steve Gray and Mike Naberezny

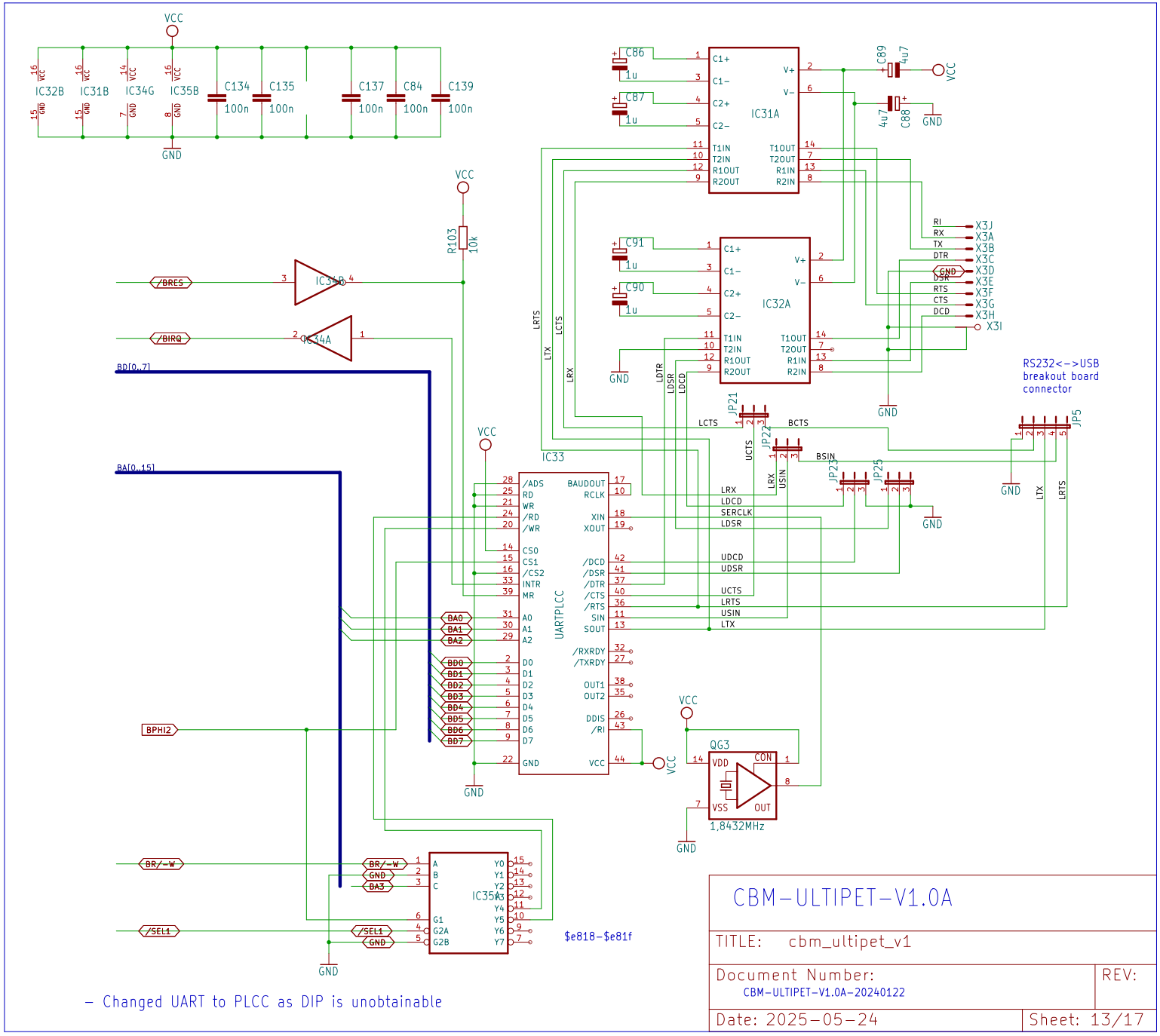


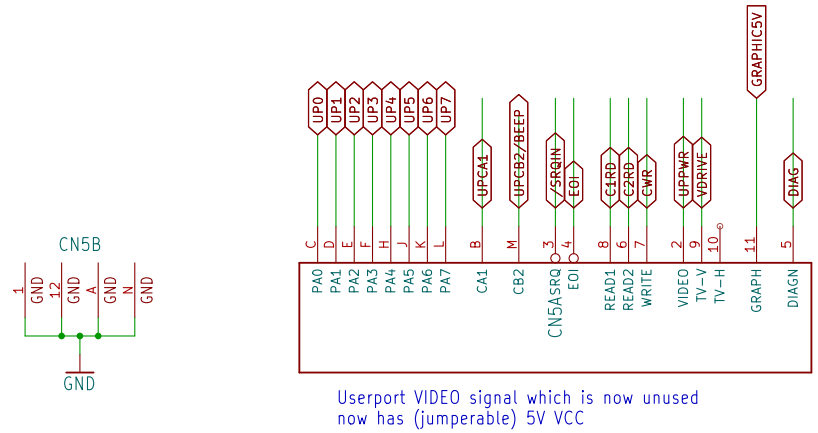
CBM-ULTIPET1.0A	
TITLE: cbm_ultipet_v1	
Document Number: CBM-KEYLOCK-1.0B-20240104	REV:
Date: 2025-05-24	Sheet: 11/17

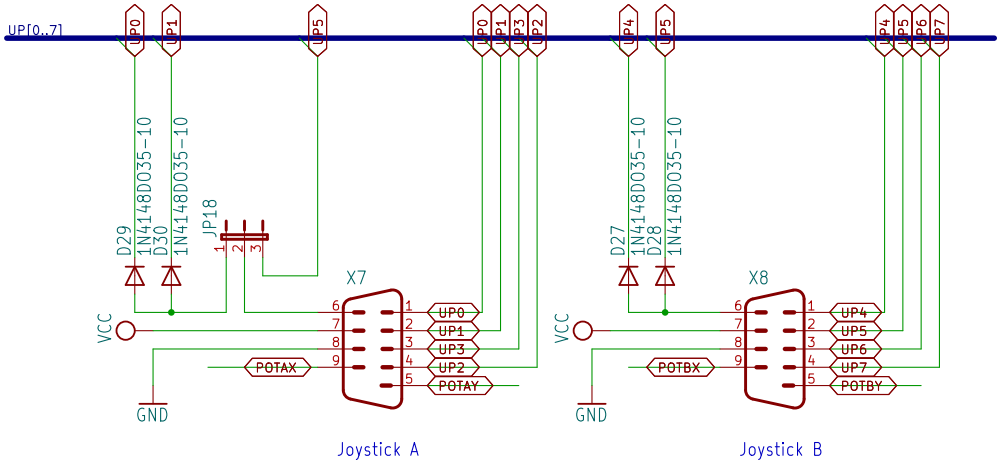


CBM-ULTIPET-V1.0A

TITLE: cbm_ultipet_v1	
Document Number: CBM-ULTIPET-V1.0A-20240104	REV:
Date: 2025-05-24	Sheet: 12/17

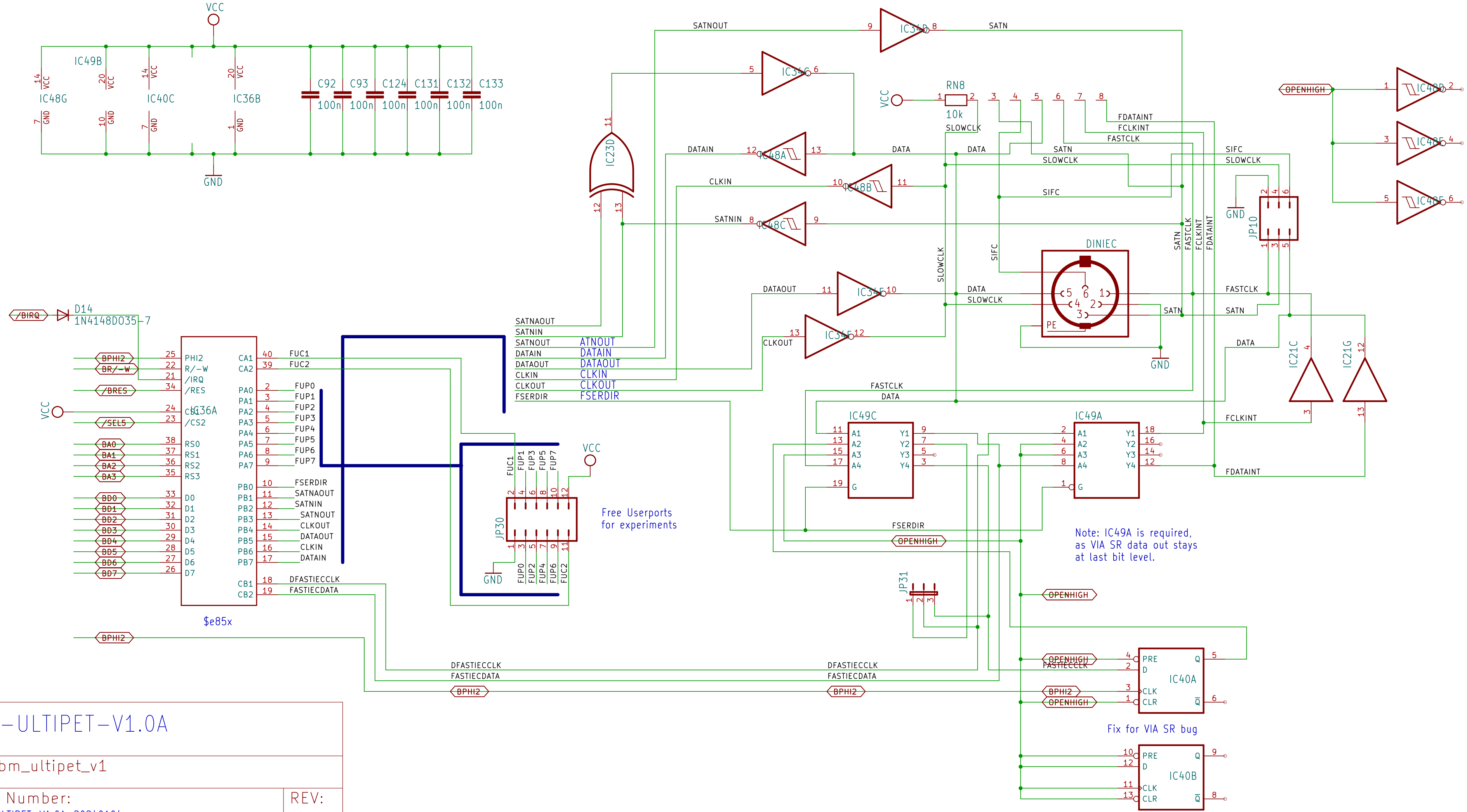

VCC
IC32B
IC31B
IC34G
IC35B
C134
C135
C137
C84
C139
100n
GND
C86
C87
1u
IC31A
C89
4u7
C88
R103
10k
/BRES
/BIRQ
IC31B
IC34A
BD[0..7]
BA[0..15]
C91
C90
IC32A
RI
RX
TX
DTR
DSR
RTS
CTS
DCD
X3J
X3A
X3B
X3C
X3D
X3E
X3F
X3G
X3H
X3I
LRTS
LCTS
LTX
LRX
LDTR
LDSR
LDCD
RS232<->USB
breakout board
connector
JP21
JP22
JP23
JP24
JP25
JP5
LCTS
BCTS
BSIN
IC33
UARTPLCC
/ADS
RD
WR
/RD
/WR
CS0
CS1
/CS2
INTR
MR
A0
A1
A2
D0
D1
D2
D3
D4
D5
D6
D7
BAUDOUT
RCLK
XIN
XOUT
/DCD
/DSR
/DTR
/CTS
/RTS
SIN
SOUT
/RXRDY
/TXRDY
OUT1
OUT2
DDIS
/RI
LRX
LDCD
SERCLK
LDSR
UDCD
UDSR
UCTS
LRTS
USIN
LTX
BA0
BA1
BA2
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BPHI2
QG3
VDD
CON
VSS
OUT
1,8432MHz
BR/-W
/SEL1
IC35A
A
B
C
G1
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
$e818-$e81f
- Changed UART to PLCC as DIP is unobtainable
CBM-ULTIPET-V1.0A
TITLE: cbm_ultipet_v1
Document Number:
CBM-ULTIPET-V1.0A-20240122
REV:
Date: 2025-05-24
Sheet: 13/17





CBM-ULTIPET-V1.0A

TITLE: cbm_ultipet_v1	
Document Number: CBM-ULTIPET-V1.0A-20240104	REV:
Date: 2025-05-24	Sheet: 14/17



CBM-ULTIPET-V1.0A

TITLE: cbm_ultipet_v1

Document Number: CBM-ULTIPET-V1.0A-20240104

REV:

Date: 2025-05-24

Sheet: 15/17